

Preliminary simulations of a 10 bit SAR ADC

PixFEL

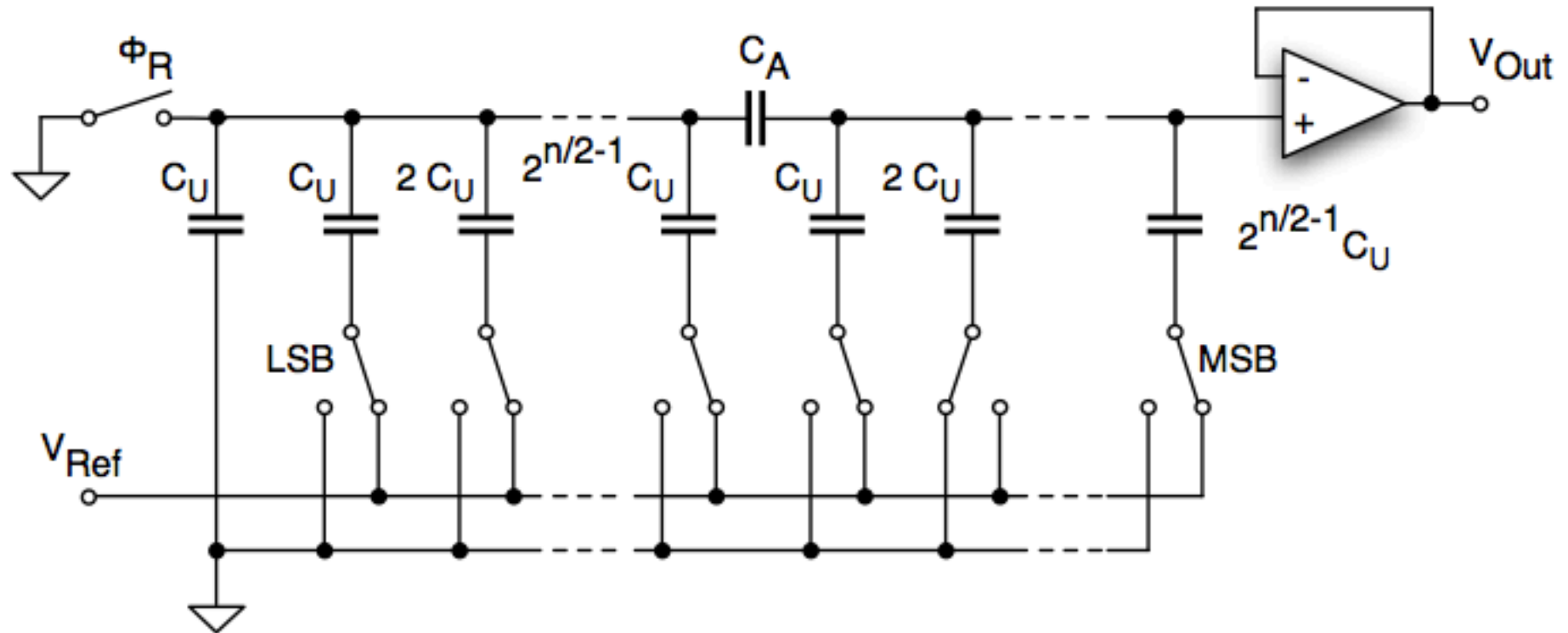
Enabling technologies, building blocks and architectures
for advanced X-ray pixel cameras at FELs

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PixFEL phone meeting, 19/12/2013

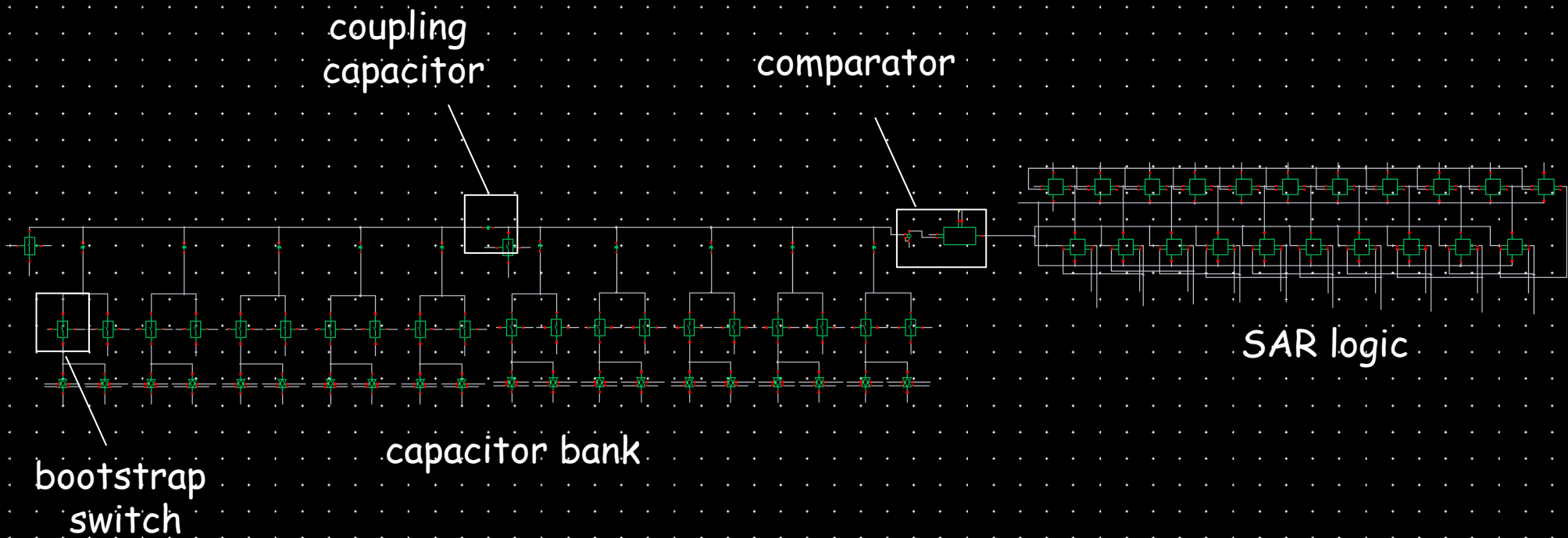
DAC architecture: capacitive divider with attenuator



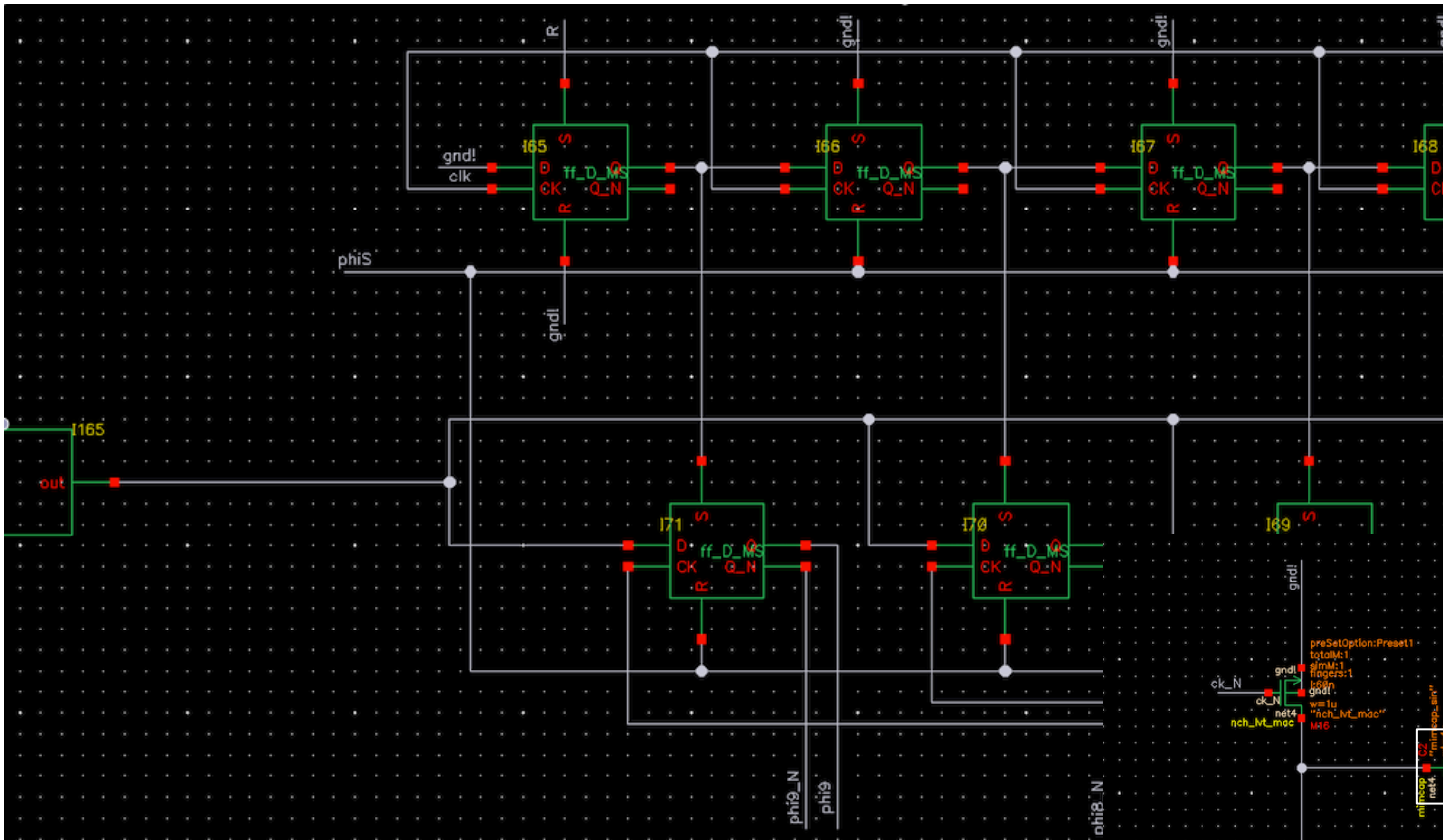
- no of unit elements C_U : $2^{n/2}$
- C_A is critical

Simulated scheme

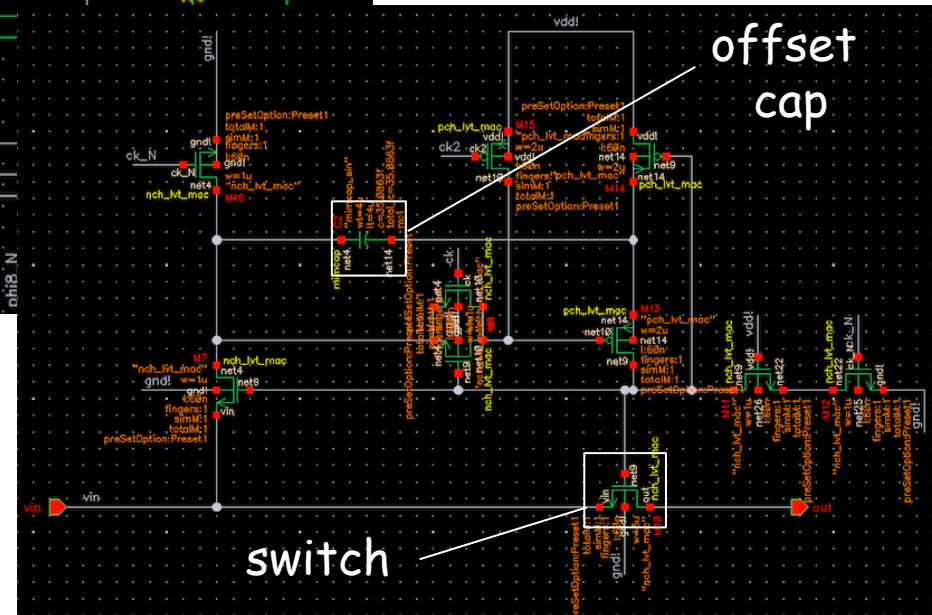
- SAR ADC with charge redistribution scheme and attenuator



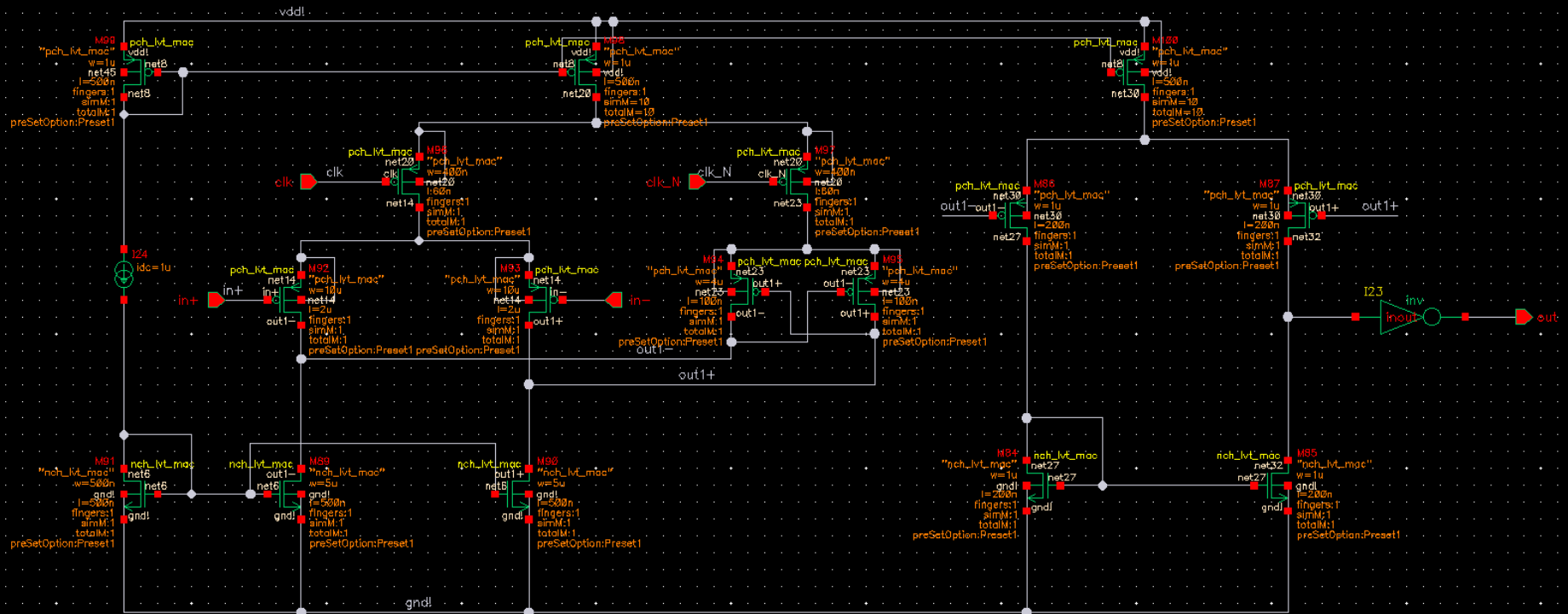
SAR logic and bootstrap switch



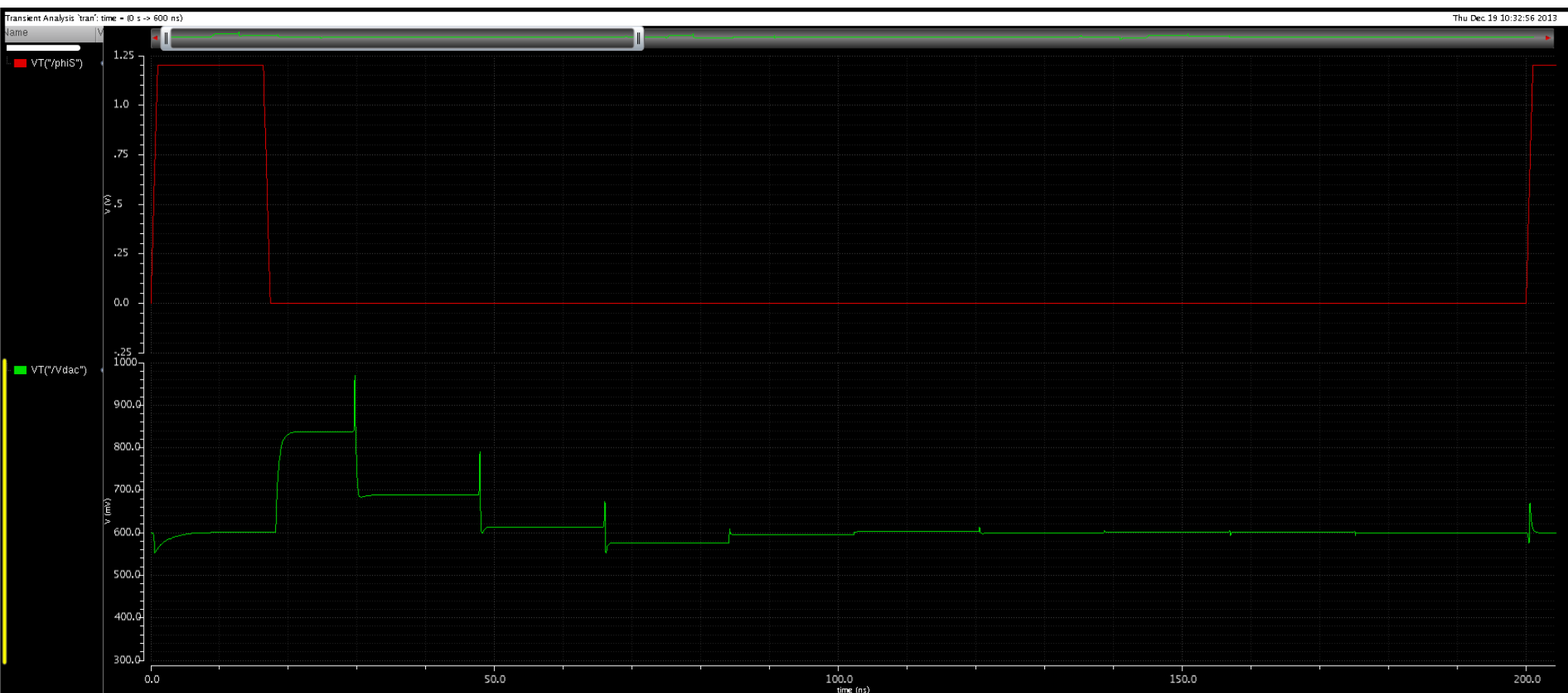
- Guarantees correct operation of the switch for any input level



Latched comparator



Some simulation results - comparator input



Some simulation results - output bits

