PixFEL
WP2: Building blocks

Massimo Manghisoni[1,2]

[1] Università degli Studi di Bergamo
[2] INFN Sezione di Pavia

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WP2 main tasks and milestones

Tasks

Design of the fundamental building blocks for the readout of a pixel detector

- Development of individual stages
- Integration of building blocks in a single tier 8×8 matrix
- Design of a 32×32 single tier matrix to be interconnected to pixel sensor

Milestones

2014

- Specification of the X-ray imager
- Design of test structures with single blocks (CSA with signal compression, SAR ADC, circuits for gain calibration, single MOS capacitors)[1]
- Design of a 8×8 pixel matrix, with a 100 μm pitch with simple readout electronics (no data storage in-pixel)[1]

2015

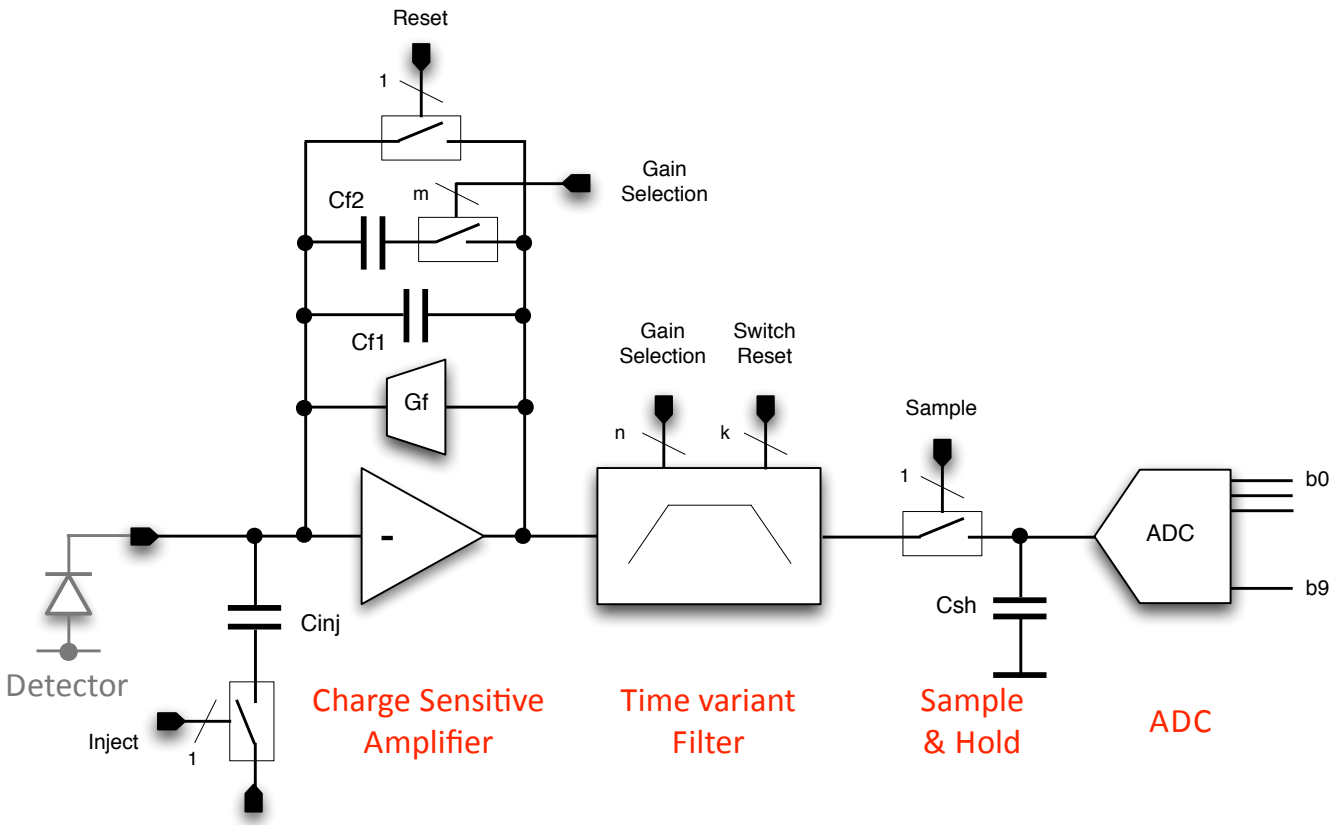
- Characterization of the test structures submitted in the first year runs
- Design of a 32×32 chip with 100 μm pitch (4.5 μm×4.5 μm)

2016

- Test of the 32×32 readout chip
- Interconnection and tets of the 32×32 readout chip to a pixel sensor

[1] 1920 μm×1920 μm chip, through Europractice with the mini@sic option, 65 nm CMOS technology

Readout channel block diagram

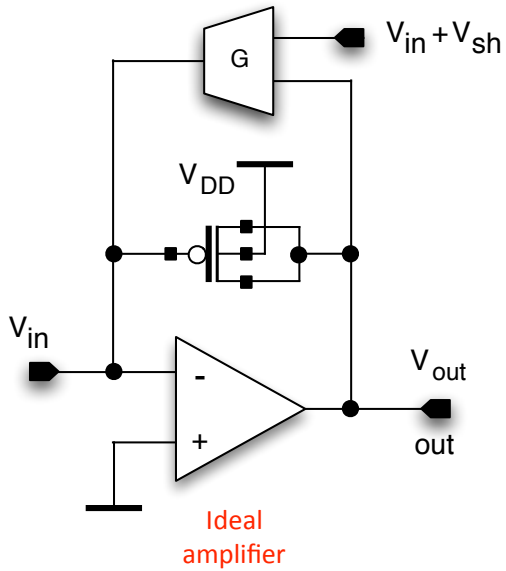


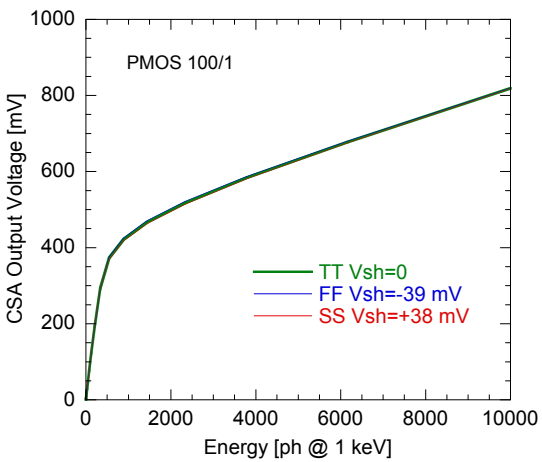
The analog channel consists of

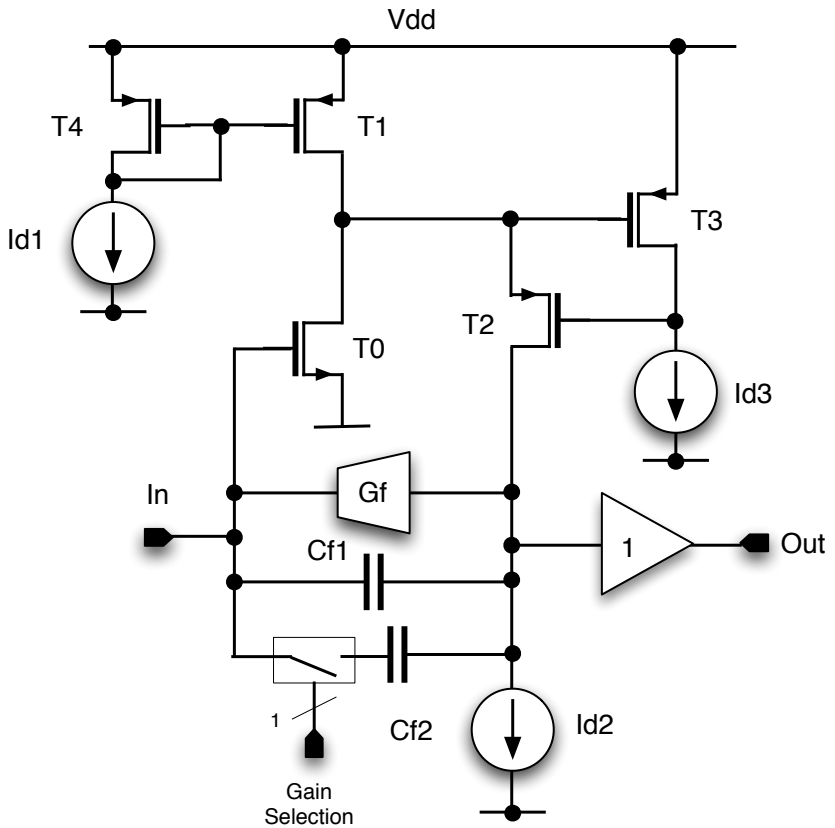
- Charge-sensitive preamplifier with signal compression
- Time-variant filter with gain and integration time selection options
- Sample & Hold
- Analog-to-Digital conversion performed by a 9-10 bit SAR ADC
- Sequencer for fast signals generation (switch, reset, injection,...)

Charge sensitive amplifier with signal compression

Use the non-linear features of MOSFET capacitors to dynamically change the gain with the input signal amplitude







Amplifier architecture:
active folded cascode (with local feedback) loaded by an active cascoded load and output stage

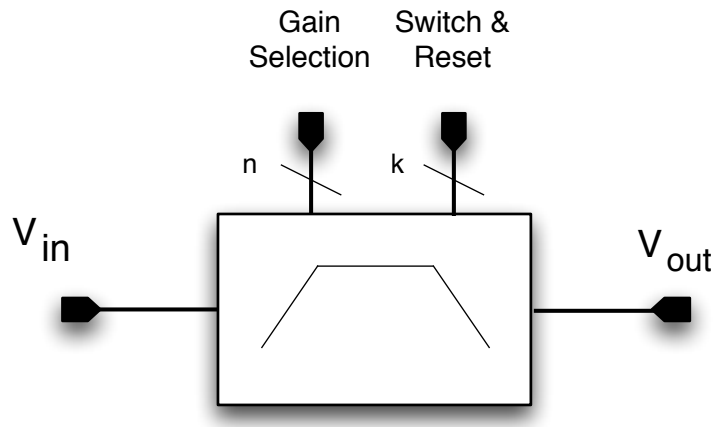
Time-variant Filter

In the case of events with a known repetition rate, time variant shaping may provide some advantage with respect to continuous time processing

- Reduced time to return to base
- May be designed in such a way to provide the sample to ADC at its output

Trapezoidal weighting function

- Gated integrator
- Correlated Double Sampling (CDS)

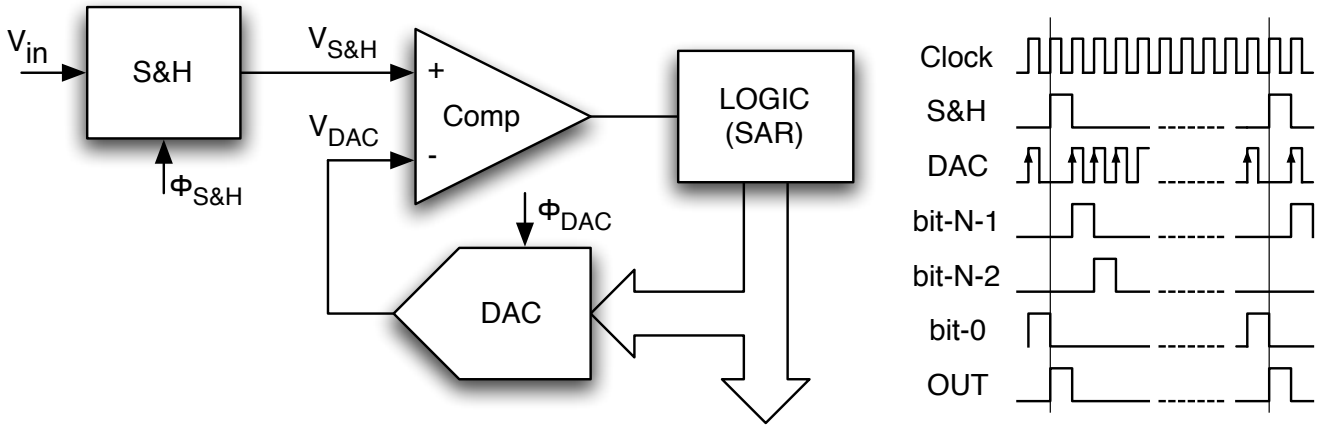


To be investigated

- Time-invariant filter (RC-CR or CR-RC^2)
- RC-CR shaper with gated integrator
- Multiple Correlated Double Sampling (MCDS)
- Rail-to-rail output stage

Analog-to-digital converter

Based on a successive approximation register (SAR) architecture



Specifications

- resolution: 9-10 bits $\Rightarrow$ guarantees single photon resolution at small signal, small quantization noise in Poisson-limited regime
- sampling rate: 5 MS/s $\Rightarrow$ for operation at the Eu-XFEL
- area: $<$5000 μm^2

Readout options

- Parallel conversion and readout
- Independent conversion and readout

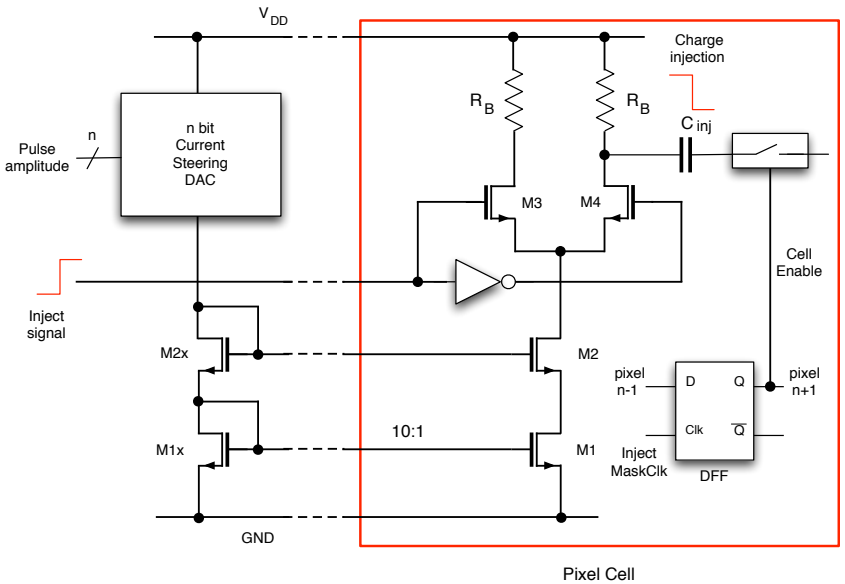
Calibration circuit

Programmable signal generator circuit integrated in each pixel for gain calibration

The proposed circuit consists of two main parts

- The Digital-to-Analog Converter located in the matrix chip periphery
- The Pulser to be included in the pixel cell

The current provided by the DAC is mirrored into each pixel, where the pulser injects a charge directly into the input of the amplifier by applying a voltage step to a small injection capacitor

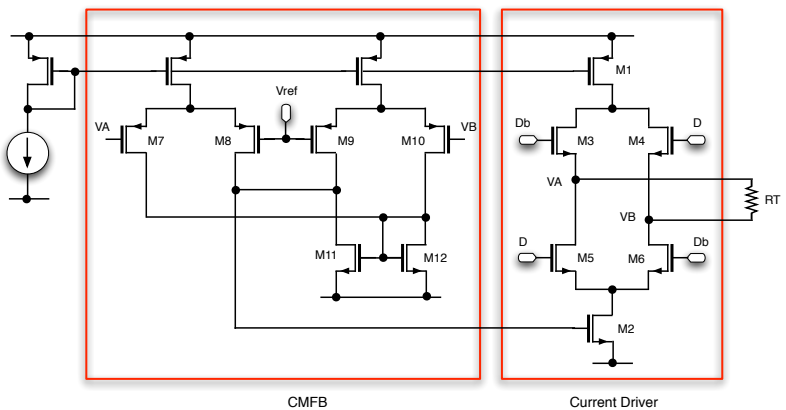


The granularity of the generated signal amplitude should be chosen to provide a significant number of experimental points also in the high gain portion of the input-output front-end curve and not to exceed the ADC resolution

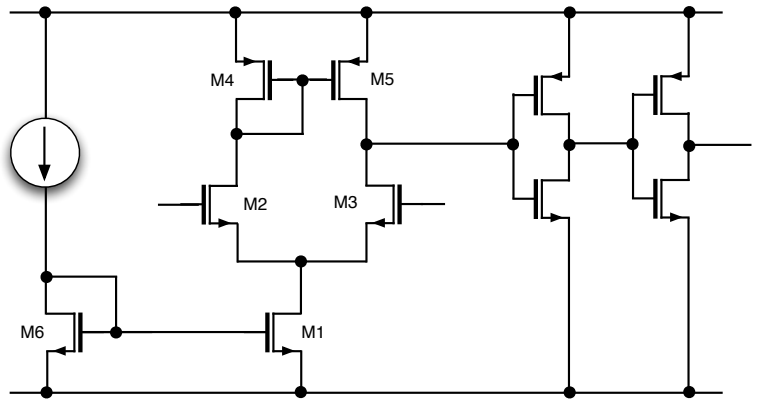
Other blocks

I/O circuits to transfer data off-chip and to feed the clock to the ADC, the time variant shaper, the memory and the readout circuits

CMOS to LVDS converter



LVDS to CMOS converter



Power supply/temperature independent band-gap reference circuits to provide stable voltage references to in-pixel blocks (e.g., the ADC).

Kits and tools

Configuration in Pavia

Cadence	cadence_6.16.010
Calibre	ixl_cal_2010.2_13.12
MMSIM	MMSIM_12.11.164
IMEC DK	T-N65-CM-SP-007-K3 (Cadence OA PDK 1.7A)
	T-N65-CM-SP-007-K4 (PATCH)
Files	t-n65-cm-sp-007-k3_1_7a_20120927.zip
	tn65cmsp007k4_1_7a_1.zip
	t-n65-cm-sp-007-x1_1_5a.zip
	t-n65-cl-dr-001_2_2_20130829[1].zip
Settings	Select process : RF
	Select voltage : 1.2V / 2.5V / 2.5V under-drive 1.8V / 2.5V over-drive 3.3V
	Select MiM cap : MIM_2.0fF
	Select metal option : 1p9m_6X1Z1U_ALRDL *ind_1z1u *Star_RC *Cal_RC *QRC

Collect this data and try to agree on common versions