PixFEL- Attivita' a Pisa

PixFEL Meeting 19 Dic. 2013

G. Rizzo

Aim of the PixFEL project

- •Studying, designing and testing the building blocks (CMOS 65 nm) for the front-end electronics, complying with the application requirements
  - low noise, (reconfigurable) wide input range front-end channel with dynamic compression
  - 9 bit (effective), 5 MS/s ADC
  - circuits for gain calibration

- •Investigating the enabling technologies for the design of chips with minimum dead area and high functional densities
  - standard and slim edge sensors
  - vertical integration for double tier design of the front-end
  - low density TSVs for chip interconnection to the hybrid board
  - interposers (?) for sensor to front-end pitch adaptation

- •Looking into architectures for fast chip operation and readout
  - frame storage mode (memory cell, maximum memory size, readout)
  - continuous readout mode (maximum speed, accounting for DAQ limitations)
  - reconfigurability (impact on the performance)

Activities

- 2014
  - define chip specifications.
  - design of test structures with single blocks (analog front-end, ADC, circuits for gain calibration, single MOS capacitors, I/O circuits), CMOS 65 nm
  - design of a 8x8 matrix, 100 um pitch
  - design of standard pixel sensors
  - start investigation on readout electronics

- 2015
  - test the structures from the first run
  - start investigation on 3D integration processes, including low density TSVs
  - design of the 32x32 matrix (accounting for low density TSVs)
  - design of slim edge pixel sensors
  - interconnect the front-end chip to the (slim edge) pixel sensor
  - start writing VHDL and design some elementary digital block (memory cells, buffers)
  - start organizing the test beam

- 2016
  - test the 32x32 front-end chip
  - test the chip after interconnection with the detector
  - test structures including low density TSVs
  - complete VHDL design of the readout electronics
  - test the chip on a beam

Attivita' a Pisa

2014

- Collaborazione a definizione delle specifiche
- Collaborazione progetto convertitore SAR
- Logica in-pixel e architettura readout semplificata per chip prototipo singolo layer (matrice 8x8)
- contatti con le facilities FEL

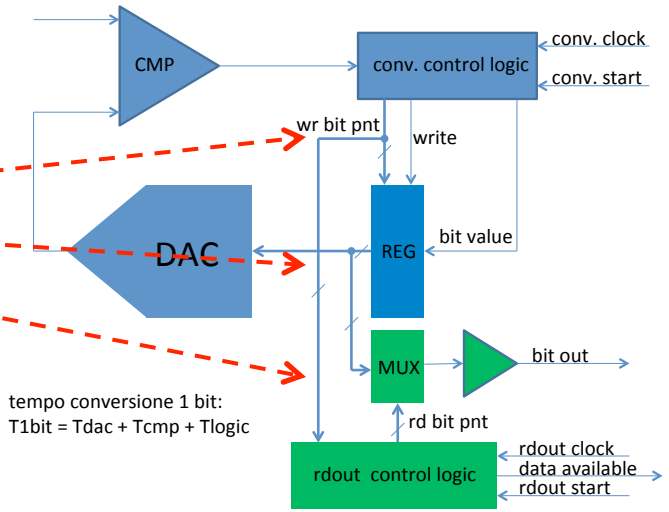
2015-2016

- Collaborazione al design del II prototipo 32x32
- contributo al progetto del chip digitale per prototipo 2 layers (3D)
- caratterizzazione in lab dei vari chip prodotti
- Partecipazione testbeam

1. Design prime strutture di test con target sottomissione Ott. 2014

- Asap installare a Pisa design kit per 65 nm (collaborazione da PV)
- Definizione logica in-pixel per:
  - Controllo ADC SAR
  - interfaccia SAR per matrice 8x8
  - Qualche idea gia' sviluppata a giugno
- Iniziare a pensare al readout per la matrice 8x8
  - Importante la testabilita' dell'oggetto con gli strumenti attualmente in uso (PG/LA)

schema a blocchi dell'ADC e logica di readout
(readout e conversione indipendenti)



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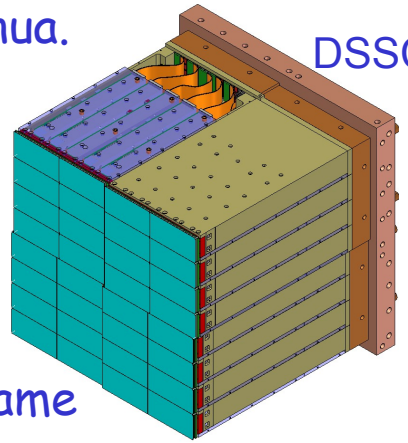
... due diap pixFEL, Fabio Morsani, 22-05-2013

2. Definizione delle specifiche

- Modularita' del rivelatore per coprire 20x20 cm2.
- Necessita' di banda (su chip e ladder) per applicazione a diversi FEL & sviluppo architettura operabile in burst mode/continua.



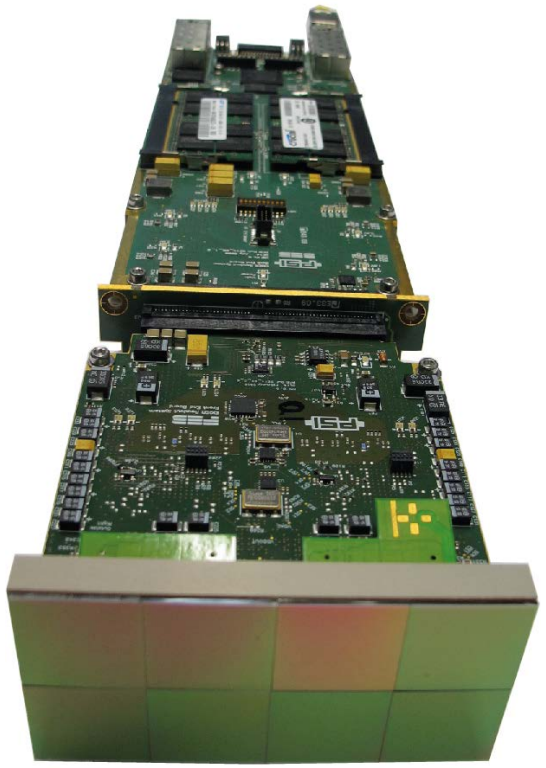
Qualche numero:

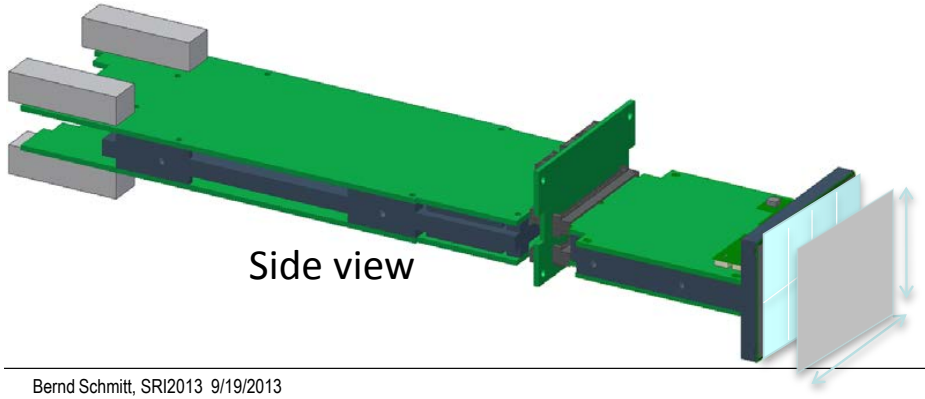
- chip da 64x64 pixel (100 um) e 16 chip/ladder
- 10 bit risoluzione
- LCLS: 120 Hz frame rate continuo
  → banda 5 Mb/s/chip e 80 Mb/s/ladder
- XFEL: 4.5 MHz frame rate, 1% duty cycle, 1k frame/3k frame storati
  → banda: 600 Mb/s/chip e 9 Gb/s/ladder (vedi next slide)
- In queste condizioni XFEL equivale ad una macchina continua con frame rate 15 kHz.
- Ci possiamo spingere oltre questi 15 kHz equivalenti in continua?
- Futuri FEL Macchine continue a 1 MHz (LCLS2 va in questa direzione)
- Capire cosa c'e' in giro:
  - sviluppi molto interessanti al PSI su detector per synchrotron light source la parte analogica non e' quella giusta ma la periferia del modulo ha un buon match con le specifiche per XFEL

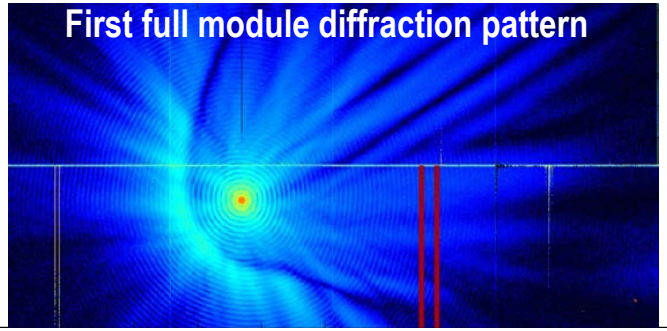
Da talk a Vertex 2013

Eiger, the next generation pixel detector

- Single photon counting pixel detector
- Sensitive area of 38 X 77 mm^2
- Pixel size 75 μm
- 524k pixel module
- Dead time free mode of operation
- Maximum frame rates
  - 23 kHz in 4 bit mode
  - 12 kHz in 8 bit mode
  - 8 kHz in 12 bit mode
- 8 GB of memory on a module
- Two 10 GbE data links per module

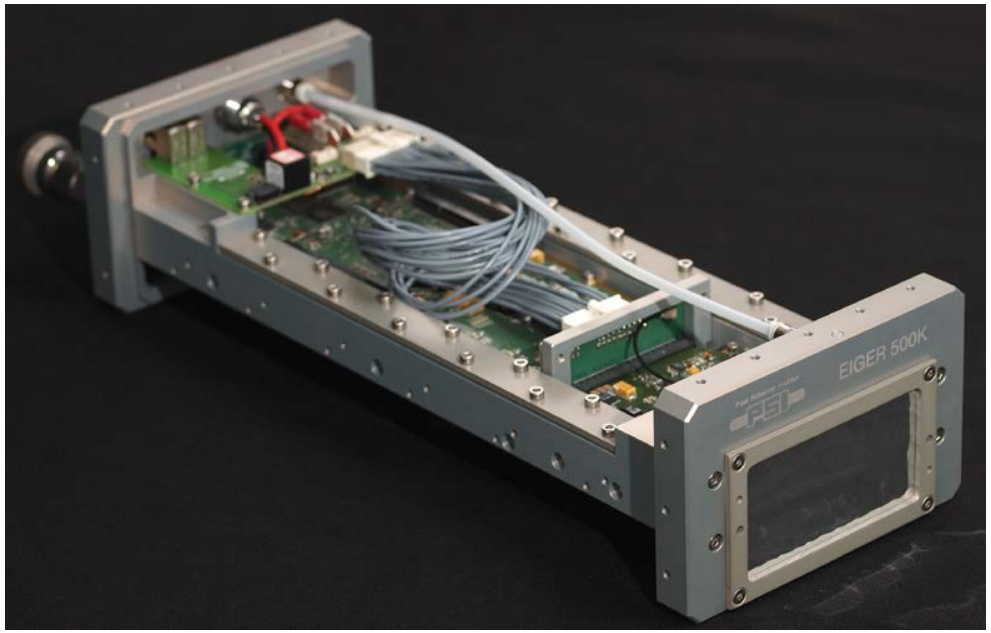




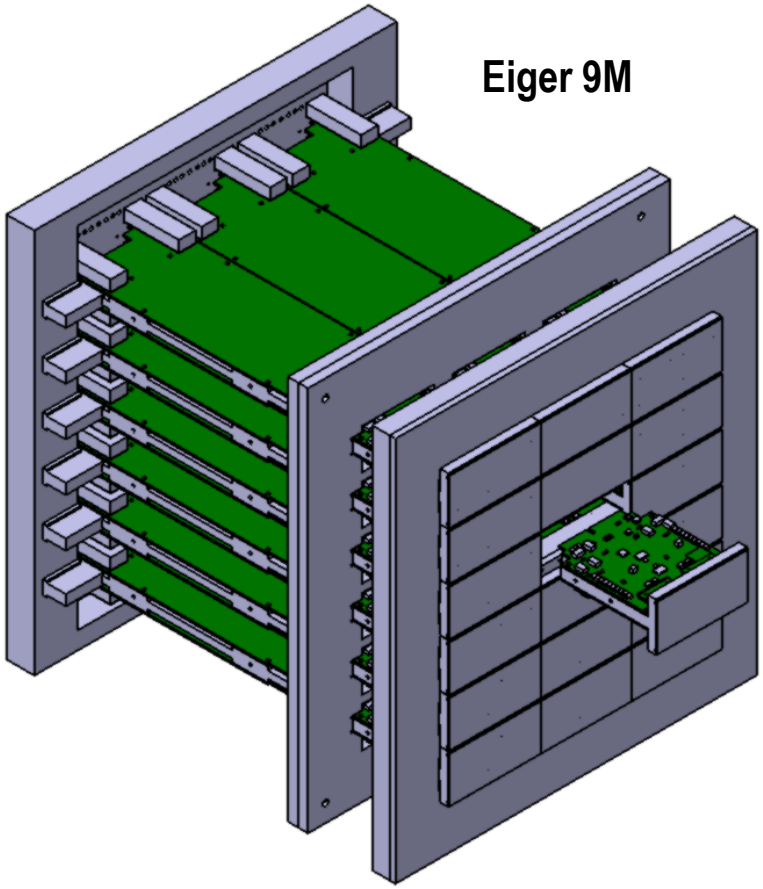


Eiger systems

500k single module



Eiger 9M



	Number of pixels	On board storage (frames/4 bits)	Data rate[1] @ 12 kHz	Data rate[2] @ 1kH	Data rate[3] @ 100 Hz	Data rate[4] @ 10 Hz
Module	524 k (512 x 1024)	~32,740	50.3 Gb/s	6.29 Gb/s*	839 Mb/s*	168 Mb/s*
9M Detector	9.44 M (3072x3072)	~32,740	906 Gb/s	113 Gb/s	15.1 Gb/s*	3.02 Gb/s*

1) 8 bit, equivalent to ~4@23 kHz and 12@8 kHz. 2) 12 bit. 3) 16 bit. 4) 32 bit. *) Foreseeable continuous storage rates (~20 Gb/s).

3. Contatti con esperti/facilities FEL

- … da iniziare
- Upgrade di LCLS (LCLS2) pare che vada verso macchina in continua a ~1 MHz.