RD53 and CHIPIX65: Pixel FE-chip for HL_LHC

L. Demaria (INFN Torino)

on behalf of CMS and ATLAS Collaborations, RD53 and CHIPIX65
Talk layout

- HL_LHC challenges for pixel FE-chip
- RD53 Collaboration
  - Description, status and outlook
- INFN Contribution
  - CHIPIX65 project
- Conclusions
Phase 2 pixel challenges

**HL_LHC LUMINOSITY:**
- Instant ➔ Very high particle rates: 500MHz/cm²: pixel rates: 1-2 GHz/cm²
- Integrated ➔ Unprecedented hostile radiation: 10MGy(1Grad), 10^{16} n(eq)/cm²

**Maintain detector performance**
- Smaller pixels: (25–50 x100 um²): good resolution; improved two track resolution
- Low threshold: 2500 e⁻ → 1000e⁻ (less signal from sensor)
- Low mass --> Low power: less average power per pixel

**L1 challenges:**
- Increased rate: 100kHz → 1MHz
- Increased trigger latency ➔ 3 to 20 usec
- Contribution to first/second level trigger?

<table>
<thead>
<tr>
<th>PARAMETER or FEATURE</th>
<th>1st generation LHC phase 0</th>
<th>2nd generation LHC Phase 1</th>
<th>3rd generation LHC Phase 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>CMOS technology</td>
<td>250nm</td>
<td>250nm / 130nm</td>
<td>65nm</td>
</tr>
<tr>
<td>Max Particle Flux</td>
<td>~50 MHz/cm²</td>
<td>~200 MHz/cm²</td>
<td>~500 MHz/cm²</td>
</tr>
<tr>
<td>Max Pixel Flux</td>
<td>200 MHz/cm²</td>
<td>600 MHz/cm²</td>
<td>2 GHz/cm²</td>
</tr>
<tr>
<td>Rad. Hardness</td>
<td>1.5 M Gy</td>
<td>3.5 M Gy</td>
<td>10 M Gy</td>
</tr>
<tr>
<td>Pixel Dimension</td>
<td>100x150 μm², 50x400 μm²</td>
<td>100x150 μm², 50x250 μm²</td>
<td>25x150 μm², 50x100 μm²</td>
</tr>
<tr>
<td>Signal Threshold</td>
<td>2500-3000 e⁻</td>
<td>1500-2000 e⁻</td>
<td>~1000 e⁻</td>
</tr>
<tr>
<td>L1 Trigger Latency</td>
<td>2-3 μs</td>
<td>4-6 μs</td>
<td>6-20 μs</td>
</tr>
<tr>
<td>L1 Trigger Rates</td>
<td>100 KHz</td>
<td>~100 KHz</td>
<td>200-1000 kHz</td>
</tr>
<tr>
<td>L1 Trigger contribution</td>
<td>no</td>
<td>no</td>
<td>clustering info @L0 self-triggering</td>
</tr>
<tr>
<td>ASIC side</td>
<td>~1 cm²</td>
<td>~4 cm²</td>
<td>1-4 cm²</td>
</tr>
<tr>
<td>Hit memory per chip</td>
<td>0.1 Mb</td>
<td>1 Mb</td>
<td>~16 Mb</td>
</tr>
<tr>
<td>Chip output bandwidth</td>
<td>~40 Mb/s</td>
<td>~320 Mb/s</td>
<td>~3 Gb/s</td>
</tr>
<tr>
<td>Power Budget</td>
<td>~0.3 W/cm²</td>
<td>~0.3 W/cm²</td>
<td>&lt;0.4 W/cm²</td>
</tr>
</tbody>
</table>

Hybrid pixel detector:
- fast, low power electronics
- Lot of data storage needed ➔ local buffering

➔ higher VLSI integration, beyond CMOS 130nm
Why CMOS 65nm for HEP?

- Use of strong industrial technology looking to industrial standards in planar technology, accessible to HEP community.

- CMOS 130nm is today the top technology in HEP, next technology nodes are 90nm, 65nm, 40nm, 28nm.
  - 90nm is not a solid technology node (not much used);
  - 28 and 40nm are too expensive and radiation hardness is not obvious, since it uses dielectric other than SiO$_2$.

- CMOS 65nm is chosen.
  - Clear and substantial gain (see next slide)
  - Stable technology node: long-lifetime
  - Still affordable
  - Uses SiO$_2$ as inter-dielectric that is known ok for radiation damage.

Technology gap: HEP late compared to real-life applications.
What we gain using CMOS 65nm

- **Radiation Tolerance** (dose, hadrons, SEU)
  - Uses thin gate oxide
  - Verified for up to 200 Mrad, better than 130nm: to be confirmed for 1 GRad

- **Large amount of digital logic/memory**
  - Vital for small pixel
  - Logic density: 250nm:~1; 130nm:~4x; **65nm:**~16x
  - Speed: 250nm~1, 130nm~2x; **65nm:**~4x

- **Low power (digital)**
  - 250nm: 1, 130nm: (1/2-1/4); **65nm:** (1/8-1/16)

- **Many metal(Cu) layers**:
  - Power distribution, signal distribution, pixel readout busses, etc.

- **Affordable (still...)**
  - **MPW** from foundry and Europractice;
  - Masks cost a lot: ~1 M$ for an engineering RUN
  - Production similar as 130nm

---

L. Demaria: CHIPX65 pixel FE for HL_LHC - INFN Future Detector Workshop 2014

12 March 2014
RD53: ATLAS-CMS pixel ROCs

- A group of Institutes from CERN Member and non-Member States, and CERN, have agreed to collaborate to form the RD53 Collaboration for the development of pixel readout integrated circuits for extreme rate and radiation.

- Letter of Intent CERN-LHCC-2013-008 (LHCC-P-006) presented at LHC Committee on June 12th, 2013 and received the recommendation to create a RD group.

- The CERN Research Board approved the RD53 Collaboration at its 205th meeting on August 28th, 2013.

- RD53 is now a recognized “experiment”

<table>
<thead>
<tr>
<th>Country</th>
<th>Town</th>
<th>Institute</th>
<th>Representative</th>
<th>Experiment</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 Czech</td>
<td>Prague</td>
<td>(FNSPE-CTU / IP-ASCR)</td>
<td>Miroslav Havranek</td>
<td>ATLAS</td>
</tr>
<tr>
<td>2 France</td>
<td>Marseille</td>
<td>CPPM</td>
<td>Alexandre Rozanov</td>
<td>ATLAS</td>
</tr>
<tr>
<td>3 France</td>
<td>Paris</td>
<td>LPNHE</td>
<td>Giovanni Calderini</td>
<td>ATLAS</td>
</tr>
<tr>
<td>4 France</td>
<td>(Paris)</td>
<td>(Omega / LAL)</td>
<td>A Loumis / C De La Taille</td>
<td>ATLAS</td>
</tr>
<tr>
<td>5 Germany</td>
<td>Bonn</td>
<td>Bonn University</td>
<td>Hans Krüger</td>
<td>ATLAS</td>
</tr>
<tr>
<td>6 Italy</td>
<td>Bari</td>
<td>INFN and Politecnico</td>
<td>Flavio Loddo</td>
<td>CMS</td>
</tr>
<tr>
<td>7 Italy</td>
<td>(Milano)</td>
<td>INFN and University</td>
<td>Valentino Liberati</td>
<td>ATLAS</td>
</tr>
<tr>
<td>8 Italy</td>
<td>Padova</td>
<td>INFN and Politecnico</td>
<td>Dario Bisello</td>
<td>CMS</td>
</tr>
<tr>
<td>9 Italy</td>
<td>Pavia</td>
<td>INFN and University</td>
<td>Valerio Re</td>
<td>CMS</td>
</tr>
<tr>
<td>10 Italy</td>
<td>Perugia</td>
<td>INFN and University</td>
<td>Gian Mario bilei</td>
<td>CMS</td>
</tr>
<tr>
<td>11 Italy</td>
<td>Pisa</td>
<td>INFN and University</td>
<td>Fabrizio Palla</td>
<td>CMS</td>
</tr>
<tr>
<td>12 Italy</td>
<td>Torino</td>
<td>INFN and University</td>
<td>Natale Demaria</td>
<td>CMS</td>
</tr>
<tr>
<td>13 Netherlands</td>
<td>Amsterdam</td>
<td>NIKHEK</td>
<td>Nigel Hessey</td>
<td>ATLAS</td>
</tr>
<tr>
<td>14 Switzerland</td>
<td>Geneva</td>
<td>CERN</td>
<td>Jorgen Christiansen</td>
<td>ATLAS, CMS, CLIC4p</td>
</tr>
<tr>
<td>15 Switzerland</td>
<td>Villigen</td>
<td>PSI</td>
<td>Roland Horisberger</td>
<td>CMS</td>
</tr>
<tr>
<td>16 UK</td>
<td>Didcot</td>
<td>RAL Centre for Instrumentation (CFI)</td>
<td>Mark Prydcher</td>
<td>CMS/ATLAS</td>
</tr>
<tr>
<td>17 USA</td>
<td>Chicago</td>
<td>Fermilab</td>
<td>David Christian</td>
<td>CMS</td>
</tr>
<tr>
<td>18 USA</td>
<td>Berkeley</td>
<td>LBNL</td>
<td>Maurice Garcia-Sciveres</td>
<td>ATLAS</td>
</tr>
<tr>
<td>19 USA</td>
<td>New Mexico</td>
<td>University of New Mexico</td>
<td>Sally Seidel</td>
<td>ATLAS</td>
</tr>
<tr>
<td>20 USA</td>
<td>Santa Cruz</td>
<td>U.C. Santa Cruz</td>
<td>Alex Grillo</td>
<td>ATLAS</td>
</tr>
</tbody>
</table>
Scope of RD53 Collaboration

- The development of pixel readout Integrated Circuits (IC) for the next generation of pixel readout chips to be used for the ATLAS and CMS Phase 2 pixel detector upgrades and future CLIC pixel detectors.

- This does not imply that ATLAS and CMS must use the same exact pixel readout chip, as most of the development, test and qualification effort needed is independent of the specific implementation of the final chips.
  - Multiple implementations are possible using the same technology foundation. In order to be effective, this collaboration is specifically focused on the design of pixel readout chips, and not on more general chip design or on other aspects of pixel technology.

- The IC challenges include: smaller pixels to resolve tracks in boosted jets, very high hit rates, unprecedented particle fluence, much higher output bandwidth, and large IC format with low power consumption in order to instrument large areas while keeping the material budget low.

- Although data rates, radiation levels, and trigger requirements are different, there is synergy with the development of pixel detectors for future $e^+e^-$ linear collider detectors and therefore collaboration is foreseen.
Main Bodies of the Collaboration:
- Collaboration/Institute Board
- Management Board
- Working Groups

Status
- Regular CB and management meetings have started
- RD53 workshop: April 10-11 at CERN
- MOU in the pipeline
- Working groups have regular meetings

<table>
<thead>
<tr>
<th>No.</th>
<th>Name</th>
<th>Role</th>
<th>Town / Group</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Jorgen Christiansen</td>
<td>Spokesperson for CMS</td>
<td>CERN</td>
</tr>
<tr>
<td>2</td>
<td>Maurice Garcia-Sciveres</td>
<td>Spokesperson for ATLAS</td>
<td>LBNL</td>
</tr>
<tr>
<td>3</td>
<td>Natale Demaria</td>
<td>CB Chair</td>
<td>INFN-Torino</td>
</tr>
<tr>
<td>4</td>
<td>Marlon Barbero</td>
<td>WGC - Radiation qualification</td>
<td>Marseille</td>
</tr>
<tr>
<td>5</td>
<td>t.b.d.</td>
<td>WGC - Top Level Design</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>Tomaz Hemperek</td>
<td>WGC - Simulation Test Benches</td>
<td>Bonn</td>
</tr>
<tr>
<td>7</td>
<td>t.b.d.</td>
<td>WGC - I/O</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>Valerio Re</td>
<td>WGC - Analog Design</td>
<td>Bergamo/Pavia</td>
</tr>
<tr>
<td>9</td>
<td>t.b.d.</td>
<td>WGC - IP Blocks</td>
<td></td>
</tr>
</tbody>
</table>

WG1 Radiation test/qualification
- Qualification of technology to 10 MGy TID, $10^{13}$ n.eq/cm². Transistor simulation models after irradiation. Evaluation of logic cell libraries after irradiation. Expertise on radiation effects in 65nm

WG2 Top level design
- Design methodology, verification and test of ~5 x 10³ transistor IC. Analog integration in large digital chip. Power distribution Synthesis constraints. Clock distribution and optimization

WG3 Simulation and verification test bench
- System Verilog simulation and Verification framework. Optimization of global architecture/pixel regions/pixel External system and external physics data. Verification of test chips and evolving designs

WG4 I/O
- Definition of readout and control interfaces (e.g. LPGBT). Definition of standardized I/O protocols and performance Implementation of readout and control interface blocks. Standardized interfaces: Control, Readout, etc.

WG5 Analog design
- Evaluate and compare alternate amplifier designs.
- Evaluate and compare charge ADC techniques vs. number of bits (TOT, shared ADC, etc.)

WG6 IP blocks
- Define common requirements for IP block design. Evaluate, document, and keep library of IP blocks
- Generate overview and recommendations. Each block will have its own prototyping milestones
RD53 WG status/progress

- **RADIATION:**
  - Systematic radiation testing program has started for 1Grad TID
  - **PMOS** transistors have shown significant degradation, relevant for digital electronics (minimum size)
    - Some mysteries to be understood/resolved
    - New unexplored territory (e.g. space $10^{-4}$ less radiation)
  - **Annealing scenario critical** (e.g. running pixel cold)

- **ANALOG:**
  - Front-end specs under definition
  - A large set of front-end architectures will be evaluated, designed and tested.

- **IPs:**
  - ~30 IP blocks have been defined
  - Good progress on defining who makes what.
  - Needs to define how to make IPs

- **SIMULATION:**
  - Prototype framework implemented in system Verilog + UVM
  - Benchmarked tool chain with FEI4 behavioural and gate level model
  - Framework will be used for initial comparison of different latency buffer architectures (critical for CMS with long trigger latency)
  - Starting to work on making realistic hit patterns/rates and link to Geant 4 simulations

- **TOP:**
  - Discussions have started on appropriate design methodology to implement large complex mixed signal IC.
  - Global architecture proposals will be collected and a program to compare/simulate these will be defined.

- **IO:** Not yet started
RD53 Outlook

2014:
- Release of CERN 65nm design kit: Very soon!
- Detailed understanding of radiation effects in 65nm
  - Radiation test of few alternative technologies.
  - Spice models of transistors after radiation/annealing
- IP block responsibilities defined and appearance of first FE and IP designs/prototypes
- Simulation framework with realistic hit generation and auto-verification.
- Alternative architectures defined and efforts to simulate and compare these defined
- **Common MPW submission 1:** First versions of IP blocks and analog FEs

2015:
- **Common MPW submission 2:** Near final versions of IP blocks and FEs.
- **Final versions of IP blocks and FEs:** Tested prototypes, documentation, simulation, etc.
- IO interface of pixel chip defined in detail
- **Global architecture defined and extensively simulated
- **Common MPW submission 3:** Final IPs and Fes, Small pixel array(s)

2016:
- Common **engineering run:** Full or reduced sized pixel arrays(s).
- Pixel chip tests, radiation tests, beam tests

2017:
- Separate or common ATLAS – CMS full – final pixel chip submissions.
RD53 Chip architecture

Pixels: ~256k, Chip size = ~2.6cm x ~3cm
~1G transistors, ~3Watt (~10uW per pixel; 0.4 W/cm²)

ReadOut and Configuration: assumption is to use the Low Power version of GBT, called LP-GBT and under-development in 65nm (up to 10 Gb/s output; 5 Gb/s input)
Constrains on FE-chip:
CMS case for L1@1 MHz

1–8 data links: 0.32–1.2 Gbits/s
2-10m cable driver with pre-emphasis

1 control link: 320 Mbits/s
Cable equalizer

Power: 3 – 6 W

Overall Band Width defined by the L1 trigger rate and the Band Width of LP-GBT:
4x1 CHIP modules in L1, with TWO LP-GBT

LP-GBT well outside Pixel:
Lots of cable but less cooling

LP-GBT on module: rad-hard? Power and cooling increased, cable. Place for LP-GBT
INFN interest in Pixel-FE

- Started on year 2010 with four CMS institutes (To, Pg, Pi, Pd) and on 2011 we had approved an initial funding. Collaboration with FNAL already started.

- On 2013 six INFN institutes took part to the foundation of **RD53 Collaboration**: Bari, Padova, Pavia, Perugia, Pisa, Torino

- On 2013 the Scientific Committee of INFN for Technological Research launched a call for large R&D projects and we submitted the proposal **CHIPiX65** that eventually was selected in October 2013. In the project both CMS and ATLAS groups/members were invited
  - Milano group joined, has large experience in 65nm with the FTK Atlas project

NB: if you see few names cited in slides are those of PhD students or young PostDoc working actively to the shown item (together with experienced staff)
CHIPIX65 CALL Project Proposal 2013 – CSN5

Principal Investigator: L. Demaria

Project Outline (from Project Abstract)

- The goal of this three years project is the development of an innovative CHIP for a PIXEL detector, using a CMOS 65nm technology for the first time in HEP community, for experiments with extreme particle rates and radiation at future High Energy Physics colliders. New circuits will be built and characterized, a digital architecture will be developed and eventually a final assembly of a first prototype will be made.

- CHIPIX65 a unique opportunity for an efficient propagation across INFN of CMOS 65nm technology and constitutes the greatest collaboration on a microelectronics project ever made across INFN.

Participant Research Units: Bari, Milano, Padova, Pavia, Perugia, Pisa, Torino

35 members of which 20 are micro-electronics designers. 9.85 FTE. 6 units involved in CMS, 1 in ATLAS. New members from this year (2 new PhD students)

Work Packages:

- Radiation Hardness – P. Giubilato (Padova)
- Digital Electronics – R. Beccherle (Pisa)
- Analog Electronics – A. Rivetti (Torino)
- Chip Integration – V. Re (Pavia/Bergamo), V. Liberali (Milano)

International Collaborations / supports: RD53, ATLAS, CMS – All wrote support letters

Funding: ~700 kEuro for a three year project, subject to yearly peer review (milestones achieved).

- Mainly consumables and foundry submissions, no man power.
CHIPIX65 + RD53/INFN members

- **Bari**: Fabio Ciciriello, Francesco Corsi, Giuseppe De Robertis, Flavio Loddo, Camillo Tamma, F.Liciulli, Cristoforo Marzocca

- **Milano**: Valentino Liberali, Seyedruhollah Shojaii, Alberto Stabile

- **Padova**: Marta Bagatin, Dario Bisello, Lili Ding, Piero Giubilato, Alessandro Paccagnella, Nicola Bcchetta, Martino Dall’Osso, Stefano Gerardin, Andrea Neviani, Alessandro Paccagnella, Daniele Vogrid, Jefferey Wyss

- **Pavia/Bergamo**: Francesco De Canio, Lorenzo Fabris, Luigi Gaioni, Massimo Manghisoni, Valerio Re, Gianluca Traversi, Carla Vacchi, Alessia Mannazza, Lodovico Ratti, Stefano Zucca

- **Perugia**: Gian Mario Bilei, Elia Conti, Mauro Menichelli, Daniele Passeri, Pisana Placidi, Sara Marconi

- **Pisa**: Fabrizio Palla, Guido Magazzu, Fabio Morsani, Roberto Beccherle, Massimo Minuti, Maria Teresa Gripppo, Luca Fanucci, Ronaldo Bellazzini, Andrea Rizzi, Sergio Saponara

- **Torino**: Natale Demaria, Pierluigo Civera, LucaPacher, Angelo Rivetti, Manuel Rocha Rolo, Ennio Monteil, Gianni Mazza
## CHIPIX65: Main Contributions to RD53

<table>
<thead>
<tr>
<th>Location</th>
<th>Radiation Hardness</th>
<th>Simulation Test Benches</th>
<th>Analog Front End</th>
<th>IP-Blocks (see next slide)</th>
<th>I/O</th>
<th>Top Level</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bari</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>yes</td>
<td>To be discussed in RD53</td>
</tr>
<tr>
<td>Milano</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>yes</td>
<td>To be discussed in RD53</td>
</tr>
<tr>
<td>Padova</td>
<td></td>
<td>X-ray machine SIRAD facility</td>
<td></td>
<td></td>
<td>yes</td>
<td>To be discussed in RD53</td>
</tr>
<tr>
<td>Pavia</td>
<td></td>
<td>Design of VFE</td>
<td></td>
<td></td>
<td>yes</td>
<td>To be discussed in RD53</td>
</tr>
<tr>
<td>Perugia</td>
<td></td>
<td>Expertise in space rad-hard</td>
<td>Architectural studies</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Pisa</td>
<td></td>
<td>Clustering, L1</td>
<td></td>
<td></td>
<td>yes</td>
<td></td>
</tr>
<tr>
<td>Torino</td>
<td></td>
<td>Design of VFE</td>
<td></td>
<td></td>
<td>yes</td>
<td></td>
</tr>
</tbody>
</table>

Additional contribution to I/O and Top Level are foreseen.
Characterization of the technology at the required radiation levels is of fundamental importance for the experiment. In particular:

- **TID (Total Ionising Dose)** Total effects on test structures and then on transistors at standard, reference,
  - X-ray machine
  - CN accelerator at LNL (low energy protons)

- **DD (Displacement Damage)** effects by exposing test structures to proton and neutron beams.
  - the SIRAD irradiation facility at the LNL Tandem+ALPI accelerator system
  - The CN accelerator at LNL

- **Sensitivity to SEE (Single Event Effects)** of logic cells with ion beams, in particular to
  - ion beams at the SIRAD+IEEM irradiation facility at the LNL Tandem+ALPI accelerator system

At \( D=1 \text{ cm} \) from the sample with \( I=50 \text{ mA} \) it is possible to reach \( 2000 \text{ rad(Si)/s} \) (7.2 Mrad(Si)/h or 4.2 Mrad/h (SiO}_2\) on a square area \( 5 \text{ mm}^2 \).

1w to reach 1 GRad
Protons at CN Accelerator (Laboratori Nazionali di Legnaro)

- Monoenergetic protons with energy between 2 MeV and 6 MeV
- Maximum proton current $\sim 1 \mu A$ (1 Grad can be reached in few hours, if needed)
- Samples are placed in a vacuum chamber
- Used for total ionizing dose and displacement damage studies in electronic chips for space applications

First irradiation of CMOS 65nm test structures with low energy protons for Total Dose study. Few TID points will be taken, up to 1 Grad and for few Identical test structures

Planned for 31st March
CHIPIX65: Digital architecture

- Single pixel region with custom number of pixels
- PR buffer is an array of SystemVerilog queues

Verification Environment

Used Universal Verification Methodology (UVM)
CHIPIX65: Very Front End

- Amplifier (CSA) with different feedback architectures (Krummenacher, Constant current, Discrete time)
- Asynchronous front-end (Bg/Pv)
- Synchronous front end (Torino)
  - Off-set compensation (Self-Calibration of threshold trimming)
- Different Signal Measurement
  - ToT-based, ADC, binary
- Signal injection and calibration

![Graph showing ENC vs. total input capacitance](image1)

**ENC vs. total input capacitance**

- (~100fF planar, ~300fF 3D sensors)
- Preamp Noise

**MIP signal**

(10ke and 100fF input capacitance)

- Noise floor ~2 mV RMS
- (120e RMS ENC)

L.Pacher, E.Monteil (Torino)
Very Front End: synchronous comparator

- Always in-time answer
- No discriminator delay (threshold timewalk)
- Possibility of threshold variation self-calibration

>50% efficient for 1000e- signal

Tested for mismatch (process variations)

HIT generation

Input signal to Latch

CSA output (1000e-)

25ns strobe to comparator
Very Front End: self compensation of threshold variation

- No need for off-line calculation of threshold trimming
- Trimming calibration done by hardware (calibration cycle)
  - Process variation causing ~1500e- peak-to-peak threshold variation, normally corrected by off-line threshold trimming
  - Self-calibration compensate for those variation (<500e- peak-to-peak)
Out of 34 IP-block identified in RD53, INFN has proposed to contribute at ~16 of them:

- as main organizer (11)
- as participant (5)

In the following few slides on first prototypes ready for submission in a short time (design in 65nm already present):
- Band-Gap
- SLVS driver
- SRAM

others IP-blocks could be ready for end of year

<table>
<thead>
<tr>
<th>Group</th>
<th>Bari</th>
<th>Pav/Berg</th>
<th>Milano</th>
<th>Padova</th>
<th>PiSal</th>
<th>Torino</th>
</tr>
</thead>
<tbody>
<tr>
<td>ANALOG: Coordination with analog WG</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Temperature sensor</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Radiation sensor</td>
<td>to be evaluated</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Band gap reference</td>
<td>O</td>
<td>O</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MIXED</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>8 - 12 bit biasing DAC</td>
<td>O</td>
<td>O</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>10 - 12 bit slow ADC for monitoring</td>
<td>O</td>
<td>O</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PLL for clock multiplication</td>
<td>P</td>
<td>P</td>
<td>P</td>
<td>P</td>
<td></td>
<td></td>
</tr>
<tr>
<td>High speed serializer (~Gbit/s)</td>
<td>P</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(Voltage controlled Oscillator)</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DIGITAL</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SRAM for pixel region</td>
<td>O</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SRAM/FIFO for EOC.</td>
<td>P</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DICE storage cell ?</td>
<td>O</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LP Clock driver/receiver</td>
<td>P</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(Dedicated rad hard digital library)</td>
<td>to be clarified</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(compact mini digital library for pixels)</td>
<td>to be clarified</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>IO: Coordination with IO WG</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Low speed SLVS driver (&lt;100MHz)</td>
<td>O</td>
<td>O</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>High speed SLVS driver (~1Gbits/s)</td>
<td>O</td>
<td>O</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SLVS receiver</td>
<td>O</td>
<td>O</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>POWER</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LDO(s)</td>
<td>P</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SOFT IP: Coordination with IO WG</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Control and command interface</td>
<td>O</td>
<td></td>
<td></td>
<td></td>
<td>O*</td>
<td></td>
</tr>
<tr>
<td>Readout interface (E-link ?)</td>
<td>O</td>
<td></td>
<td></td>
<td></td>
<td>O*</td>
<td></td>
</tr>
</tbody>
</table>
Band Gap reference ($P_v$)

- State of the art at $P_v$:
  - Sub 1V operation bandgap voltage reference - 3 versions
    - (1) BJT version; (2) Diode version; (3) MOS WI version
  - Layouts ready
  - Evaluate their performance and study their radiation hardness
Low-Medium / High speed SLVS* driver (Pv, To, Pi)

• **PAVIA**
  - Design of low-voltage differential signaling driver + receiver with supply voltage of 1.2V (with only core transistors)
  - Present activity:
    - Design 1: 320MHz frequency operation with maximum power consumption=1.25 mW
    - Design 2: 640MHz frequency operation with maximum power consumption=2.5 mW
  - Schematics of the TX and RX were obtained by a merging of the UniBG and CERN version (in 130nm IBM) provided by Kostas

• **Torino**
  - There are design in 130nm for Panda (ToPix) that goes to 1 GHz and could be translated in 65nm

• **Pisa** is also interested

(*) Scalable Low Voltage Signaling – variant of LVDS
DICE RAM Cell (Mi)

- Interest of Milano (in CHIPIX65, applying for RD53) to develop radiation hard SRAM

- array of 256x256 DICE (Dual Interlocked storage Cell) RAM cells almost ready for integration. It comes from a work done in AIDA. Size of about 1.8x3.3 $\text{um}^2$

- Layout made in three different version, one smaller (size about 1.8x3.3 $\text{um}^2$) the other more resistant to latch-up and/or Single Event Upset

- This could be used either in the Pixel Unit Cell or in the End Of Colum
### CHIPIX65 Milestones

<table>
<thead>
<tr>
<th>Descrizione</th>
<th>Data completamento</th>
</tr>
</thead>
<tbody>
<tr>
<td>Results on Basic radiation test structures</td>
<td>30-10-2014</td>
</tr>
<tr>
<td>Test results on first Analog Blocks and Very Front End chain</td>
<td>30-11-2014</td>
</tr>
<tr>
<td>Test of digital basic IP blocks</td>
<td>30-09-2015</td>
</tr>
<tr>
<td>Digital architecture: pixel/region basic models in SystemVerilog</td>
<td>30-07-2015</td>
</tr>
<tr>
<td>Definition of Very Front End analog architecture</td>
<td>30-09-2015</td>
</tr>
<tr>
<td>Measurement with ion beam of SEU rate in digitasl cells</td>
<td>30-11-2015</td>
</tr>
<tr>
<td>Qualification of 65nm technology to 10 MGy TID, 10**16 n/cm2</td>
<td>30-11-2015</td>
</tr>
<tr>
<td>Ready for chip integration of prototype</td>
<td>15-12-2015</td>
</tr>
<tr>
<td>Definition of digital Architecture of chip Prototype</td>
<td>30-03-2016</td>
</tr>
<tr>
<td>Mixed signal blocks functional and radiation test results</td>
<td>30-03-2016</td>
</tr>
<tr>
<td>Submission of prototype to foundry</td>
<td>30-07-2016</td>
</tr>
<tr>
<td>Test results of chip prototype</td>
<td>30-10-2016</td>
</tr>
<tr>
<td>Final Report</td>
<td>10-12-2016</td>
</tr>
</tbody>
</table>

2014: measurement of basic structure for WP1; design and testing for WP2, WP3.

2015: TID and SEU characterization (WP1); definition of architecture (WP2, WP3); ready for chip integration

2016: results on small pixel array; design of small chip prototype, its submission and test.
CHIPIX65 SUBMISSIONs for 2014

- INFN / CHIPIX65 is foreseeing to submit designs on silicon to the foundry via MPW:
  - Small pixel matrix for studies of Very Front End analog designs
    - Synchronous front end
      - Binary, off-set compensated
      - Fast ToT
    - Asynchronous FE
  - IP-block prototypes

For the pixel matrix important to establish the PUC dimension (25x100, 50x50 ?). to make the pixel matrix bump-bondable to a silicon sensor: this should be better evaluated.

Earliest submission: July 2014, Area: ~\(3\times4\)mm\(^2\).

- Other submissions: possibly sharing with other collaborators (specially for IP-blocks). Open discussion in within CMS and RD53.
Conclusions

- INFN contribution to innovative pixel chip well structured and with presence of reputed experts in the field
  - CHIPIX65 project provide excellent synergy and coordination among institutes and finance oxygen for the R&D phase

- Good participation of INFN to the RD53 Collaborative effort and in all the area needed for the chip design

- Considerable experience already in hand on CMOS 65nm via Europractice. Now the CERN contract with TSMC / IMEC design kit for 65nm in order to speed up the work of designing in CMOS 65nm

- Right timing of RD53, CHIPIX65 for the R&D phase needed to eventually go to CMS and ATLAS pixel FE-chips ready for module prototypes in ~2018

- A wide experience in the CMOS 65nm to FE-electronics is important also for research areas other than pixel at HL_LHC
BACKUP SLIDES
Pixel Upgrades

- **Phase 2 upgrades:**
  - Installation: ~ 2022-23 → *First Modules prototypes should be ready for ~2018*
  - **Pixel chip R&D:** needed NOW
  - **Pixel Sensors R&D:** needed NOW
  - 3 years of dedicated R&D + 2 years to develop first prototype modules
Installed Capacity by Technology

More than half of today’s commercial products are made with technologies beyond what HEP uses.

My Note: 0.25 um and 130nm production lines are STILL operational this makes 10-11 years of technology availability...

Source: TSMC
Example of complex IC: FEI4 chip

Made by 5 institutes (Bonn, CPPM, Genova, LBNL, NIKHEF)

Team of 14 designers

Design responsibility split in several parts (or IP-blocks):

- Shuldo
- DC-DC
- Vref
- Cref
- ADC
- Efuse
- Cal Pulse
- Alt. SEU
- Alt. Comp
- CapMeas
- ConfSR
- PLL

- DAC
- Config.Register
- Command Decoder
- **Front End**
- Digital Double Column
- End of Digital Column
- End of Chip Logic
- Data Output Block
- MUX3to1
- LVDS-rcvr
- LVDS-drivr

L. Demaria: CHIPIX65 pixel FE for HL-LHC - INFN Future Detector Workshop 2014

12 March 2014
CHIPIX65 Research Units

<table>
<thead>
<tr>
<th>Unit</th>
<th>Unit Responsible</th>
<th>FTE Unit</th>
<th>No. of members</th>
<th>No. of designer</th>
<th>Involvements in CHIPIX65</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Bari</td>
<td>LODDO Flavio</td>
<td>1.65</td>
<td>5</td>
<td>3</td>
</tr>
<tr>
<td>2</td>
<td>Milano</td>
<td>LIBERALI Valentino</td>
<td>1.0</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>3</td>
<td>Padova</td>
<td>BISELLO Dario</td>
<td>1.6</td>
<td>5</td>
<td>1</td>
</tr>
<tr>
<td>4</td>
<td>Pavia</td>
<td>TRAVERSIO Gianluca</td>
<td>1.5</td>
<td>7</td>
<td>4</td>
</tr>
<tr>
<td>5</td>
<td>Perugia</td>
<td>PLACIDI Pisana</td>
<td>1.4</td>
<td>5</td>
<td>3</td>
</tr>
<tr>
<td>6</td>
<td>Pisa</td>
<td>PALLA Fabrizio</td>
<td>1.15</td>
<td>5</td>
<td>3</td>
</tr>
<tr>
<td>7</td>
<td>Torino</td>
<td>DEMARIA Natale</td>
<td>1.55</td>
<td>5</td>
<td>3</td>
</tr>
<tr>
<td></td>
<td>TOTAL</td>
<td></td>
<td>9.85</td>
<td>35</td>
<td>20</td>
</tr>
</tbody>
</table>

Detailed short description for every unit in following slides: I will not go through all of them in detail, they are there for reference.
8-12 bit programmable biasing DAC (Ba)

- **Previous** experience of Bari:
  - Rad-hard 8-bit DAC for the slow control of the pixel chip of ALICE (250 nm CMOS)

- **In progress**: VFAT3, a new FE chip for GEM detectors for the upgrade of CMS muon detector (130 nm CMOS). Submission on Feb. 2014
  - Calibration & Bias circuitry, *8-bit thermometer coded current steering DAC*, Constant Fraction Discriminator

**Thermometer coded DAC:** 255 “identical” unit current sources connected to output node through switches controlled by a binary-to-thermometer decoder
- monotonicity is guaranteed
- matching conditions more relaxed → common centroid is not required
10-12 bit slow ADC for monitoring (Ba)

- Previous experience of Bari:
  - Two-step 8-bit ADC with max. conversion speed: 20 MS/s (0.35 \( \mu m \) CMOS)

- Correction logic for both “bubble” errors and wrong “fine” threshold selection
- Boost circuits for the clock phases applied to the CMOS switches
- Final ADC structure: two ADCs, operated in “interleaved” mode
- Total power consumption: 22.4mW
- Maximum conversion speed 20MS/s

Reference generator: resistor ladder (same as full flash ADC)

“Coarse” (MSBs) conversion phase: the “coarse” refs Vrc are compared with Vin and the “fine” refs Vrf are selected

“Fine” (LSBs) conversion phase: the selected Vrf’s are compared with Vin.

Test chip (2.18 x 1.74 mm\(^2\))
PLL and VCO design expertise (Pd, Pi, To)

- **Padova group (University of Padova – Engineering department)**
  - Research group expertise:
    - RF design, Baseband design, Testing and characterization
    - Radiation testing and qualification (Engineering department)

- Design of a 6.5-18.4 GHz PLL in 65nm CMOS for the local oscillator (LO) generation in a short-range radar front-end (M. Caruso et al., proceedings of ESSCIRC 2013)


- Design of an LC tank VCO in 90nm CMOS for a fast-hopping LO generator operating between 6 and 9 GHz based on sub-harmonic injection locking (S. dal Toso et al., IEEE Int. Solid-State Circ. Conf., 2008)

- Pisa has expertise (see later)

- Torino interested too
Serializer (Pi)

Based on experience on two ASICS designed in the IBM 130nm (2012-2013) Collaboration between INFN-PISA (Guido Magazzu) and UCSB (Physics Department and Electronic Engineering Department): Developments of radiation tolerant IP-cores for high speed serial links:

- **UCCF1** (submitted 2012)
- **UCCF2** (submission in early 2014)
- **Rescaling** of the IP-cores into the TSMC 65nm technology since February 2014 (submission of the first test ASIC foreseen in fall 2014)

- PLL and Clock Data Recovery (CDR) with Triple Modular Redundancy (TMR) to protect against Single Event Effects (SEEs)
- Same Serializer (SER) and Deserializer (DES) modules used in UCFF1

- Clock Data Recovery
- PLL with x25 frequency multiplication (input frequency = 40MHz => output frequency = 1GHz)
- Voltage Controlled Oscillator (VCO); Charge Pump (CP) => It provides the control voltage to the VCO module; Frequency Divider (1/25)
- Phase/Frequency Detector (PFD) => It compares the frequency and the phase of the input reference clock and of the local reference clock and it generates the control signals for the Charge Pump
- VCO modules (3x) => Same power supply and control voltages used in the PLL
- Low Drop-Out (LDO) regulator (providing power supply voltage to all the VCO modules)
Threshold Timewalk

- Example of FEI4 chip

20 ns timewalk for $2 \text{ ke}^{-} < Q_{in} < 52 \text{ ke}^{-}$ & threshold @ 1.5 ke$^{-}$