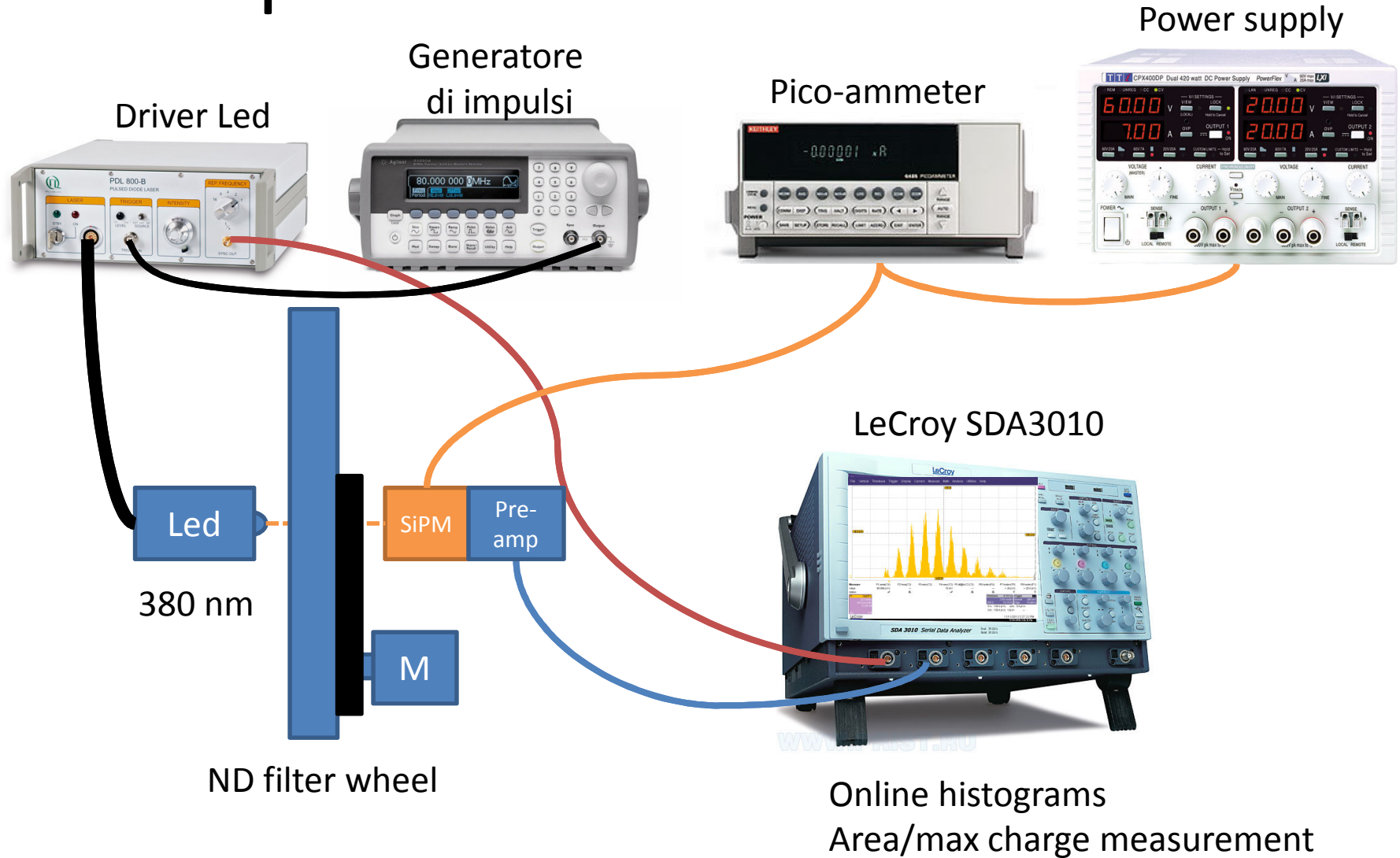


Results on Target5 (current status and future developments)

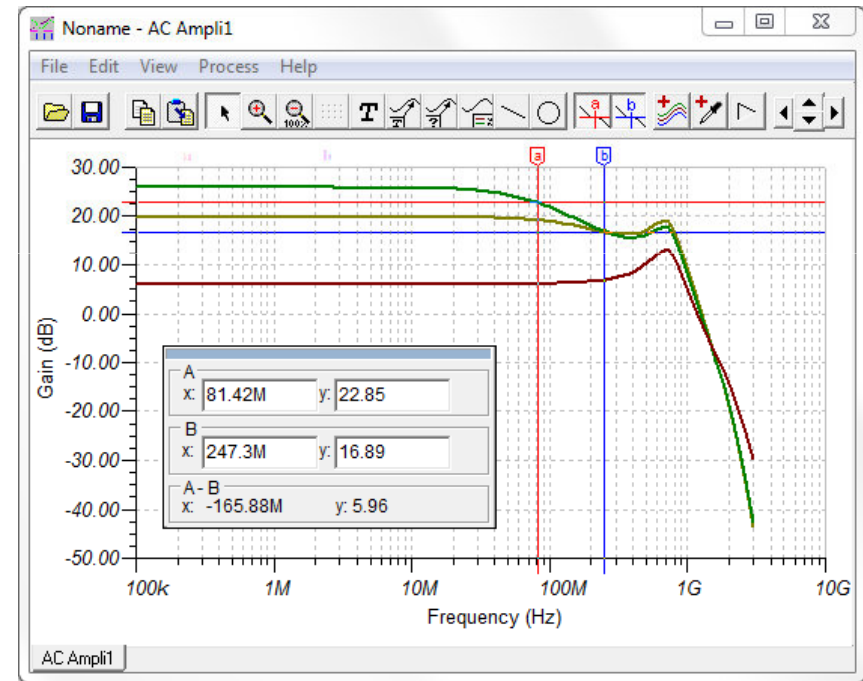
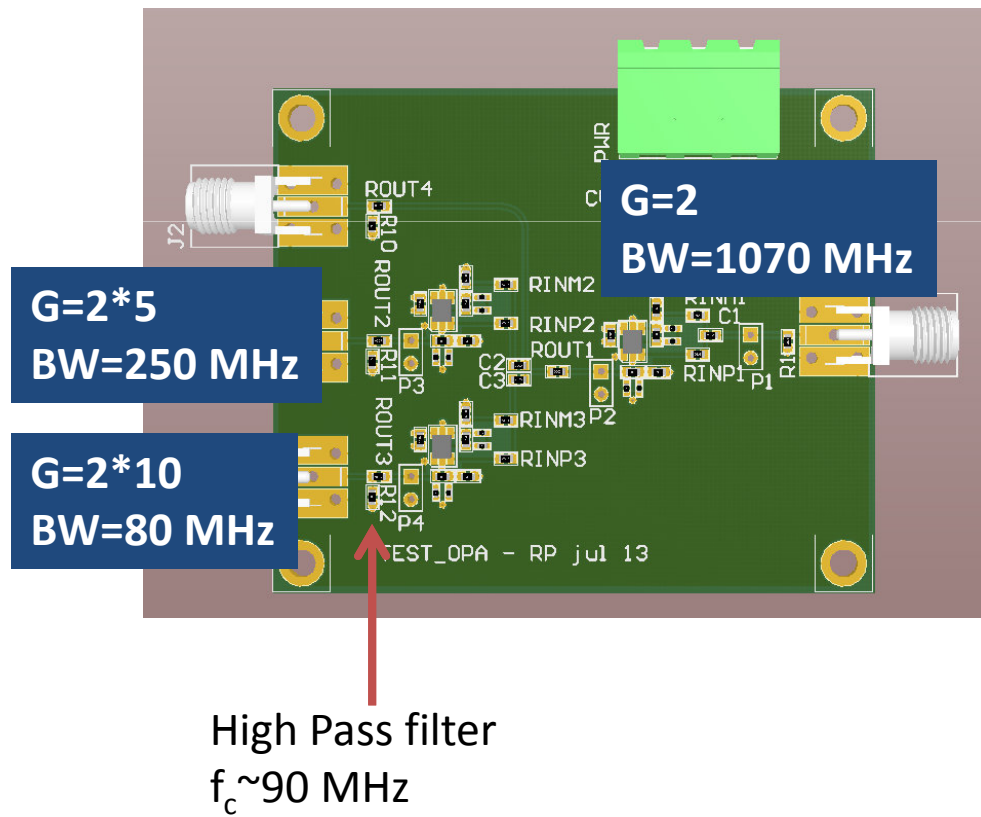
S. Zaza, R. Paoletti

SFTA Department, Physics section
University of Siena

Setup for SiPM measurements

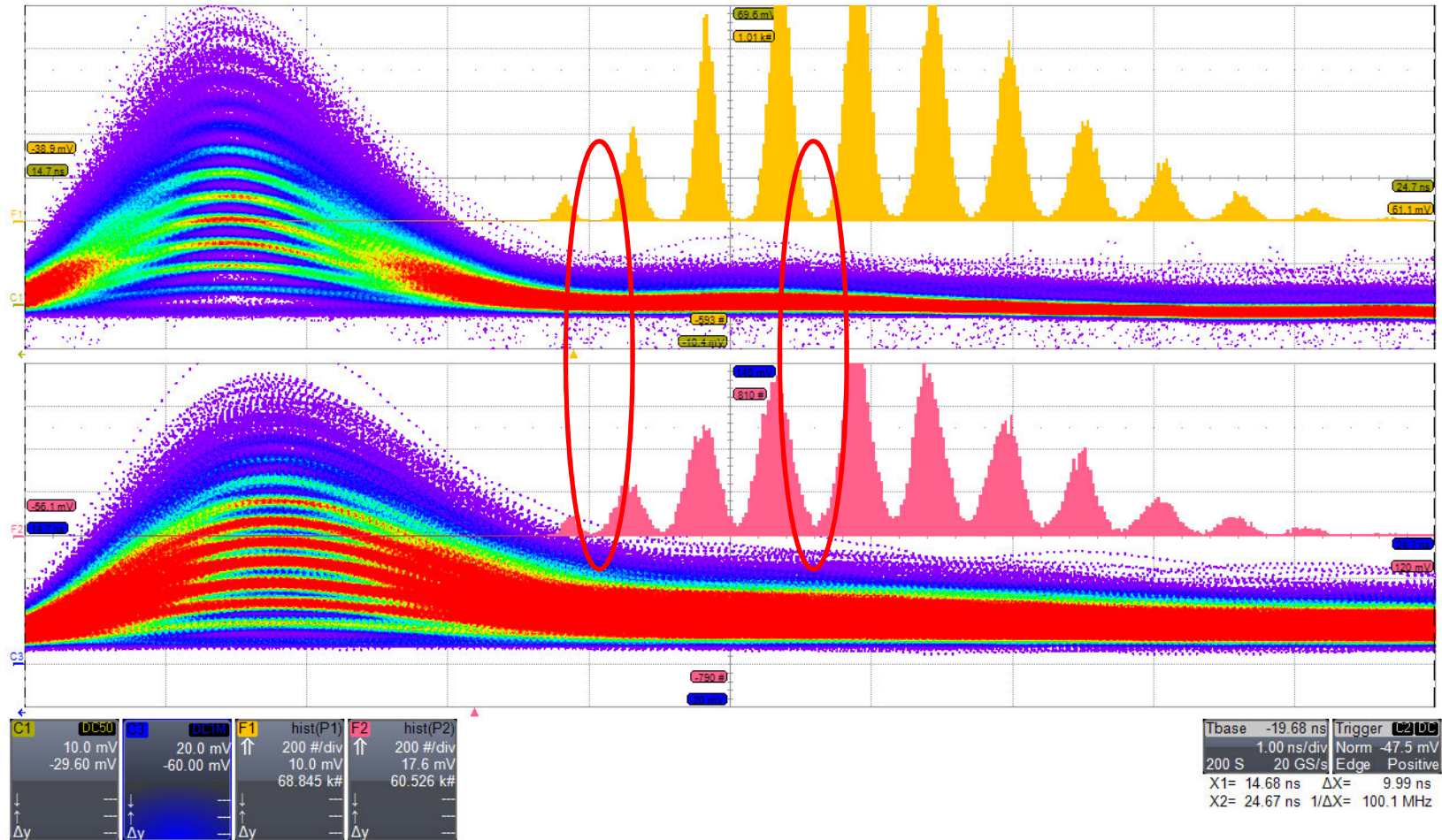


Preamplifier



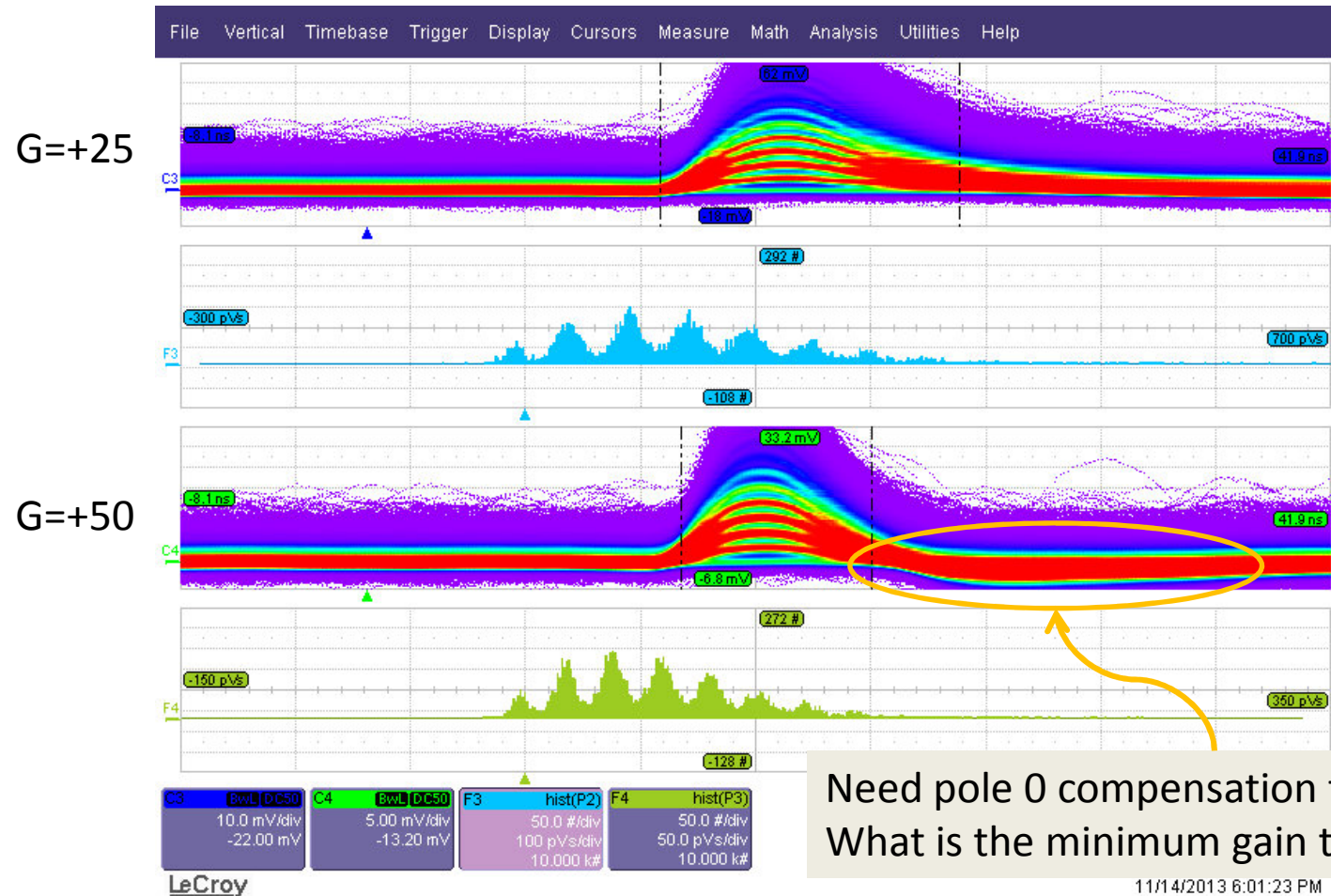
Comparison SiPM 1x1mm² NUV4

HP filter-no HP filter



NUV 3x3 mm²

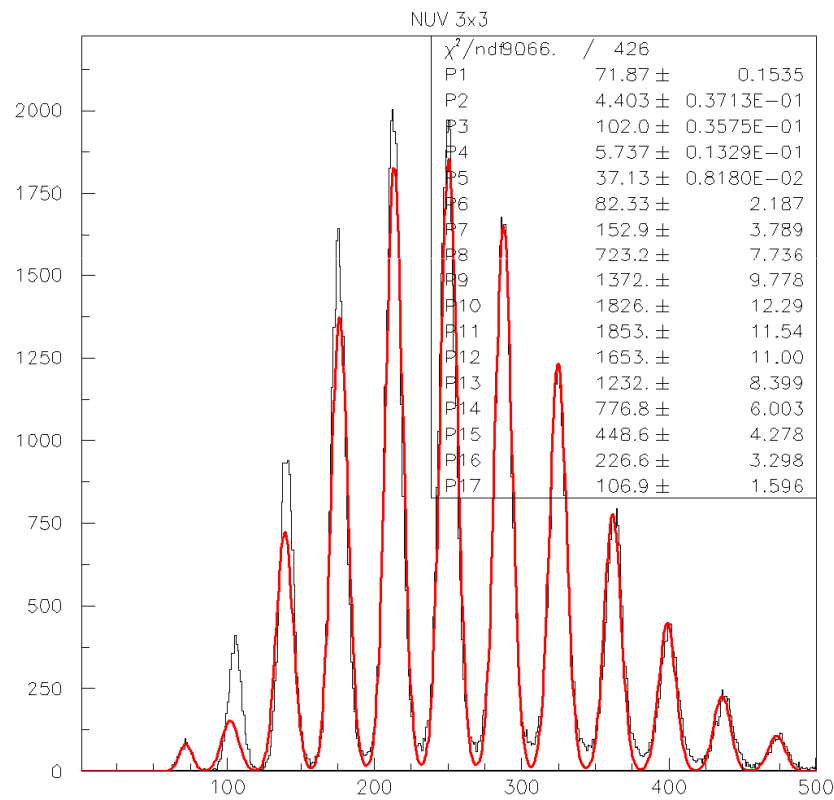
Test on pre-amp gain



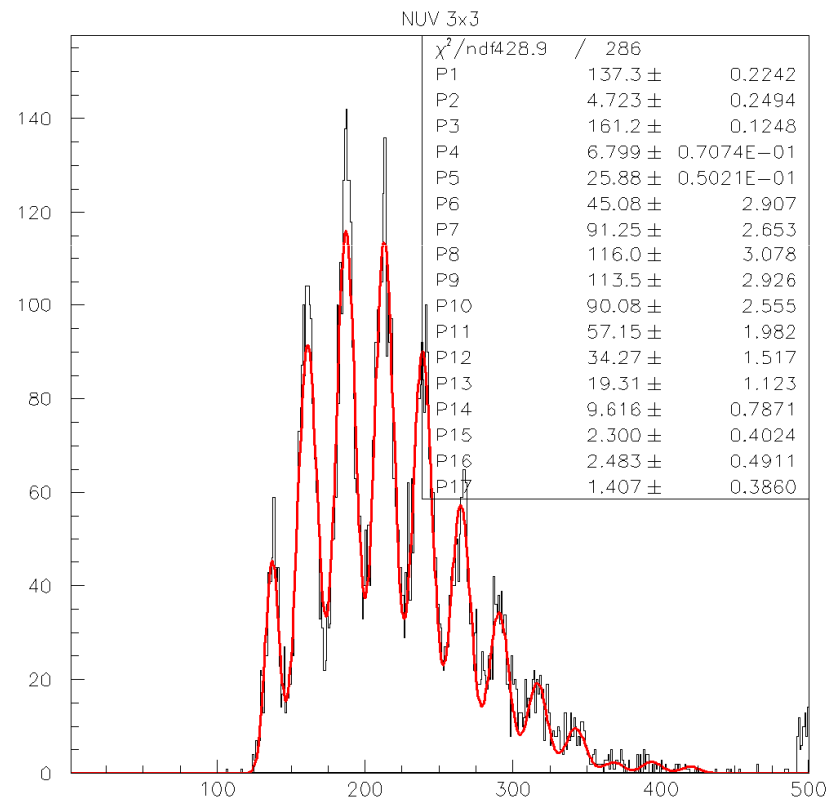
Need pole 0 compensation for high gains?
 What is the minimum gain to use? 10?

Confronto spettro

NUV4 1x1 mm²



NUV #8 3X3 mm²

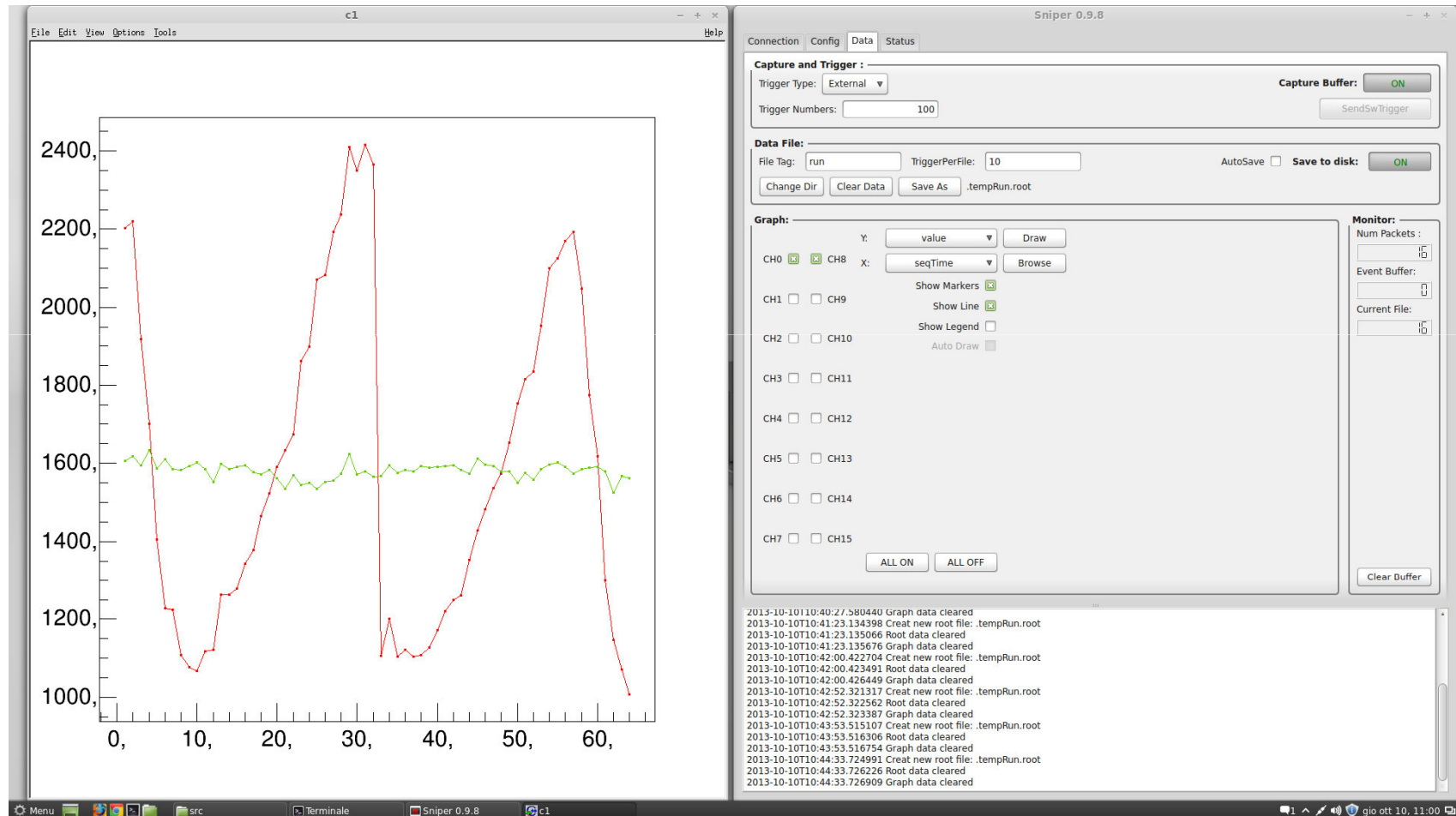


Target5 Evaluation Board

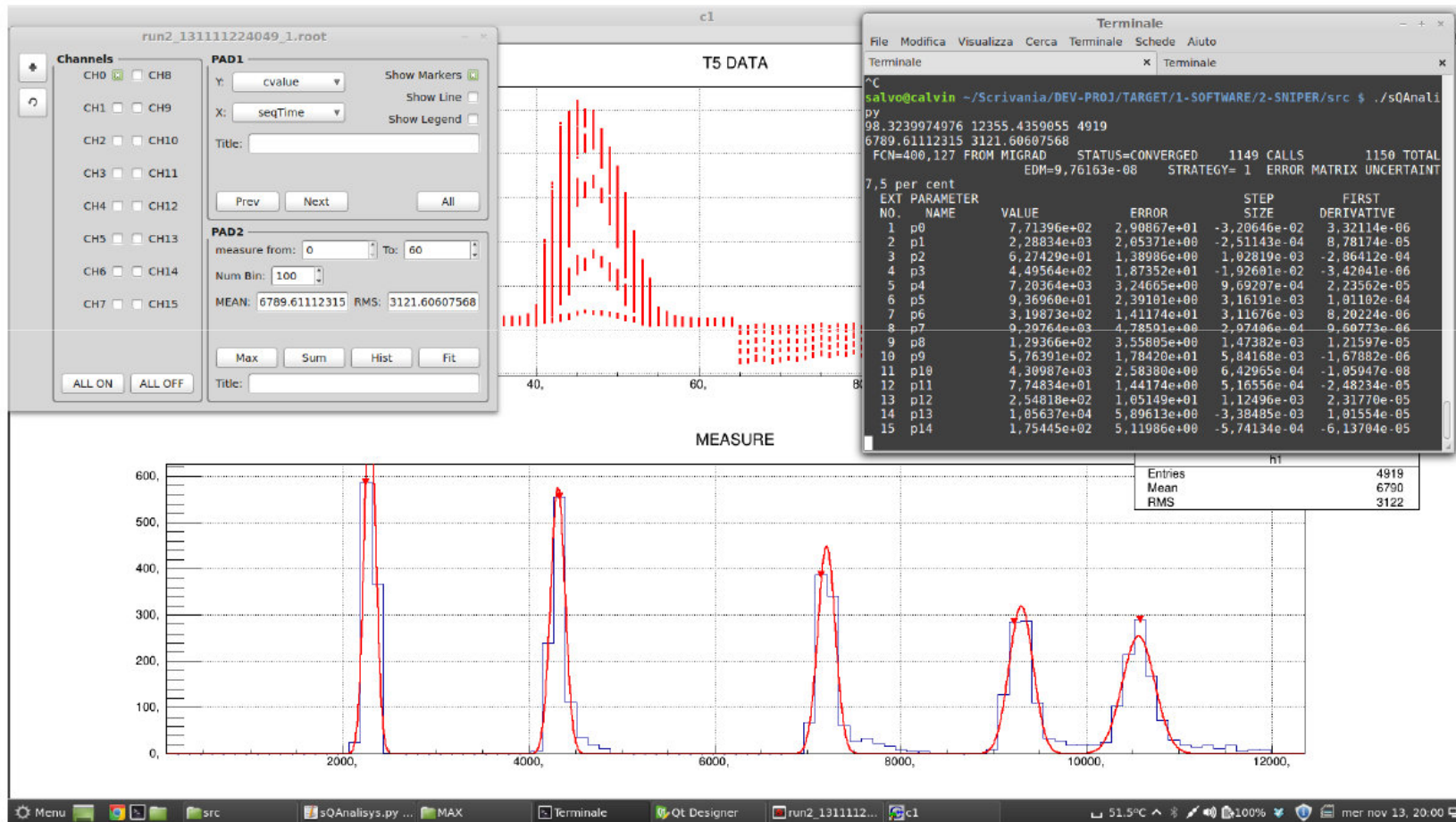
- Board built by SLAC
- 3 inputs on SMA connectors
- 1 external trigger
- Gb Ethernet interface
- Work done by Salvatore Zaza, thesis UniSi
- GUI based on python
- Analysis interfaced to Root and PyRoot



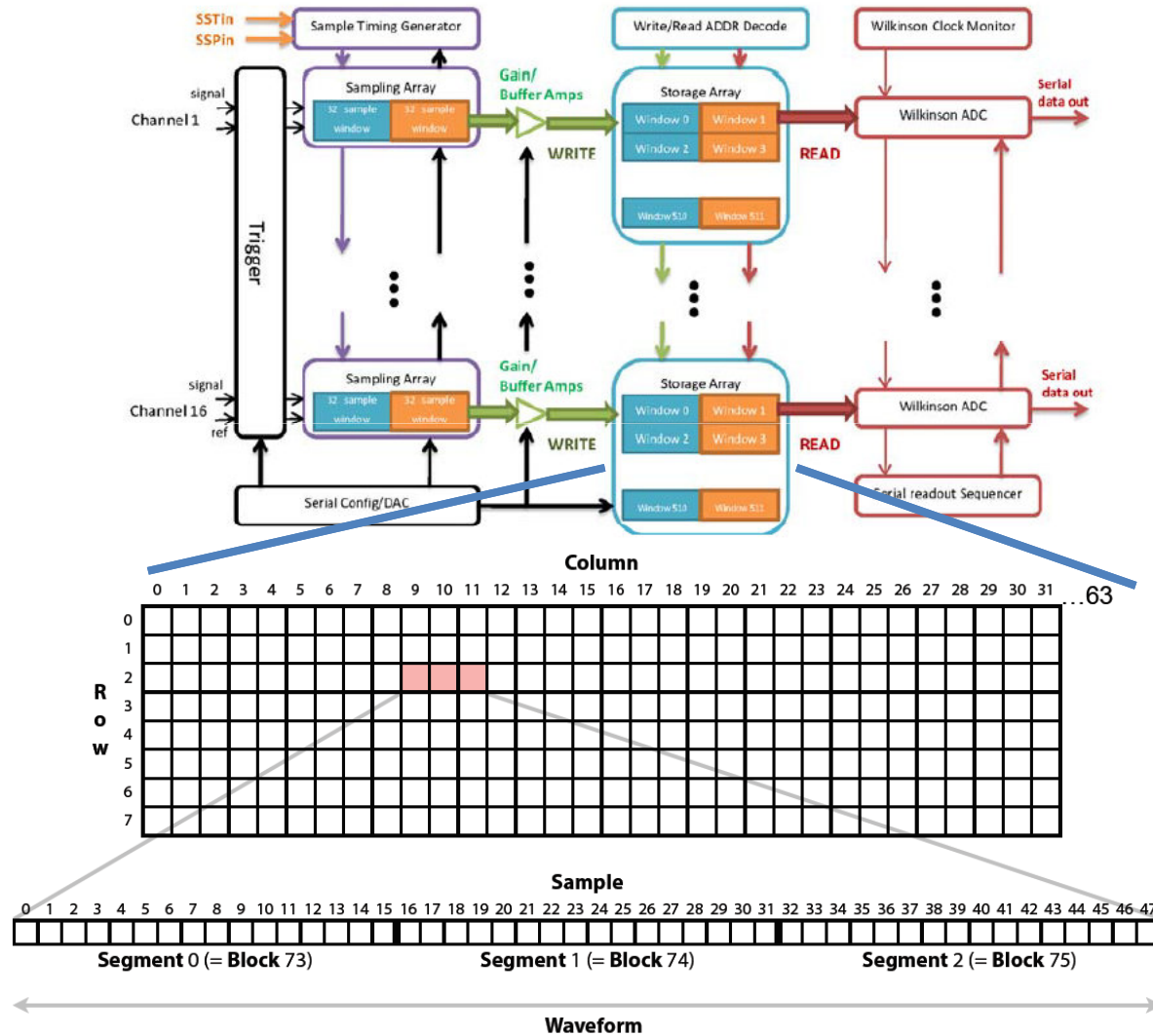
GUI Interface to T5 eval board



Analysis interface

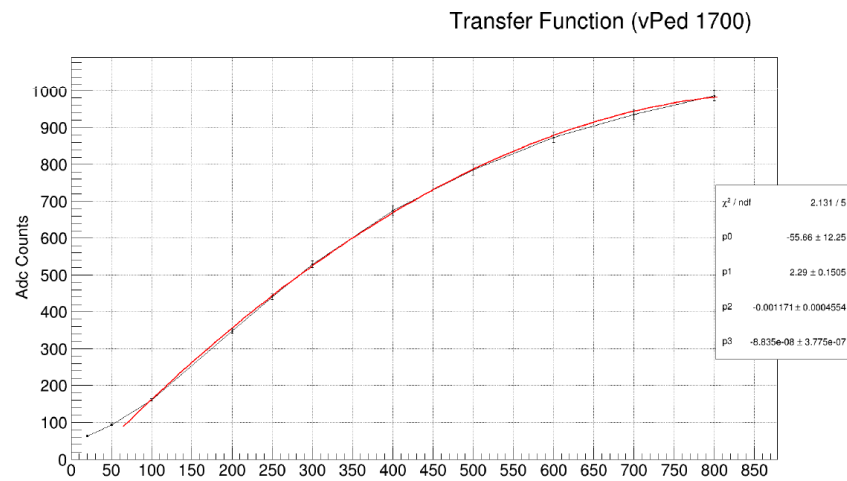


T5 Storage Cells

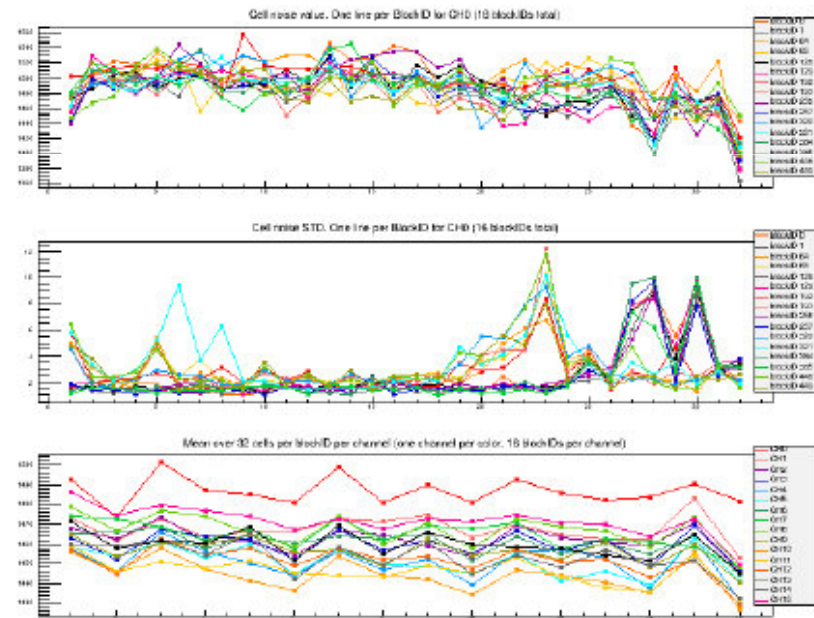


Calibration

Vped calibration

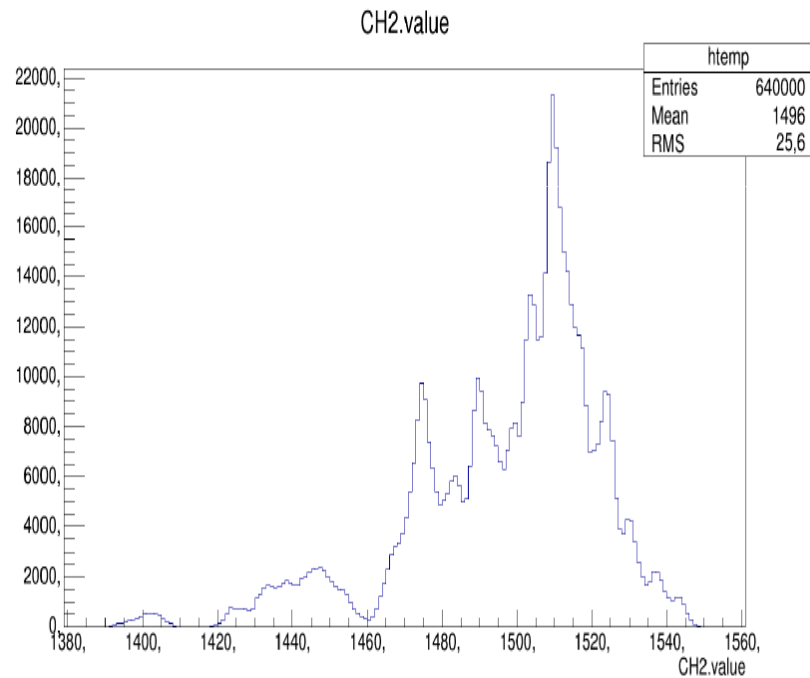


Storage cell calibration

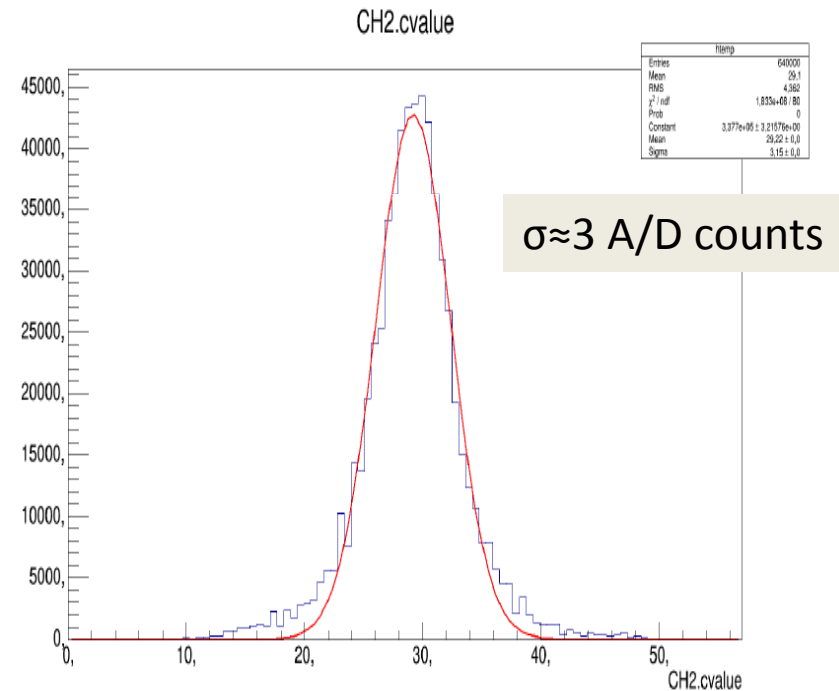


Effect of (simple) calibration

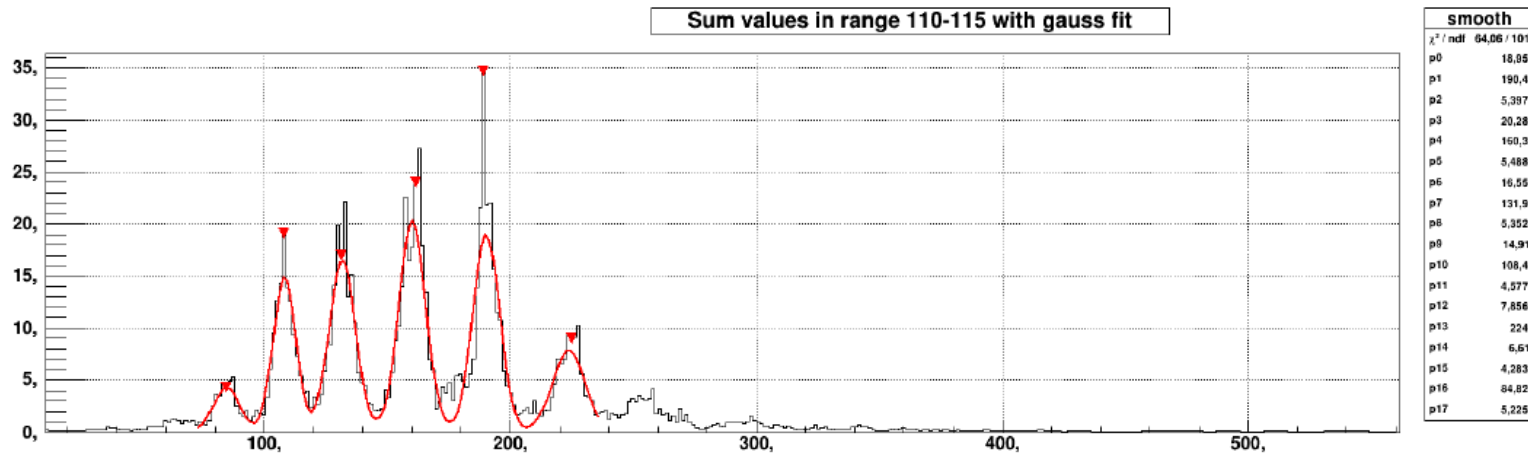
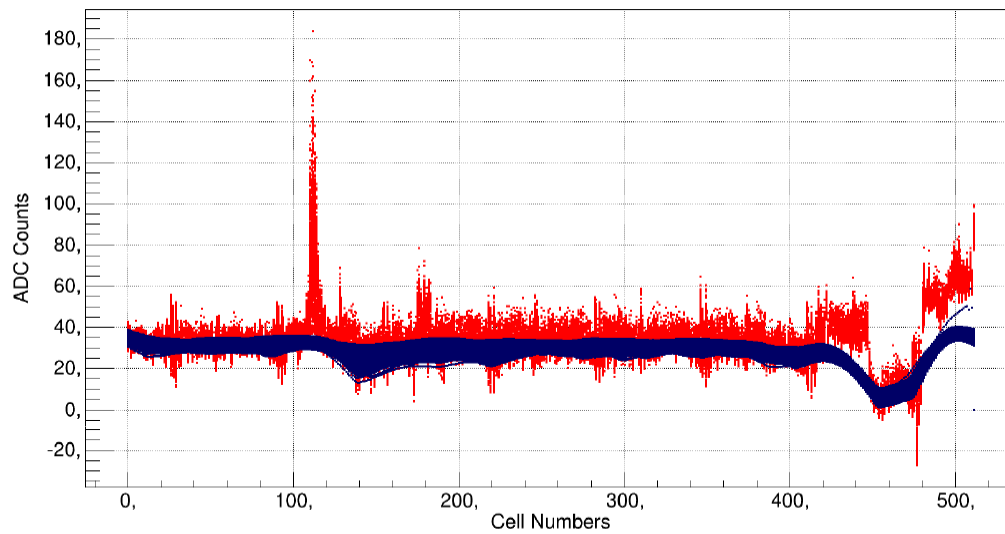
Before calibration



After calibration



Sampling of SiPM signal with T5



Conclusions

- Several activities ongoing in Pisa
 - SiPM fast “online” characterization
 - Single SiPM
 - Array 4x4 of SiPM 3x3 mm²
 - Front-end performance
 - Preamp “discrete” simulation+prototyping+comparison
 - High pass filter effect+check on signal quality
 - Sampling electronics
 - Target 5 evaluation board
 - DAQ+GUI for laboratory measurement
 - Calibration studies, performance studies
- Future activities (short term)
 - Integration of discrete front-end components
 - Design of sampling board with Target7
 - Data communication with Gb interface (SFP 3.125Gbps →PCIe x4)