Sviluppo di rivelatori a pixel per gli upgrades del tracciatore di ATLAS

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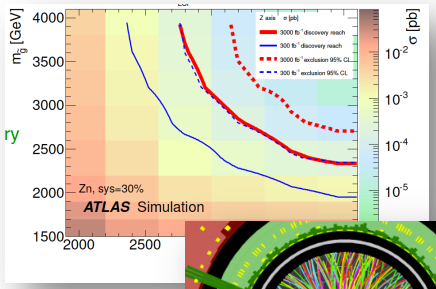
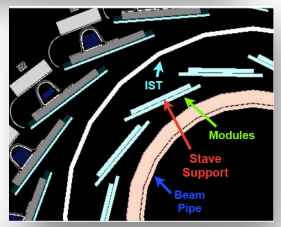
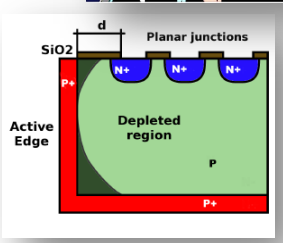
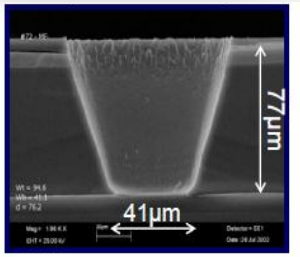
Content

- The path for the ATLAS tracker upgrade
- Phase II: what are the physics motivations
- The performance of present ATLAS pixel detectors
- IBL: new technologies for the first upgrade
- Requirements of the ATLAS Pixel system in Phase II
- Planar Pixel Sensor developments for Phase II
- Vertical Integration Technologies and new 3D module concepts

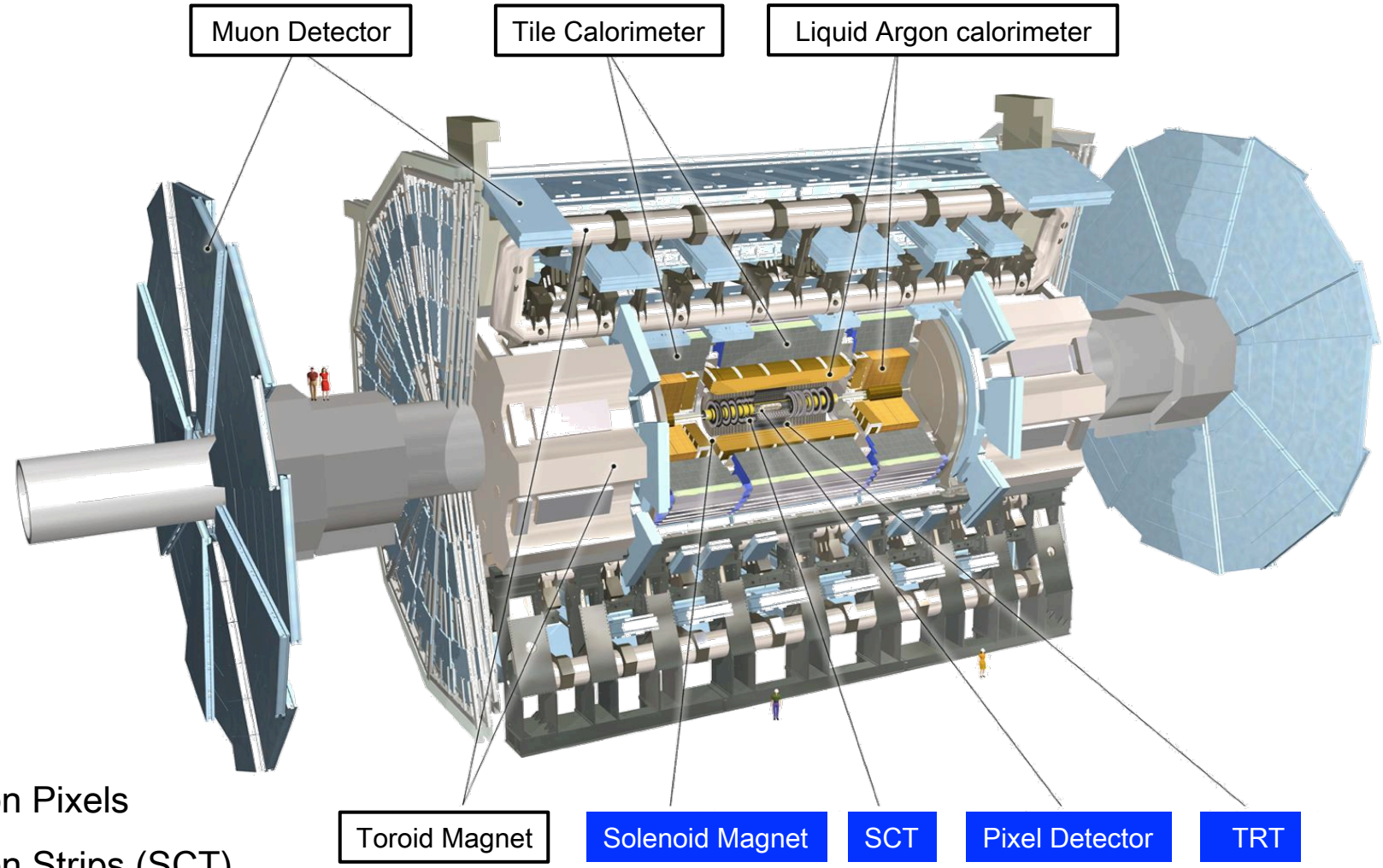








The tracking system of the ATLAS detector



- Silicon Pixels
- Silicon Strips (SCT)
- Transition Radiation Tracker (TRT) up to 36 points/track
- 2T Solenoid Magnet

ATLAS Tracker Upgrade Plan

2009 2010 2011 2012 **2013 2014 LS1** 2015 2016 2017 **2018 LS2** 2019 2020 2021 **2022 2023 LS3** … 2030

"Phase-0" upgrade: consolidation
$\sqrt{s}$ = 13~14 TeV, 25ns bunch spacing
$\mathcal{L}_{inst} \simeq 1 \times 10^{34}$ cm^{-2}s^{-1} ($\mu \simeq 27.5$)
$\int \mathcal{L}_{inst} \simeq 50$ fb^{-1}

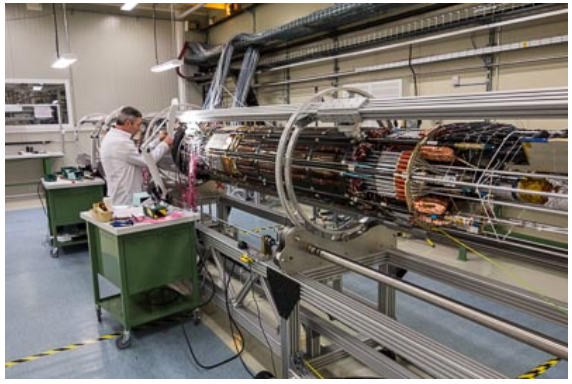
- New insertable b-layer (IBL)
- New Al beam pipe
- New pixel services

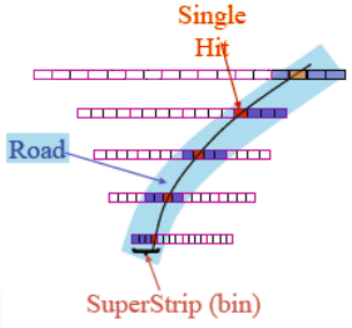
"Phase-I" upgrades: ultimate luminosity
$\mathcal{L}_{inst} \simeq 2\text{-}3 \times 10^{34}$ cm^{-2}s^{-1} ($\mu \simeq 55\text{-}81$)
$\int \mathcal{L}_{inst} \gtrsim 350$ fb^{-1}

- Fast TracKing (FTK) for level2 trigger

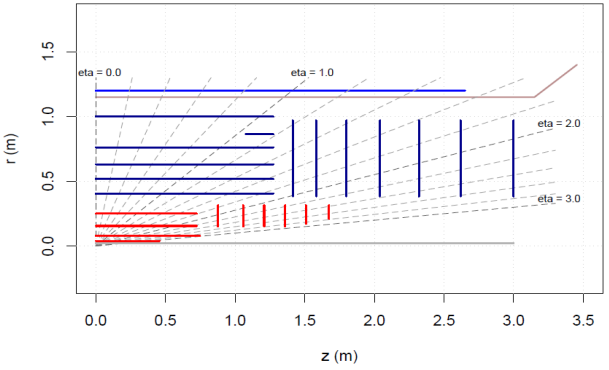
"Phase-II" upgrades:
$\mathcal{L}_{inst} \simeq 5 \times 10^{34}$ cm^{-2}s^{-1} ($\mu \simeq 140$) w. leveling
$\simeq 6\text{-}7 \times 10^{34}$ cm^{-2}s^{-1} ($\mu \simeq 192$) no level.
$\int \mathcal{L}_{inst} \simeq 3000$ fb^{-1}

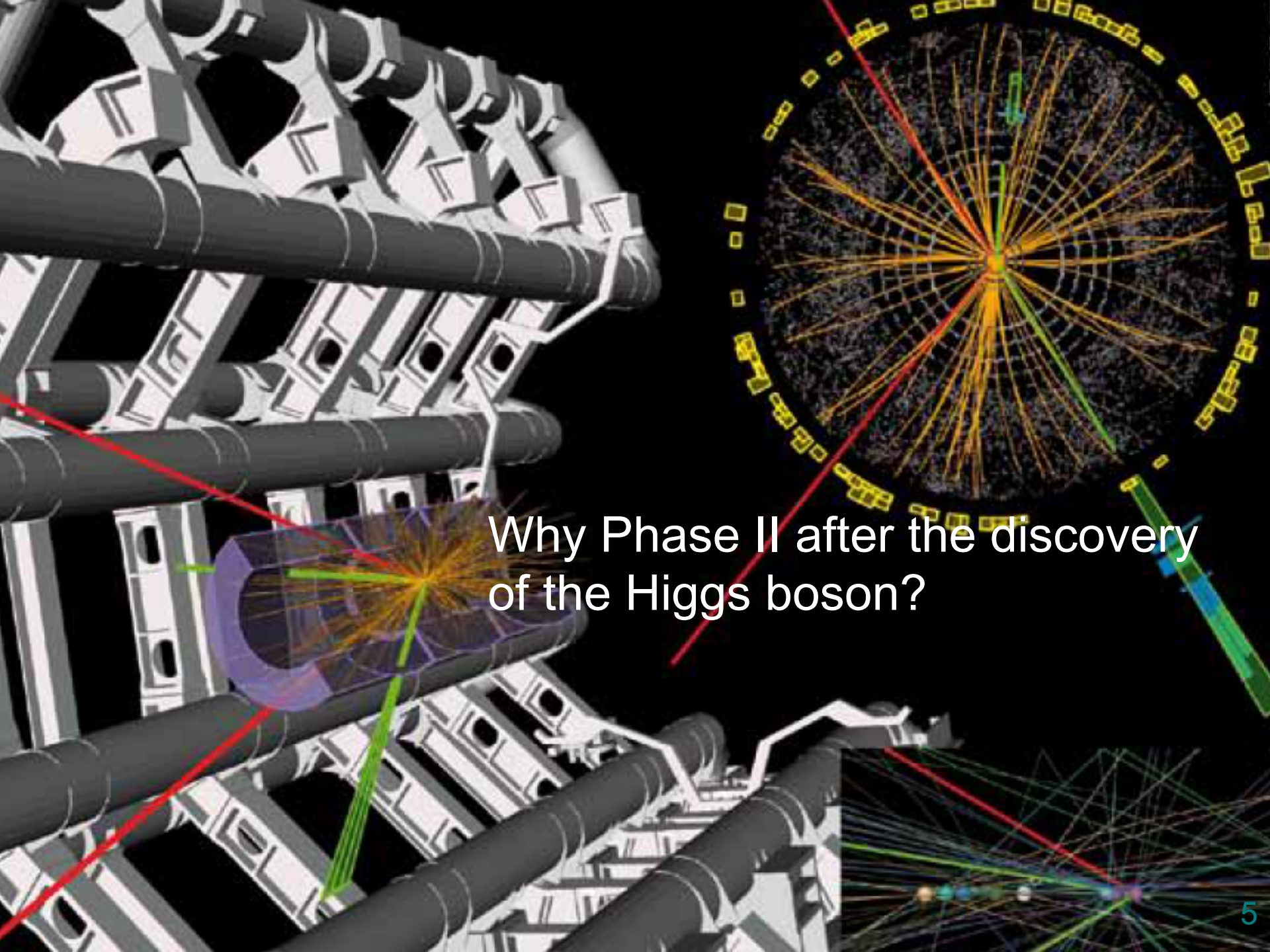
- All new tracker (baseline: long strips /short strips / pixels)





Pattern recognition in coarse resolution (superstrip➔road)

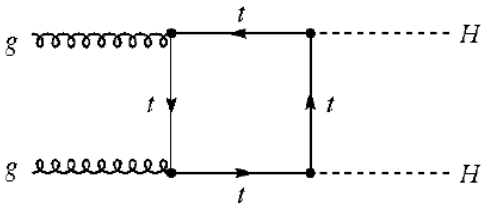


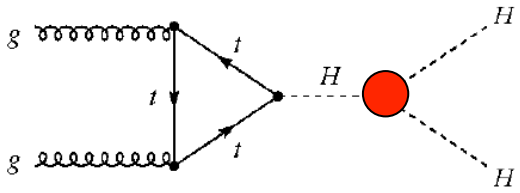

Why Phase II after the discovery of the Higgs boson?

HL-LHC Physics Programm (I)

- With LHC 13/14 TeV data until 2022 (~300 fb^{-1})
  - **Measure the Standard Model scalar boson properties**
    - Mass, J^{CP}
    - Individual couplings with 5-15% precision
  - Search for new physics at higher mass scale (new energy region)
    - SUSY, Exotics

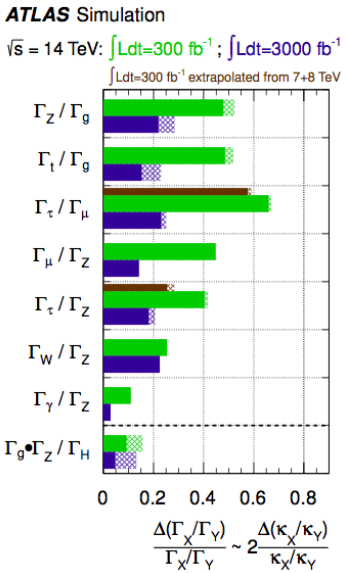
- With HL-LHC 14 TeV data until 2032 (~3000 fb^{-1})
  - **High precision SM scalar boson measurements**
    - Couplings <5%, study rare decays, self-coupling





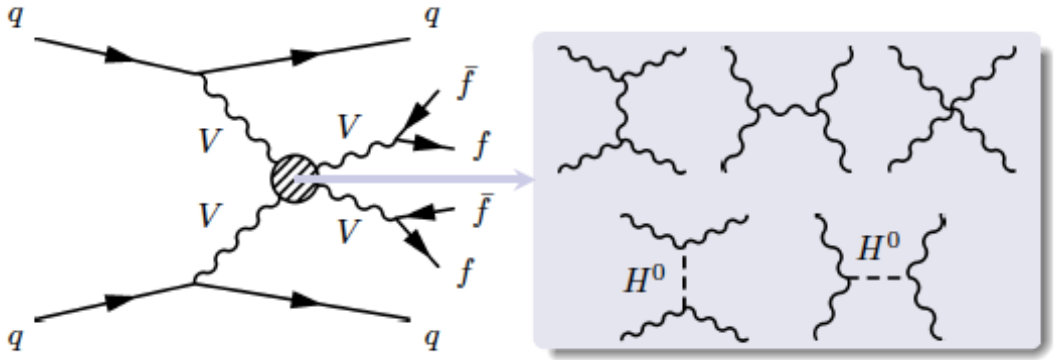
P. Wells, Lepton Photon 2013

Higgs triple self coupling



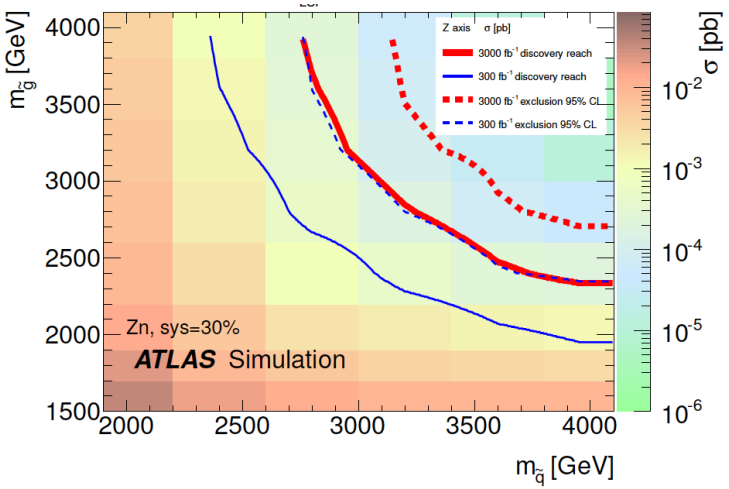
HL-LHC Physics Programm (II)

- Study VV scattering
  - Verification that Higgs boson cancel divergences in VBF



P. Wells, Lepton Photon 2013

- Direct searches of BSM particles
  - HL-LHC increases the discovery reach by ~400-500 GeV



ATLAS simplified model with zero mass LSP

The present ATLAS Pixel system

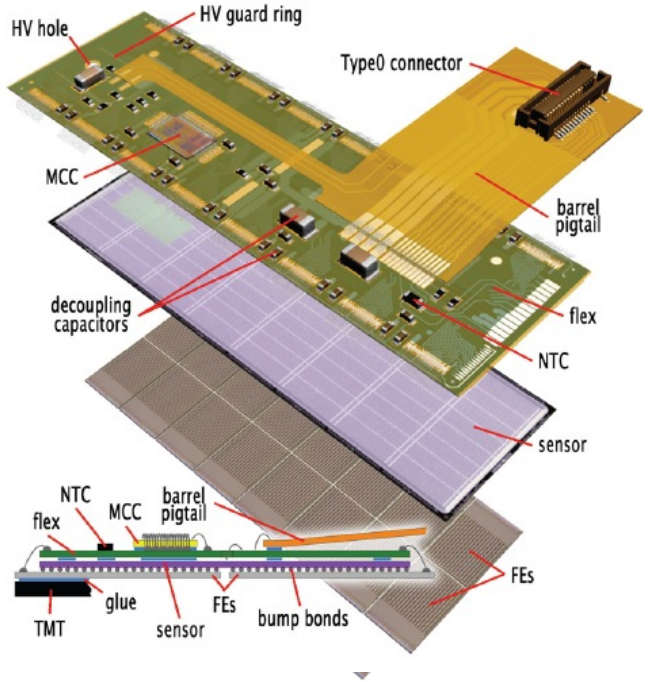
The present ATLAS Pixel system

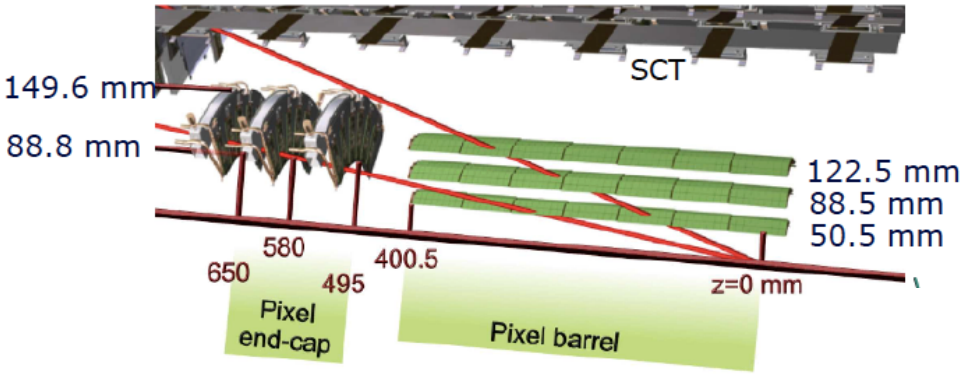
- Sensors and modules:

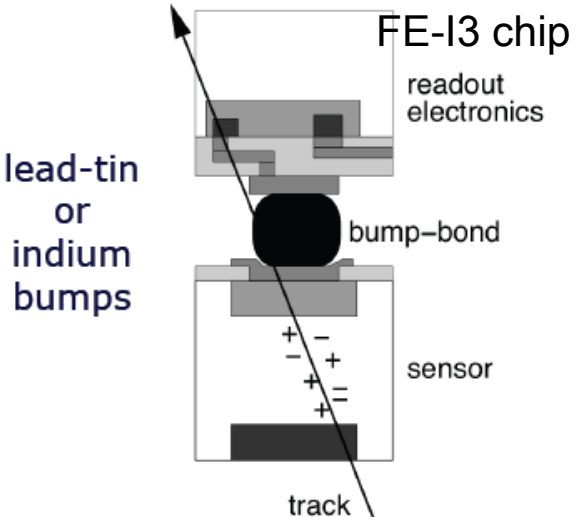
• 250 μm thick n-on-n type silicon, with typical pixel granularity of 50 μm x400 μm.

• 16 FE-I3 chips per module bump-bonded to a single sensor

1456 modules in the barrel region and 288 modules in the three end-cap discs per side



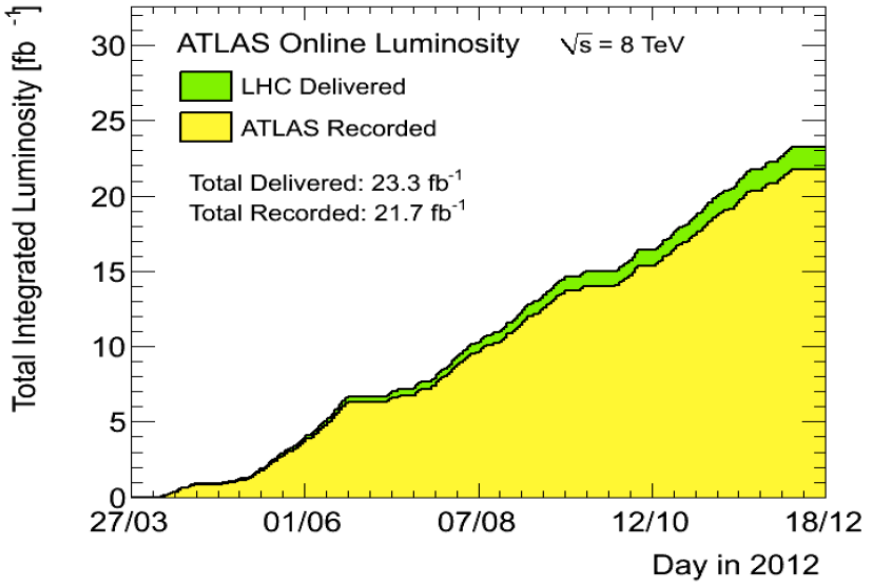




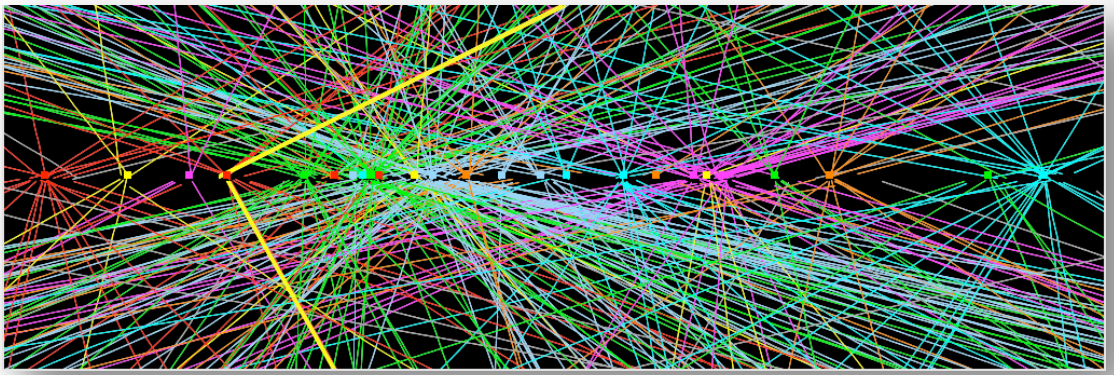
Tracker Performance today

- 99.9 % Pixel data taking efficiency in 2012
- Hit-to-track association efficiency ~99%
- 95% of modules are active during data taking in 2012
- Inoperable fraction gets addressed in LS1 repair (is now ~ 1%)

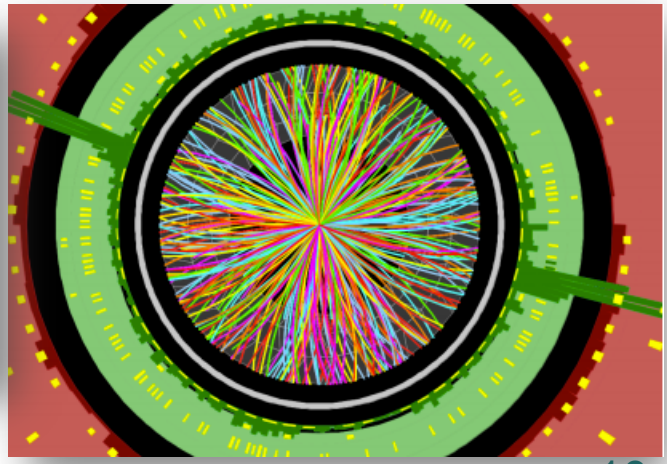
E. Stanecka, Vertex 2013



Up to ~70 interaction /BX



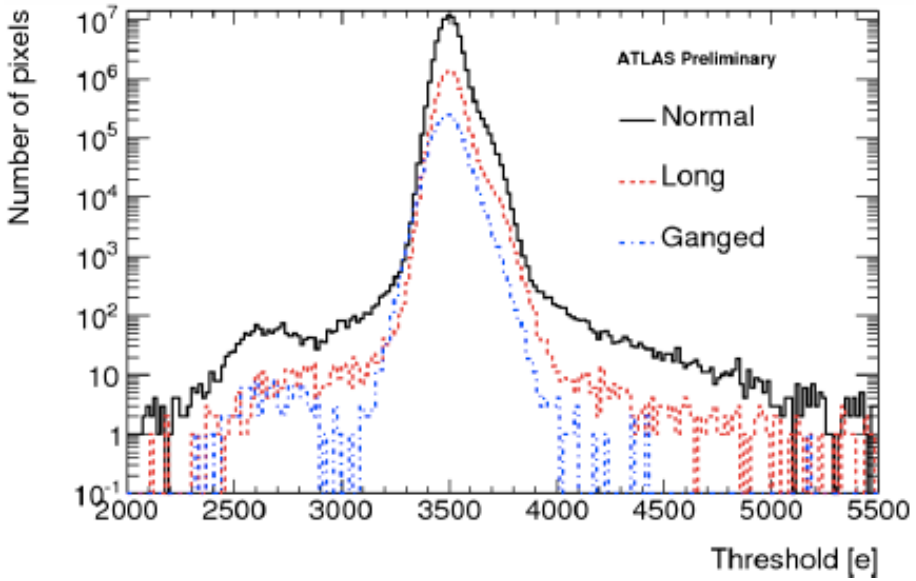
Up to 4000 tracks per event every 25 ns

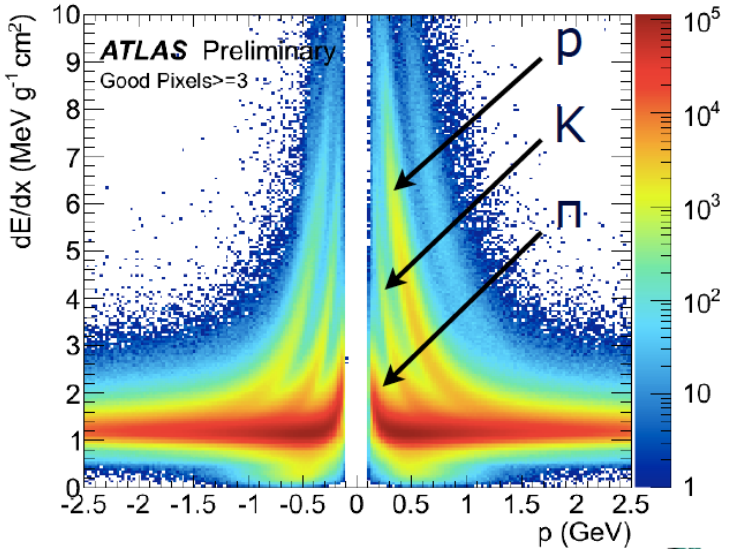


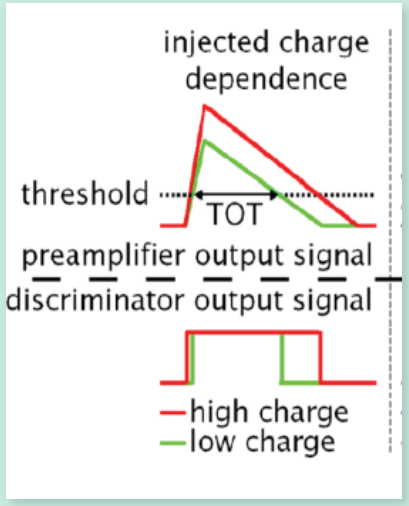
- ATLAS was designed for 23 evt /BX but continues to do an excellent job with 35

Pixel Detector Performance today

T. Ince, Siena 2013





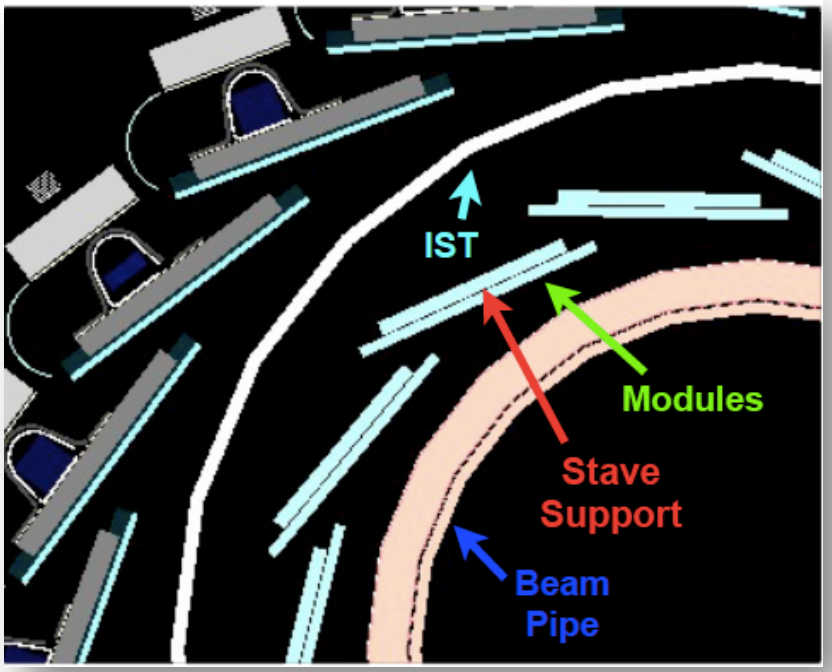


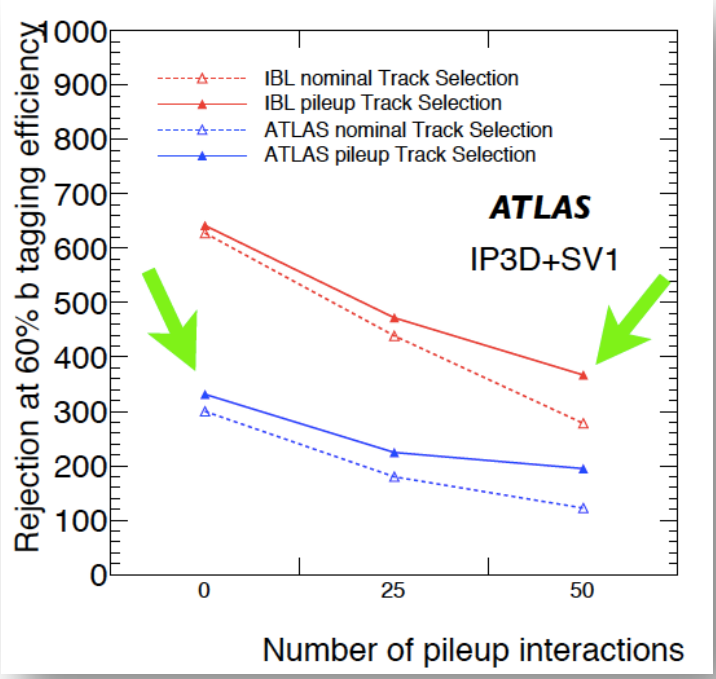
- Threshold tuned to 3500 e, with 40 e dispersion
- Time Over Threshold: time in which signal is above threshold in units of BC, 25 ns
- Tuning target is 30 BC for a charge of 20,000 e (most probable value for m.i.p.)
- Advantages:
  - improved position resolution (shared hits)
  - energy loss proportional to deposited charge ➡ particle identification

The Insertable B-layer

Phase 0 Upgrade: the Insertable B-Layer

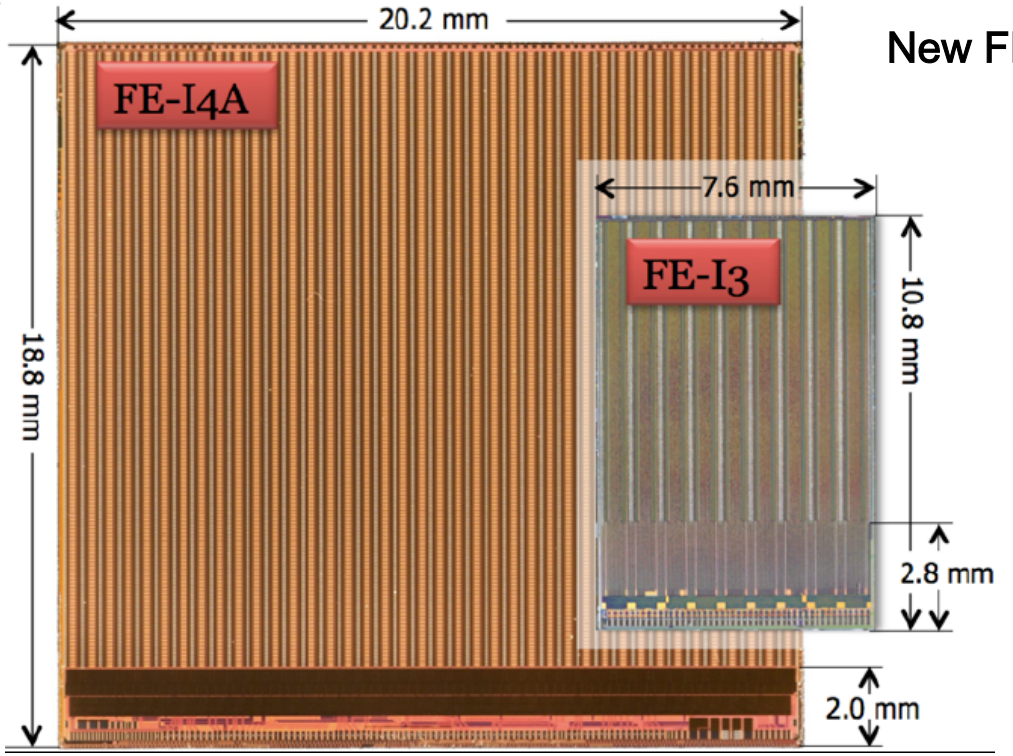
- Designed to let ATLAS cope with $\mathcal{L}=3\times10^{34}$ cm^{-2} s^{-1}
- New 4th pixel silicon barrel layer with r = 3.3 cm, 12 MegaPixel
  - Needs small radius (r = 2.35 cm) beam pipe
  - 14 staves with Φ = 14° tilt angle & no z overlap



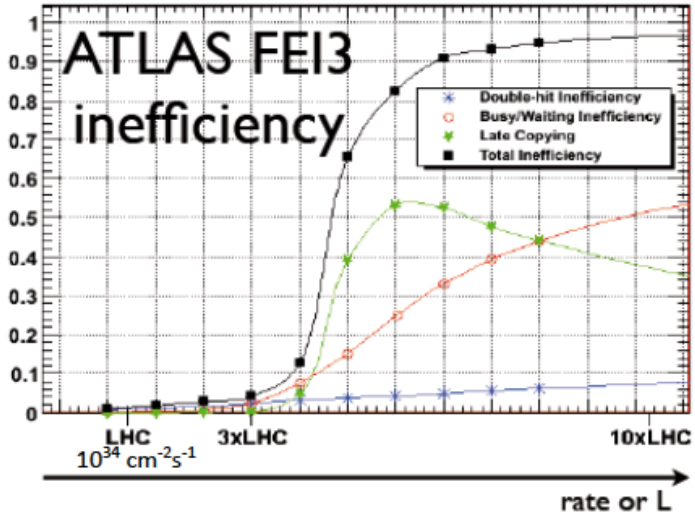


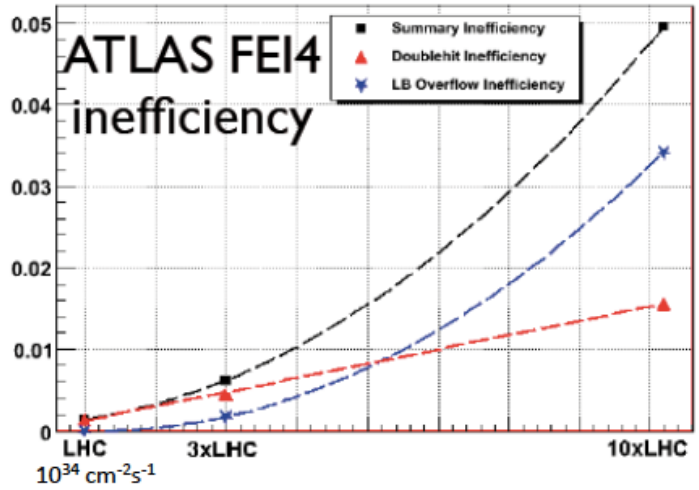
- Redundancy to control the fake rate
- Improve b-tagging
- Good performance with IBL and pile-up → as good or better as for the current ATLAS without pile-up

The ATLAS Insertable B-layer



New FE-I4 chip, 2x2 cm^2, pitch 50x250 μm^2





- 130 nm CMOS
- 150 μm thickness
- Charge by 4 bits ToT
- 160 Mb/s readout
- Power 200 mW/cm^2
- Total dose tested up to 750 MRad

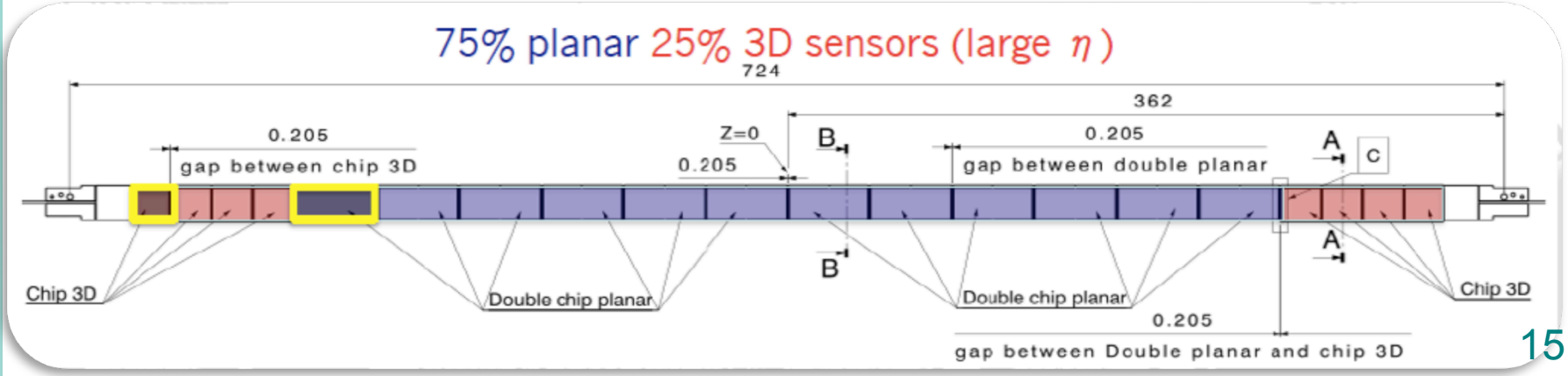
Pixel Sensors for the IBL

Planar n-in-n oxygenated Si sensor

- Pixel electrodes on surface of bulk
- Proven ATLAS Pixel Detector technology and vendor: CIS
- Very high yield (90% accepted for IBL production)
- **From old pixel system to IBL:**
  - Pixel size 50x400 μm^2 → 50x250 μm^2
  - Thickness 250 μm → 200 μm
  - Inactive edge 1 mm→ 200 μm

3D double sided silicon sensors

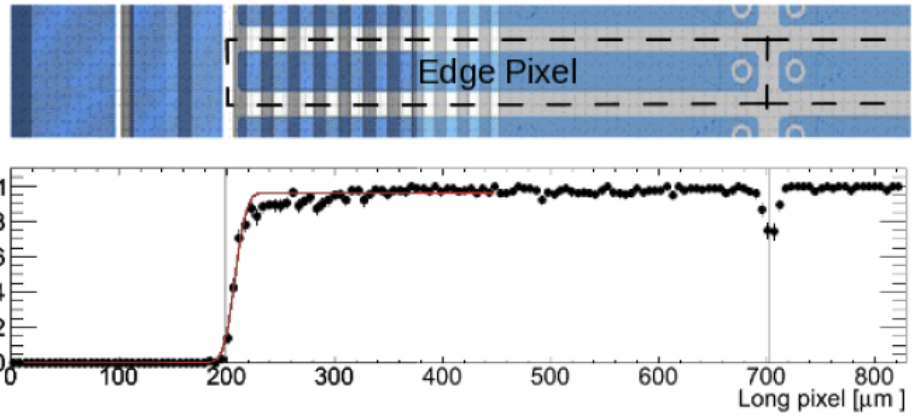
- Vertical 2E electrodes
- Reduced operational voltage after irradiation
- 230 μm thickness
- Two 3D sensor vendors (CNM and FBK)
- Acceptable yield (60% for IBL)



N-in-n pixels for IBL – Slim edge

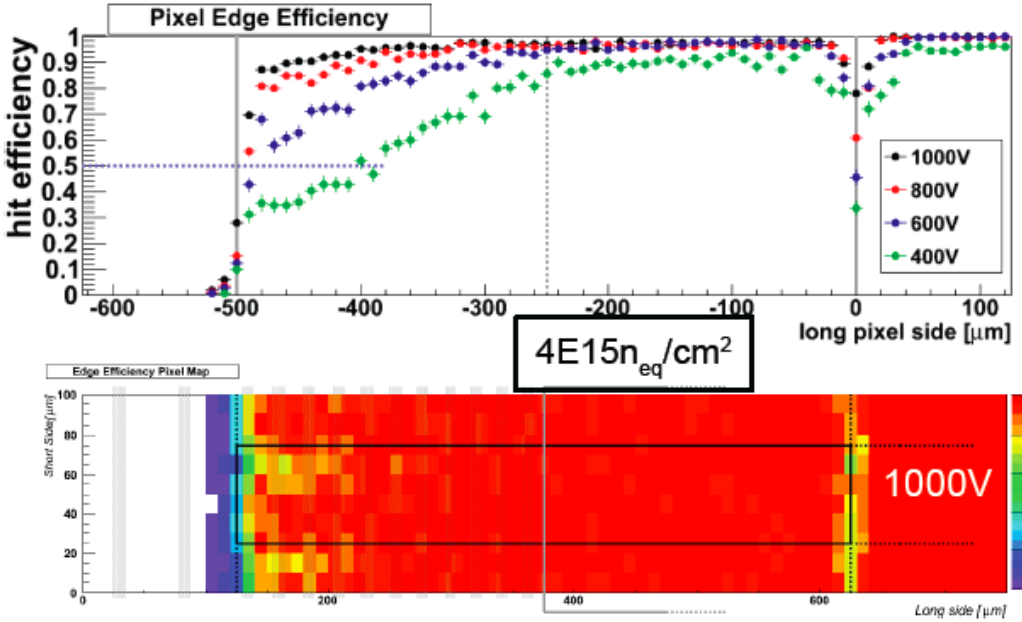
technische universität dortmund

CIS production of IBL sensors



other 100 μm to the edge

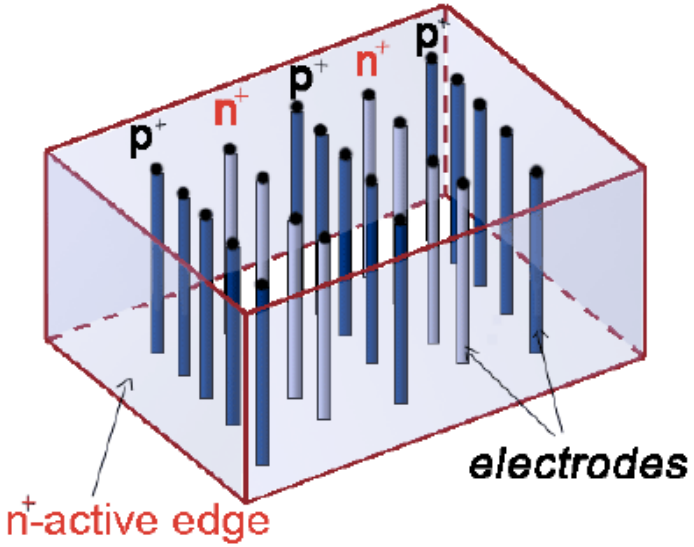
- Study of edge efficiency in beam tests for for FE-I4 n-in-n modules (IBL type)
- Before and after irradiation a clear dependence on the bias voltage is visible
- reduction of the inactive edge to ~200 μm demonstrated



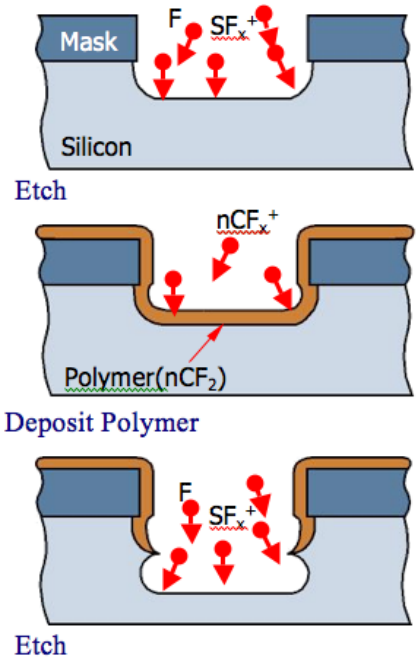
T. Wittig, Pixel 2012

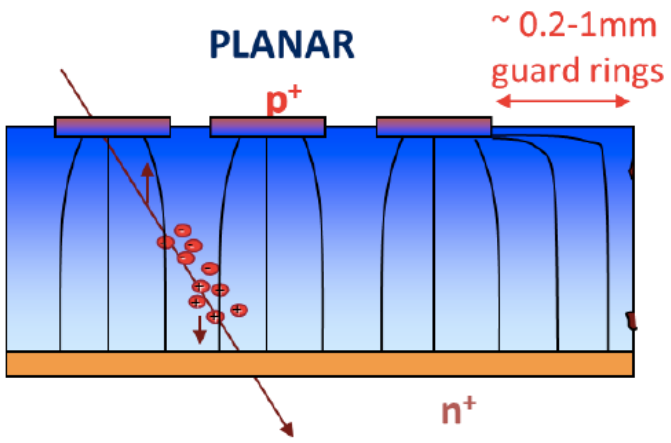
3D pixel sensors

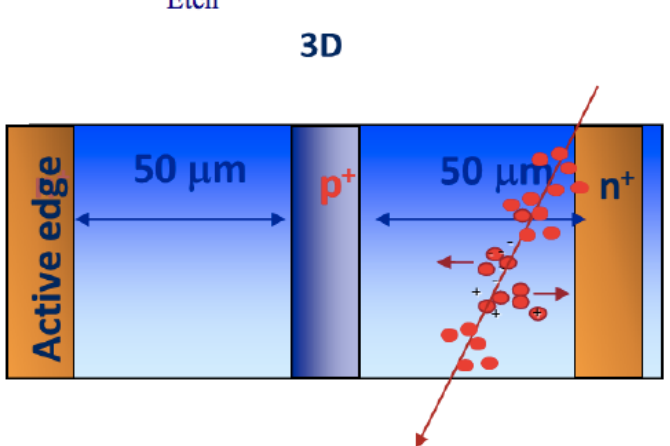
First proposed by S. Parker et. al. in NIMA 395 (1997), 328



Columns etched with Deep Reactive Ion Etching







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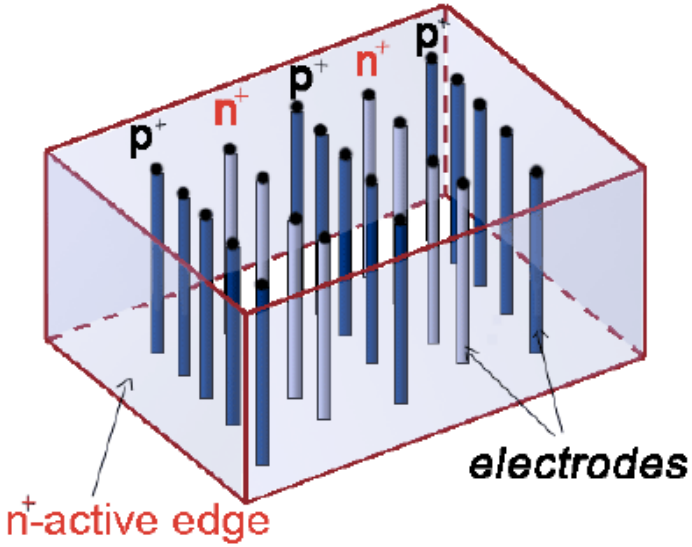
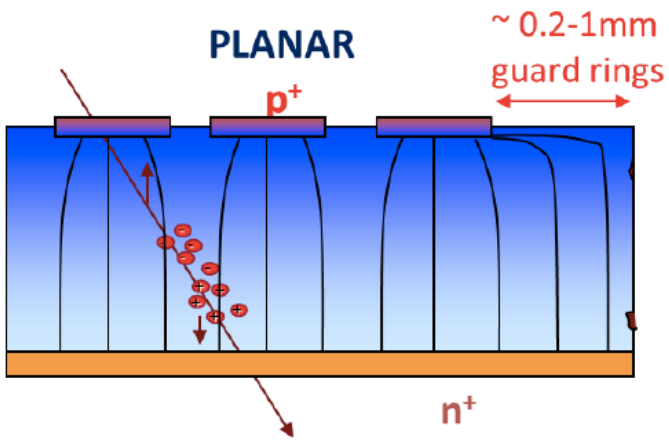


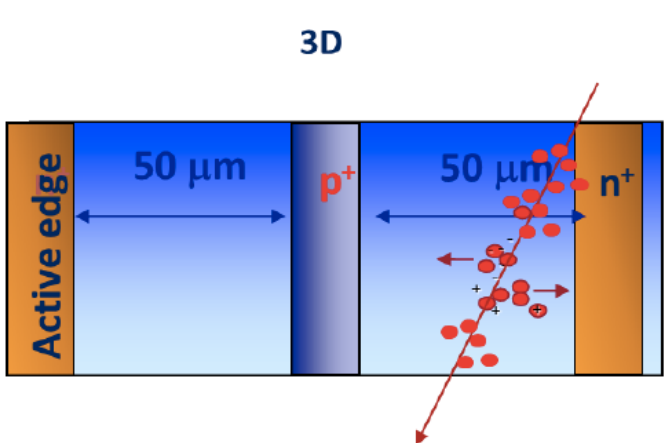
ADVANTAGES

- Electrode distance and substrate thickness decoupled
- High speed
- Good charge collection efficiency → good radiation hardness

DISADVANTAGES

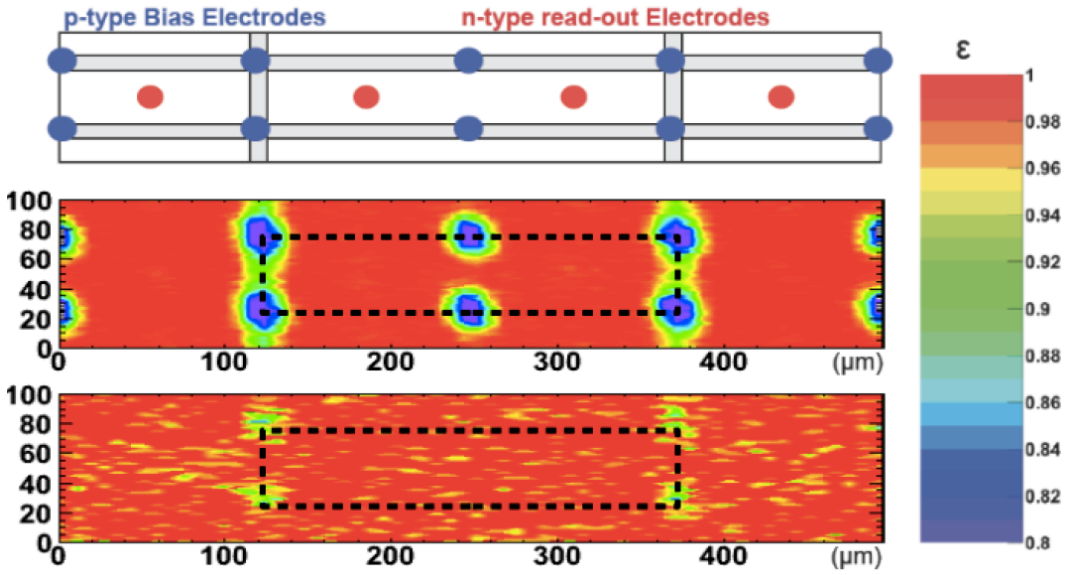
- Non uniform response due to electrodes
- Complicated technology
- Higher capacitance with respect to planar



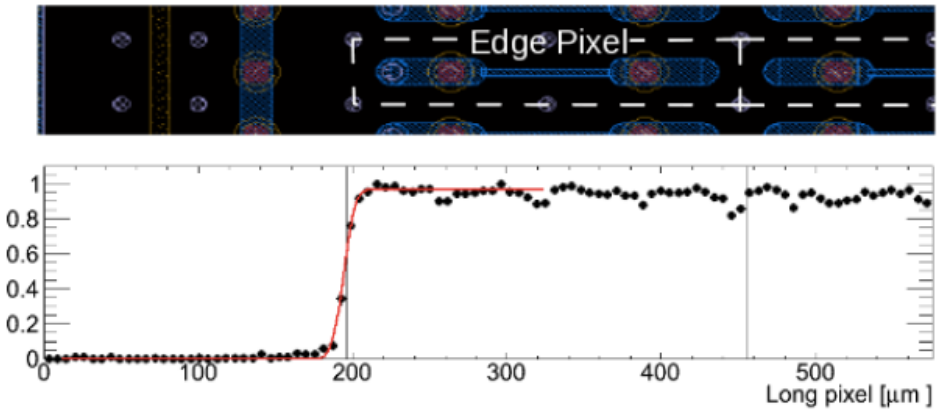


3D pixel sensors for IBL

CNM sensors, V_{bias}=160 V, Φ=5x10^{15} n_{eq} cm^{-2}



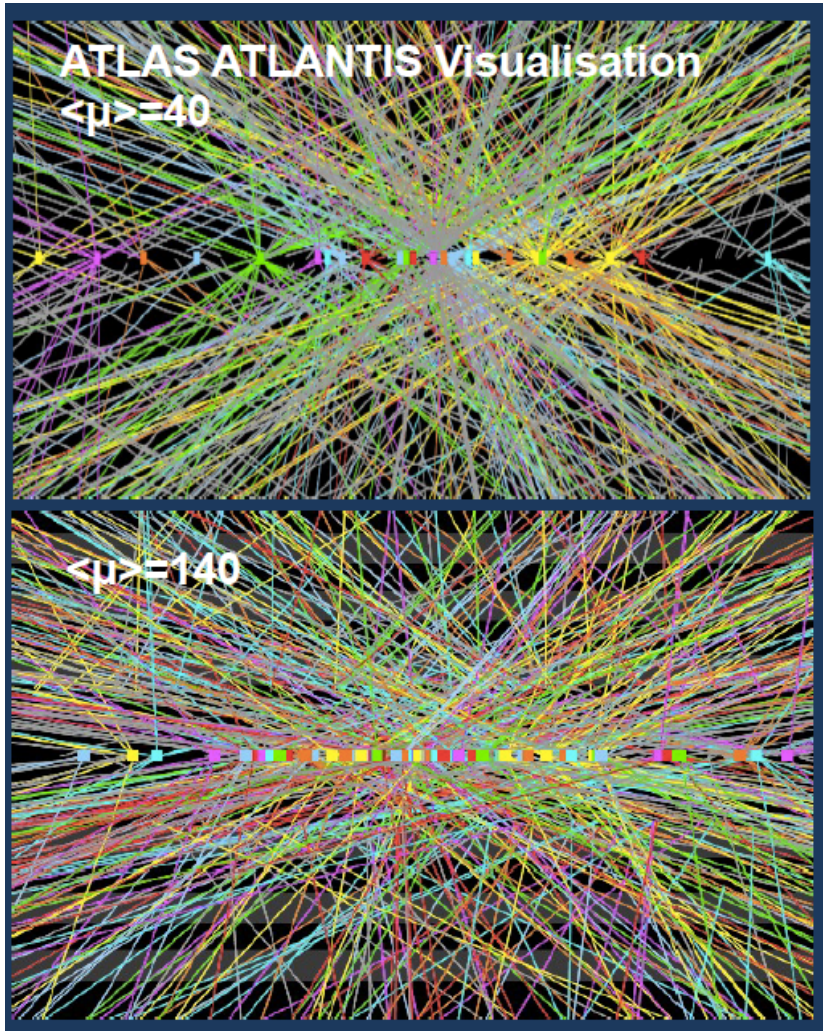
- Inefficiency at columns (not sensitive areas)
- Overall efficiency 97.5% (99%) at 0° (15°)
- 15° corresponds to IBL tilt angle.



- Slim-edge: Dead region along the beam axis < 225 μm

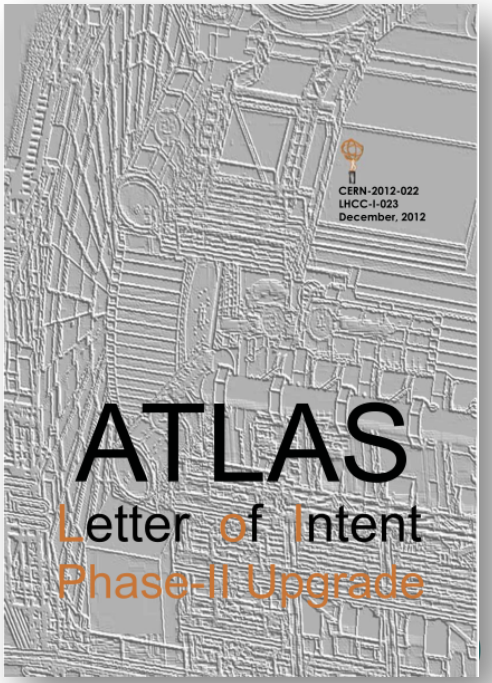
C. Gemme, Vertex 2013

The ATLAS Pixel System in the Phase II Upgrade



Proton-proton collision energy $\sqrt{s}$=14 TeV

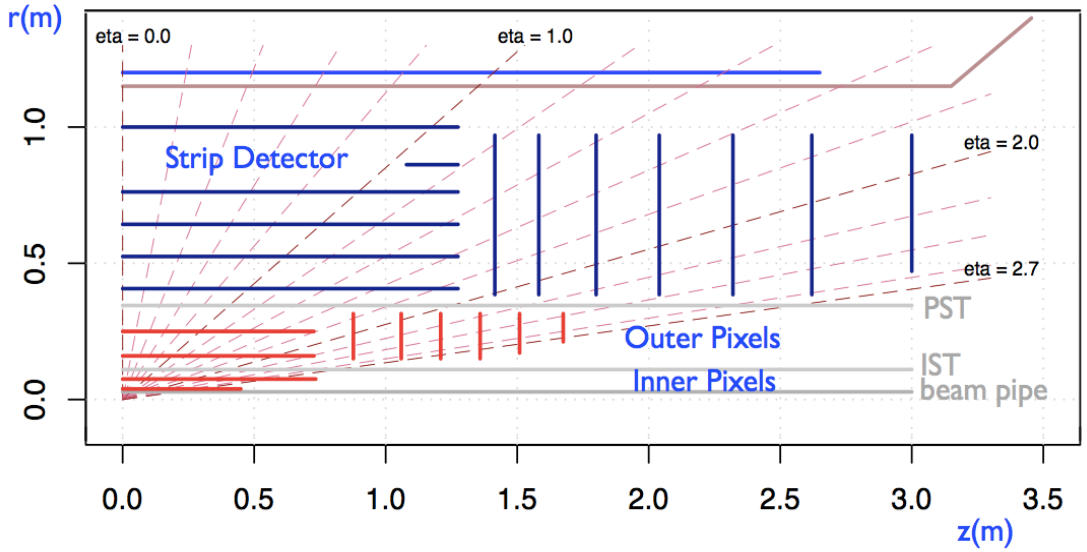
- Instantaneous luminosity of $L=5\times10^{34}$ $cm^{-2}s^{-1}$
- Average number of 'pile-up' collisions per event <μ> = 130-140
- Integrated luminosity 3000 fb^{-1} over the entire run



I. Gregor, DESY

Development of planar pixel sensors for Phase II

Phase II Pixel System Layout and requirements



The layout proposed in the LoI provides 14 points/track to |n| < 2.7

Pixel: 4 layers + 6 disks

2 Outer Barrel Layers / Disks

- Probably planar n-in-p
- Sensor thickness 150 μm
- Pixel size 50x250 μm^2
- 2x2 (Quad) and 2x3 (Hex) chip modules

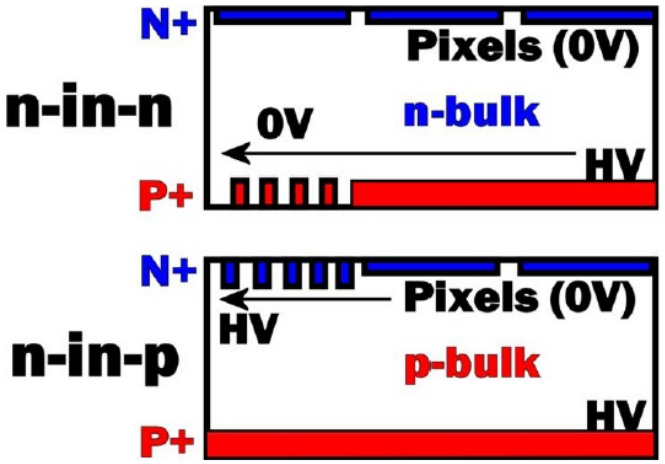
2 Inner Barrel Layers

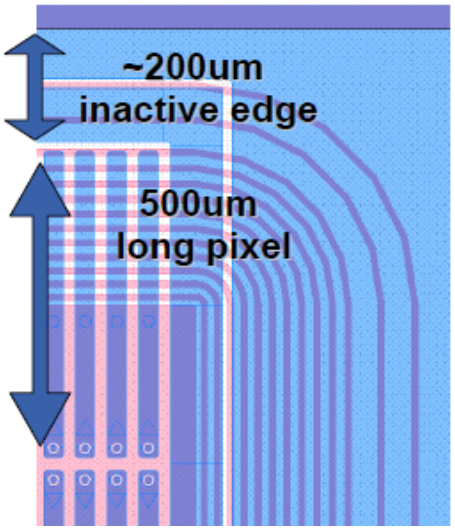
- Sensors: different materials and technologies possible
- Radiation hardness up to $2x10^{16}$ n_{eq}/cm^2
- Thickness: 150 μm or lower
- Pixel size 25x150 μm^2 → FE-chip in 65 nm CMOS technology

H. Hayward, Hiroshima 2013

Comparison between n-in-n and n-in-p technologies

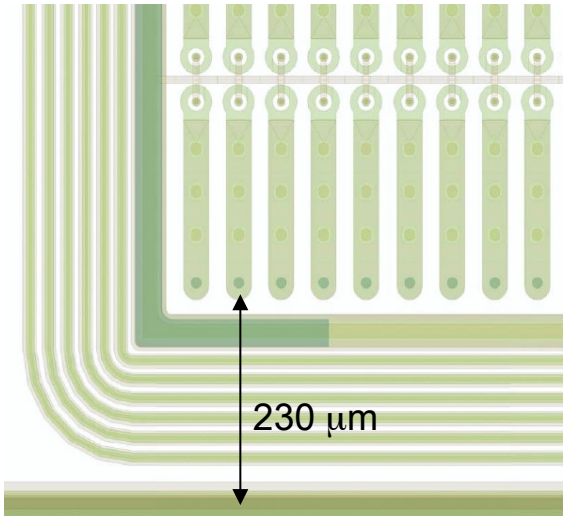
M. Benoit et al., IEEE Trans. On Nuclear Science, VOL. 56, NO. 6, DECEMBER 2009





n-in-n technology

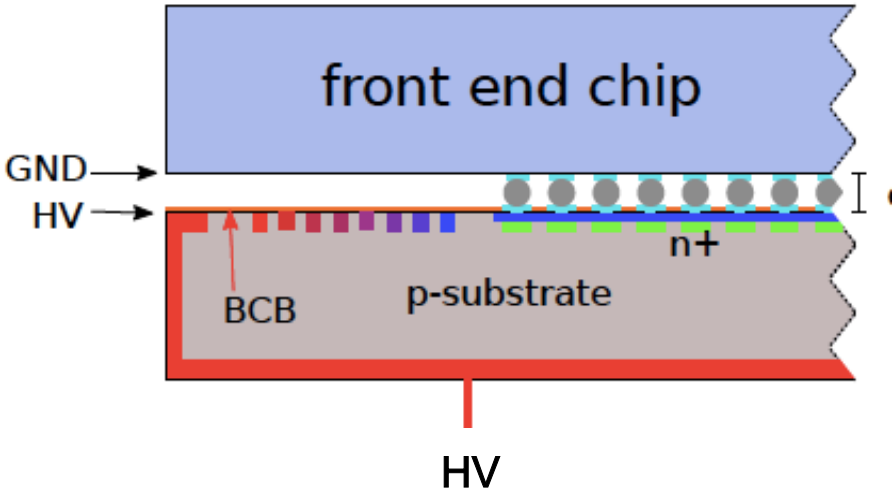
- ❑ double sided
- ❑ slim edges down to 200 μm possible



n-in-p technology

- Depletes from the segmented side
- Single sided process
- 30-40% cheaper than n-in-n
- More foundries and available capacity world-wide
- Easier handling-testing due to lack of patterned back-side implant

Sensor-chip isolation techniques for n-in-p pixels



- Danger of sparks between the chip and the sensor edges at HV
  - distance of the order of the bump height ~ 30 μm

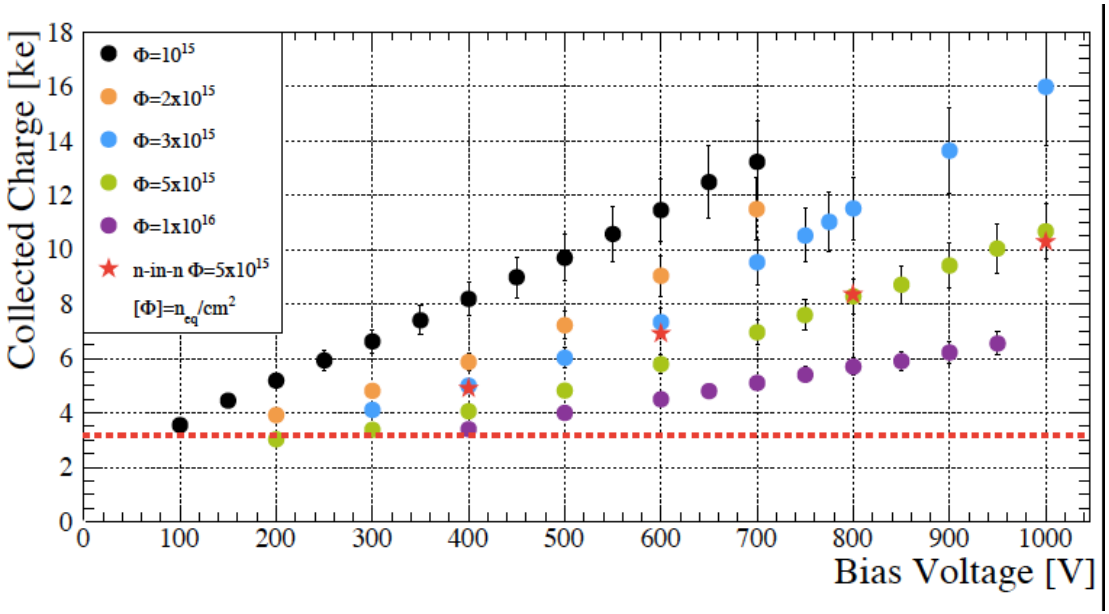
- 3 μm of Benzocyclobutene (BCB) on the sensor surface, litography needed → No sparks observed up to 1000V
- Parylene-C deposited all over the module (5-10 μm per side) → tested up to 650V, no sparks.

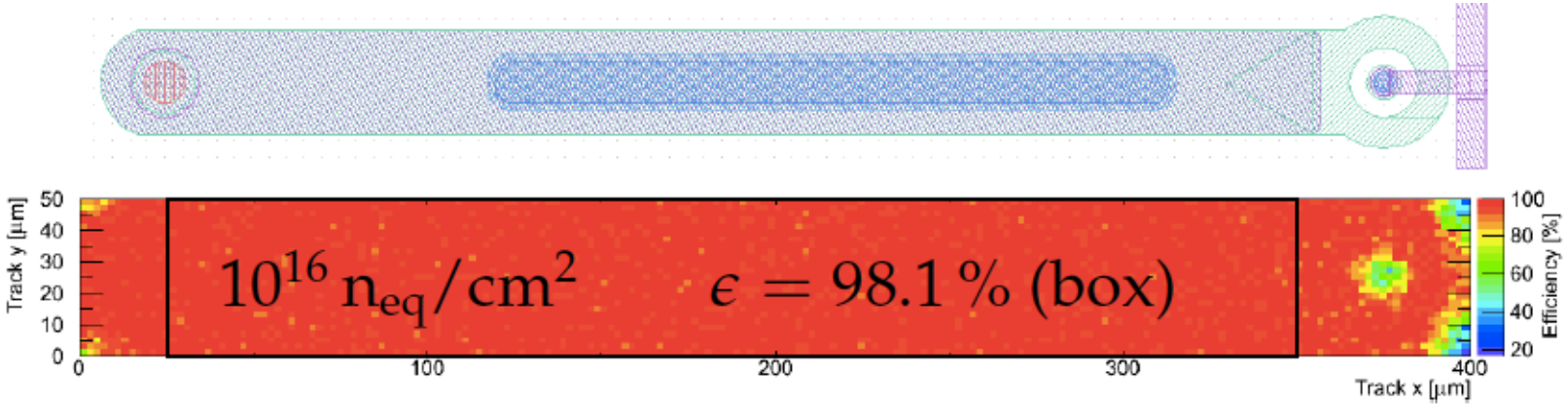
  Some hints of radiation damage from preliminary studies on test-structures. Parylene-N seems more resistant
- Silicon adhesive on the wire bonding side → no sparks observed up to 1000V

n-in-p performance – FE-I3 modules

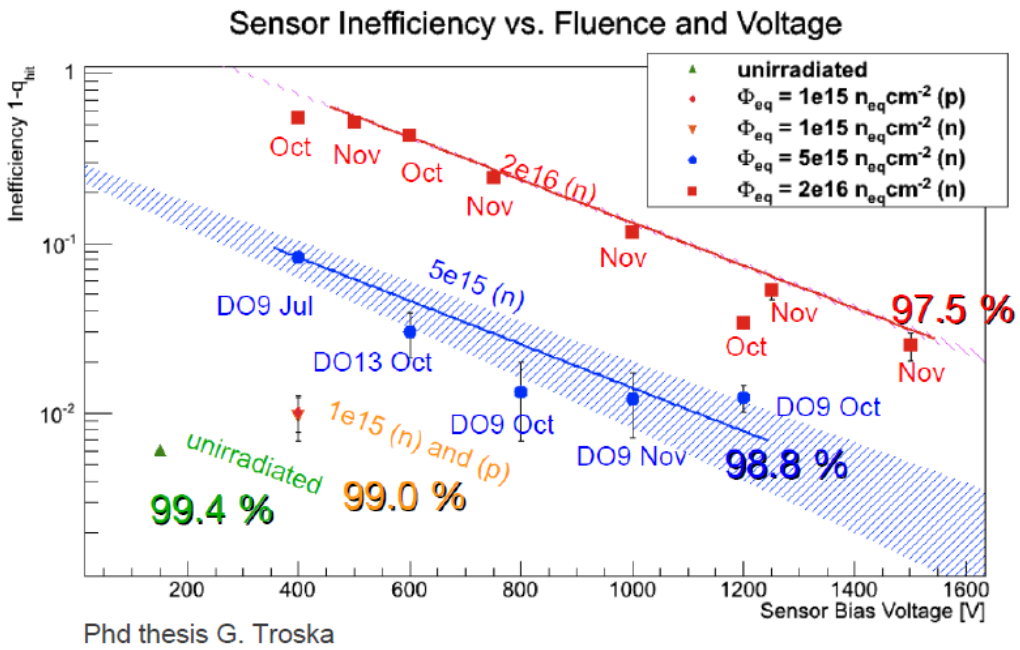
- MPP/HLL design produced by CiS on 285 μm FZ. n-irradiated up to 10^{16} n_{eq}/cm^2

- Charge exceeds threshold by a factor of 2
- Testbeam with Eudet telescope
  - Hit efficiency of 97.2% at highest fluence, 600V and threshold of 2 ke (98.1% in central region)
- Main losses in punch through and corners for perpendicular tracks





n-in-n performance – FE-I3 modules

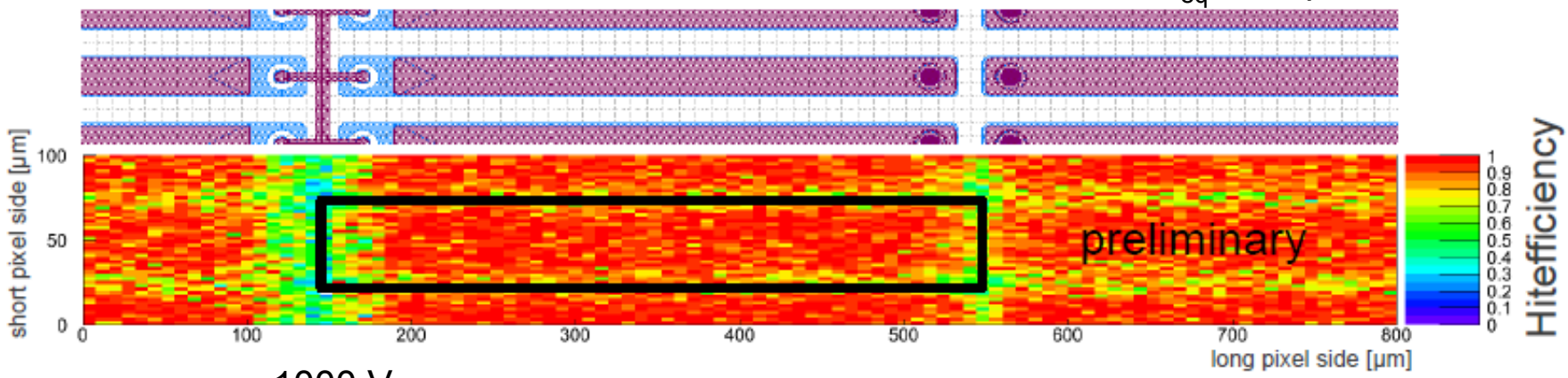


Phd thesis G. Troska

technische universität dortmund

- FE-I3 samples n-in-n
- 250 μm thickness
- PbSn bump-bonded

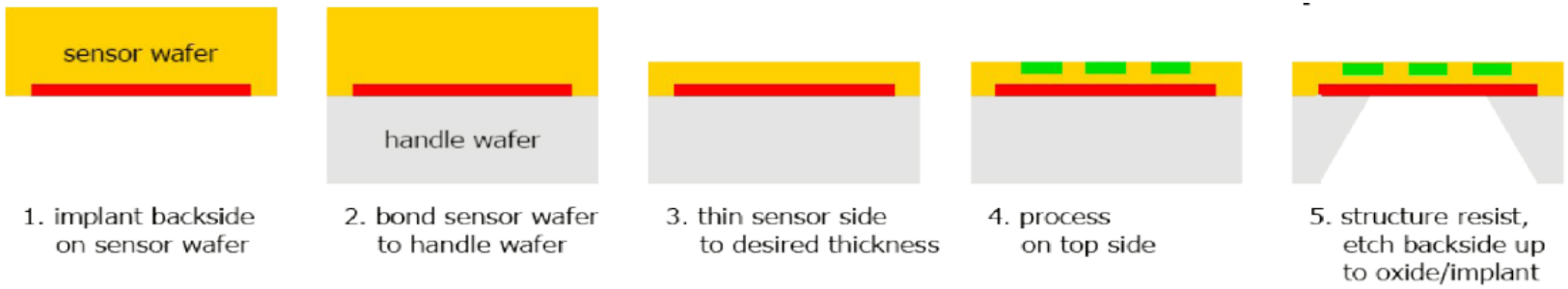
Φ=1.4x10^{16} n_{eq}/cm^2, p irr.



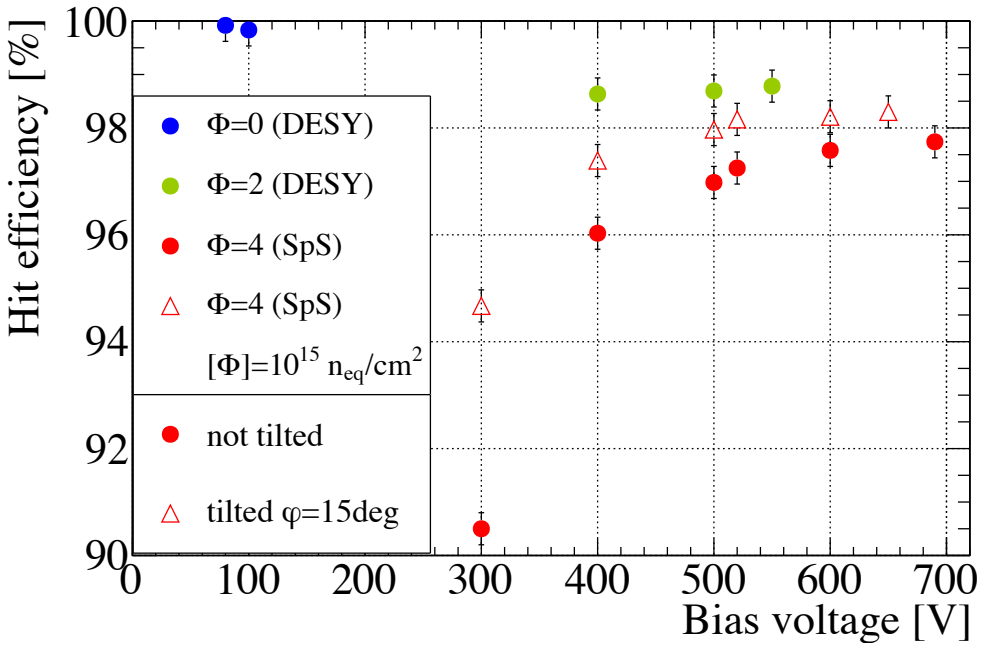
1000 V

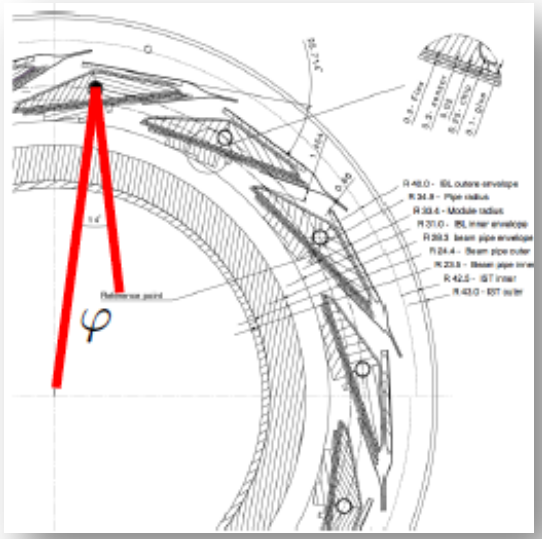
T. Wittig, Pixel 2012

FE-I4 modules 150 μm thick



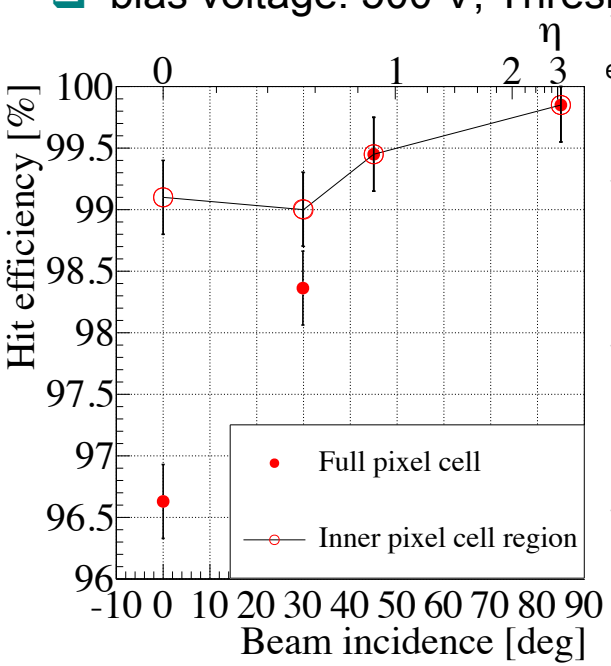
- designed and produced by MPP/HLL
- 6" wafers with FE-I4 sensors interconnected with bump-bonding at IZM
- irradiated up to 4×10^{15} n_{eq}/cm^2 in KIT and Los Alamos

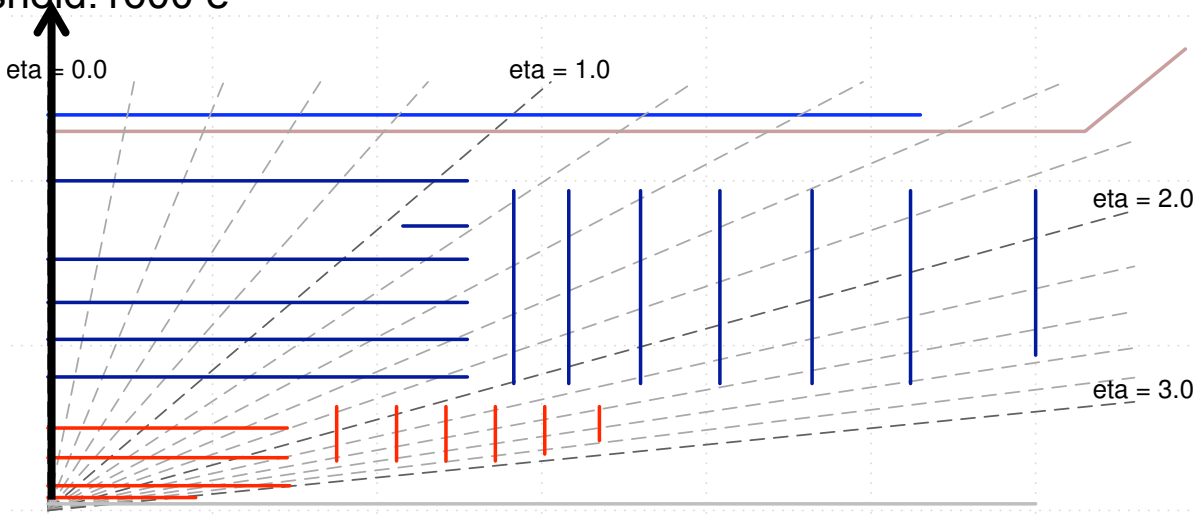




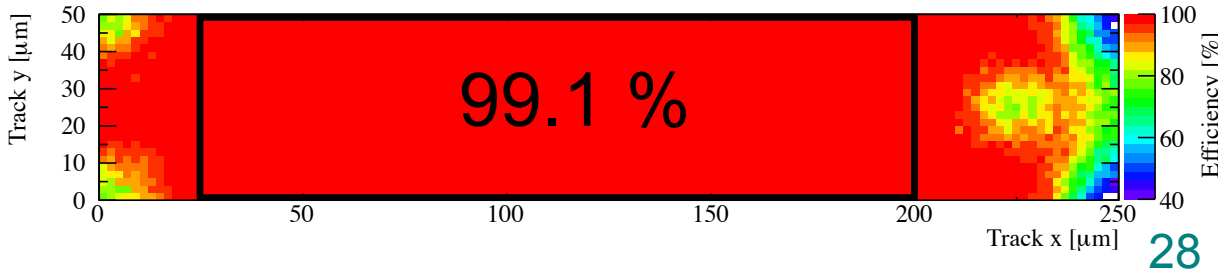
Hit efficiency at different η incidence

- FE-I4 150 μm thick, irradiated to 4x10^{15} n_{eq}/cm^2 in Los Alamos
- bias voltage: 500 V, Threshold:1600 e-



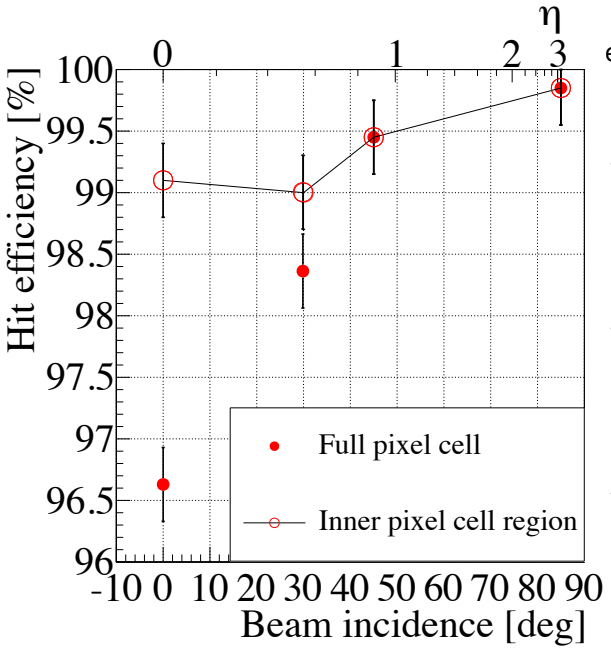


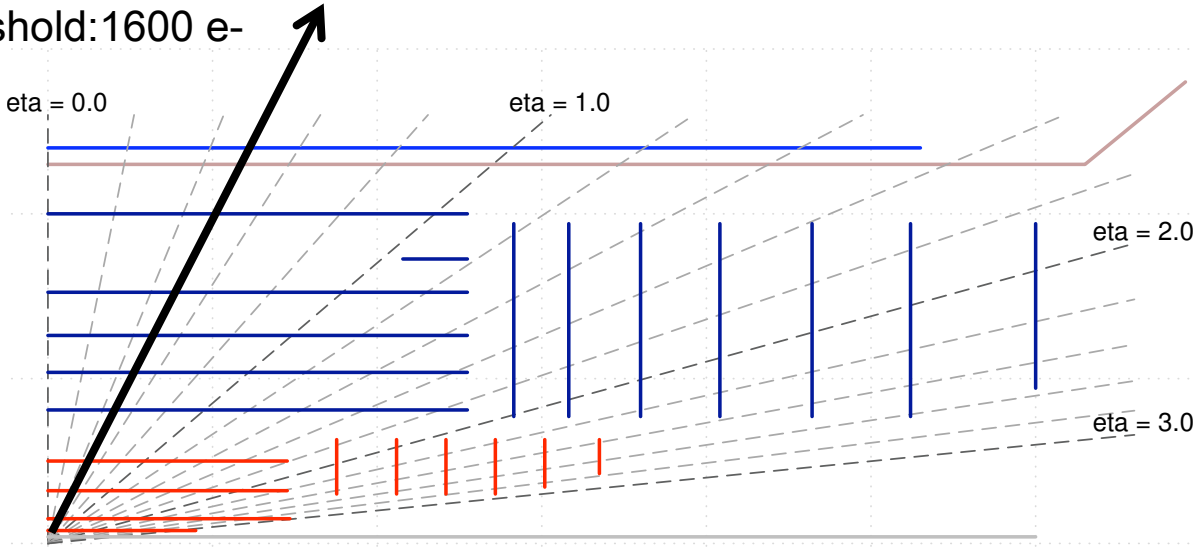
- 96.6 % hit efficiency for the full module at perpendicular incidence (500V)



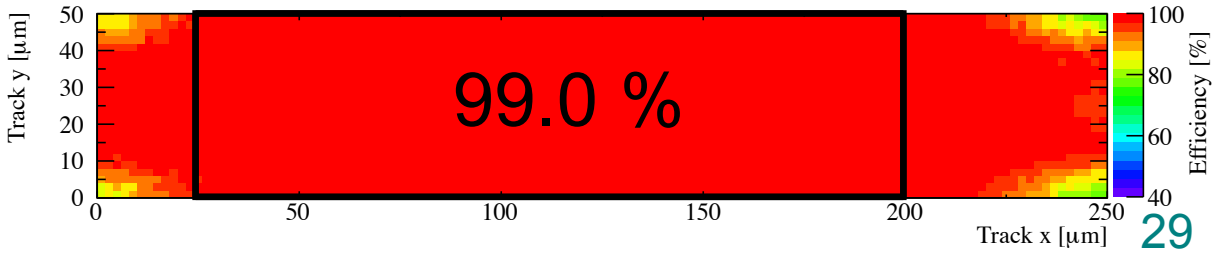
Hit efficiency at different η incidence

- FE-I4 150 μm thick, irradiated to 4×10^{15} n_{eq}/cm^2 in Los Alamos
- bias voltage: 500 V, Threshold:1600 e-



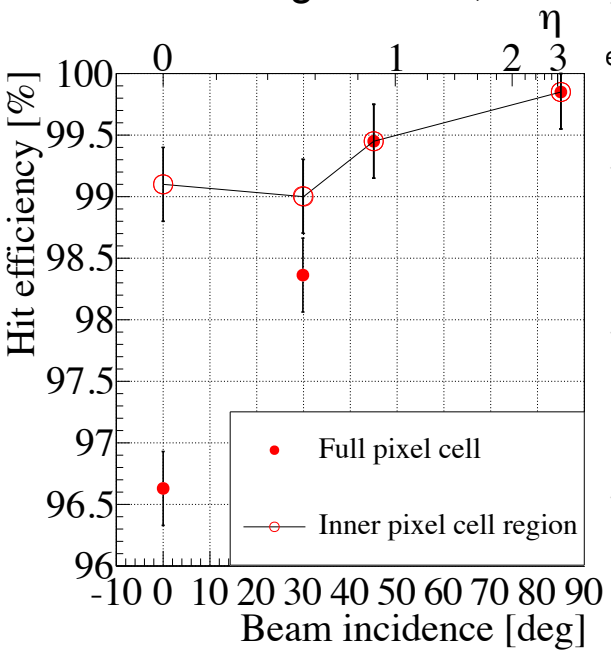


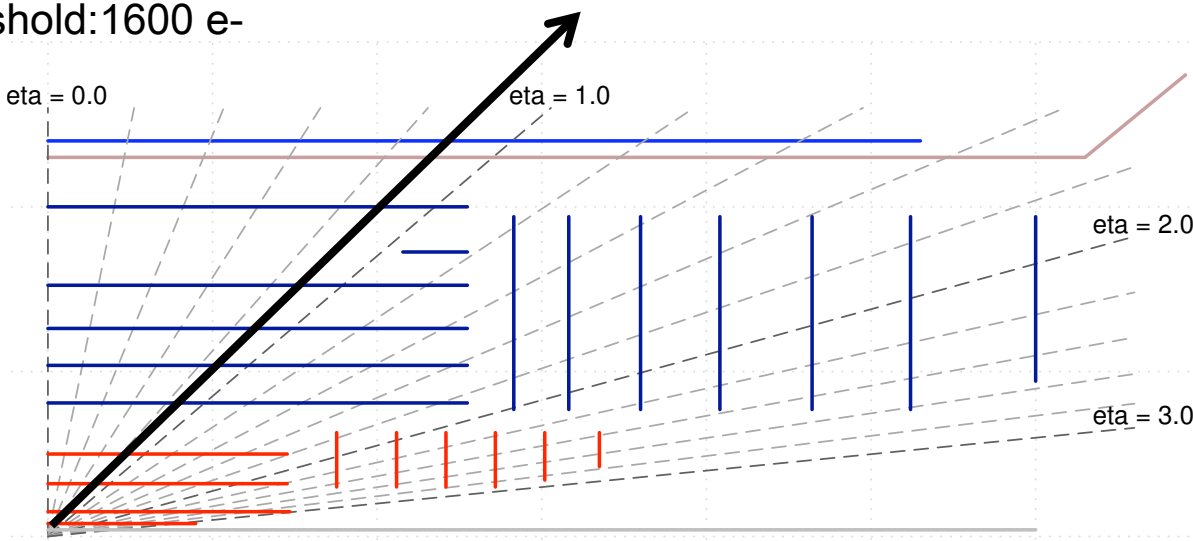
- 98.4 % hit efficiency for the full module at θ=30° (η=0.55) incidence (500V)

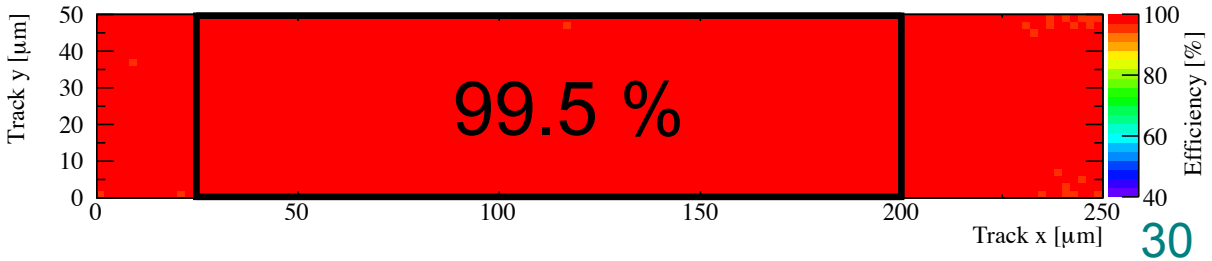


Hit efficiency at different η incidence

- FE-I4 150 μm thick, irradiated to 4×10^{15} n_{eq}/cm^2 in Los Alamos
- bias voltage: 500 V, Threshold:1600 e-



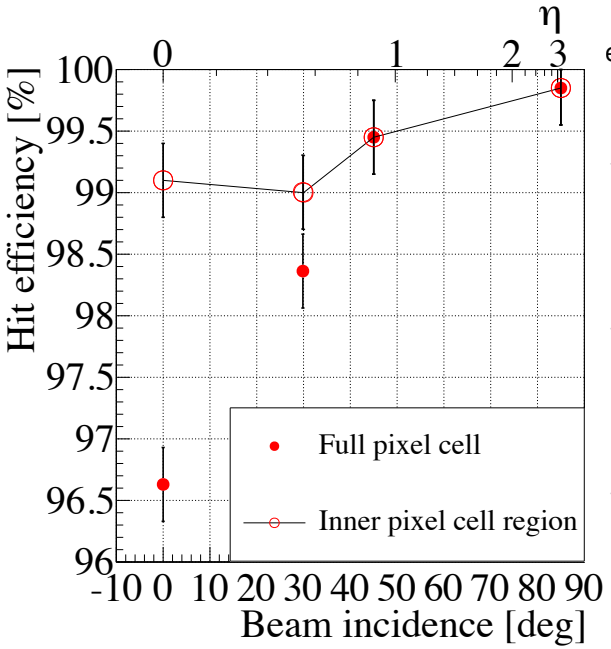


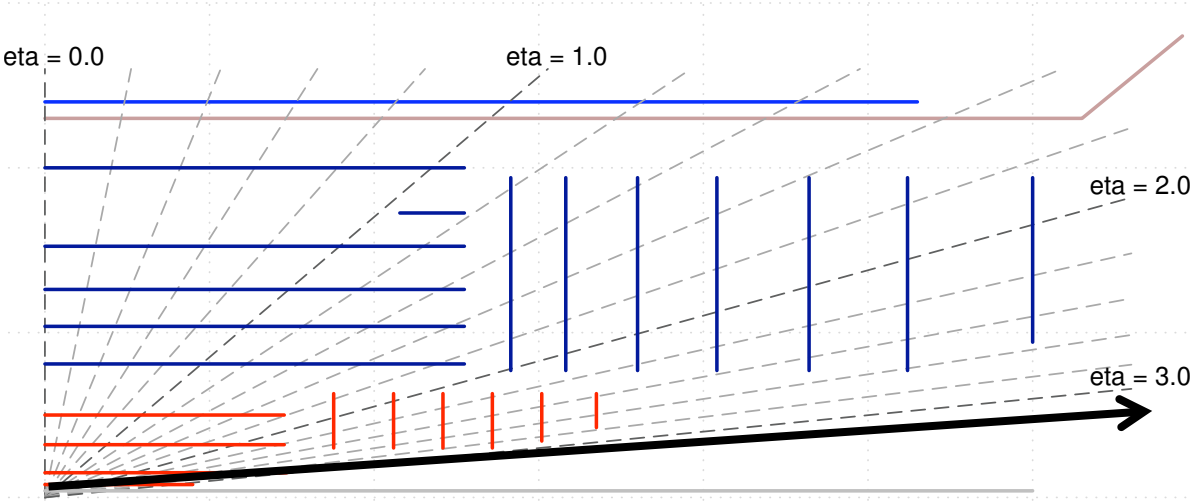


- 99.5 % hit efficiency for the full module at θ=45° (η=0.88) incidence (500V)

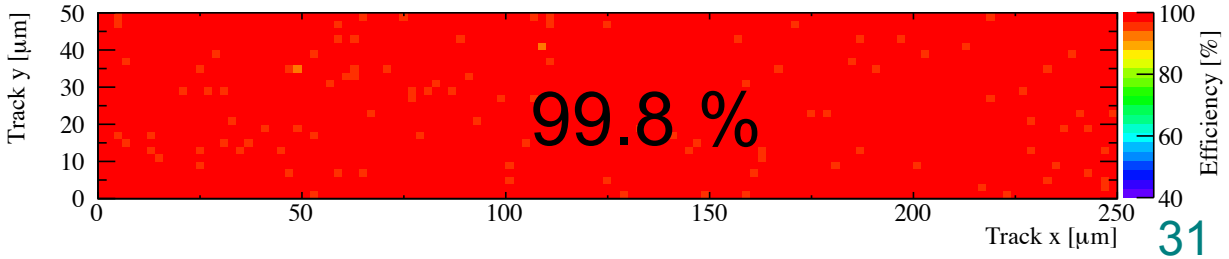
Hit efficiency at different η incidence

- FE-I4 150 μm thick, irradiated to 4×10^{15} n_{eq}/cm^2 in Los Alamos
- bias voltage: 500 V, Threshold:1600 e-





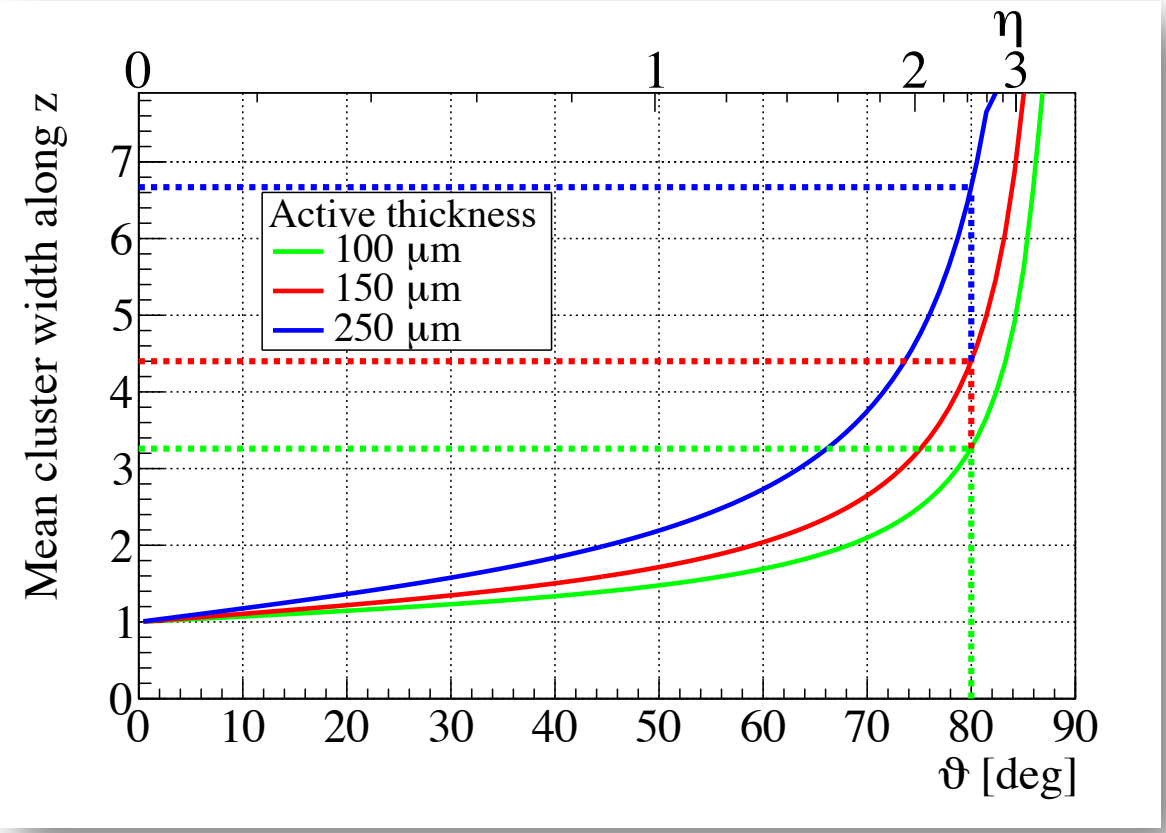
- 99.8 % hit efficiency for the full module at θ=85° (η=3.1) incidence (500V)



Sensor thickness and occupancy at high eta

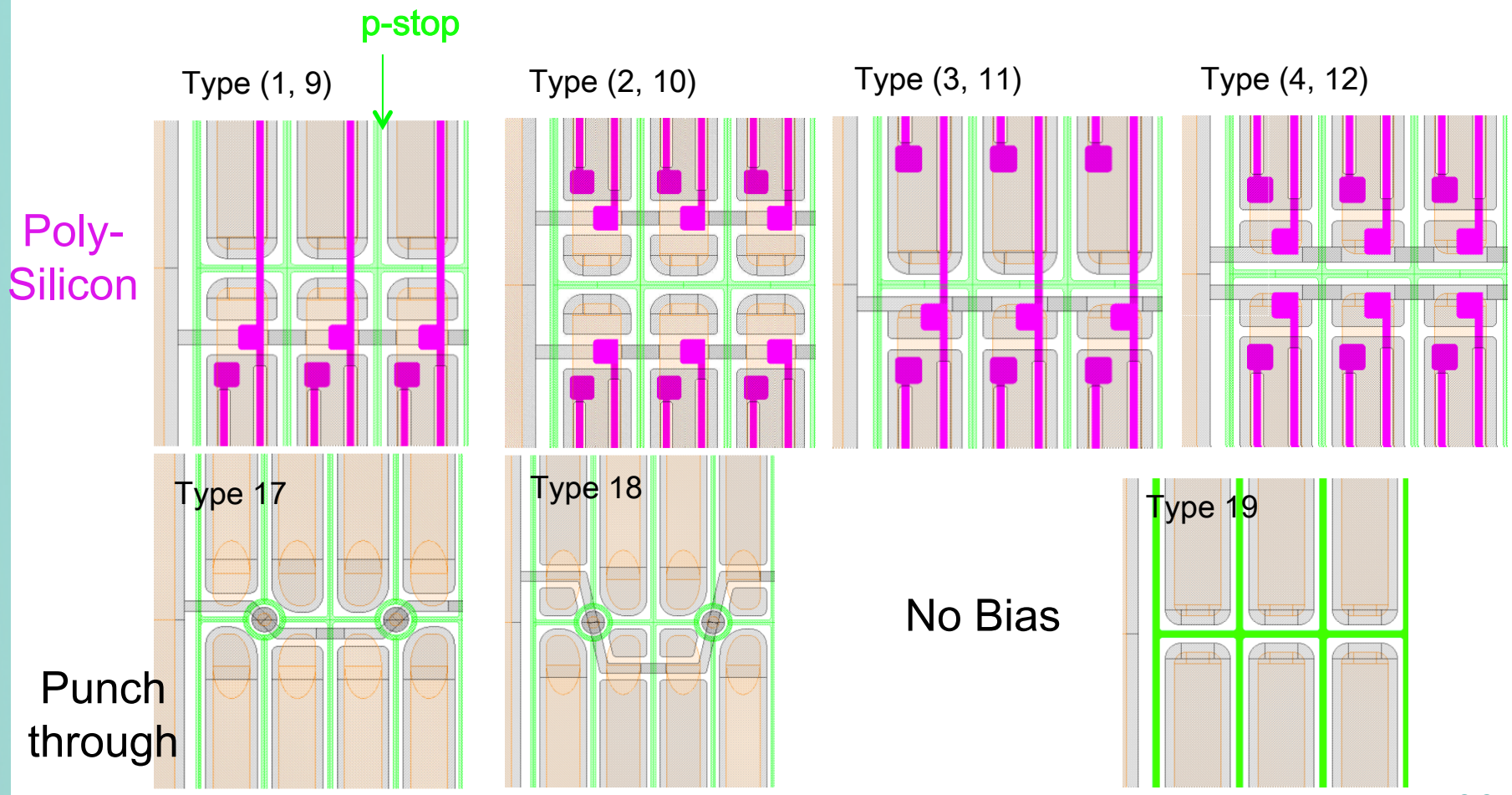
- Mean cluster width along the beam direction as a function of the pseudo-rapidity
- Assumed FE-I4 chip pitch along z: 250 μm

Reduced cluster size along the beam direction for thin sensors at high eta!



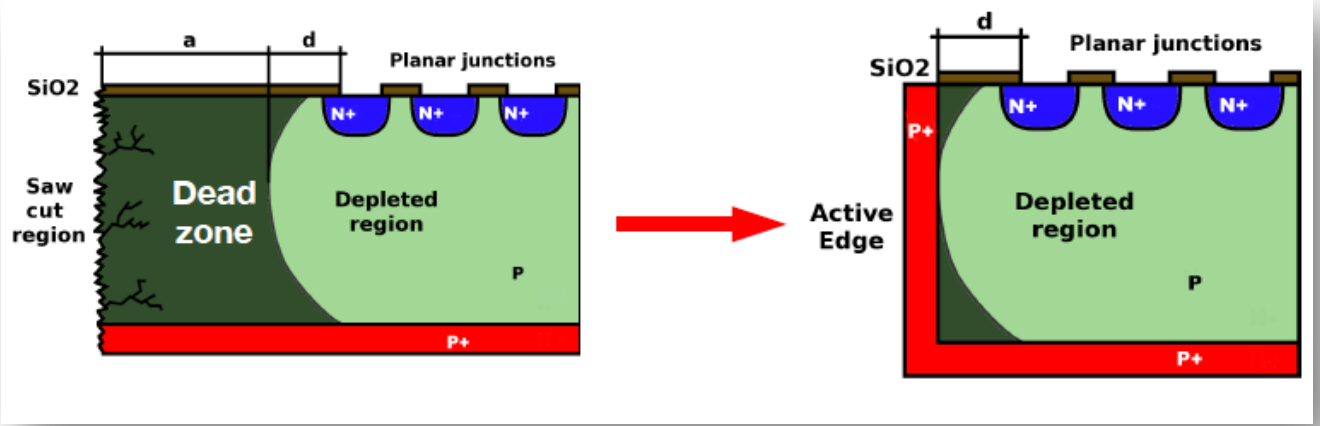
Active area design optimization

- New KEK-HPK productions of FE-I4 sensors
- Study of different pixel biasing schemes : Punch-through and poly-silicon



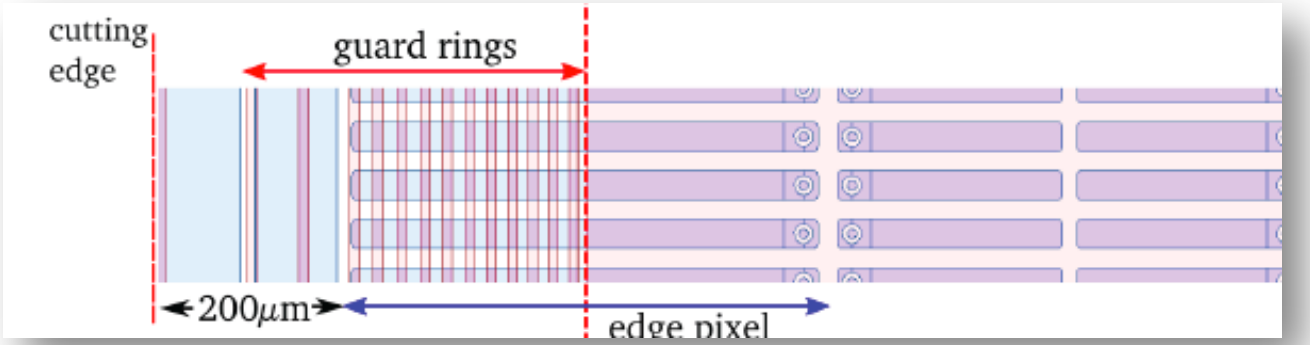
Slim edges planar pixel sensors - Overview

- Active edges for n-in-p pixels: Deep Reactive Ion Etching + Side implantation

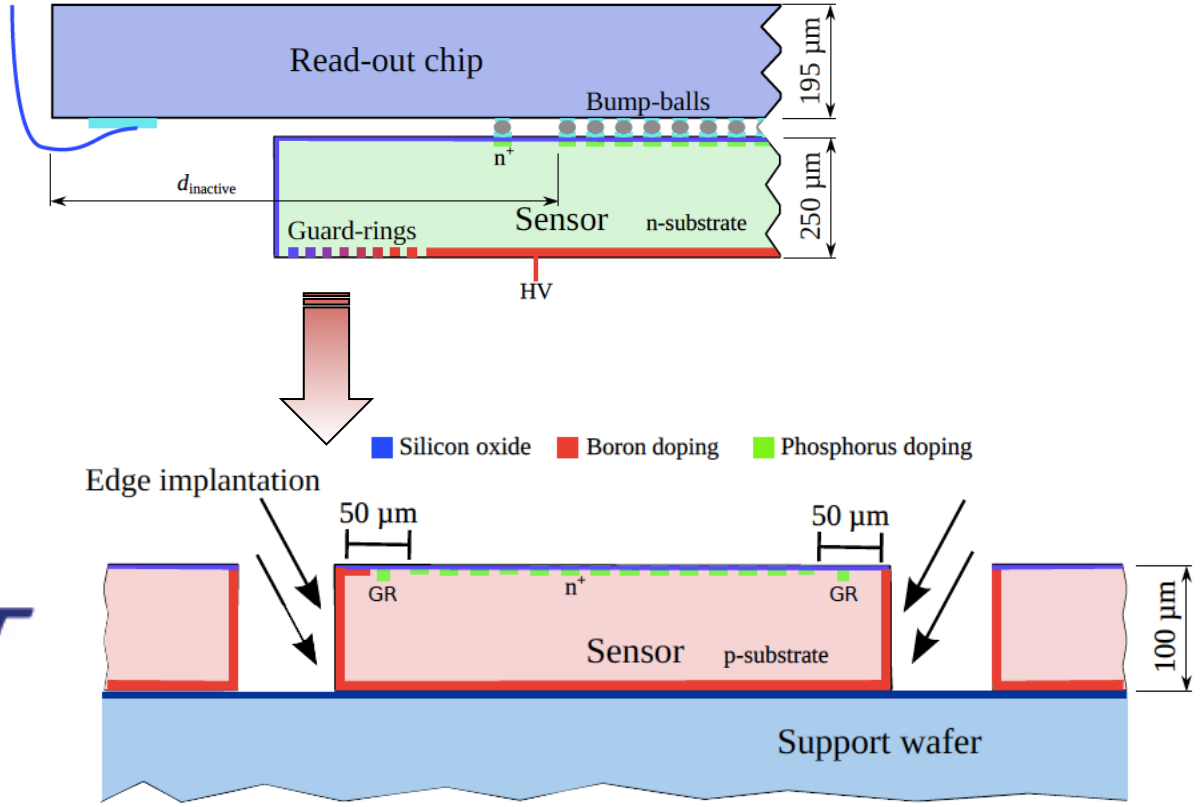


- Design optimization of the n-in-n sensors: GR on backside opposite to pixels on the front

IBL design

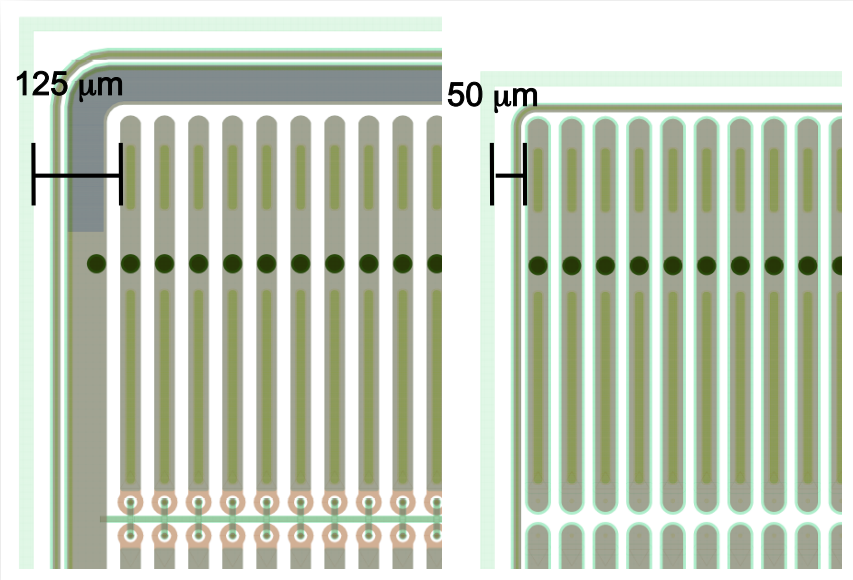


Active edge planar pixels



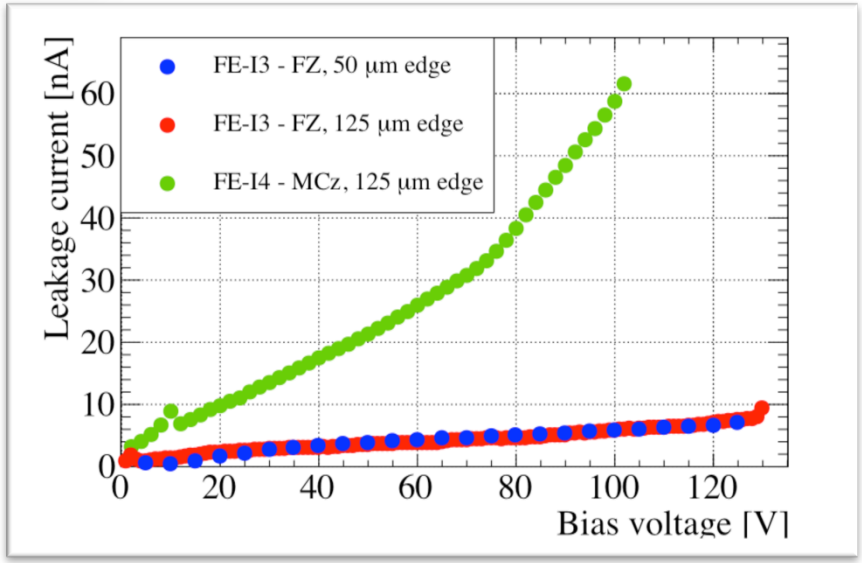
- n-in-p pixels on FZ and MCZ material
- 100 µm and 200 µm thickness →together with the active edges makes these sensors very attractive candidates for the inner layers in Phase II
- p-spray isolation method transferred from HLL to VTT
- Flip-chipping performed at VTT after removal of support wafer

Active edge: geometry and IV characterization



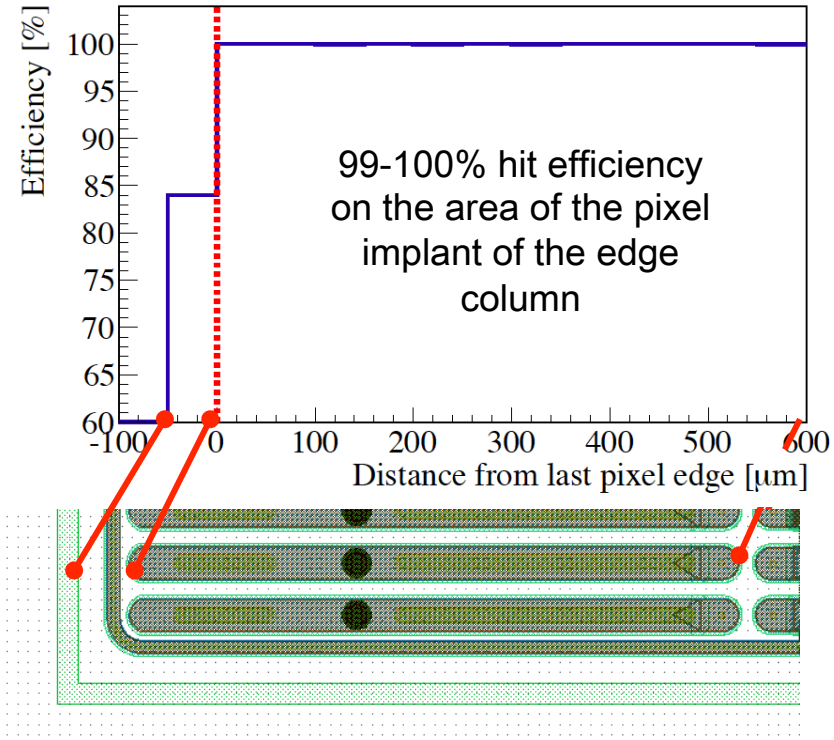
- 125 μm edge implemented In FE-I3 and FE-I4 sensors: Bias Ring + floating Guard Ring
- 50 μm implemented only in FE-I3 sensors: Floating Guard Ring

- Very low leakage current level, < 100 nA for FE-I3 and FE-I4 sensors
- Breakdown voltage at 100-110V, much higher than depletion voltage ~ 15V



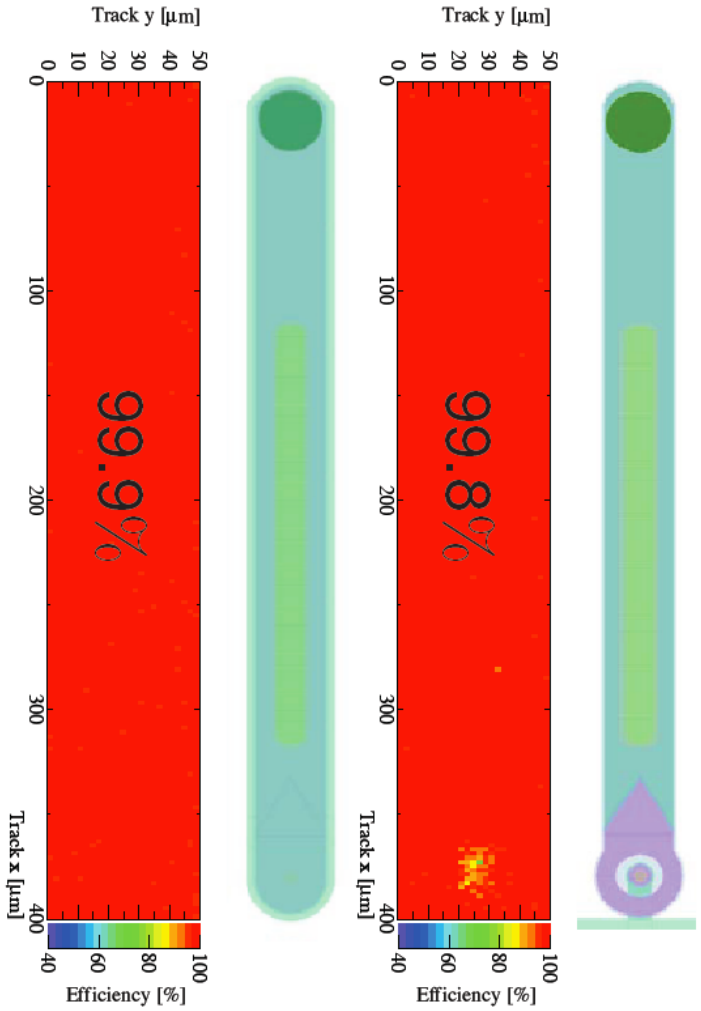
Hit efficiency in the edge region

Edge Tracking Efficiency in Beam Tests at SPS



- 84^{+9}_{-14} % efficiency in the last 50 μm of the sensor edge, beyond last pixel implant

Global Efficiency in beam test

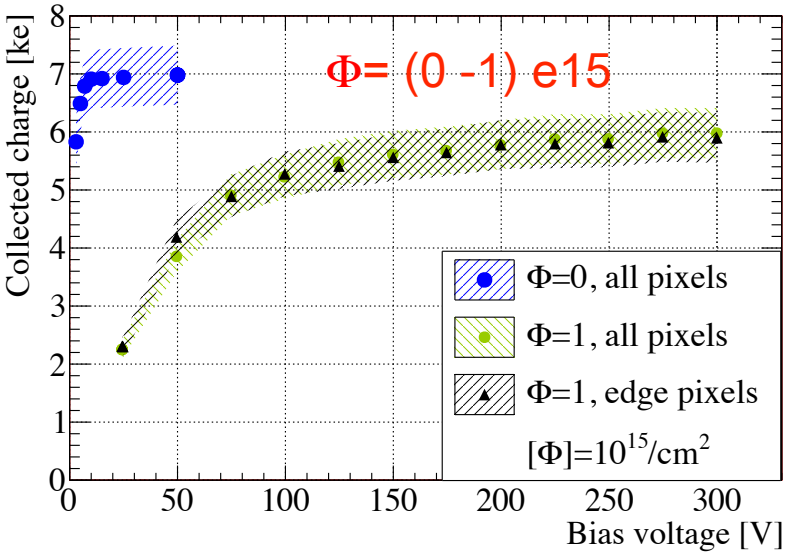


FE-I3, 50 μm edge, Vbias=20V

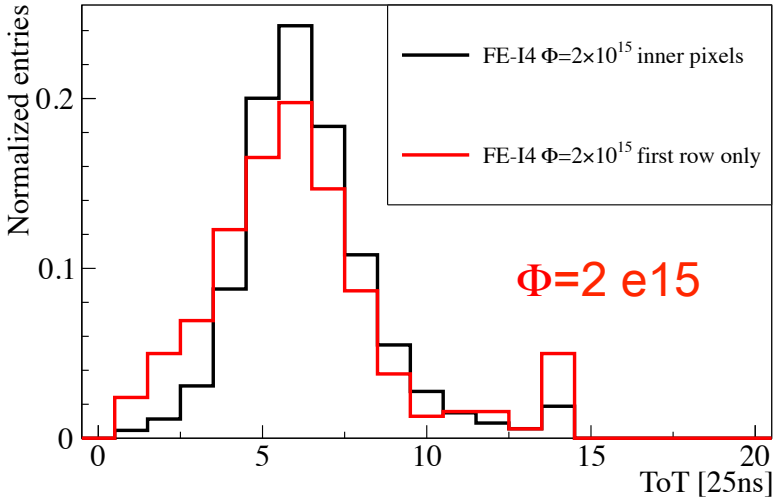
FE-I3, 125 μm edge, Vbias=20V

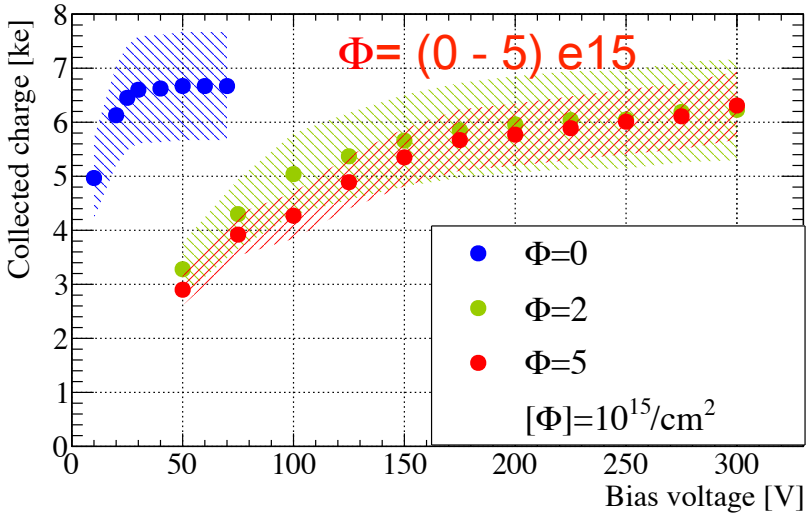
Active edge: CCE after irradiation

- FE-I3 100 μm thick sensor with 125 μm slim edge, threshold 1500 e- → 87% CCE at 300 V for both all and edge pixels after irradiation at KIT ($1x10^{15}$ n_{eq}/cm^2)



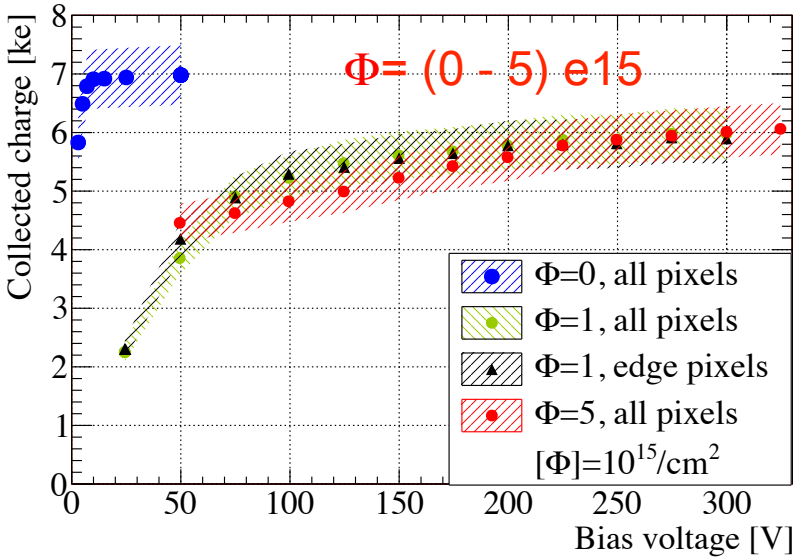
- p-type MCZ FE-I4, 100 μm thick sensor, with 125 μm slim edge, threshold 1100 e- → compatible charge collection properties between edge and internal pixels





Active edge: CCE after irradiation

- FE-I3 100 μm thick sensor with 125 μm slim edge, threshold 1500 e- → 87% CCE at 300 V for both all and edge pixels after irradiation at KIT ($1x10^{15}$ n_{eq}/cm^2) and in Ljubljana ($5x10^{15}$ n_{eq}/cm^2)



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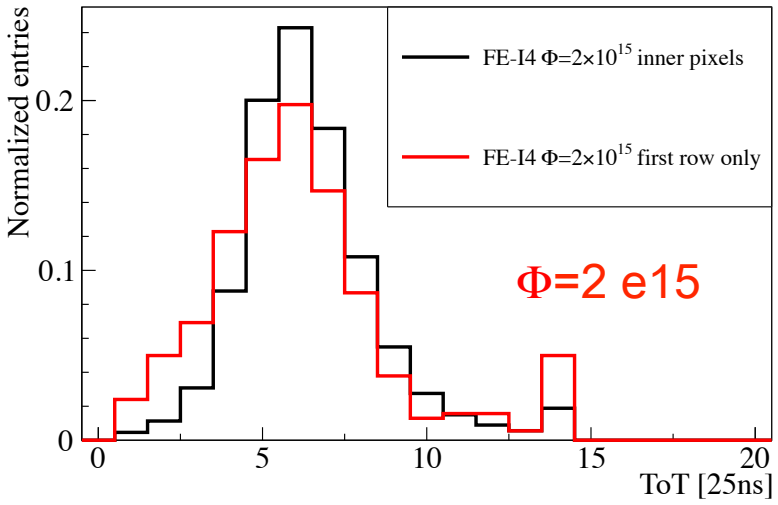
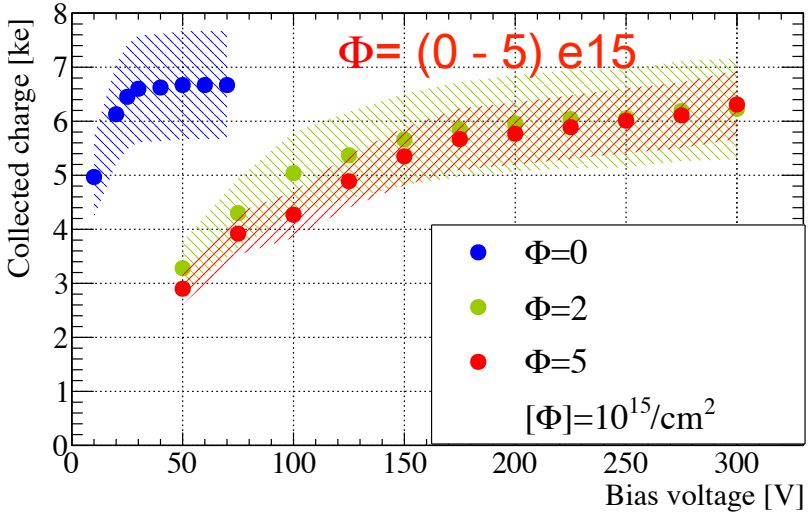
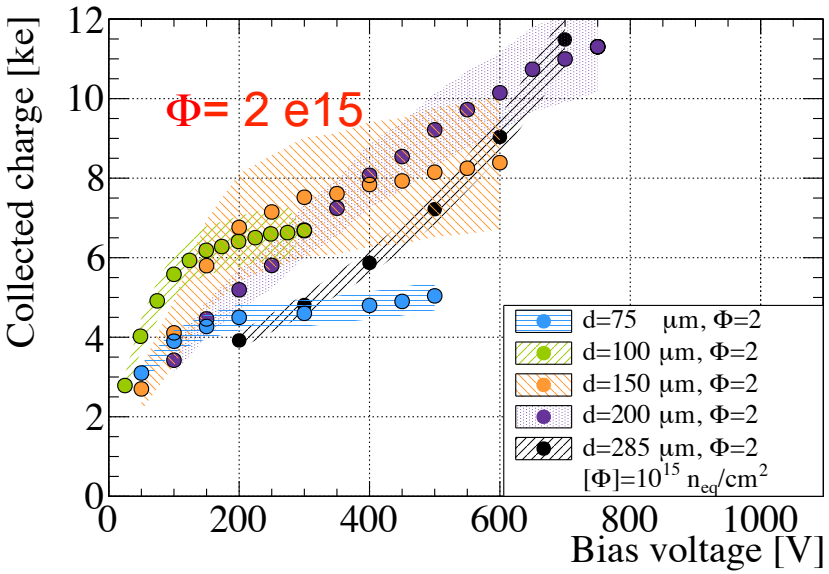
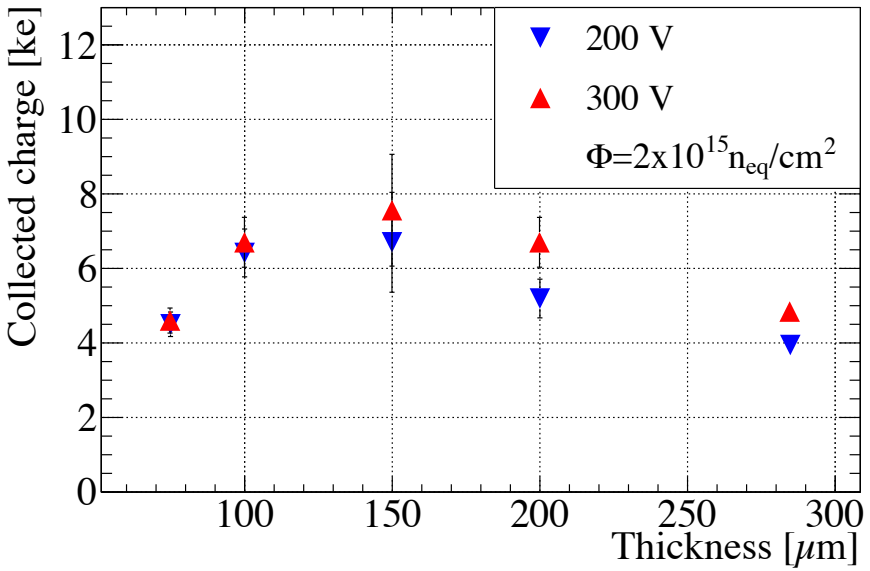
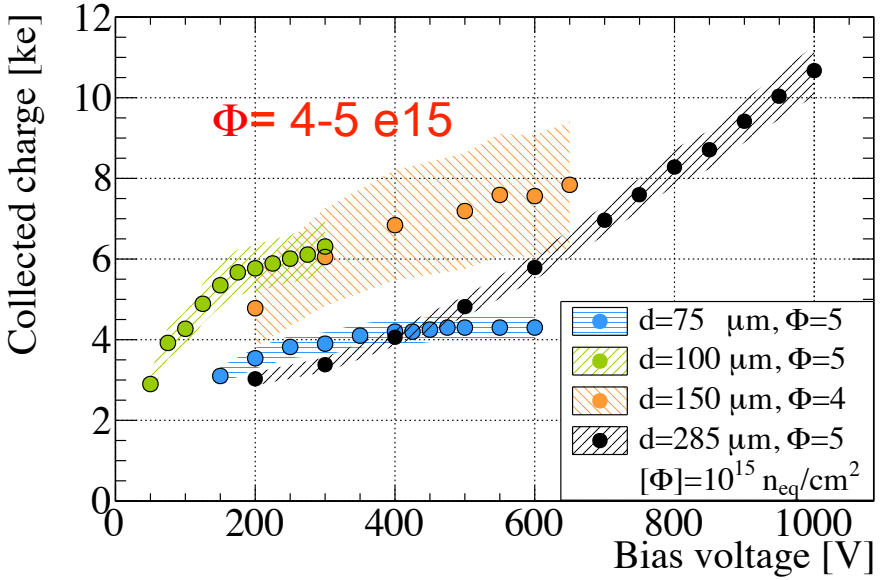


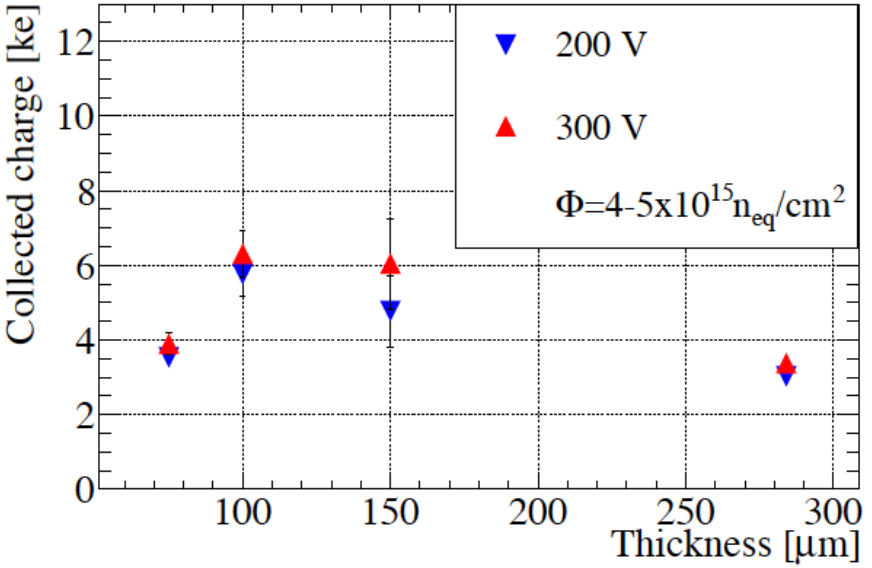


Charge collection for pixels of different thickness

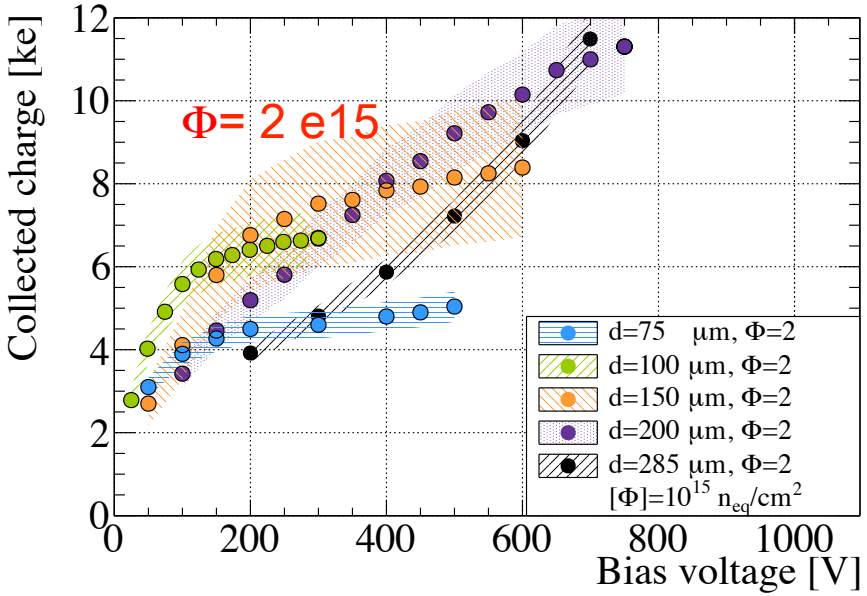




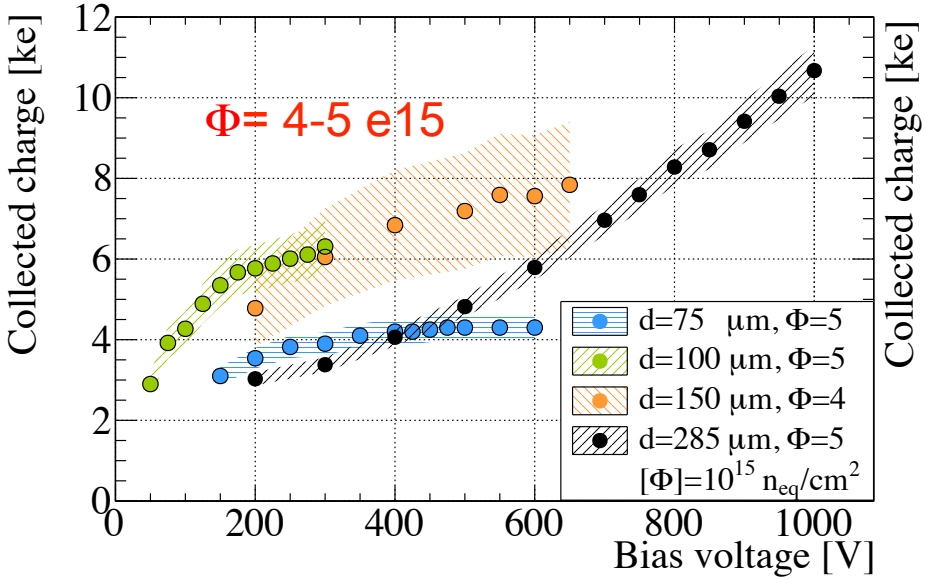


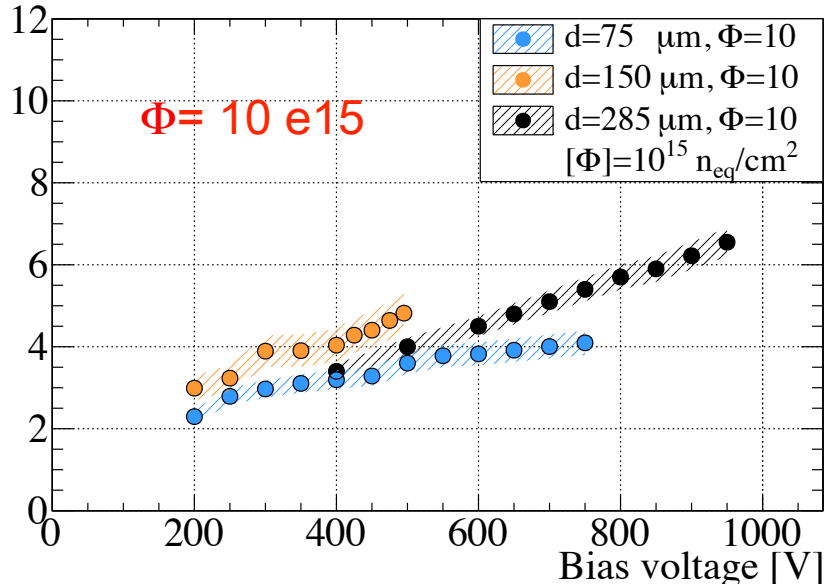


Charge collection for pixels of different thickness



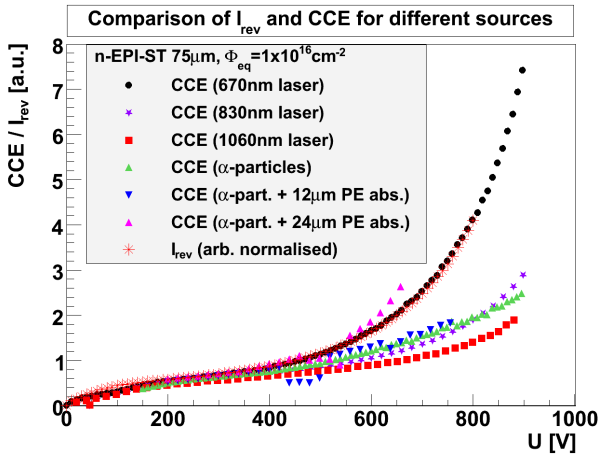
- The 100-150 μm thick sensors show higher charge collection up to a fluence of 4-5x10^{15} n_{eq} / cm^2
- At higher fluences the effect of charge trapping tends to equalize the charge collection efficiency for all thicknesses





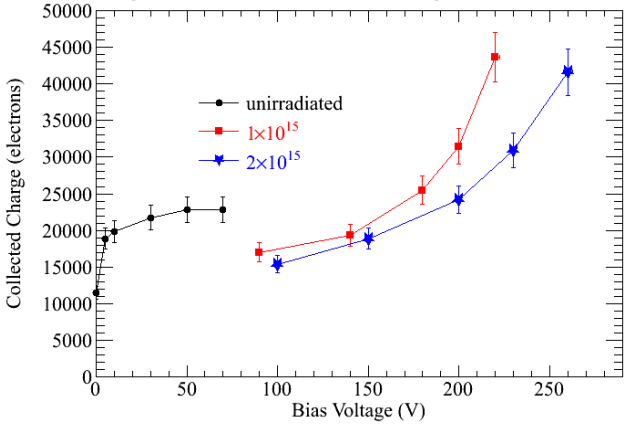
Charge multiplication

- Charge Multiplication observed and characterized after high levels of irradiation with different techniques and in several different types of devices



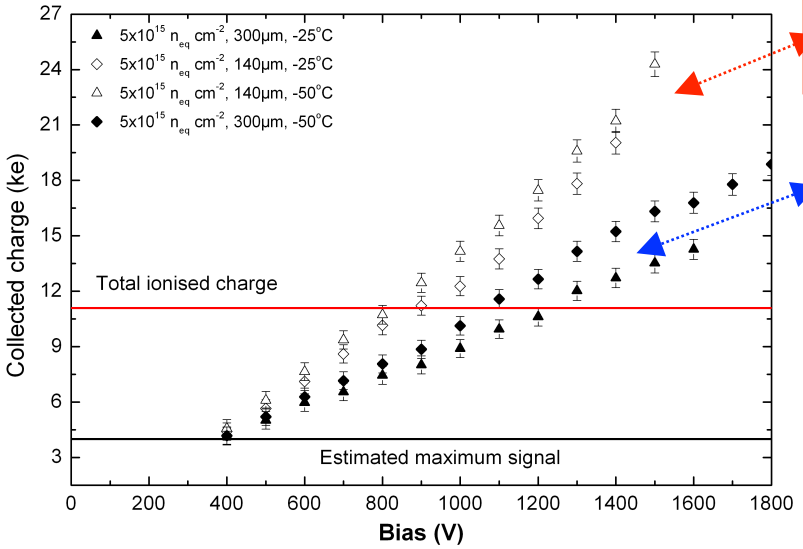
Diodes (Φ_{eq}=10^{16} cm^{-2})

Leakage Current & Charge Collection



3D sensors (Φ_{eq}=1-2×10^{15} cm^{-2})

Charge Collection (test beam)



140 μm thick device

300 μm thick device

Strip sensors (Φ_{eq}=5×10^{15} cm^{-2}, 26 MeV p)

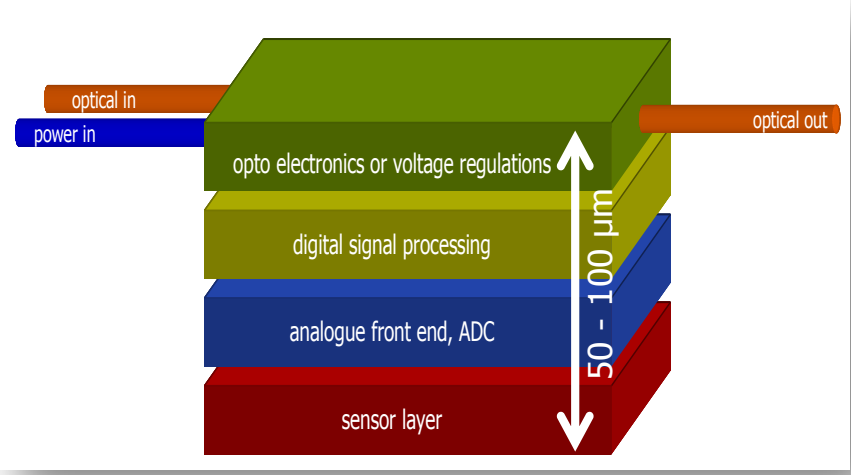
Charge Collection (Beta source, Alibava)

Ref: Diode: J.Lange et al, 16th RD50 Workshop, Barcelona
Strip: G. Casse et al., NIMA 624, 2010, Pages 401-404
3D: M.Koehler et al., 16thRD50 Workshop, Barcelona

Vertical Integration Technologies and 3D sensors for Phase II

Vertical Integration Technologies

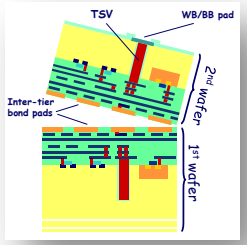
3D electronics: "the vertical integration of thinned and bonded silicon integrated circuits with vertical interconnects between the IC layers"



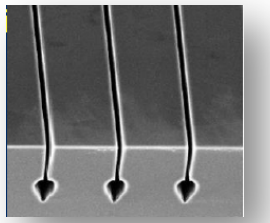
New demanding specifications for experiments at new machines:

- Improve resolution → shrink pixel size and pitch, down to 20 μm or even less
- Preserve or even increase pixel-level electronic functions: handling of high data rates (hit rates > 10 MHz/mm^2), analog-to digital conversion while reducing the pixel size
- Decrease amount of material ⇒ thin sensor and electronics chips, "zero mass" cooling
- 100-200 μm total module thickness

Evolution of Micro-Electronic Technologies



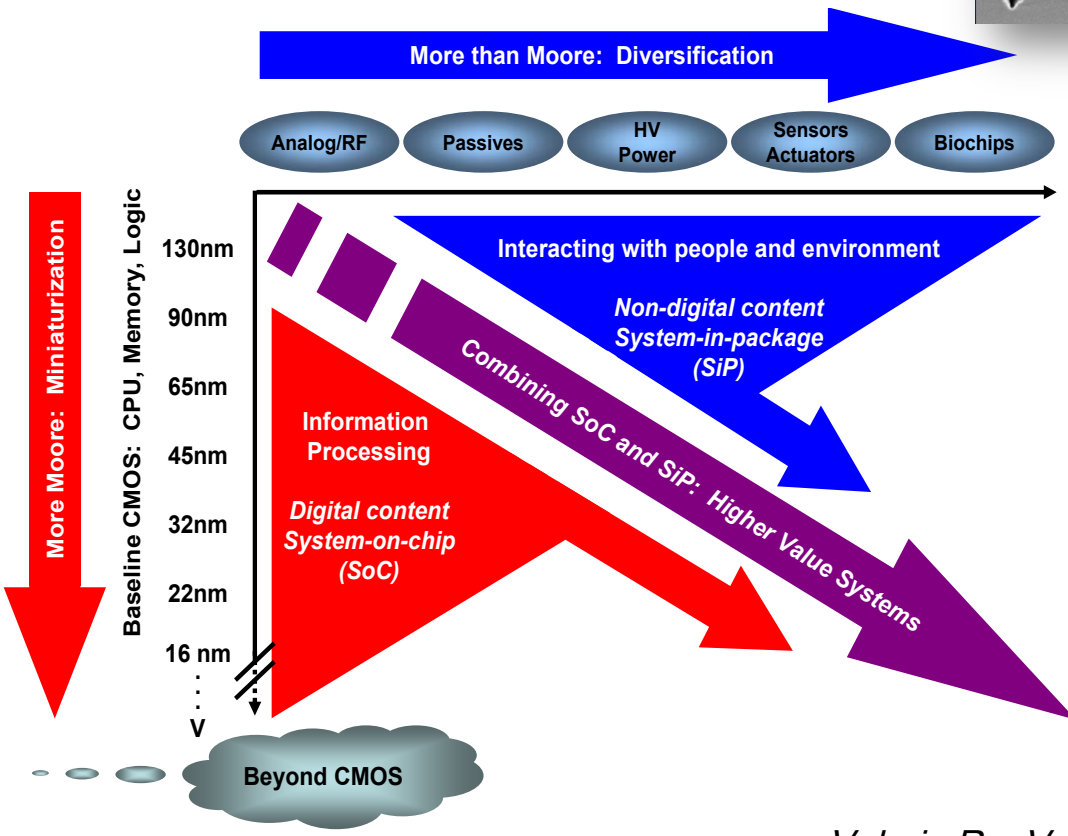
Through Silicon Vias

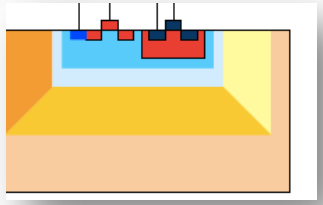


Micro-channel cooling

No roadmap, room for new ideas: monolithic sensors, 3D integration

Evolutionary roadmap: nanoscale CMOS





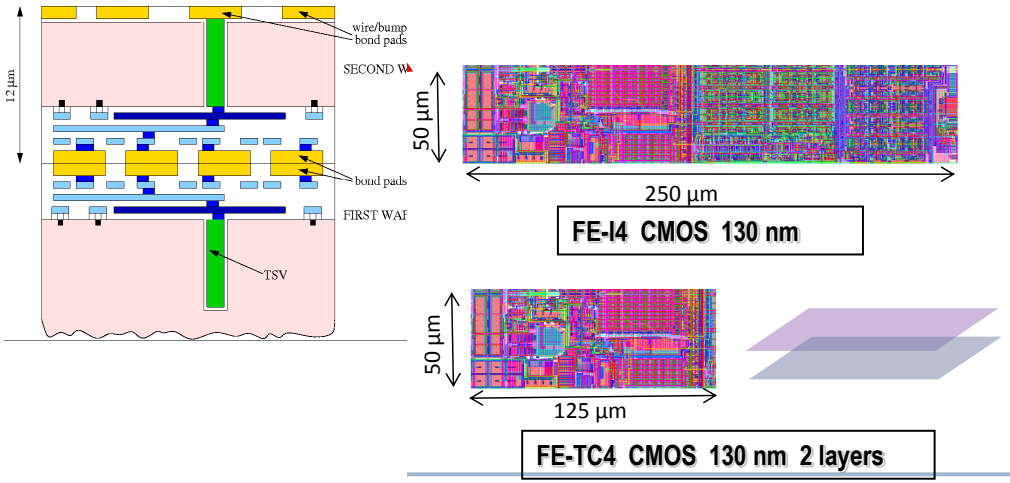
Monolithic sensors

Valerio Re, Vertex 2013

Through Silicon Vias: Via First or Via Last

Via first, Via middle: Vias are part of wafer processing at the CMOS foundry, and are inserted before or right after the fabrication of transistors

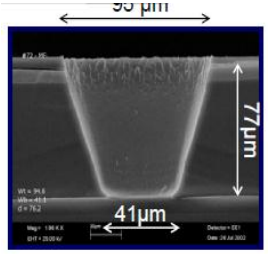
➔ **High density TSVs** (few μm pitch) through thinned wafers, allow multiple connections at the cell (pixel) level between transistor layers

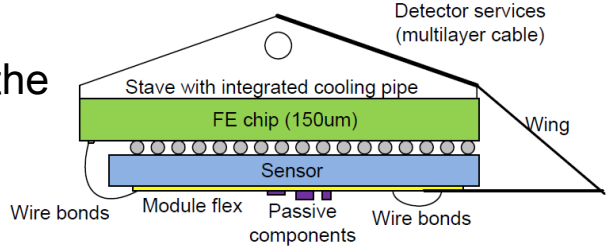


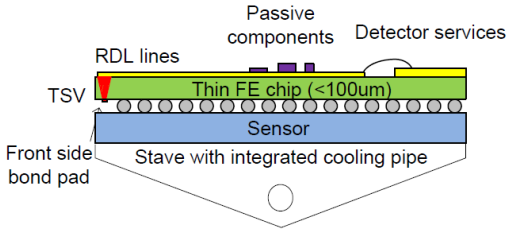
Valerio Re, Vertex 2013

Via last: Vias are fabricated on fully processed CMOS wafers, at a facility outside the CMOS foundry

➔ **Low density TSVs** (tens of μm pitch) through unthinned wafers or partially thinned wafers, allow connectivity at the pad level in the chip periphery

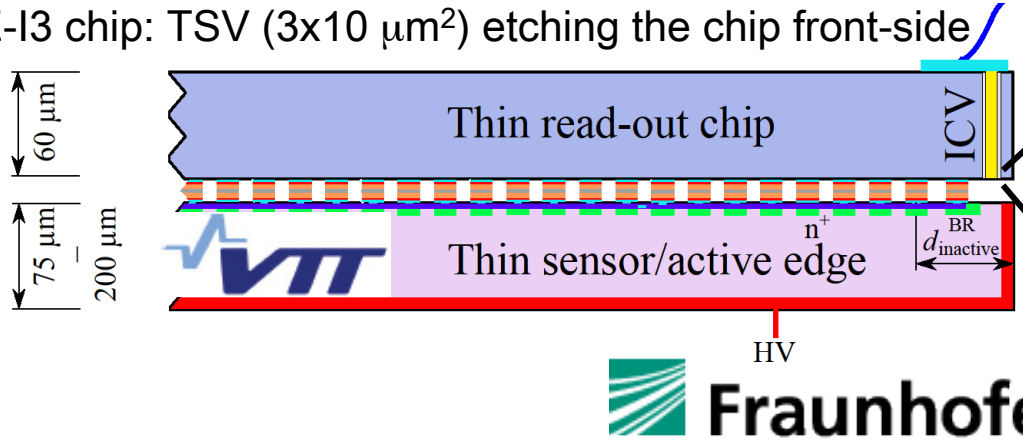




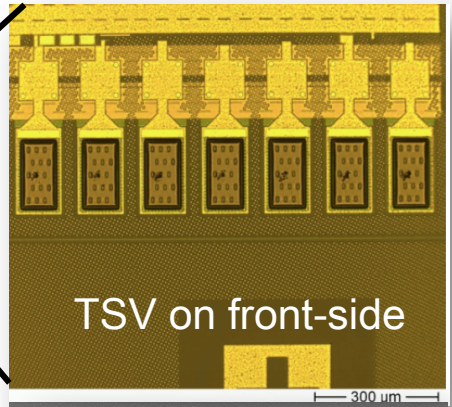


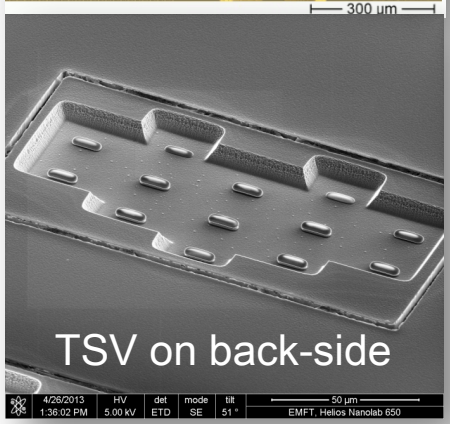
Through Silicon Vias

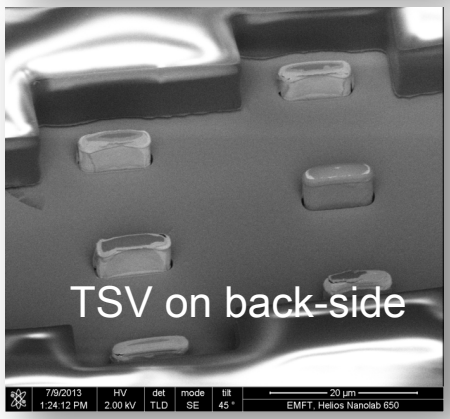
FE-I3 chip: TSV (3x10 μm²) etching the chip front-side



Fraunhofer EMFT





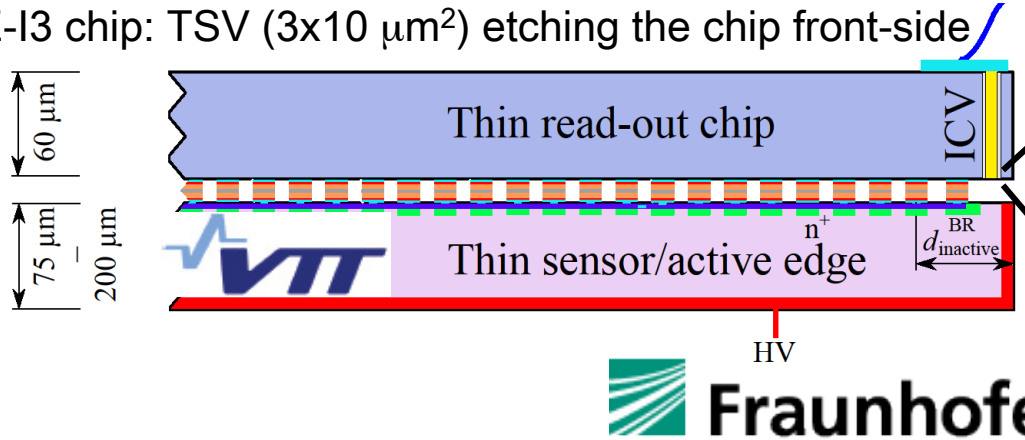


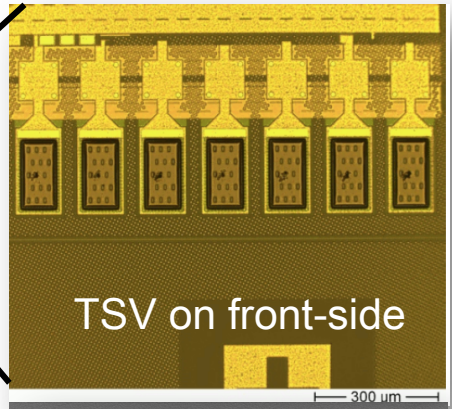
❑ Processing sequence:

- Via- and trench etching in Bosch-process, TSV cross-sect. of 3x10 μm²
- insulation with TEOS (low T)
- filling of vias with Tungsten
- attachment to handle-wafer on the top side and thinning to desired thickness of chip ~ 60 μm
- redistribution layer on the backside
- SLID-interconnection to sensor wafer.

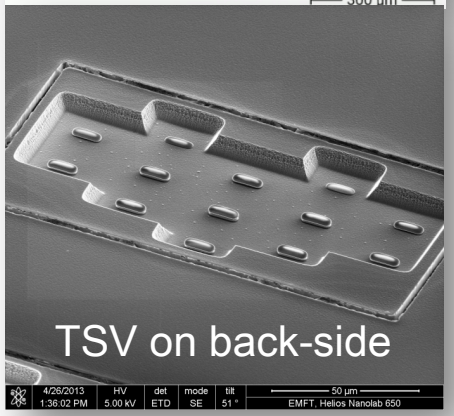
Through Silicon Vias

FE-I3 chip: TSV (3x10 μm²) etching the chip front-side





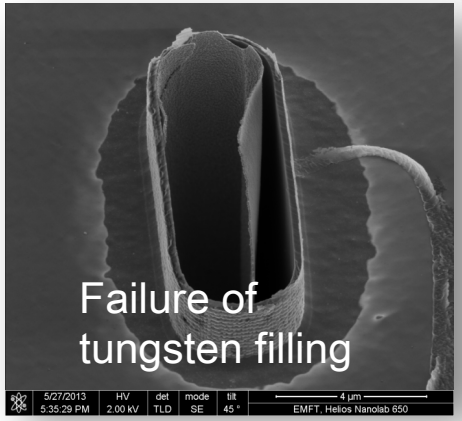
Fraunhofer EMFT

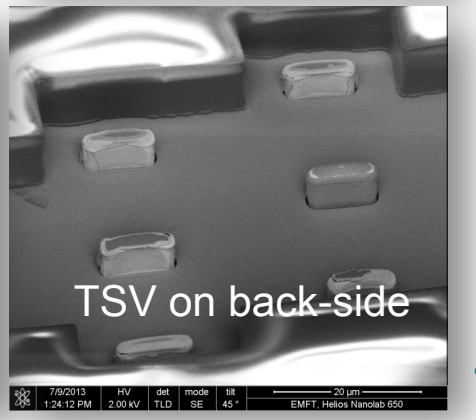


❑ Processing sequence:

- Via- and trench etching in Bosch-process, TSV cross-sect. of 3x10 μm²
- insulation with TEOS (low T)
- filling of vias with Tungsten
- attachment to handle-wafer on the top side and thinning to desired thickness of chip ~ 60 μm
- redistribution layer on the backside
- SLID-interconnection to sensor wafer.

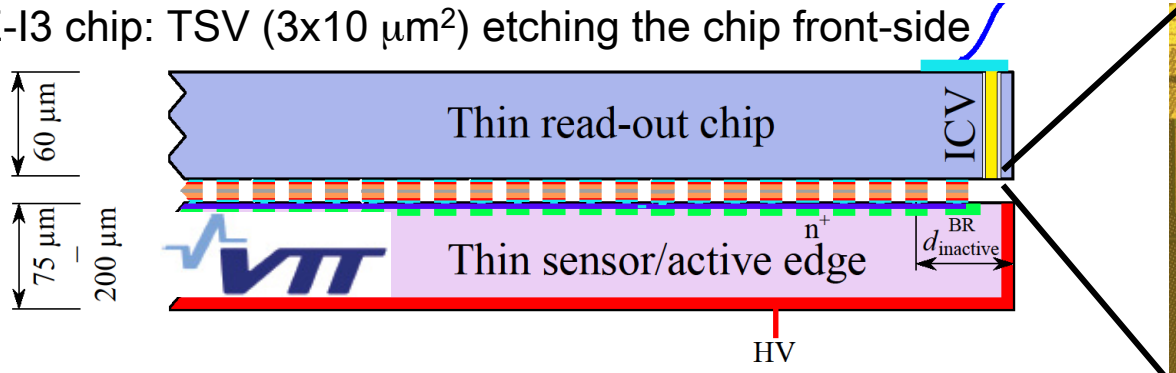
No tungsten adhesion within the TSV

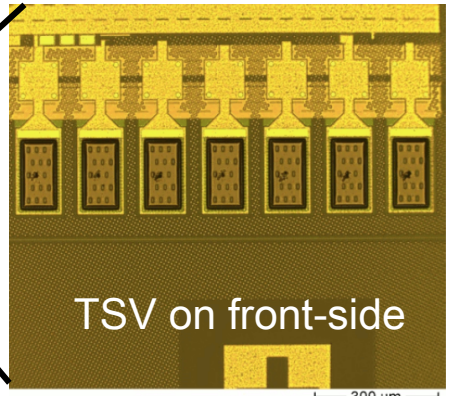




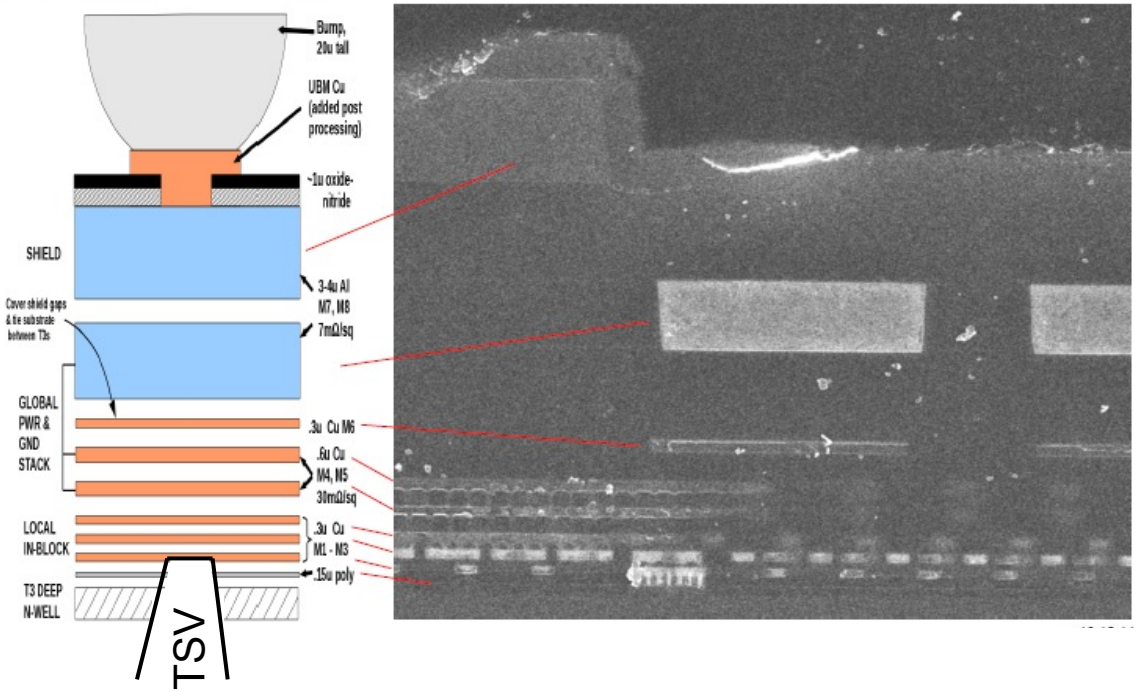
Through Silicon Vias

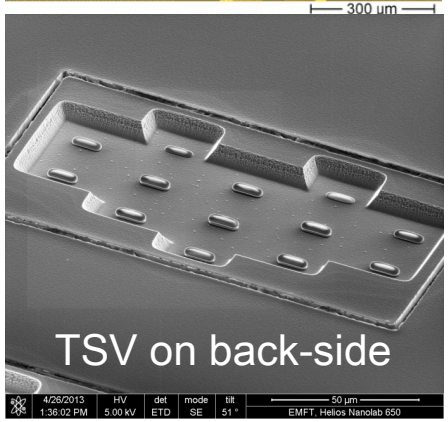
FE-I3 chip: TSV (3x10 μm²) etching the chip front-side

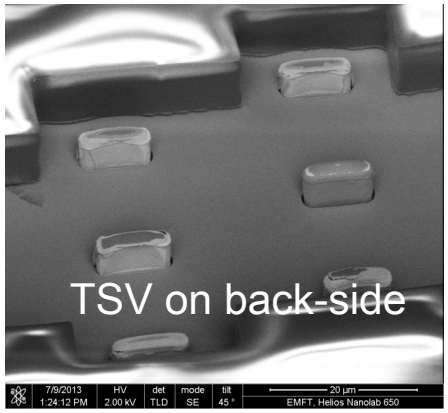




FE-I4 chip: TSV (~10x30 μm²) etching the chip back-side

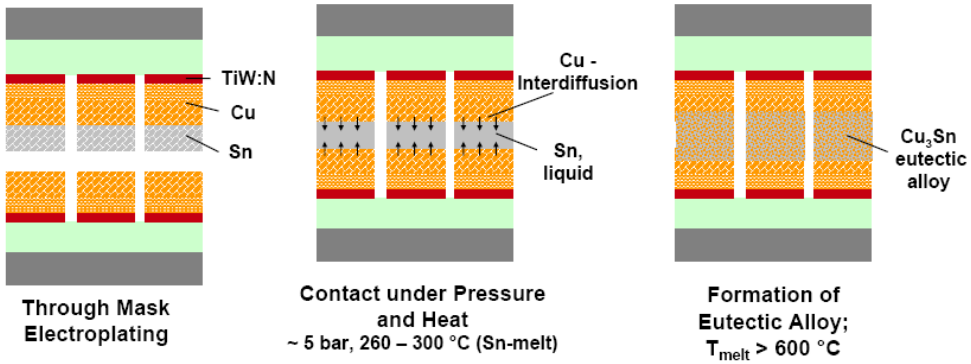






SLID Interconnection

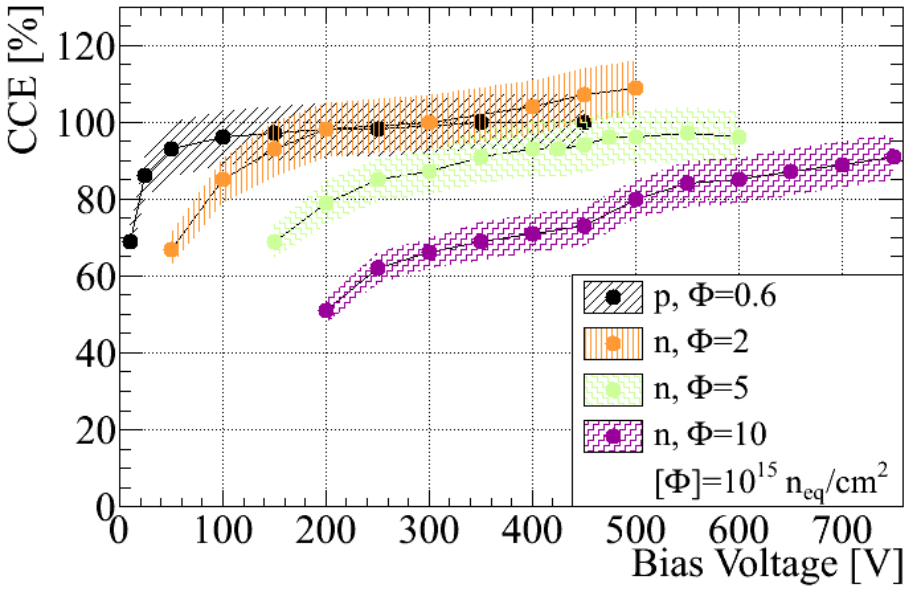
Metallization SLID (Solid Liquid Interdiffusion)



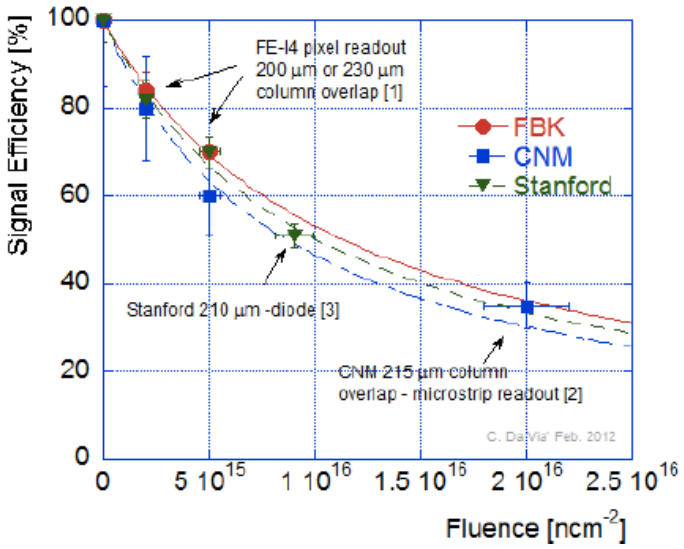
Fraunhofer EMFT

- Alternative to bump bonding (less process steps "lower cost" (EMFT)).
- Small pitch possible (~ 20 μm, depending on pick & place precision).
- Stacking possible (next bonding process does not affect previous bond).
- Wafer to wafer and chip to wafer possible.

- Successful interconnection run with FE-I3 chips and sensors with 75 μm active thickness
- Stable SLID interconnection after irradiation and thermal cycling
- Good Charge Collection efficiency after irradiation up to 10^{16} n_{eq}/cm^2



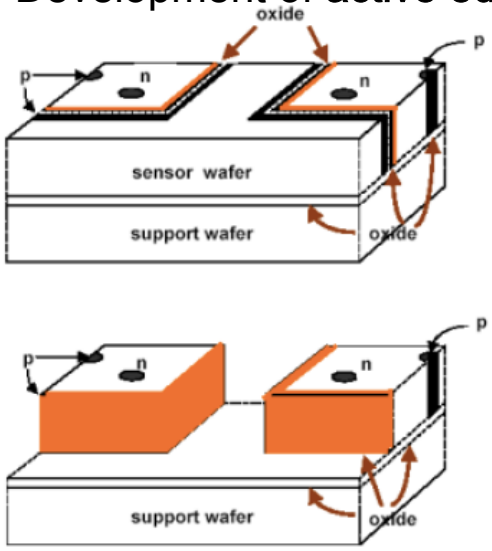
3D pixel sensors for Phase II

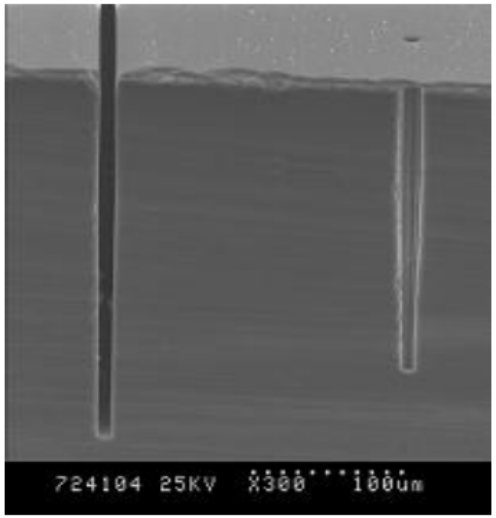


Cinzia Da Via', Hiroshima 2013

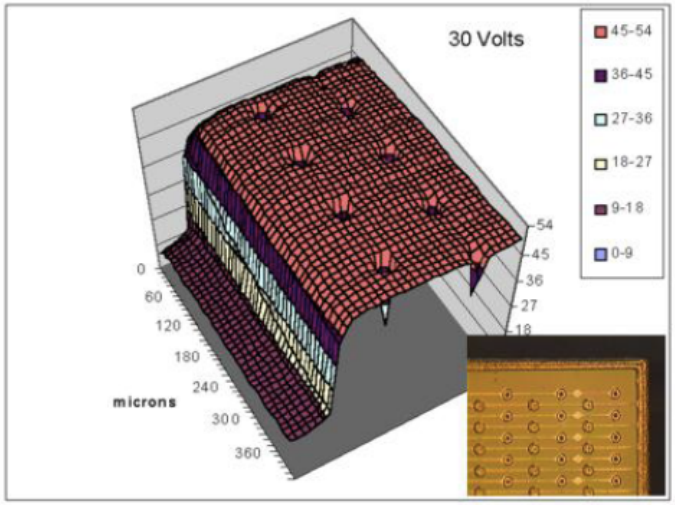
- 3D Pixels for Phase II: first indications of good **radiation resistance** up to a fluence of 2×10^{16} n_{eq}/cm^2
- R&D for Phase II:
  - Thinner sensors
  - Active edges

Development of **active edges** with the use of a handle wafer





Etched trench + electrode

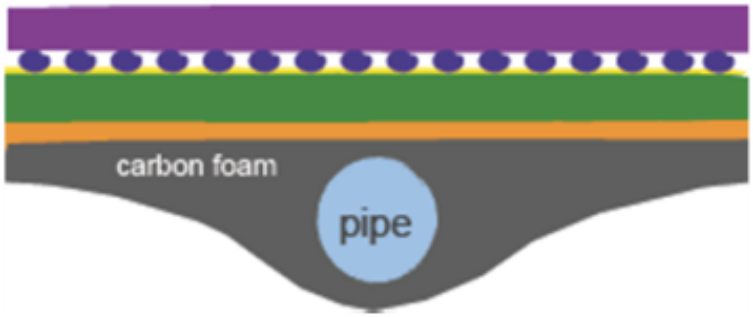


Charge Collection by X-ray beam

Micro-channel cooling

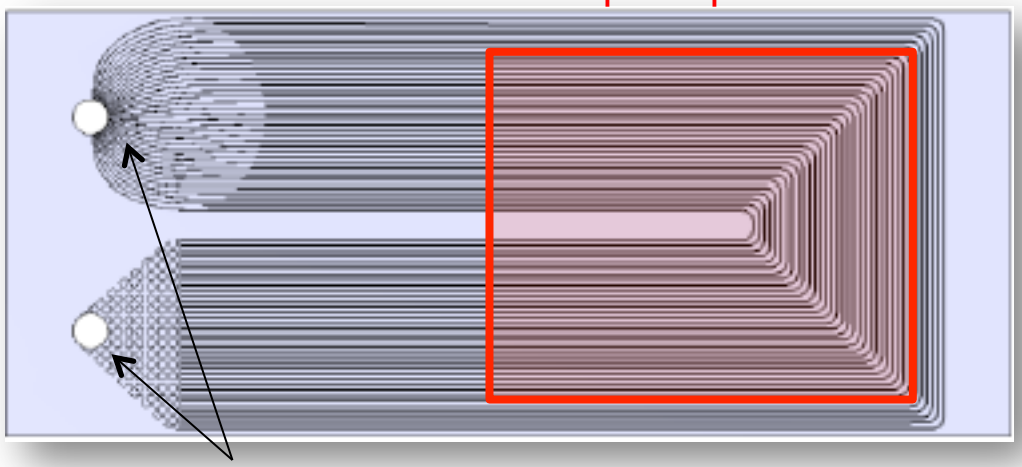
- 3D Pixels for Phase II: embedded micro-channels with CO_2 cooling

Carbon foam + metal pipe
Radiation length <Xo=0.25>



Silicon micro-channels
Radiation length <Xo=0.12>

Chip footprint



Holes for fluidic inlet and outlet

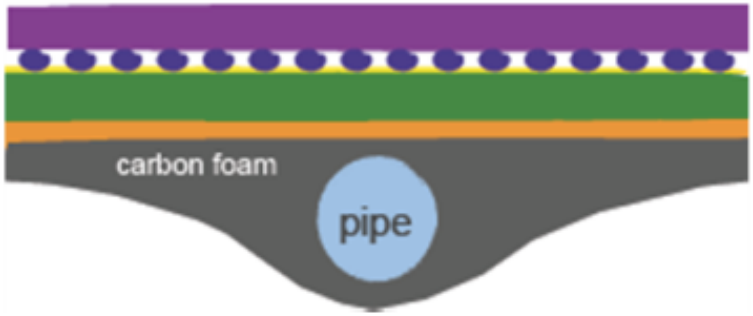
35 micro-channels

50 μm x 50 μm separated by 200 μm walls

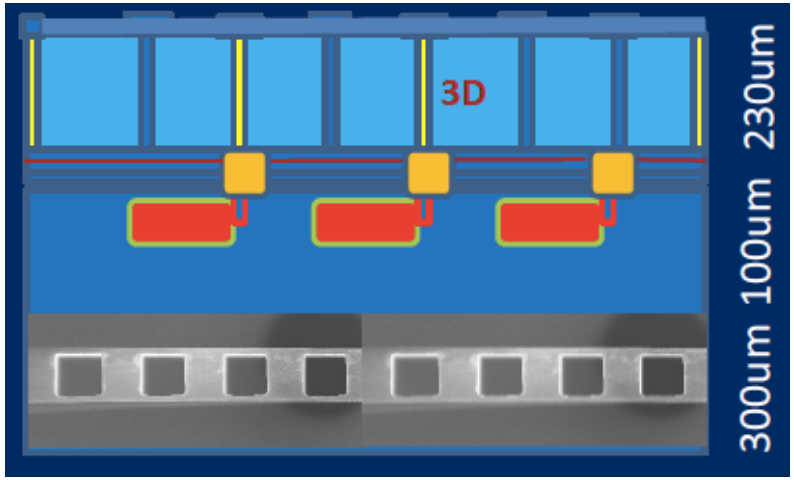
Micro-channel cooling

- 3D Pixels for Phase II: embedded micro-channels with CO_2 cooling

Carbon foam + metal pipe
Radiation length <Xo=0.25>



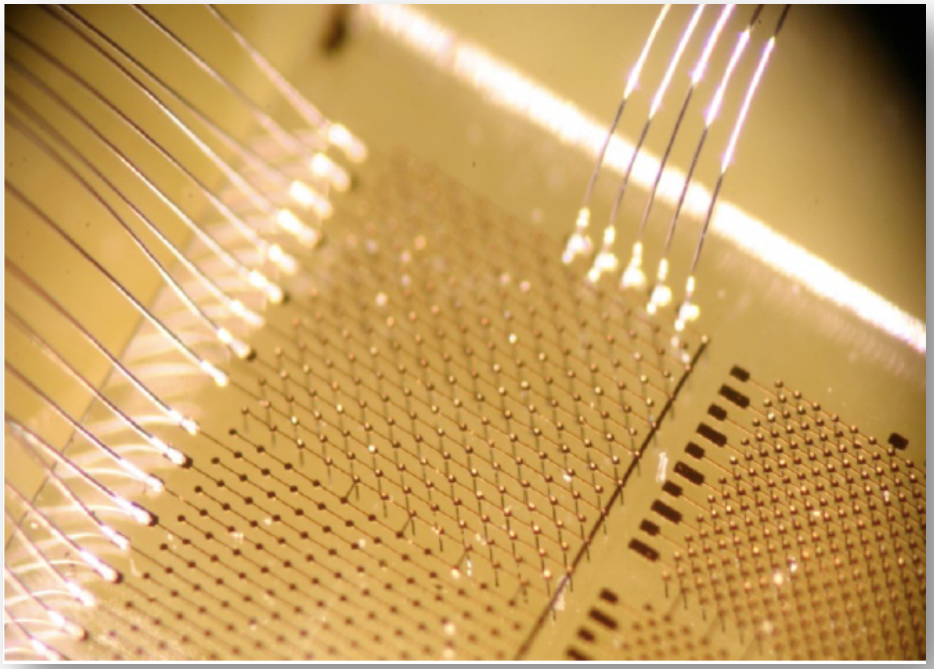
Silicon micro-channels
Radiation length <Xo=0.12>



- Target for new 65 nm chip: 400 mW/cm^2
- Power dissipation for 3D sensor at $2x10^{16}$ n_{eq}/cm^2 → 450-500 mW/cm^2

Total power: 850-900 mW/cm^2

3D diamond sensors

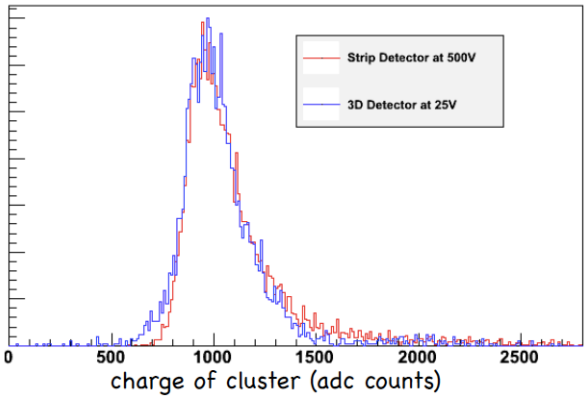


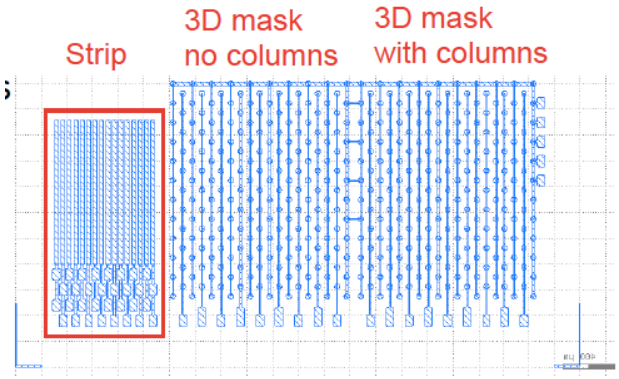
RD42 Collaboration

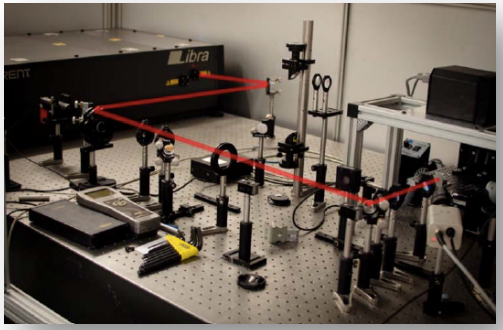
- Holes drilled with 800 nm femto-second laser
- 93% efficiency for column etching

- Diamond sensor 500 μm thick
- Cr-Au electrodes connecting a row of electrodes into a strip
- Read-put by the VA2 chip
- Columns are conductive ~1 Ω cm

S. Schnetzer, Vertex 2013







Summary and Outlooks

ATLAS pixel detector is essential for the experiment and will be upgraded in the future:

• A 4th pixel layer (IBL) is well under construction and will be installed in spring 2014 during LS1 of LHC.

• Upgrade to luminosities of $5x10^{34}cm^{-2}s^{-1}$ and ~250 pile up events pushes the challenges for pixel detectors in new directions.

Looking to the phase 2 plans of the ATLAS pixel detector is difficult now, but

❑ **For inner pixel layers:**

• hybrid pixels either with FE electronics in 65nm or 3D integrated electronics; sensors could be planar, 3D or diamond

❑ **For outer pixel layers:**

Standard hybrid pixel detectors most likely planars, with

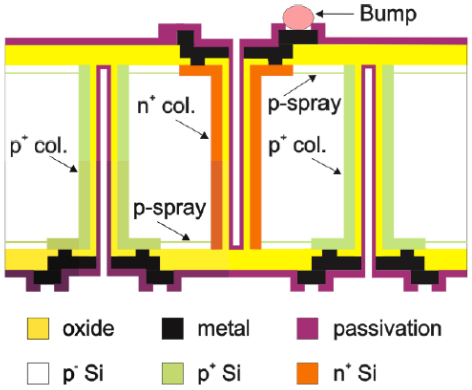
advanced concepts to save material (TSV, SLID, thin sensors, …)

A lot more R&D is needed!

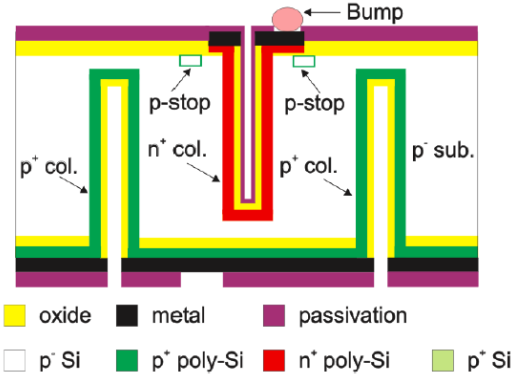
Additional material

3D pixel sensors for IBL

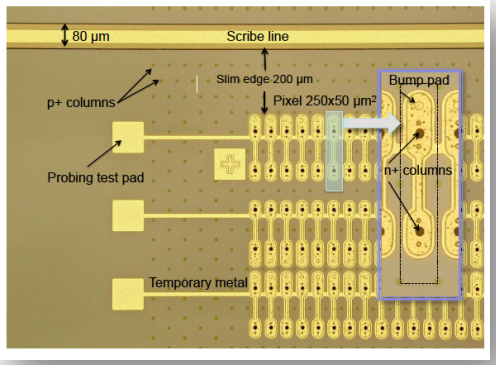
FBK

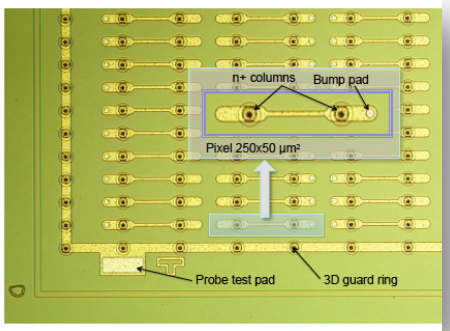


CNM



- 230μm thick 3D sensors
- Produced without handle wafer





FBK: temporary metal for testing

CNM: Guard Ring without connection to single pixels

Producer	Wafers Produced & Tested	Selected Wafers
CNM	50	41
FBK	70	33

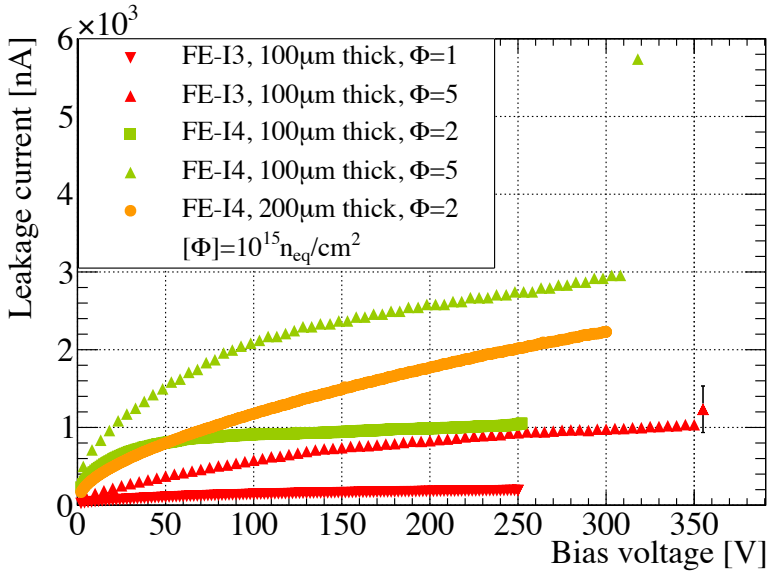
Wafers are selected for UBM if at least 3 tiles out of 8 are good (Vbk >25 V)

CNM yield significantly higher than FBK but FBK measurement on full device, CNM on Guard Ring only.

C. Gemme, Vertex 2013

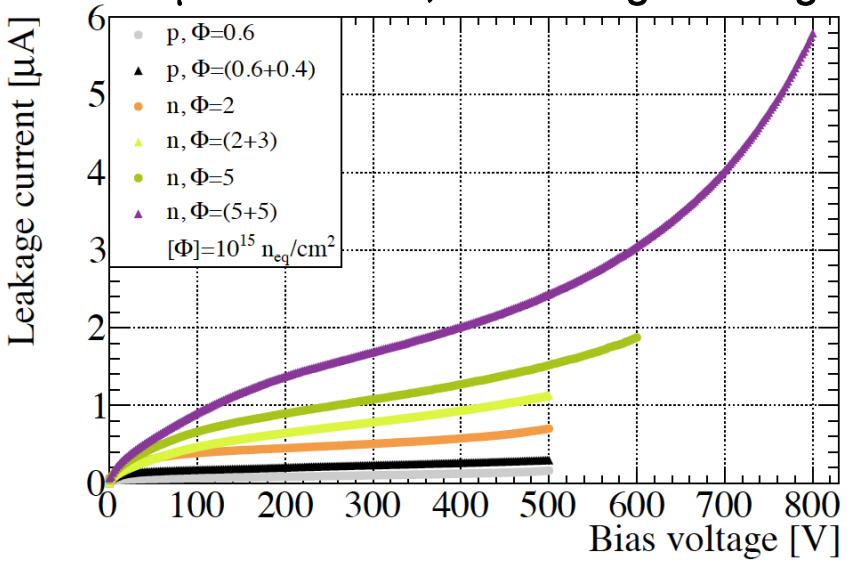
Active edge: IV after irradiation

100 and 200 μm thickness, active edge

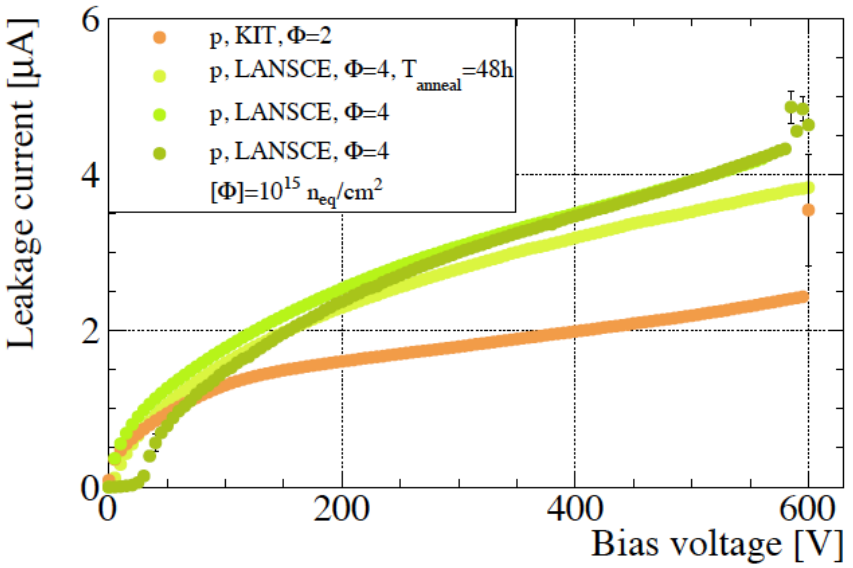


- Active edge modules irradiated up to a fluence of 5×10^{15} n_{eq}/ cm^2 have a breakdown voltage above the saturation voltage of the charge collection
- Lower breakdown voltages with respect to thin pixel devices with standard GR structure irradiated at the same fluence

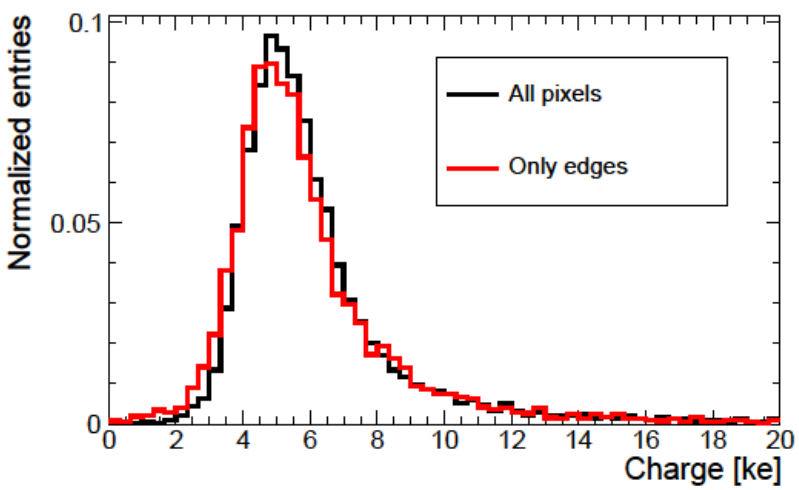
75 μm thickness, standard guard ring

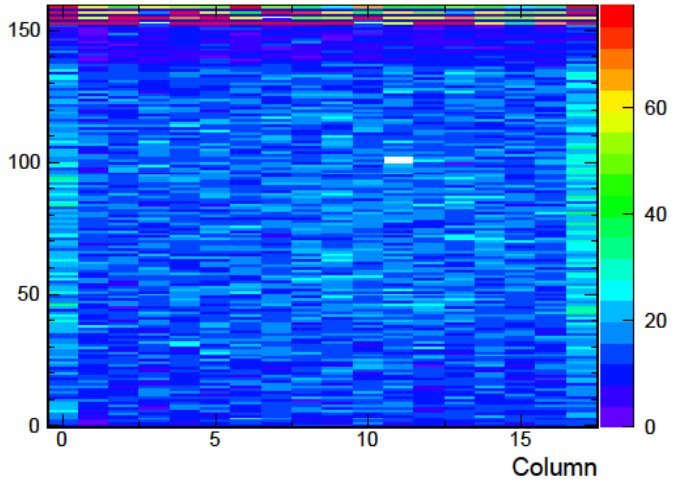


150 μm thickness, GR with 450 μm inactive edge

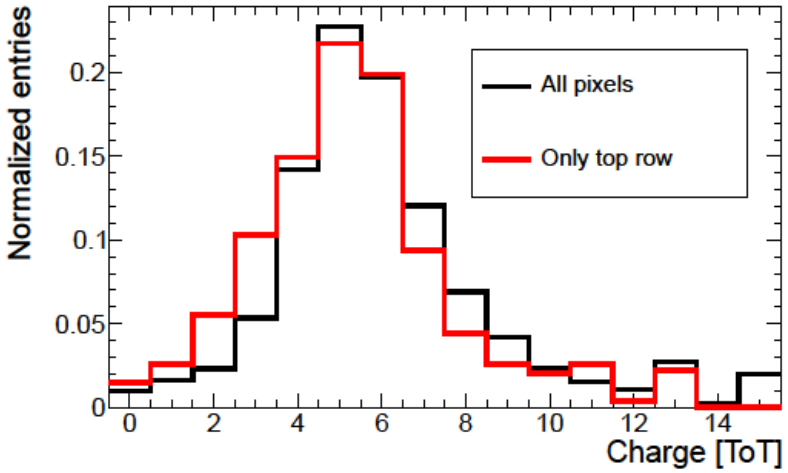


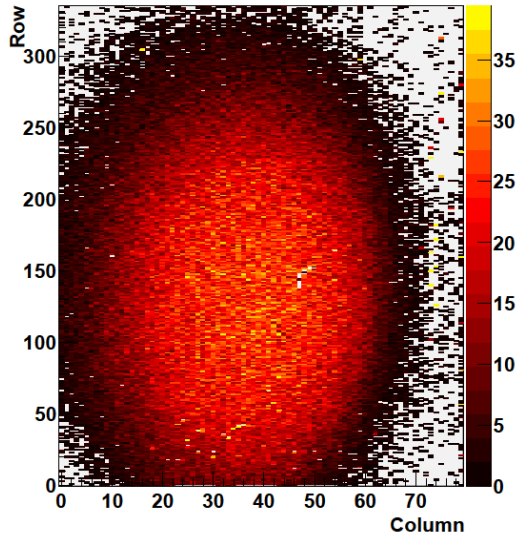
Active edge: charge collection with a ^{90}Sr a source





FE-I3
50 μm edge
V_{bias}=15 V

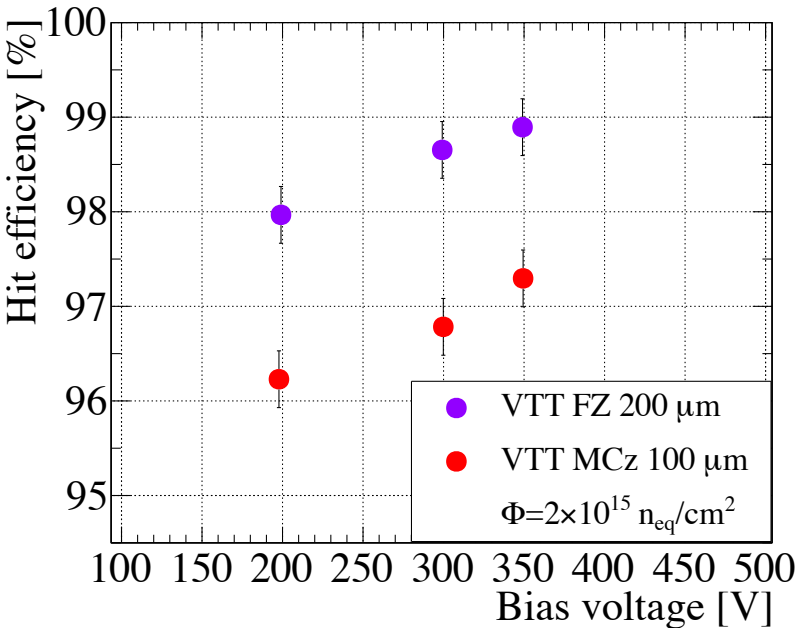




FE-I4
125 μm edge
V_{bias}=15 V

- Edge pixels show the same charge collection properties as the central ones

DESY test-beam – Active edge sensors



- VTT 100 μm MCz

threshold: 1600 e, $\Phi=2\times10^{15} n_{eq}/cm^2$

97.3% global efficiency at 350 V

- VTT 200 μm Float Zone (FZ)

threshold: 1100 e, $\Phi=2\times10^{15} n_{eq}/cm^2$

98.9% global efficiency at 350 V

- VTT 100 μm FE-I3 Float Zone

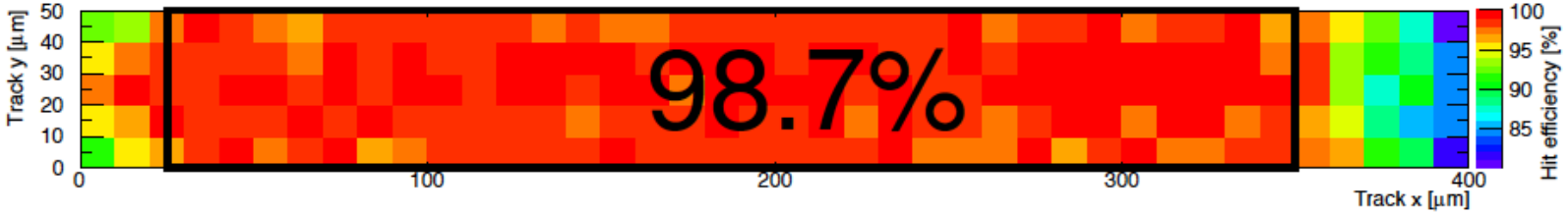
125 μm slim edge, threshold: 1500 e

$\Phi=5\times10^{15} n_{eq}/cm^2$

V_{bias}=400V

global hit efficiency

97.5 ±0.3%

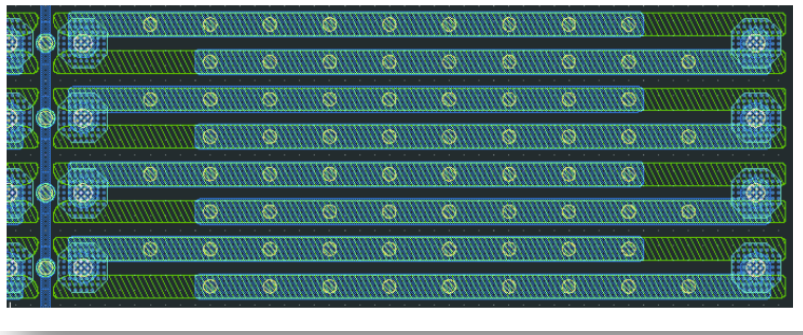


Smaller pitches for internal layers

25 μm x 500 μm pitch

MICRON – Liverpool University

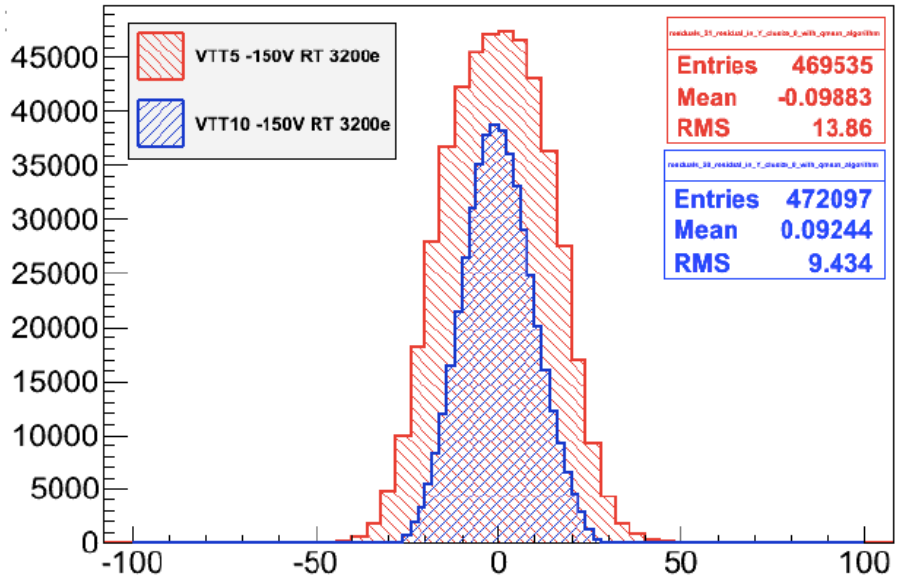
- Test for Rϕ pitch of 25 μm, as foreseen for inner layers of phase II upgrade in ATLAS
- Longer pixels in the z direction (500 μm) to restore compatibility with the FE-I4 chips
- Values of the residual are approximately what is expected for pitch / √12



500x25 : 25/√12 = 7.217μm
250x50 : 50/√12 = 14.43μm

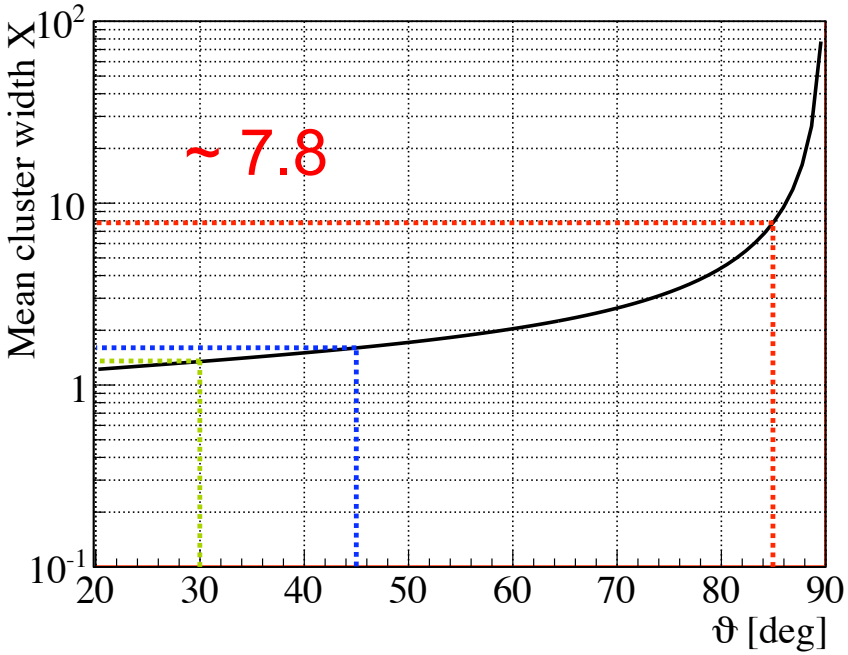
H. Hayward, Liverpool

Hiroshima Symposium 2013

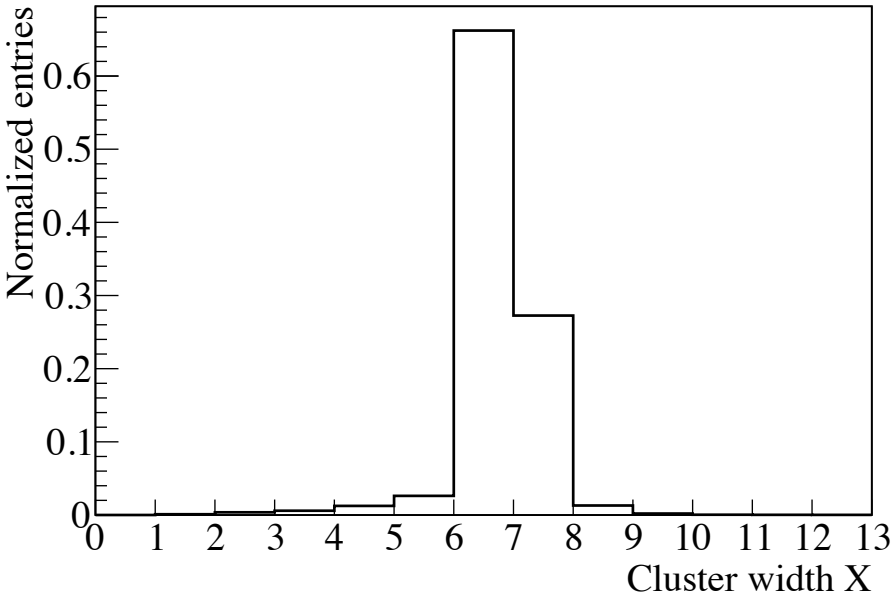


High eta cluster analysis

- FE-I4 150 μm thick, irradiated to 4×10^{15} n_{eq}/cm^2 in Los Alamos
- 85^{O} track incidence (η=3.1)
- bias voltage: 500 V
- threshold: 1.6 ke (MPV 9.5 ke)

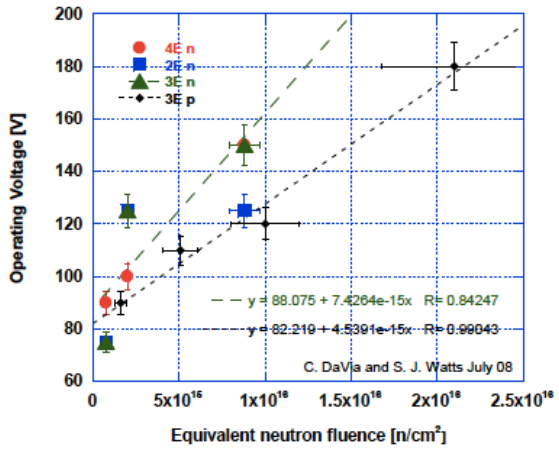


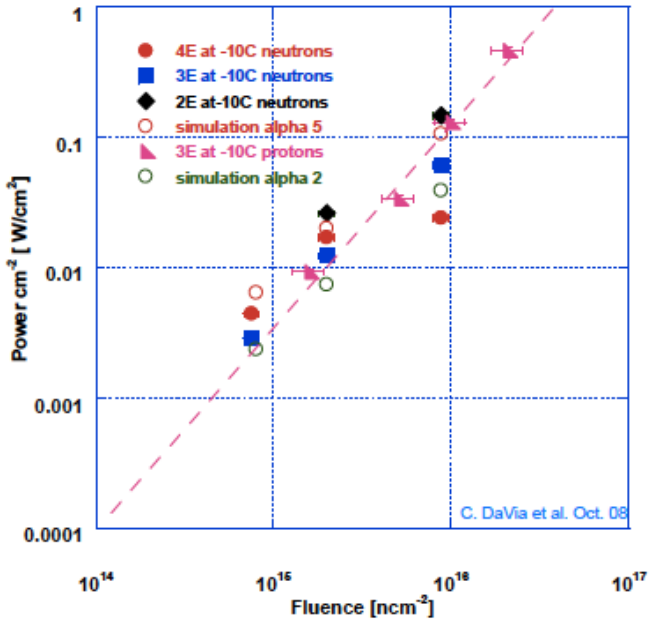
- Mean cluster width expected along the tilted direction for different incidence angles

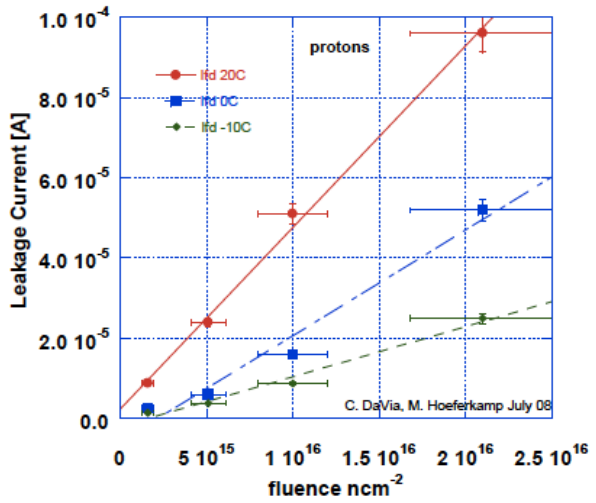


- Cluster distribution along the tilted direction.
- Distribution mean = 6.7

Power dissipation -3D



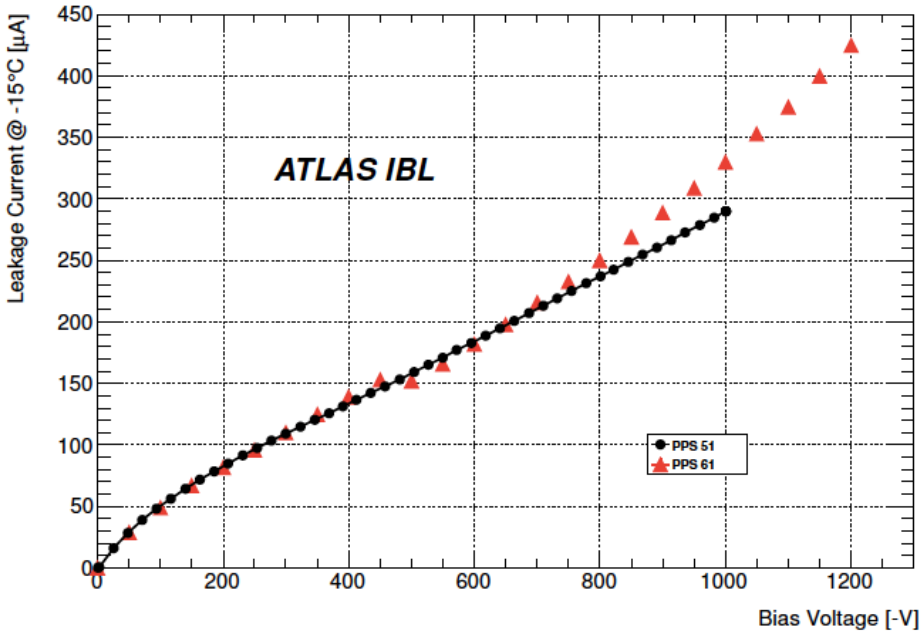




- At $2x10^{16}$ and T=-10C → power disspation =400 mW/cm2

Power dissipation - Planar

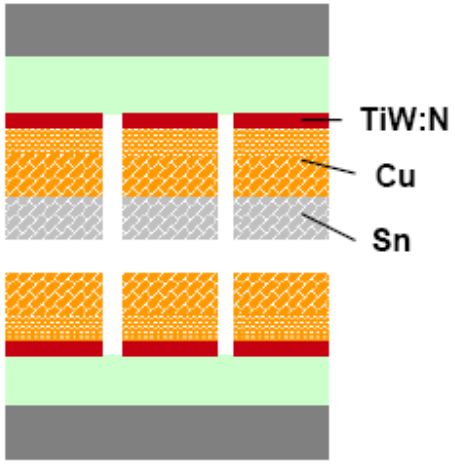
- At 2x1016 current=1 mA
- Vbias=1500 V
- T=-15C on the sensor
- Power dissipation 1.5 W



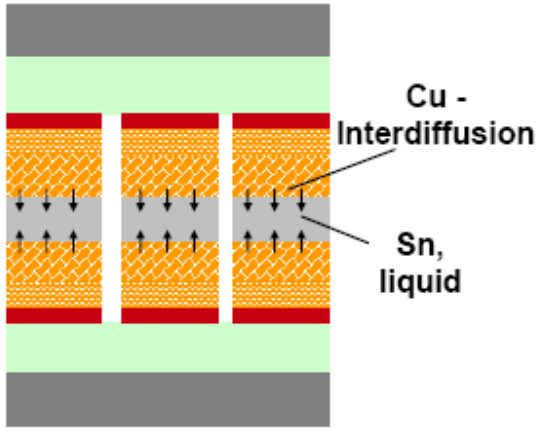
EMFT SLID Process

Metallization SLID (Solid Liquid Interdiffusion)

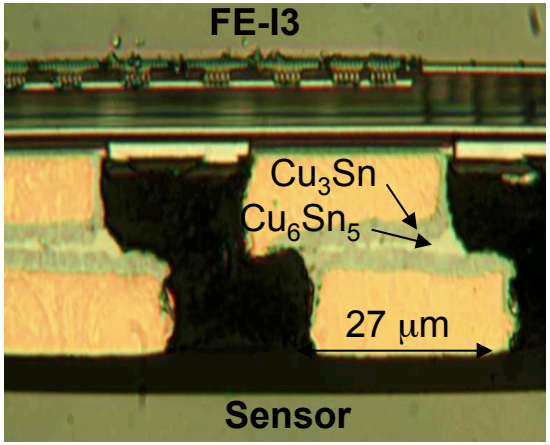
Fraunhofer EMFT



Through Mask Electroplating



Contact under Pressure and Heat
~ 5 bar, 260 – 300 °C (Sn-melt)



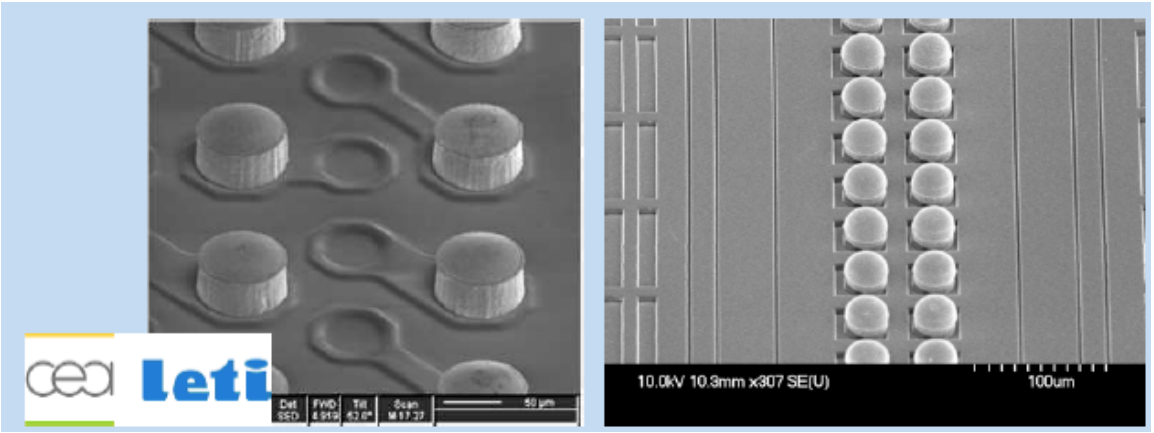
Formation of Eutectic Alloy;
T_{melt} > 600 °C

- Alternative to bump bonding (less process steps "lower cost" (EMFT)).
- Small pitch possible (~ 20 μm, depending on pick & place precision).
- Stacking possible (next bonding process does not affect previous bond).
- Wafer to wafer and chip to wafer possible.

Chip-sensor interconnection technologies

- Solder bump-bonding with different companies:
  - IZM Berlin, HPK : SnAg bumps
  - VTT (ADVACAM), SnPb bumps
  - IZM, HPK: chip thickness down to 150 μm with the use of a glass substrate
  - VTT: chip thickness down to 200 μm

Alternative interconnection technologies – Micro-Cu Pillars



- Cu post / SnAg solder
- 50 μm pitch
- 25 μm diameter
- 8-12 μm thickness

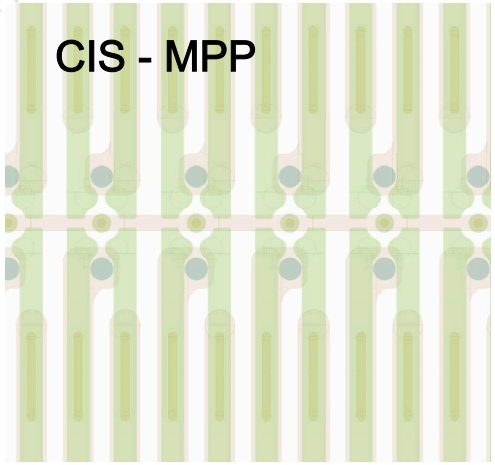
FE-I4B with micro-pillars

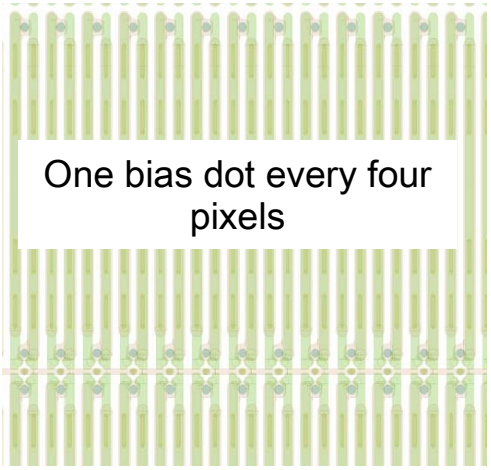
Glasgow-LETI-ADVACAM collaboration

C. Butter, Hiroshima Symposium 2013

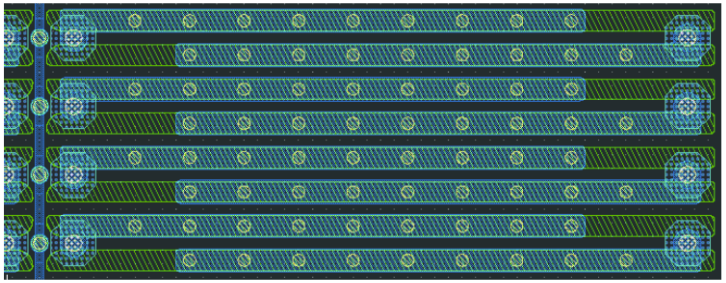
Smaller pitches for internal layers

CIS - MPP



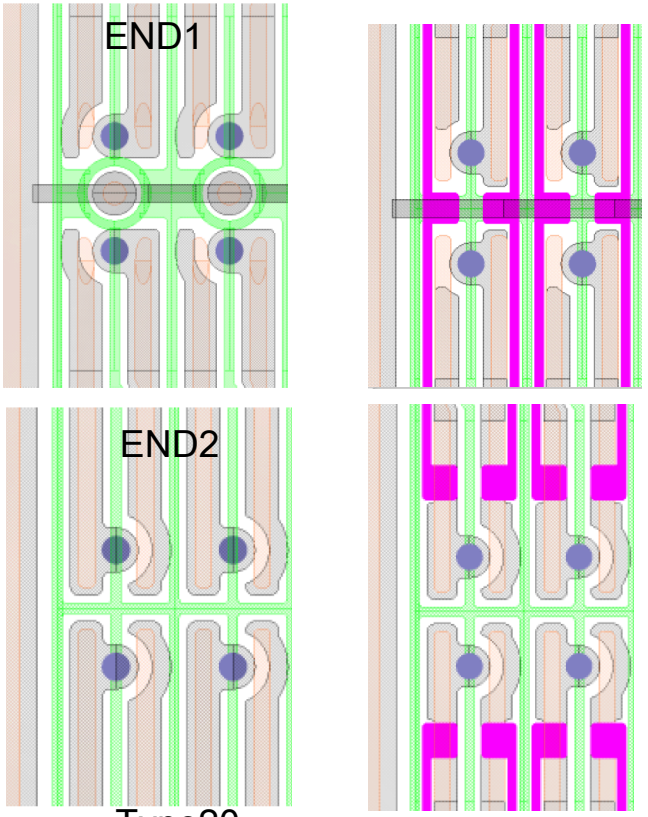


MICRON - Liverpool



KEK – HPK

Confidential for ATLAS (and CMS)



Type20
PT No offset

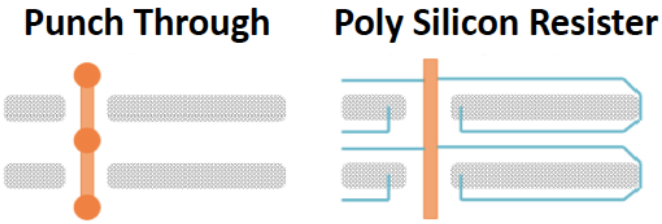
Type 21

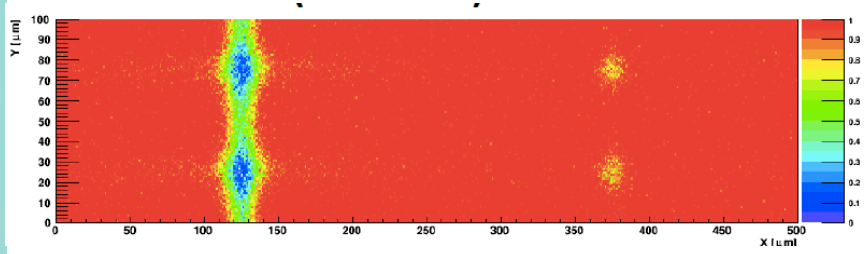
25 μm x 500 μm pitch

- Test for Rϕ pitch of 25 μm, as foreseen for inner layers of phase II upgrade in ATLAS
- Longer pixels in the z direction (500 μm) to restore compatibility with the FE-I4 chips

n-in-p performance – FE-I4 modules

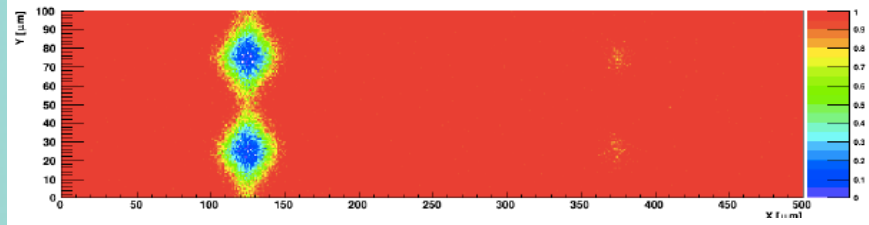
- KEK-HPK n-in-p FE-I4 sensors, 150 μm thickness
- Bump-bonded at HPK
- Irradiated at Φ=1e16 n_{eq}/cm^2, Vbias=1200 V





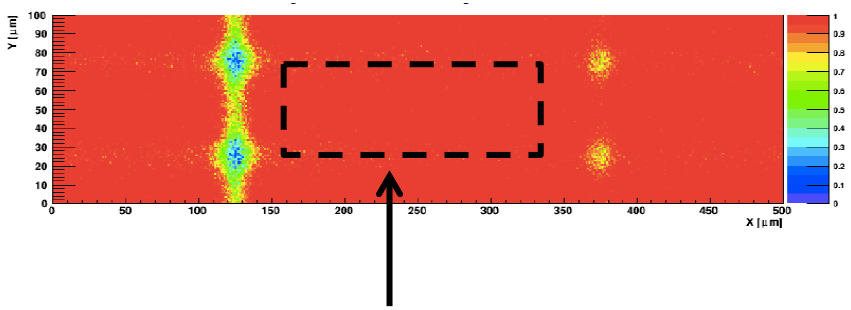
Poly-Si, p-stop

Overall hit efficiency = 96.3%



PT, p-spray

Overall hit efficiency = 97.1%



Poly-Si, p-spray

Overall hit efficiency = 97.6%

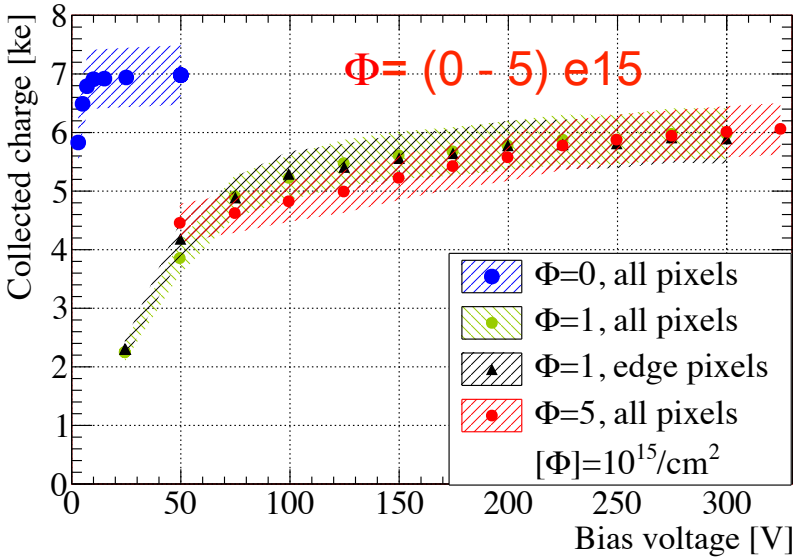
> 99.7 % already at 600V in the electrode region of each sample

Kazuki MOTOHASHI

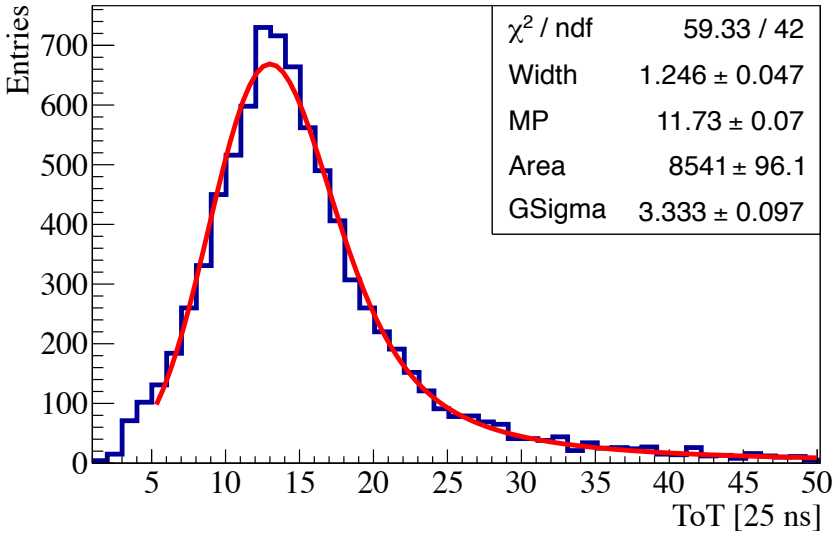
Hiroshima Symposium 2013

Charge collection efficiency after irradiation

- FE-I3 100 μm thick sensor with 125 μm slim edge, threshold 1500 e- → irradiated in Ljubljana at $5x10^{15}$ n_{eq}/cm^2

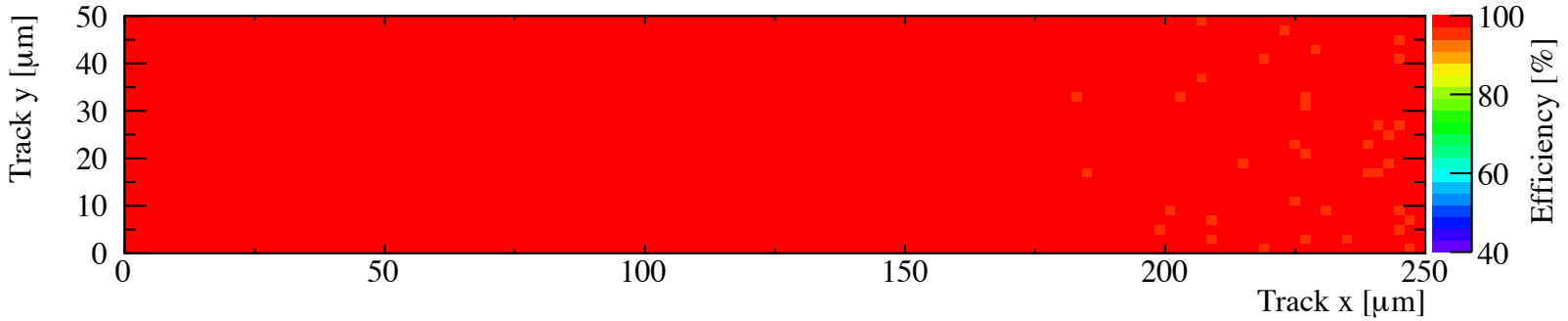


- Landau distribution obtained at the DESY test-beam with 4 GeV electrons

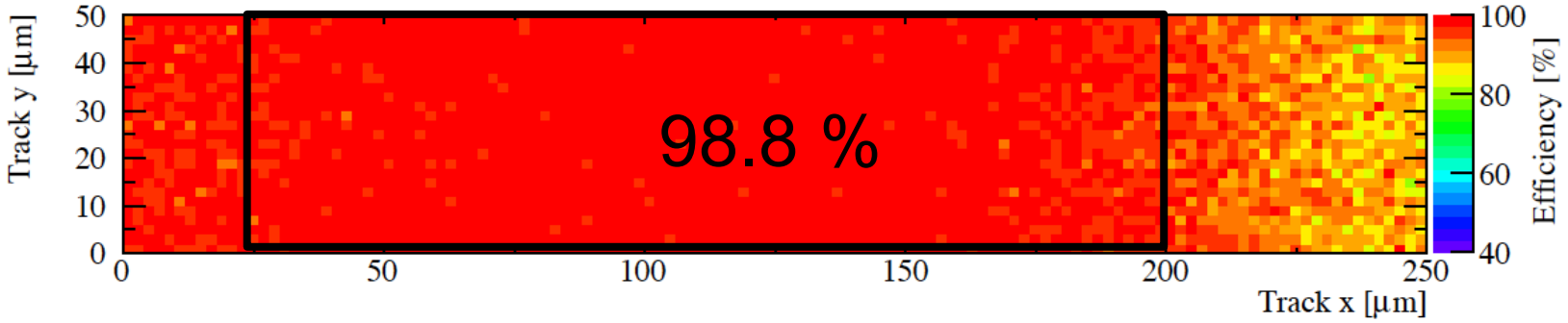


Test-beam results – 100 μm thick sensors

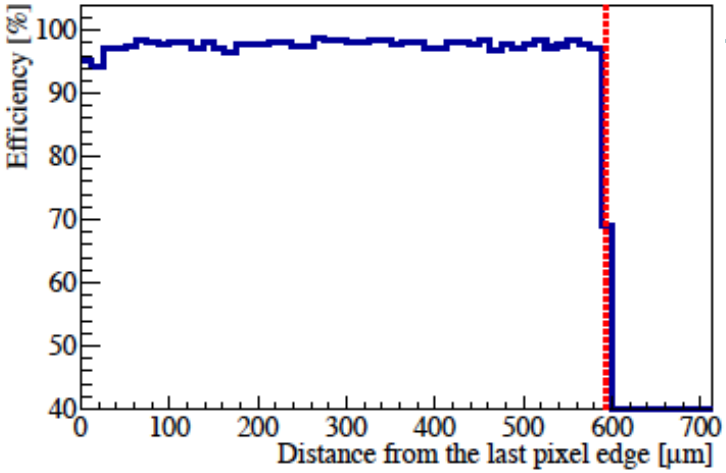
- Test-beam results from DESY test-beam 6 GeV electrons, EUDET telescope
  → due to multiple scattering the analysis of the edge efficiency is not possible
- Tuning Threshold=1600 e, 6 ToT@6ke, beam at perpendicular incidence
- VTT FZ, 100 μm thick, not irradiated → total efficiency 99.7% at 40 V

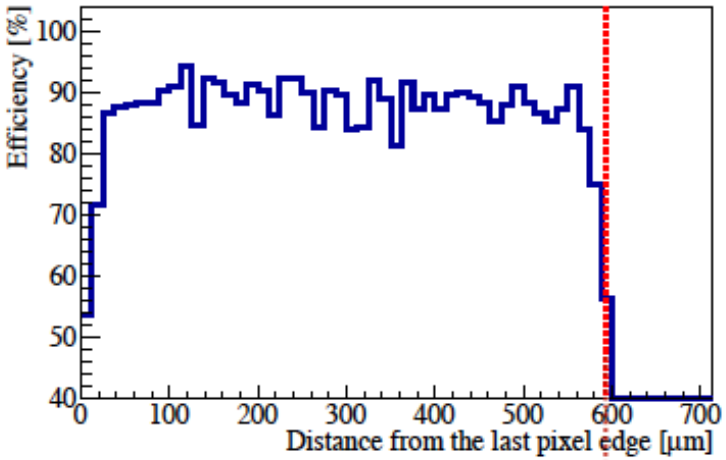


- VTT MCZ, 100 μm thick, Φ=2e15 → total efficiency 97.3% at 350 V



Edge efficiency after irradiation



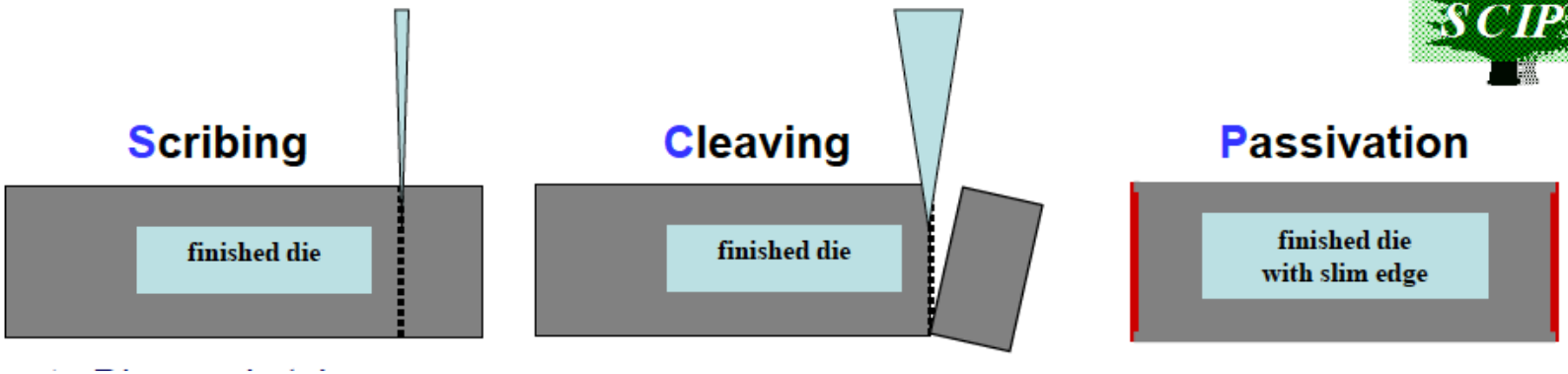


125 μm slim edge FE-I3 module with Bias Ring

- not irradiated
- threshold: 1500 e
- PPS test-beam with 120 GeV pions
- 68 ±1% hit efficiency between the last pixel implant and the Bias Ring

- $\Phi = 5 \times 10^{15}$ $\mathbf{n_{eq}/cm^2}$
- 400 V
- threshold: 1500 e
- DESY test-beam with 4 GeV e^-
- 56±4% hit efficiency between the last pixel implant and the Bias Ring

SCP: Scribe Cleave Passivate



- Diamond stylus
- Laser
- XeF_2 Etch
- DRIE Etch
- Saw cut (with cleanup step)

- Tweezers (manual)
- Loomis Industries, LSD-100
- Dynatex, GTS-150

N-type P-type
($Q_f > 0$) ($Q_f < 0$)

- Native SiO_2 + UV light or high T — ALD of Al_2O_3
- PECVD SiO_2
- PECVD Si_3N_4
- ALD "nanostack" of SiO_2 and Al_2O_3

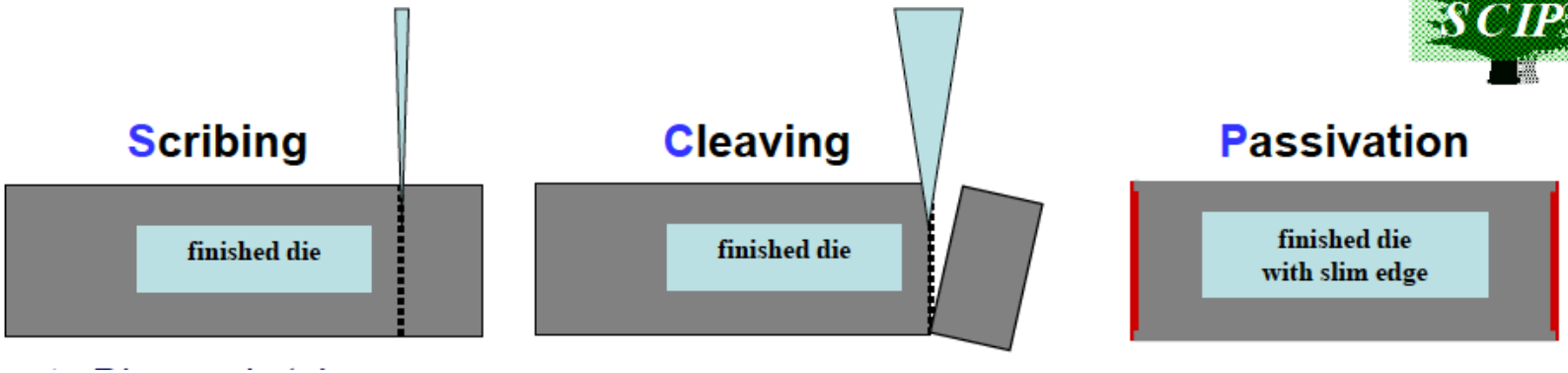
- All Treatment is post-processing & low-temp (Etch-scribing can be done during fabrication)
- Basic requirement: <100> wafers (for rectangular side cleaving) with reasonably good alignment between sensor and lattice.

V. Fadeyev

Santa Cruz Institute for Particle Physics

Hiroshima Symposium 201

SCP: Scribe Cleave Passivate



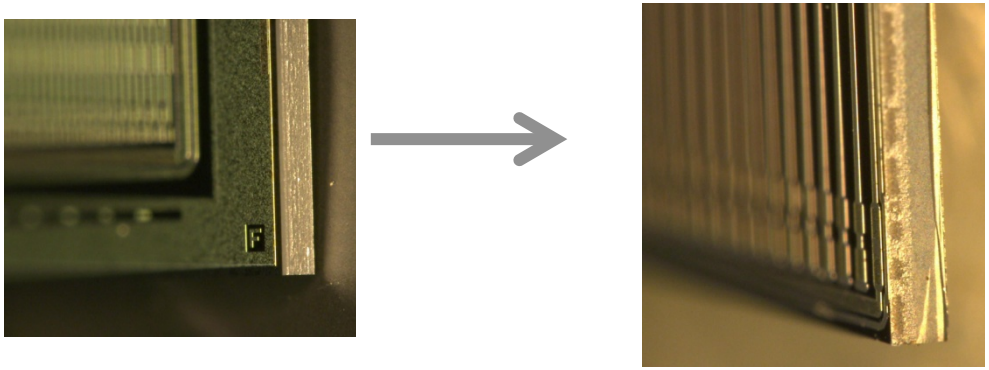
- Diamond stylus
- Laser
- XeF_2 Etch
- DRIE Etch
- Saw cut (with cleanup step)

- Tweezers (manual)
- Loomis Industries, LSD-100
- Dynatex, GTS-150

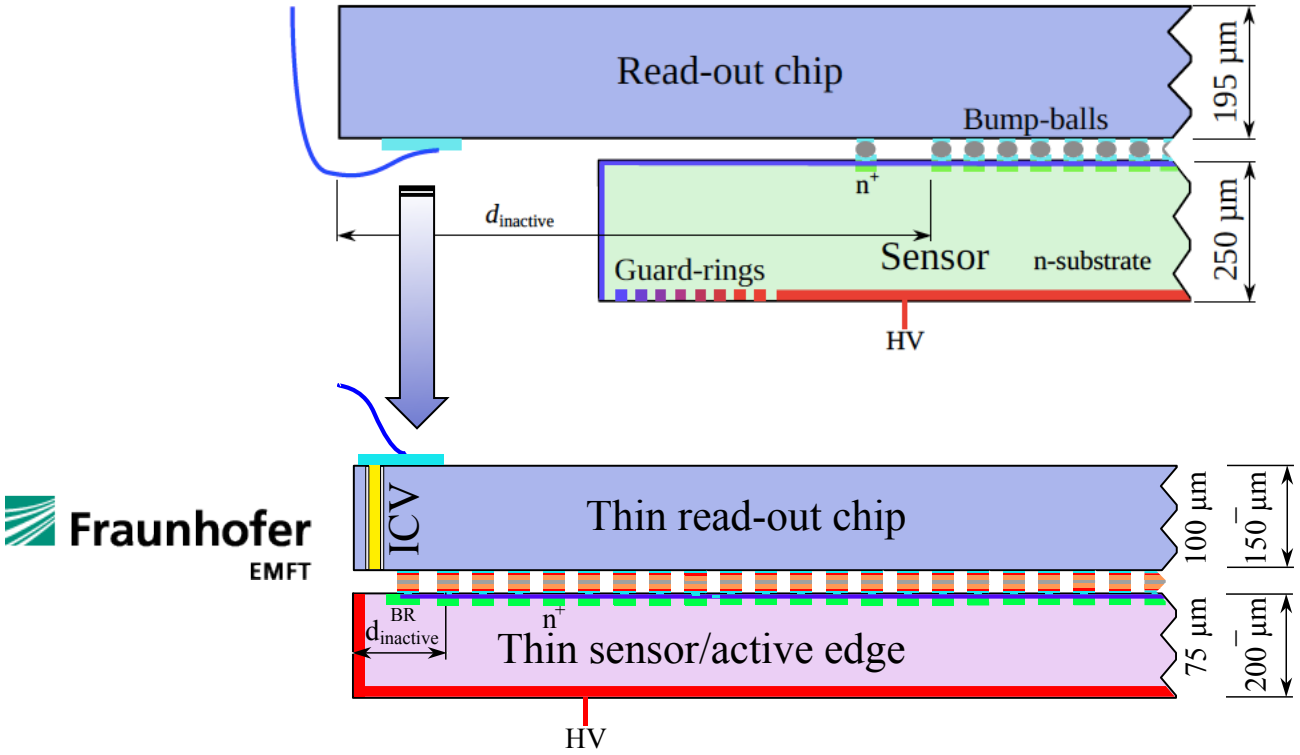
N-type P-type
(Qf > 0) (Qf < 0)

- Native SiO_2 + UV light or high T
- PECVD SiO_2
- PECVD Si_3N_4
- ALD "nanostack" of SiO_2 and Al_2O_3

ALD of Al_2O_3



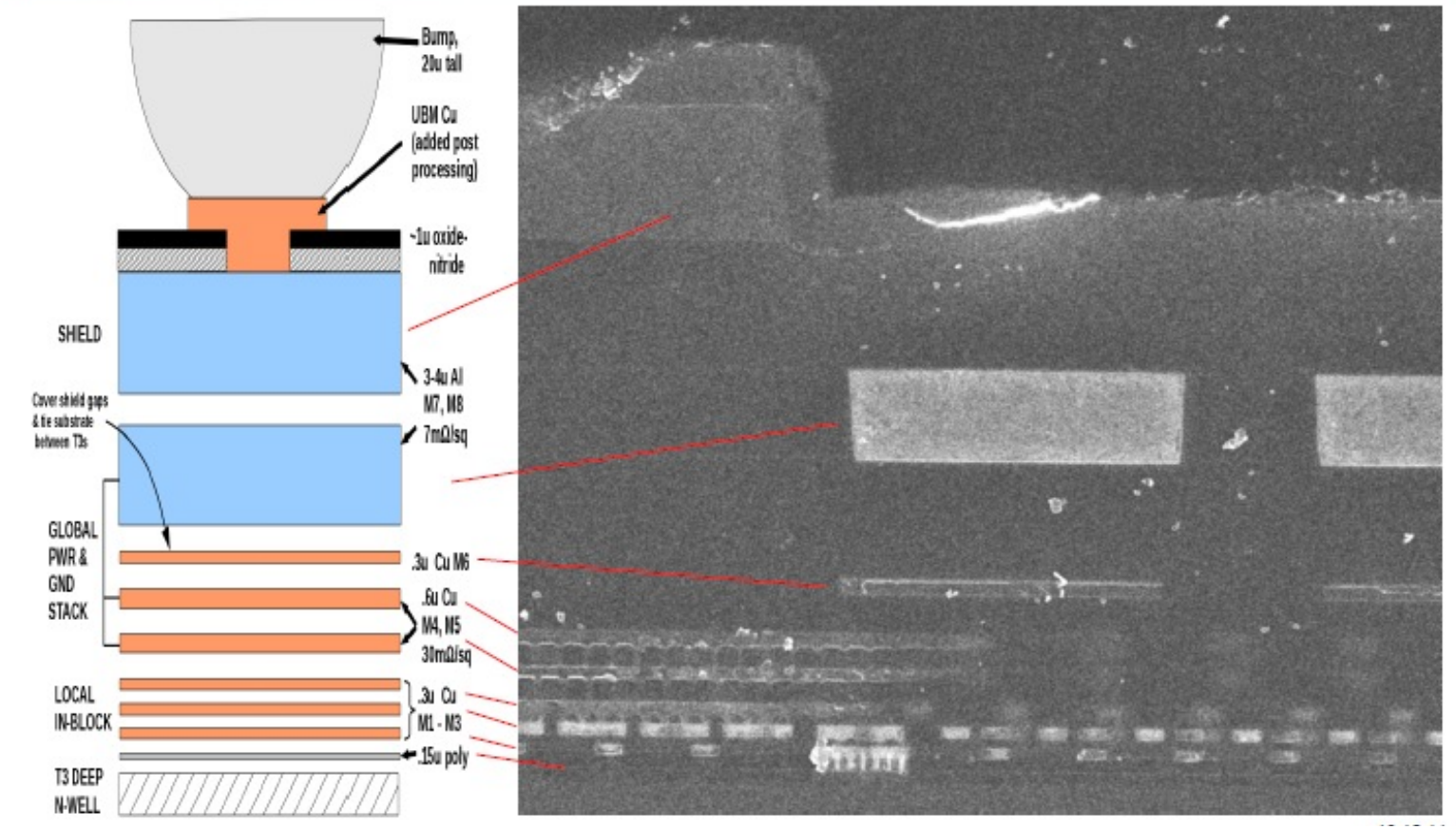
Reduction of the inactive region on the chip side



- Project within AIDA WP3, in collaboration with Fraunhofer EMFT, to develop Inter Chip Vias to show the feasibility to transport signals and services on the backside using the existing FE-I4 chip
- Inter-Chip-Vias to be etched on each wire bonding pad, cross section ~ 10x30 μm^2
- Chip and sensor connected using SLID technology

Inter Chip Vias in the FE-I4 chip

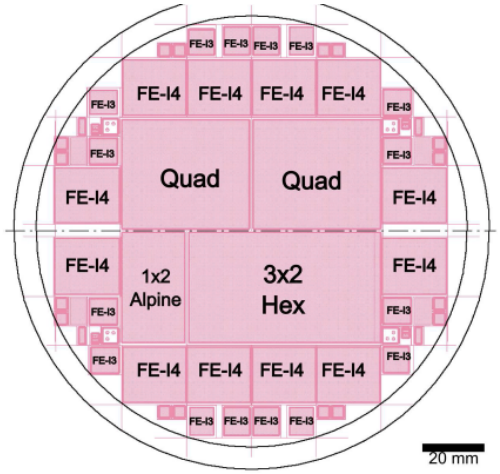
SEM analysis of the FE-I4 wire bonding pad



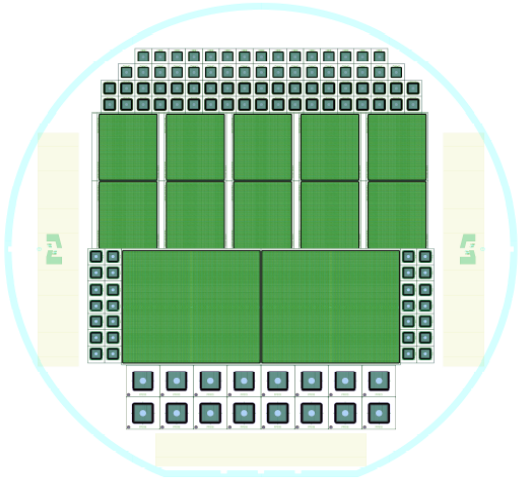
- Most of the eight FE-I4 metal layers are present in the wire bonding pads → not possible to etch ICV from the front-side
- Design and test of the ICV layout on test-wafers in on-going: target cross-section 10x30 μm^2 with a global chip thickness of 100-150 μm

Multi-chip modules

CIS n-in-n

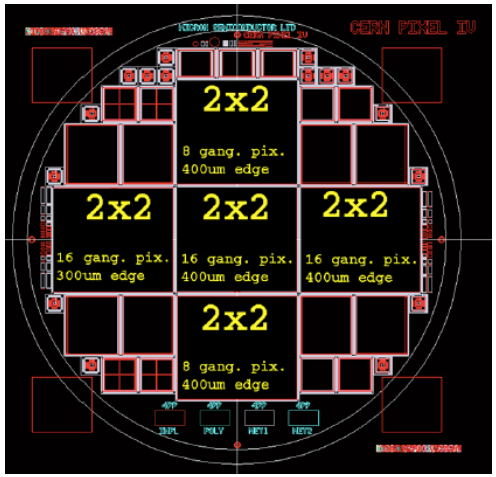


CIS n-in-p

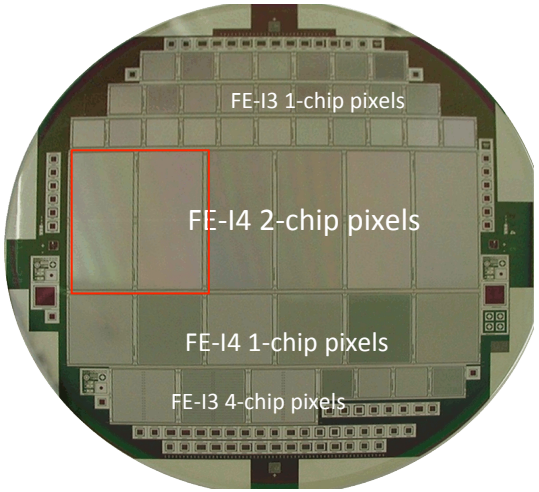


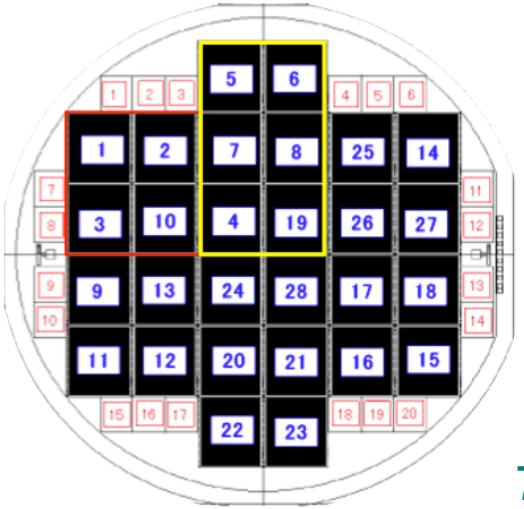
- 6” wafers from different producers – CIS is also starting the transition from 4” to 6” line
- Quad and HEX modules

MICRON n-in-p



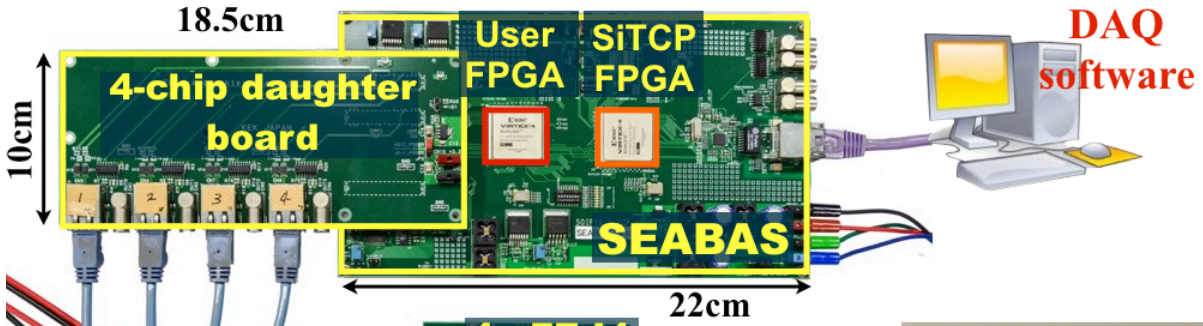
HPK n-in-p

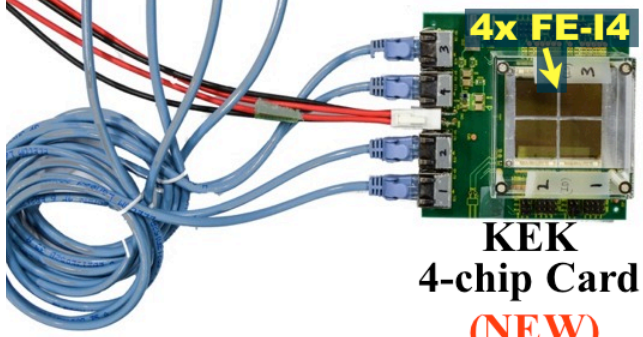




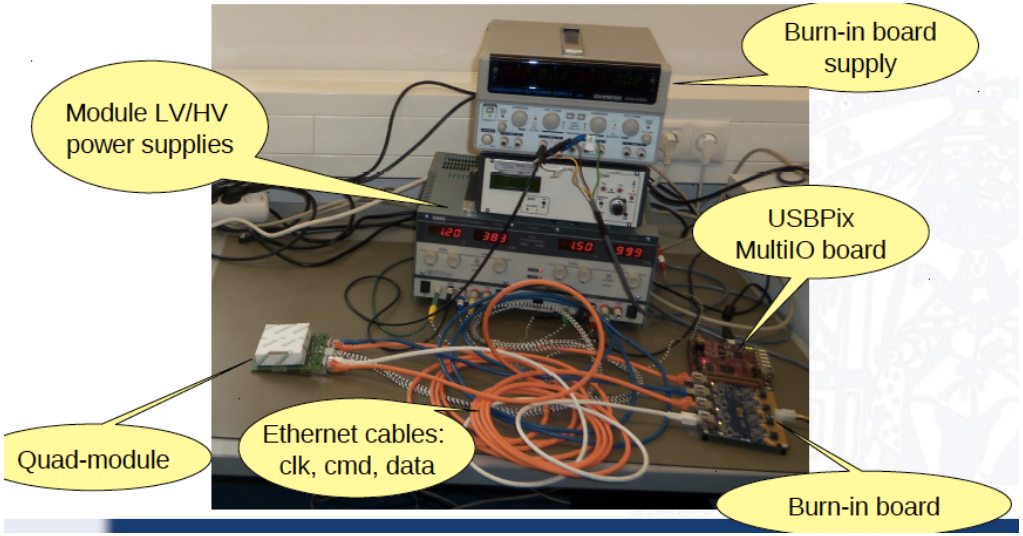
Multi-chip modules read-out systems

SEABAS (KEK))

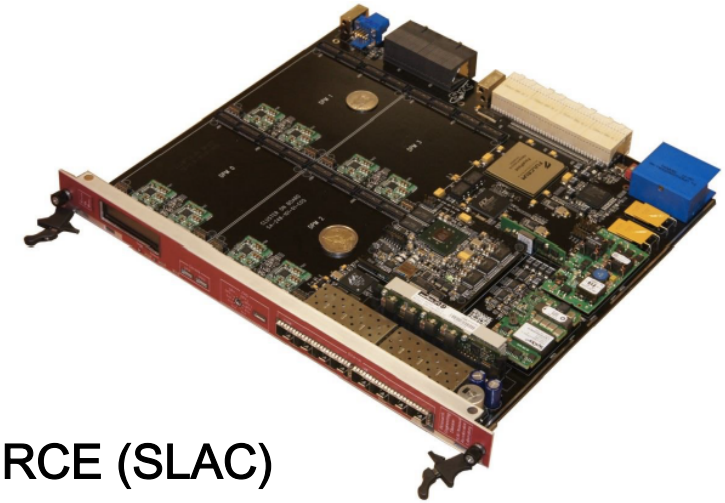




KEK 4-chip Card (NEW)



USBPix (Bonn) + STControl (Gö)

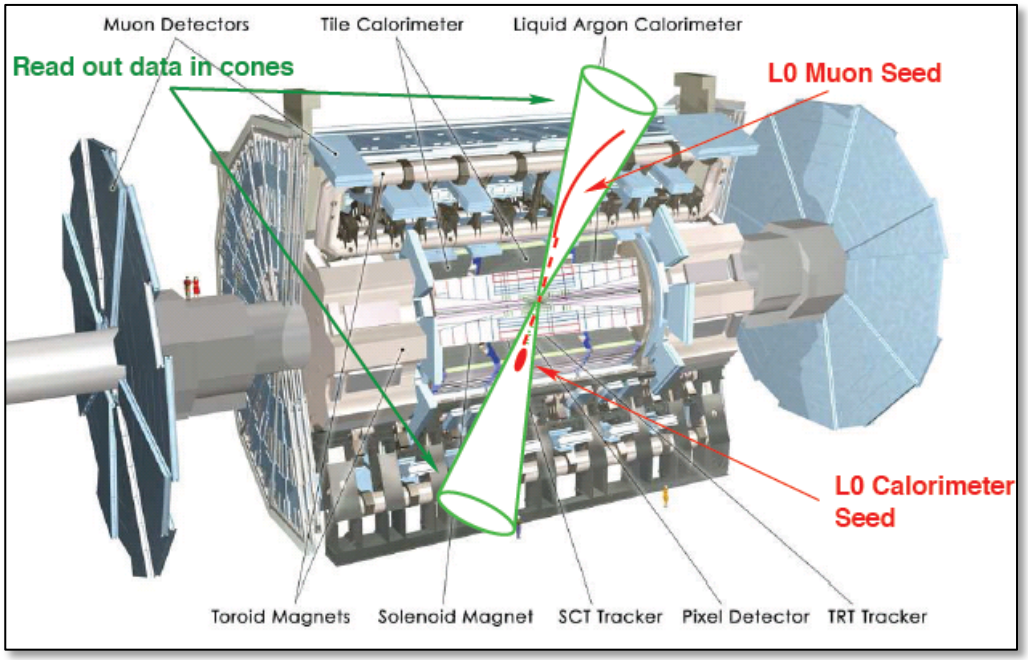


RCE (SLAC)

3 different DAQ systems available in ATLAS for simultaneous steering and reading of 4-chip modules

L1Track Trigger

- Adding tracking information at Level-1 (L1)
  - Move part of High Level Trigger (HLT) reconstruction into L1
  - Goal: keep thresholds on p_T of triggering leptons and L1 trigger rates low
- Triggering sequence
  - L0 trigger (Calo/Muon) reduces rate within ~6 μs to ≳ 500 kHz and defines RoIs
  - L1 track trigger extracts tracking info inside RoIs from detector FEs



- Challenge
  - Finish processing within the latency constraints