Test stand at PRISMA

FTK IAPP

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06/11/2013

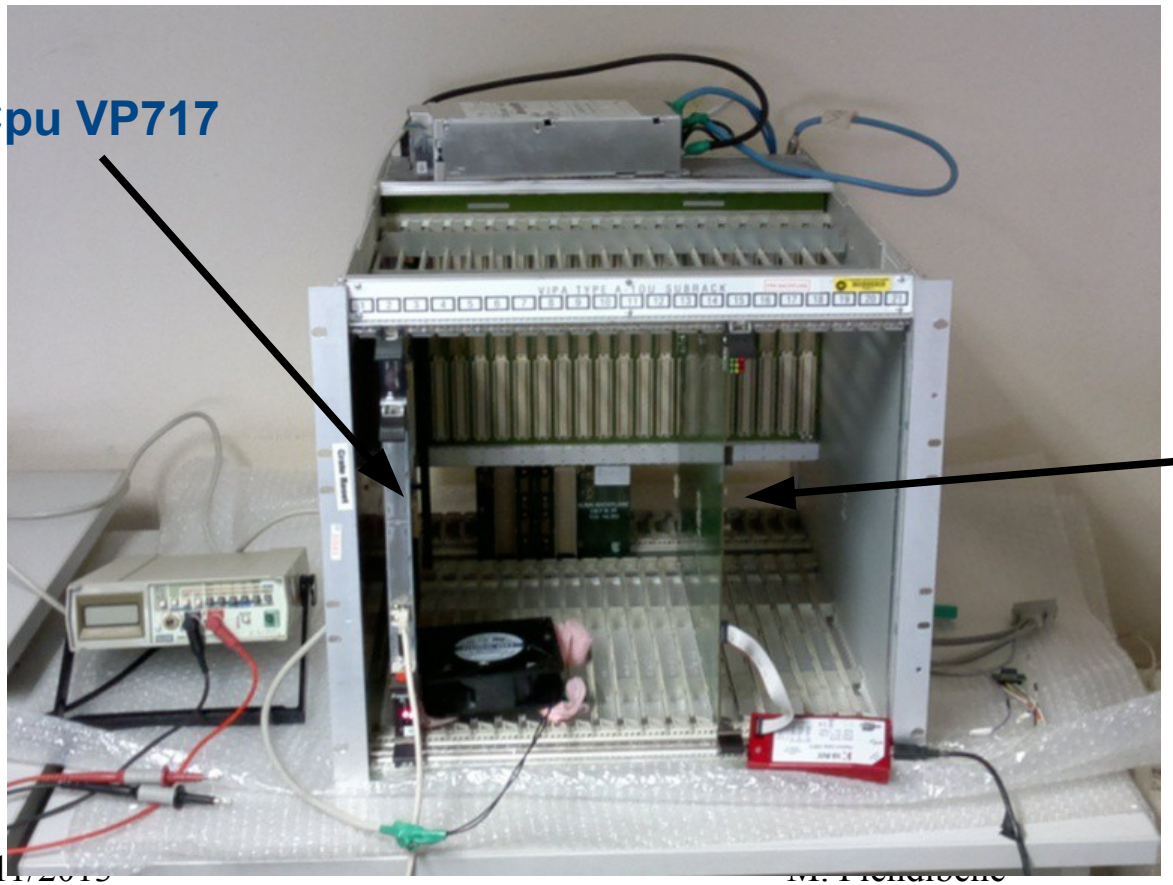
TEST STAND AT PRISMA

During the first secondment in Greece (summer 2013) a test stand in Prisma electronics, Alexandroupolis, has been installed.

At the beginning it was installed in the Prisma factory, and then, it has been moved to the headquarter in Alexandroupolis, which is reachable also without a car, so the location is better for the future secondments.

This test stand will be used to do tests of the FTK boards that will be assembled in PRISMA.

The VME crate is a 9 units crate, but with the following supplies:
5V (as a standard VME crate)
48V (on the V1, V2 pins, standard VME)
12V (instead of 3,3V, NOT STANDARD, be careful!)



The test stand in the headquarters, Alexandroupolis

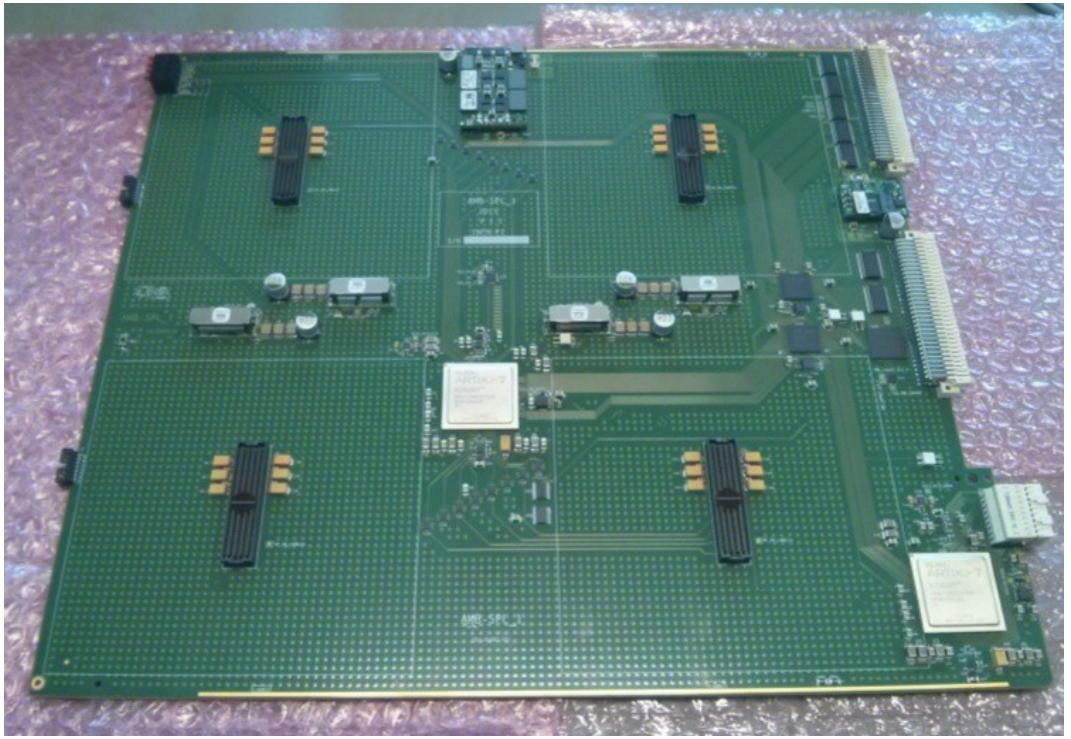
The SBC is a VP717 (Concurrent Technologies), the same that will be used at CERN for the FTK commissioning.

In this case the SBC is equipped with an hard disk on board to avoid the downloading of the operative system (Scientific Linux 5) and other software packages from the web at each boot (the rebooting will happen very frequent during tests and debug).

Now the SBC is configured on the Prisma network and we can access it also remotely (inside the Prisma LAN). In the future we will setup the system to have the access also from outside Prisma LAN.

TESTS AT PRISMA

The first prototype of the AMBSLP (the Associative Memory Board designed for FTK) arrived directly in Prisma, already assembled by an Italian company. This board is the one that use all serialized signals (GTP architecture)

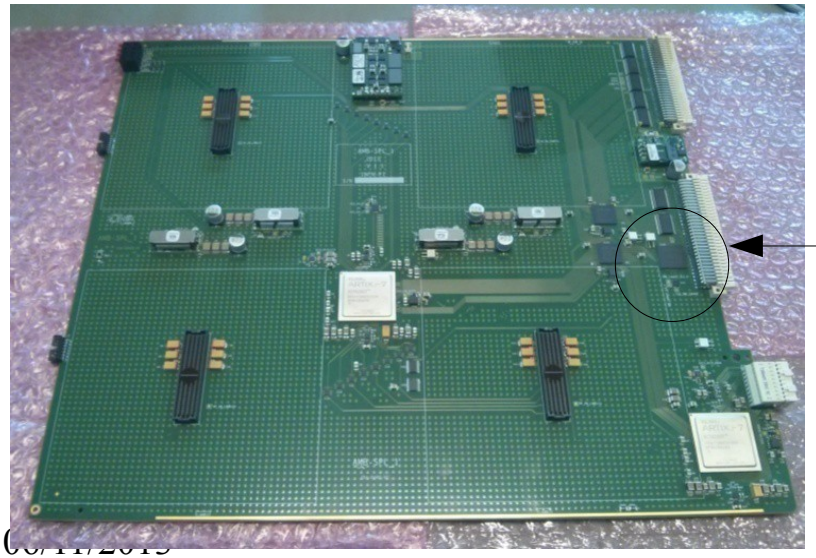


We did the preliminary tests discovering some little problems to adjust:
- wrong value of some resistors on the dc-dc converters that produce 1V (on the seq input)
- the enable pin of the LDO chips that produce 1.8V is floating and must be connected to VCC
- same problem for the dc-dc converts that generate the 2.5V: the enable pin is floating and must be connected to ground.
- on the clock generators and distributors (fan out chips) there is a resistor instead of an inductor on the power supply filter.

We did the hardware patches to correct this problems. At this point all the voltages and the clocks on the board were ok.

Trying to access via JTAG all the FPGAs on the, we discovered that one of them (VME fanout CPLD) has problems. We cannot see it on the JTAG chain. We tried all the possible patches to understand the problem without success. This chip is the one that distributes the VME signals to the other chips on the board and to the Aux board. So in this moment we have a limited VME control of the board. We are trying to understand.

All the other FPGA are ok, and we are able to program them.



The CPLD with problems

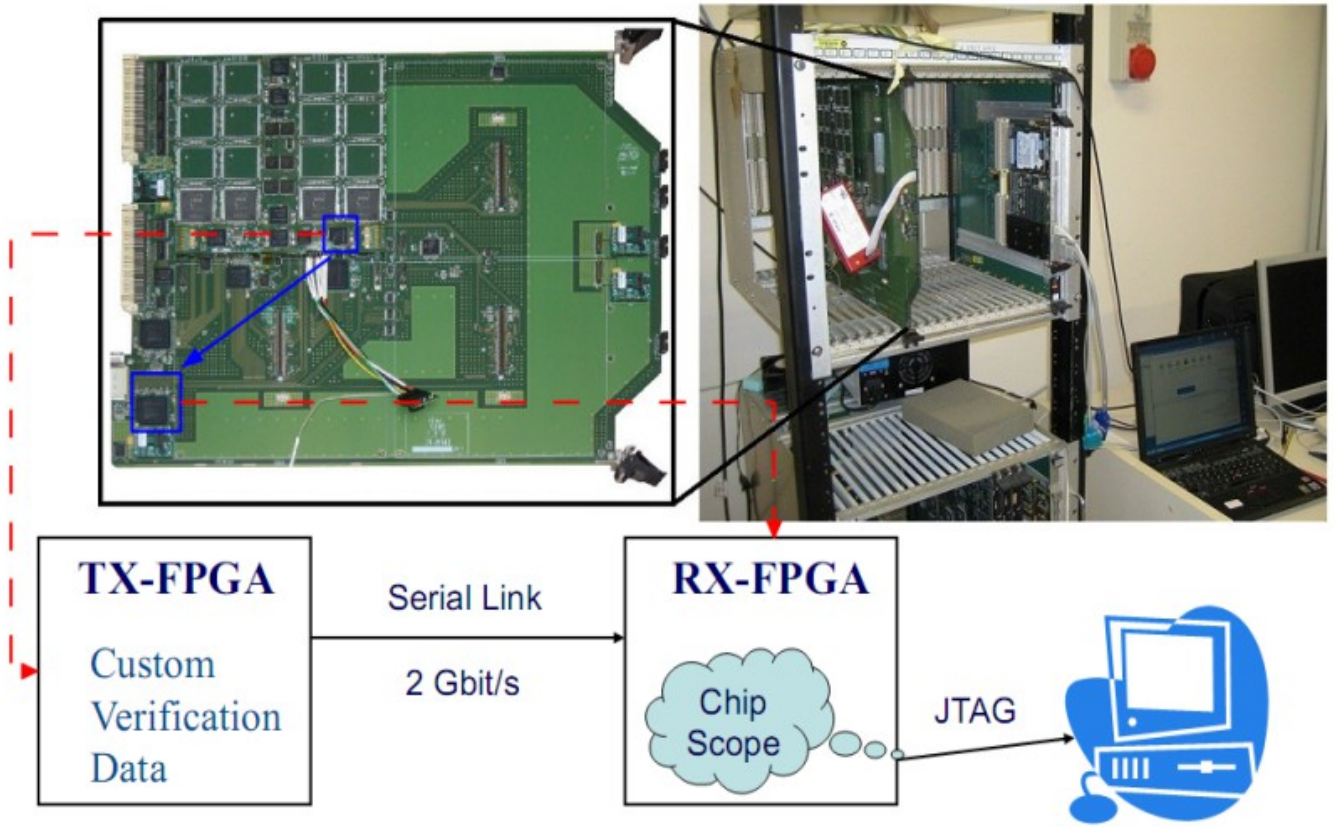
TESTS AT PISA

In Pisa we did tests on the previous version of the board, the one called AMBFTK.

This board has only partial serialized signals and a different number and type of FPGAs to control the system.

However the test done on this board has been very important to understand the functionality of the GTP transceiver (data @ 2Gbit/s) and the feasibility of the Printed Circuit Board.

1 – test of the high speed GTP transmission: we did transmission between several FPGAs. After the correct parameters have been set the transmissions were ok @ 2 Gbit/s



2 – Pattern matching test: this test has been done with the current version of the AMchip (AMchip04).
Steps of the test:
- load of fake hits In the inputs fpga
- send hits to the AMchips
- readout of the patterns recognized through the spybuffers of the outptut FPGA
- check with the simulation (expected patterns)

The test was ok but not intensive and with a limited number of AMchips on the board.

CONCLUSION

- A test stand in Prisma is ready. In this test stand we will debug the boards that will be assembled by Prisma electronics.
- We need to develop FW/SW for debugging boards
- The first prototype of AMBSLP has been debugged in Prisma. We have a problem on a CPLD. We are investigating
- In Pisa we successfully did tests on the old version of the Associative Memory Board
- We are quite confident that we can manage the new technologies (Amchip with variable resolution, High speed serial data transmission)