MARIE CURIE IAPP: FAST TRACKER FOR HADRON COLLIDER EXPERIMENTS

1ST SUMMER SCHOOL: VHDL BOOTCAMP

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FPGA Implementation

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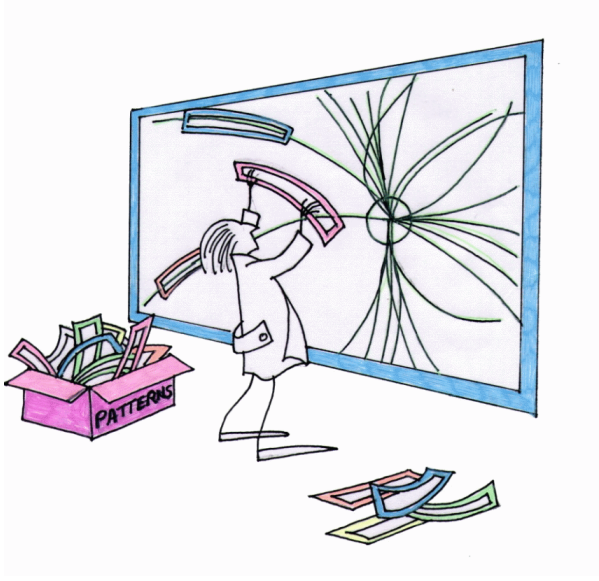

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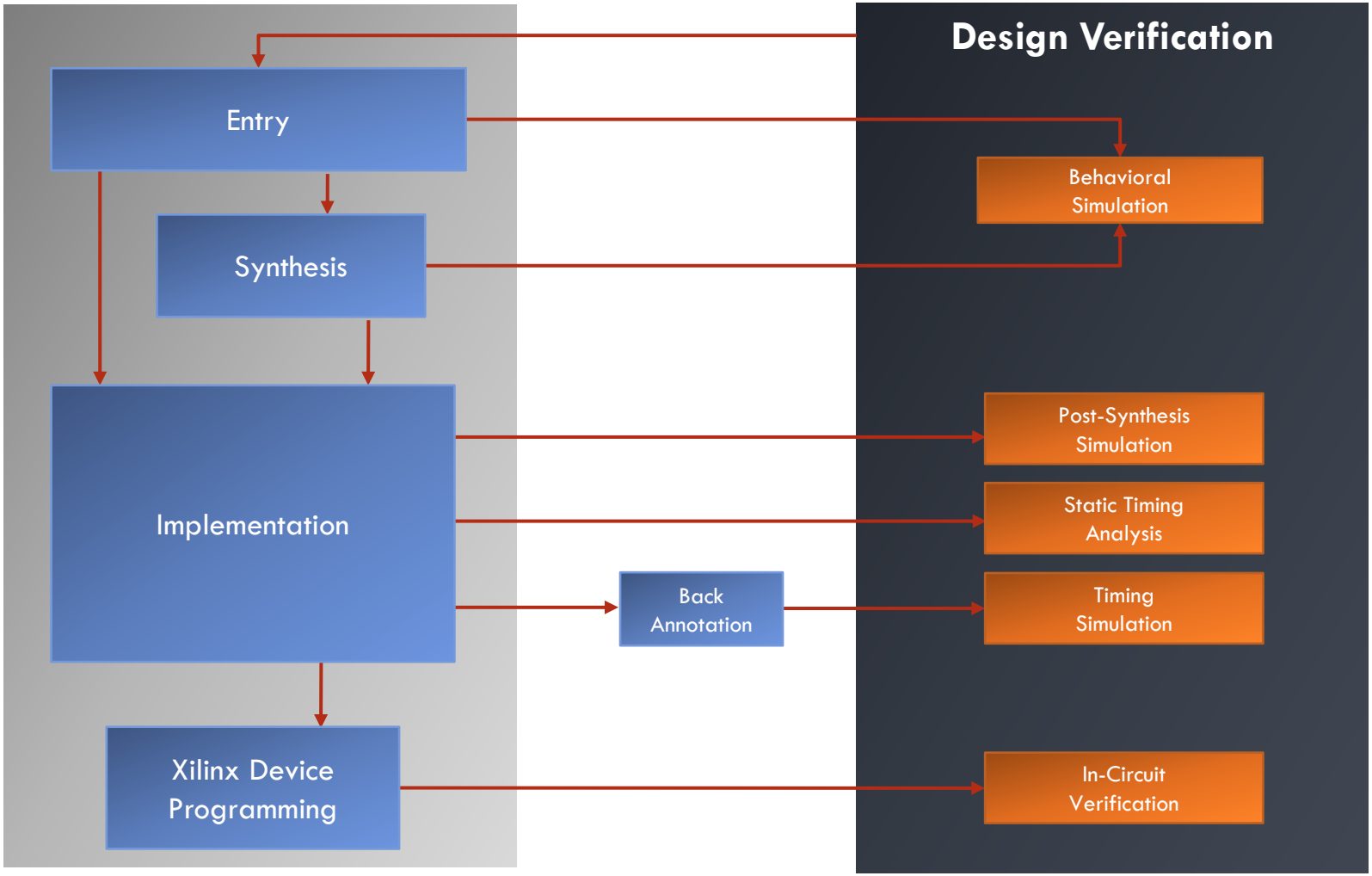
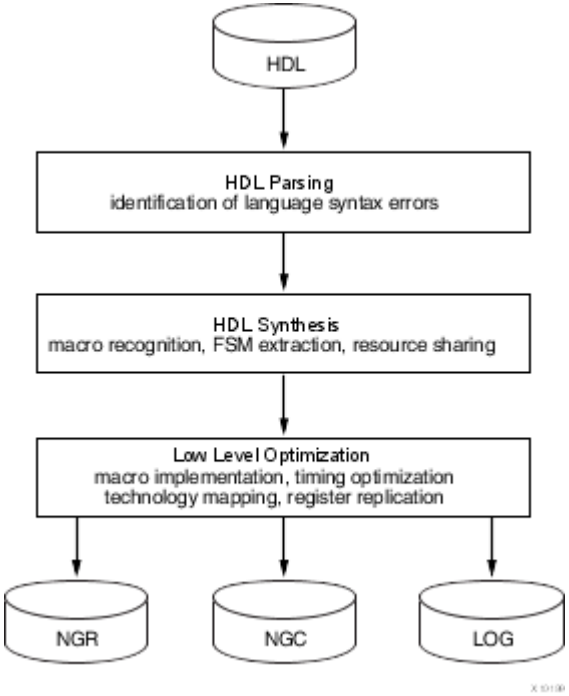
FPGA Implementation

Xilinx ISE Design Flow



Synthesis

- The XST (Xilinx Synthesis Tool) generates a Xilinx specific netlist file



Translate

- Converts input design netlists and writes results to a single merged NGD netlist. The merged netlist describes the logic in the design as well as any location and timing constraints.
- Performs timing specification and logical design rule checks.
- Adds constraints from the User Constraints File (UCF) to the merged netlist.

Constraint Editor

- Constraints are instructions placed on instances or nets in an FPGA or CPLD schematic or textual entry file such as VHDL or Verilog.
- Constraints specify **placement, implementation, naming, signal direction, and timing considerations for timing analysis and for design implementation.** In Xilinx software, logical constraints are placed in the User Constraints File (UCF).

Constraint Editor

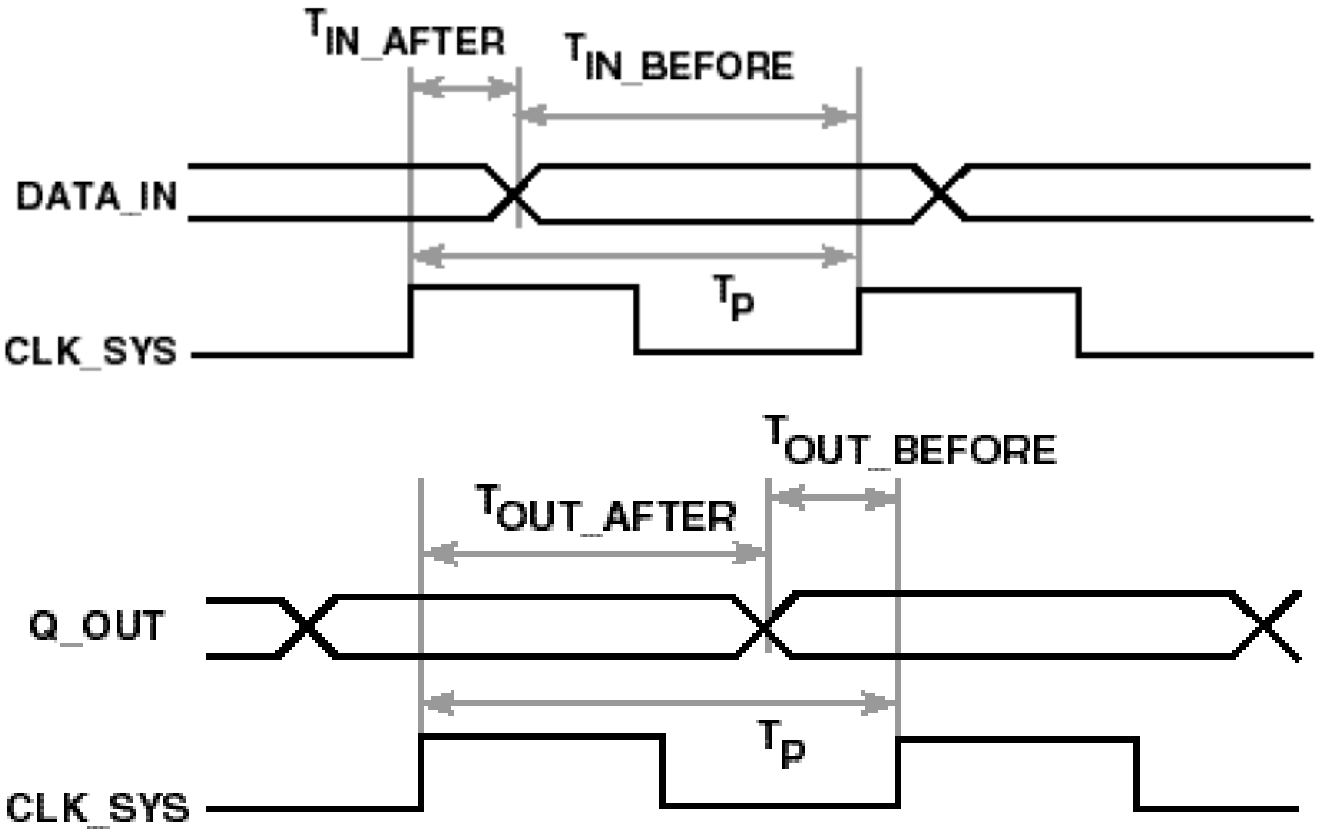
The Constraints Editor lets you do the following:

- Specify global timing constraints (PERIOD, OFFSET IN, OFFSET OUT, and operating conditions).
- Specify Groups on which to apply constraints.
  Note You can also specify groups when you need them rather than trying to anticipate all groups that you might want to use.
- Specify input timing constraints (OFFSET IN) on pad groups or pad nets.
- Specify output timing constraints (OFFSET OUT) on pad groups or pad nets.
- Specify timing exceptions for paths or nets.
- Specify miscellaneous constraints.

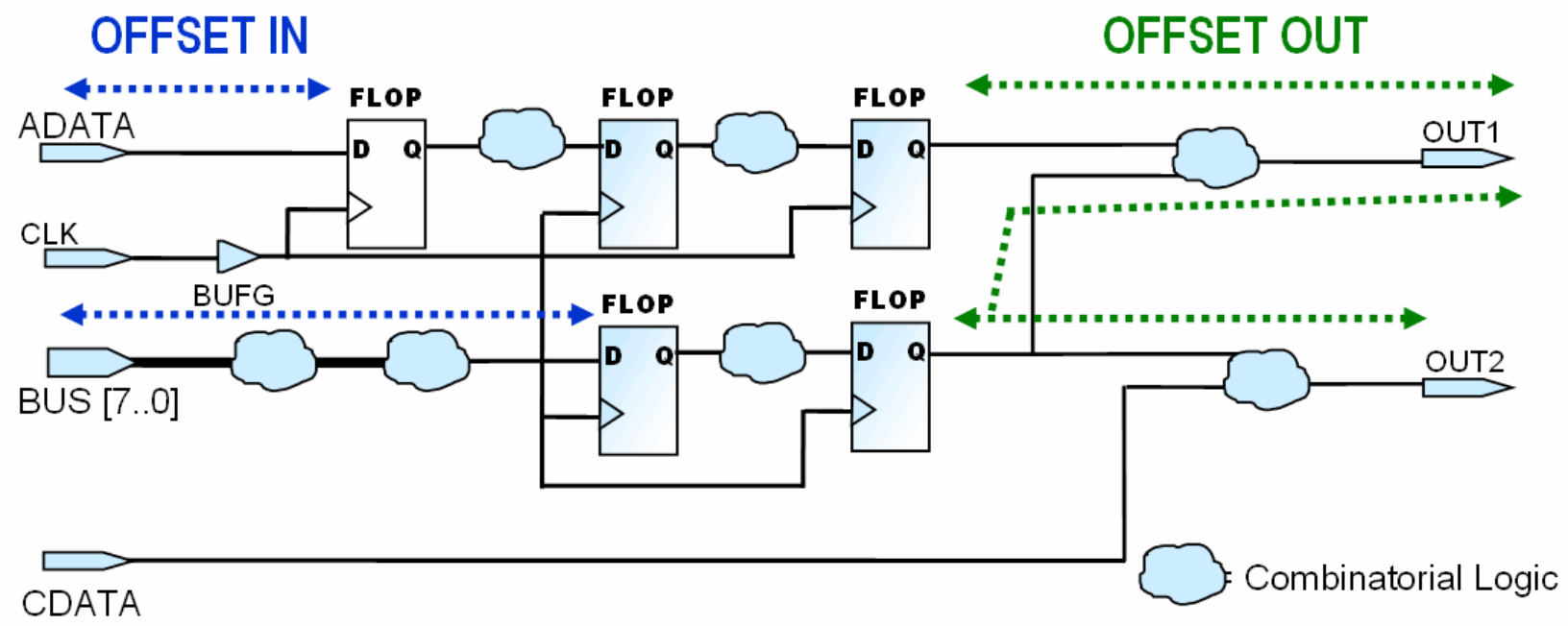
Constraints Editor

- PERIOD: Sets the desired clock period and the tool tries to meet the required performance
- OFFSET IN: Constraint used for setup and hold times of the external data to the internal flip flop
- OFFSET OUT: Constraint used for setup and hold times of the downstream devices

Constraints Editor

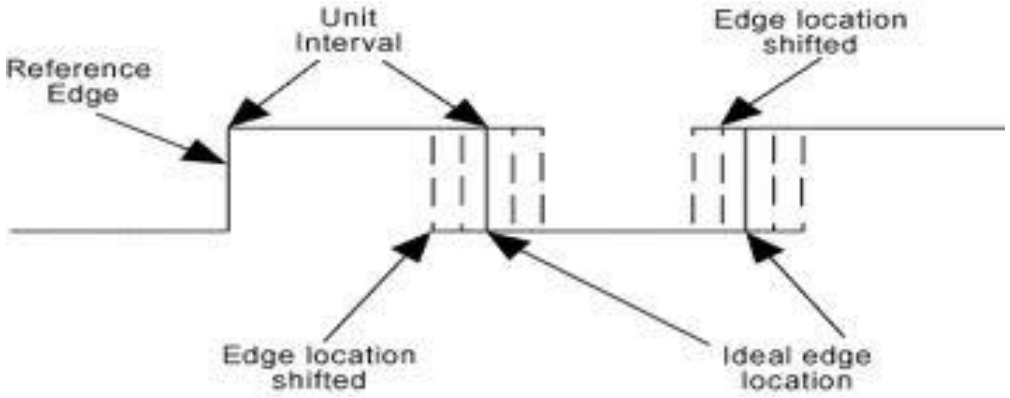


Constraints Editor



Constraints Editor

- **Jitter:**
  Jitter is the timing variations of a set of signal edges from their ideal values. Jitters in clock signals are typically caused by noise or other disturbances in the system. Contributing factors include thermal noise, power supply variations, loading conditions, device noise, and interference coupled from nearby circuits.



Map

The design is mapped into CLBs and IOBs. Map performs the following functions:

- Allocates CLB and IOB resources for all basic logic elements in the design.
- Processes all location and timing constraints, performs target device optimizations, and runs a design rule check on the resulting mapped netlist.

Place and Route

After the mapped design is evaluated, the design can be placed and routed. One of two place-and-route algorithms is performed during the Place and Route (PAR) process:

- Timing-Driven PAR:
  PAR is run with the timing constraints specified in the input netlist, the constraints file, or both.
- Non-Timing-Driven PAR:
  PAR is run, ignoring all timing constraints.