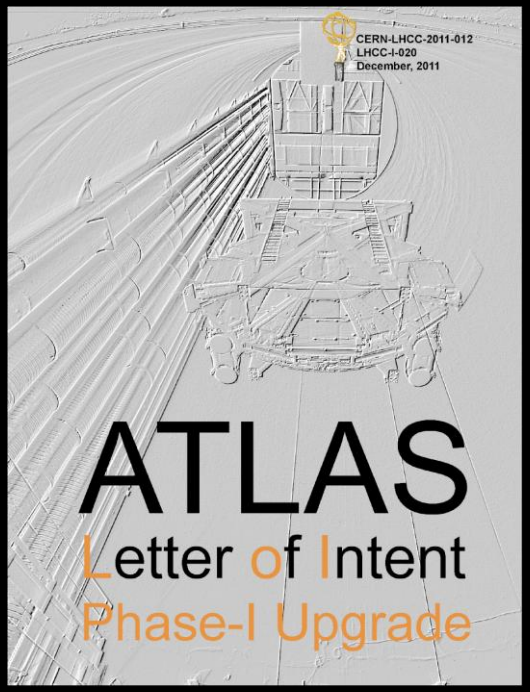
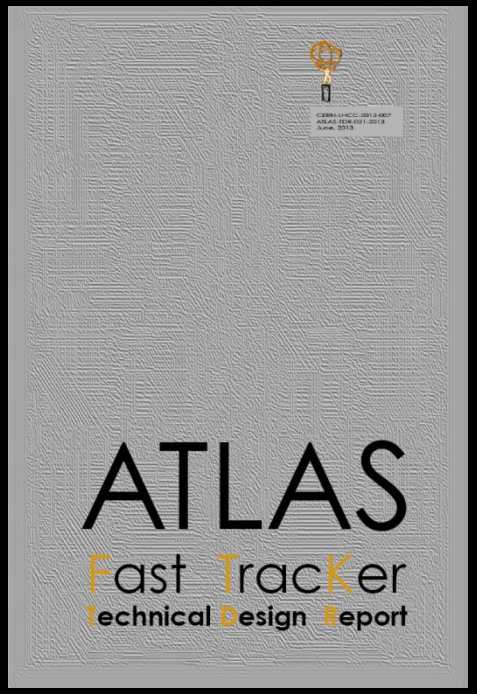
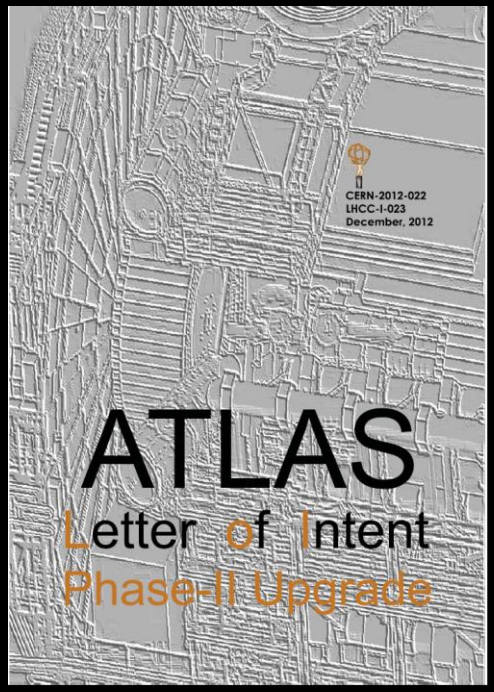




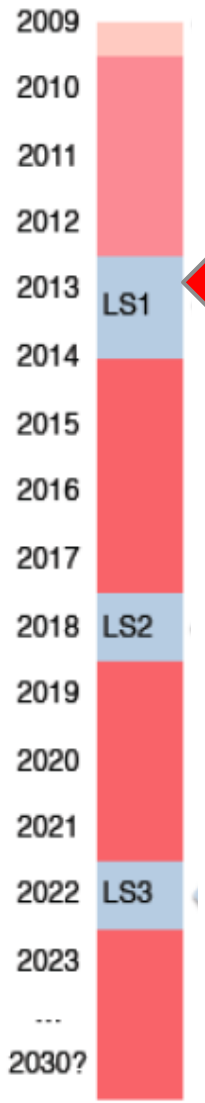


ATLAS UPGRADES

F. Tartarelli, Consiglio di Sezione (24/06/2013)

LHC and ATLAS status

- RUN 1:
  - Very successful run ended on 17/02/2013
  - Historical run thanks to the discovery of the Higgs boson
- What next?
  - Study Higgs properties: looks like SM Higgs
  - Search for new physics still on-going: SUSY, BSM,...
- Entered phase called Long Shutdown 1 (LS1) which precedes the start of new data taking period starting in 2015 (RUN 2)
- No time to relax: intense activities going
  - LHC: increase center-of-mass energy 8 → 13-14 TeV
  - ATLAS: Phase 0 activities



OGGI

RUN 1
$\sqrt{s}$=7-8 TeV, L=6x10^{33} cm^{-2} s^{-1}, 50 ns

~20-25 fb^{-1}

RUN 2 (Phase 0)
$\sqrt{s}$=13 TeV, L~1-2x10^{34} cm^{-2} s^{-1}, 25 ns

~75-100 fb^{-1}

Phase 1
L~2-3x10^{34} cm^{-2} s^{-1}

~350 fb^{-1}

Phase 2
L~5x10^{34} cm^{-2} s^{-1}

~3000 fb^{-1}

Milano activities

Tracking and calorimetry:

- with also interest in trigger aspects that will become more and more important as the luminosity increases:

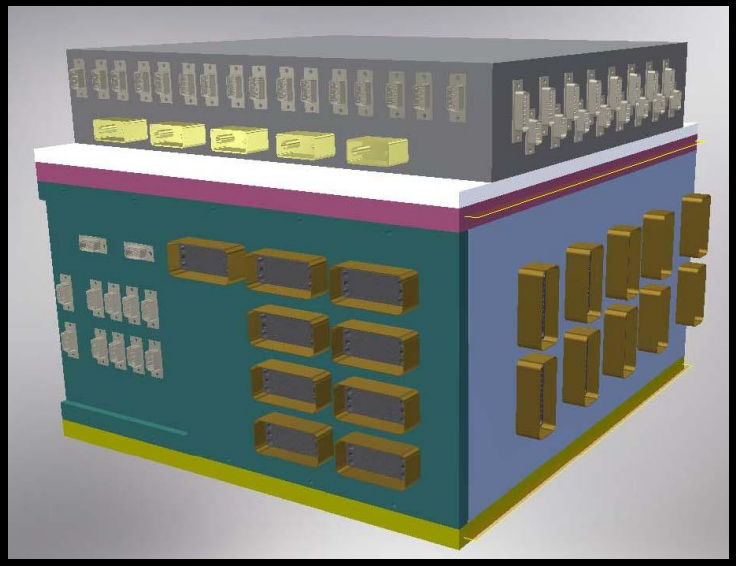
- LS1 (now!):
  - IBL (Insertable B-Layer)
  - LAr HV (Liquid Argon calorimeter high-voltage system)
- Phase 1:
  - AFP (ATLAS Forward Phyiscs)
  - FTK (Fast TracKer trigger)
  - Lar (Liquid Argon trigger upgrade)
- Phase 2:
  - ITK (Inner TracKer)
  - Lar (Liquid Argon front-end electronics upgrade)

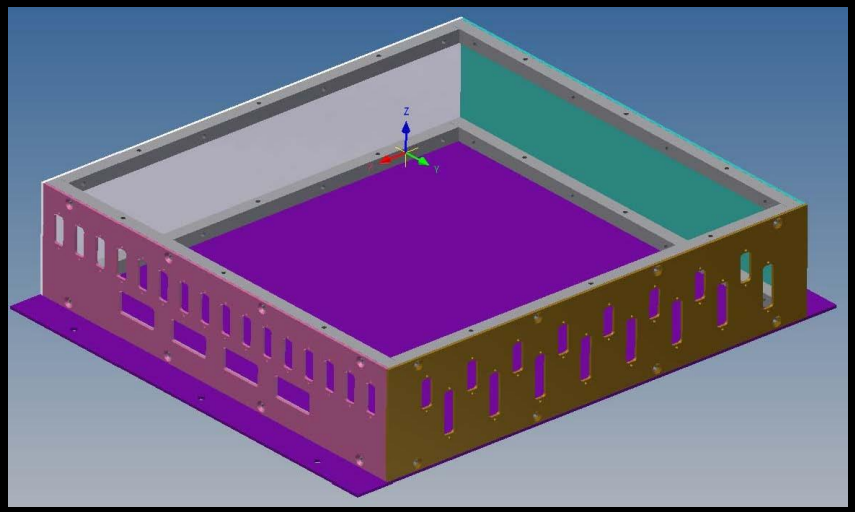
IBL (Insertable B-Layer):

- The Insertable B-Layer (IBL) is a fourth layer added to the present Pixel detector between a new beam pipe and the current inner Pixel layer (B-layer)
- Milano is responsible for the production of the Low Voltage regulation stations, called PP2 (Patch Panel 2):
  - Evolution of the design done for the pixel detector PP2
- We have to produce, test and deliver:
  - 10 crates (IBL + pixel + test set-up + AFP + spares)
  - Relative boards (controller, LV boards, VVDC boards)
  - 4 HV/DCS boxes

IBL

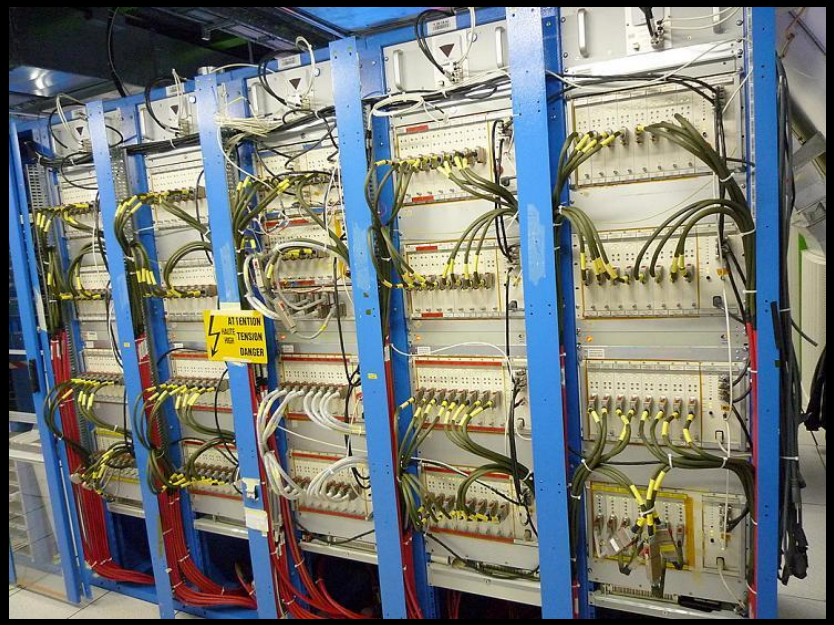
- All parts needed for the PP2 are in Milano (except some connectors from Positronics and Axon).
- All boards have been produced
  - First boards already shipped to CERN
- First crates being assembled
  - will be shipped this week to CERN (with 2 boards)
- HV boxes will be ready end of July





LAr HV system

- Milano share responsibility for the operation of the high voltage for all LAr calorimeters
- Now kept OFF with regular ramps to ~100 V
- Profit of the shutdown for HW/SW maintenance :
  - Exchange old and defective module
  - migrate PC Windows → Linux
  - Control software maintenance: FSM, alarms,..
  - PVSS II 3.8 → Simatic WinCC OA 3.1



Phase I

Status of Phase 1 upgrades

- Various upgrade projects at various stage of their approval process:

#	Project	Letter of Intent presented and approved by LHCC	Initial Design Review	Kick-off meeting	CB approval	TDR due	LHCC Session	I-MOU needed	MOU-due for signature (RRB)
1	FTK	21-Mar-12	2-Dec-10	3-Dec-10	24-Jun-11	30-Apr-13	11-Jun-13	Yes	15-Oct-13
2	nSW	21-Mar-12	29-Aug-12	31-Aug-12	5-Oct-12	31-May-13	11-Jun-13	not clear	15-Oct-13
3	LAr	21-Mar-12	9-Jan-13	11-Jan-13	8-Feb-13	15-Sep-13	24-Sep-13	not clear	15-Oct-13
4	TDAQ	21-Mar-12	21-Jan-13	23-Jan-13	8-Feb-13	15-Sep-13	24-Sep-13	not clear	15-Oct-13
5	AFP	21-Mar-12	17-Sep-12	19-Sep-12	2014	2014	2014	Yes	14-Oct-14

- In red the projects with Milano interest and involvement

FTK (Fast TracKer trigger)

- Highly parallel hardware track trigger at LVL2 using information from Pixel + Si Strips hits:
  - Works up to $3x10^{34}$ $cm^{-2}s^{-1}$, sustaining a 100 kHz LVL1 rate with 100 us max latency per event
- At the heart of the system is a dedicated custom AM (Associative memory) ASICS for pattern matching:
  - Additional logic provided via a series of FPGA
- System arranged in several AMBFTK boards (+AUX board); each board contains 4 mezzanine boards (LAMB) in turn containing 32 AM chip each

FTK

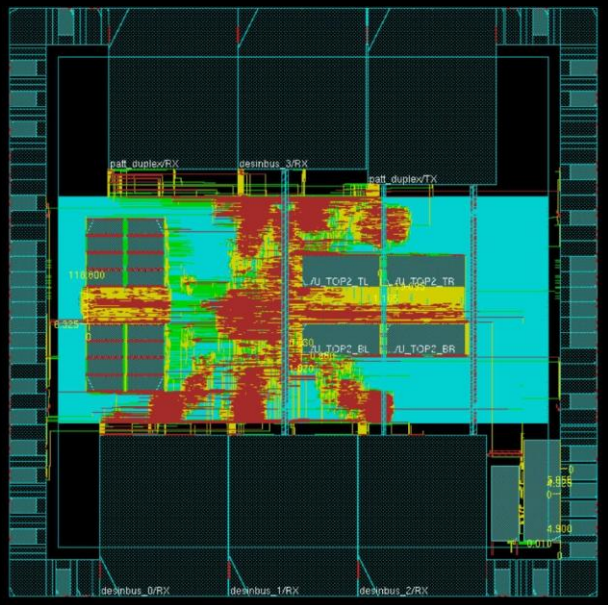
- Long development cycle for the Amchip:

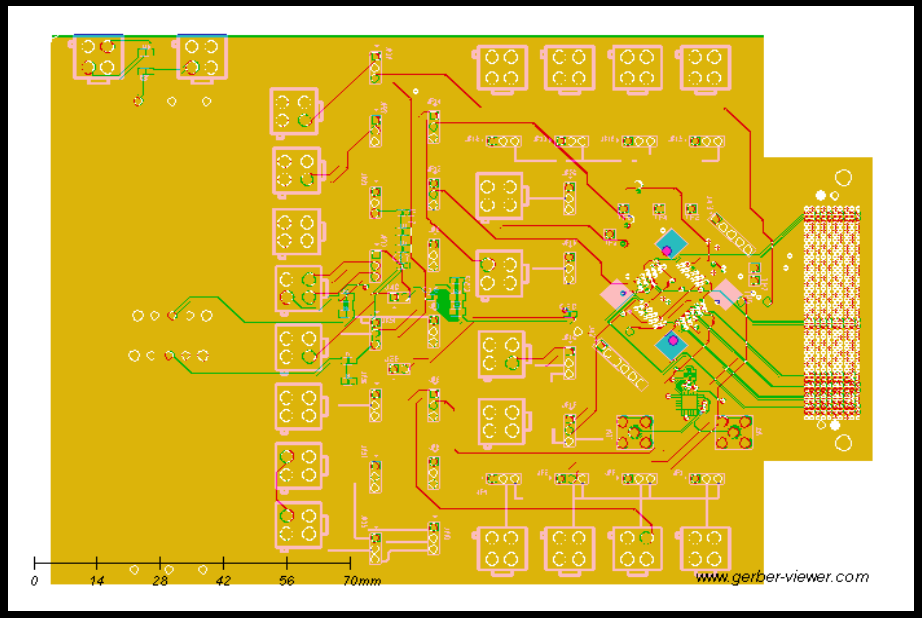
Name	# of patterns	Status	Note	Deadline
AMCHIP04	8k	Completed	It's functional	Apr. 2012
AMCHIP05miniasic	256	Fabricated	Characterization test in Jul. 2013	Jul. 2013
AMCHIP05mpw	4k	Design in progress	Submission deadline 31 Jul. 2013	Dec. 2013
AMCHIP06	128k			Dec. 2014

Final chip to be used in ATLAS

AMTKCHIP05miniasic

- Development of a new chip to verify new features:
  - New low power cell XOR+RAM (Power consumption minimization)
  - Serializer and deserializer @ 2 GHz (PCB routing reduction)
- PCB for the AMCHIP05miniasic test:
  - Design completed
  - Test planned for July 2013





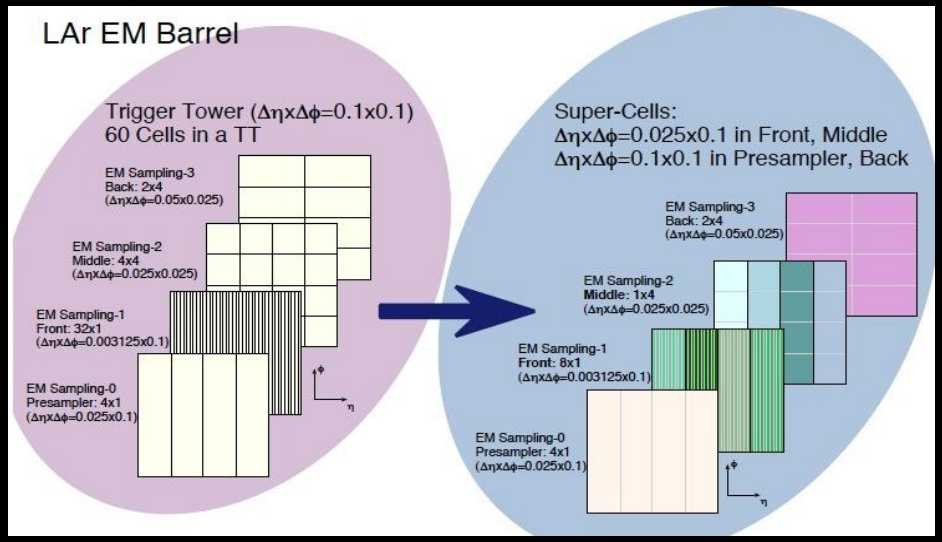
ATLAS Forward Physics (AFP)

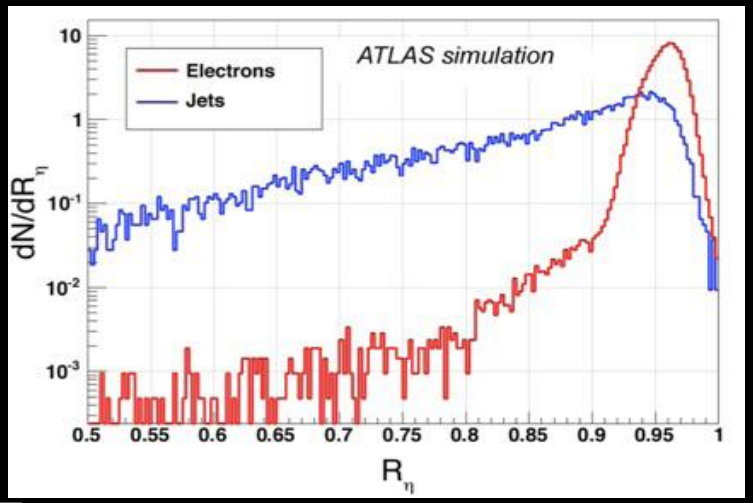
- Forward proton detectors at 220 m and 420 m from the interaction point on both sides of the ATLAS experiment.
- The AFP project is progressing. Areas to be more closely followed :
  - beam background evaluation/modeling
  - test beams in 2013 for timing and tracking
  - Physics Review preparation
- Milano contributions:
  - Power distribution based on "voltage regulation" in detectors proximity: IBL PP2 crate adapted to AFP needs (2 crates in total, 6+6 boards)
  - Bump bonding of sensors (Selex)

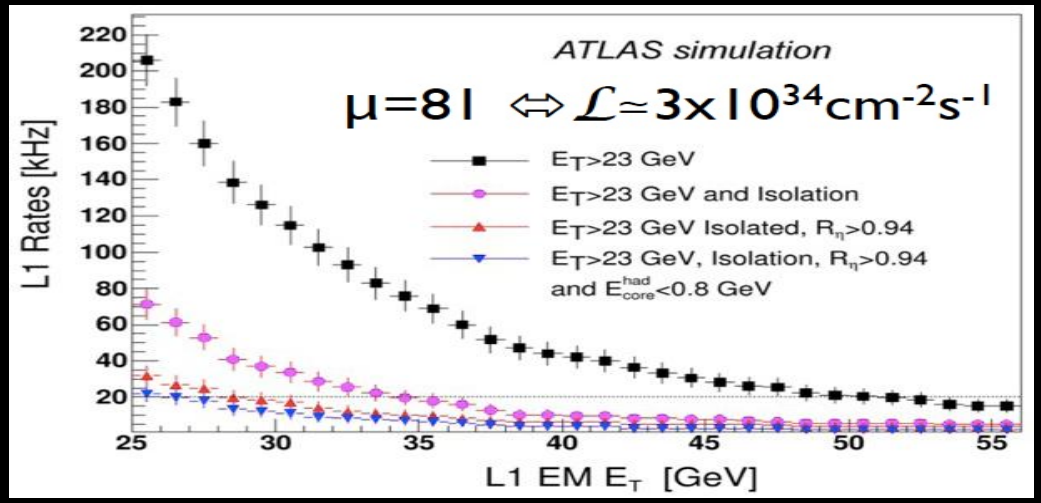
LAr trigger upgrade

- Increasing the granularity of the L1 calorimeter trigger will help to gain a factor 3 in L1 EM rates due to better jet rejection using lateral shower shape
- Showers from jets (broader) have smaller R_η than electron showers.

$$R_\eta = \frac{E_{[\Delta\eta\times\Delta\varphi=0.075\times0.2]}}{E_{[\Delta\eta\times\Delta\varphi=0.175\times0.2]}}$$



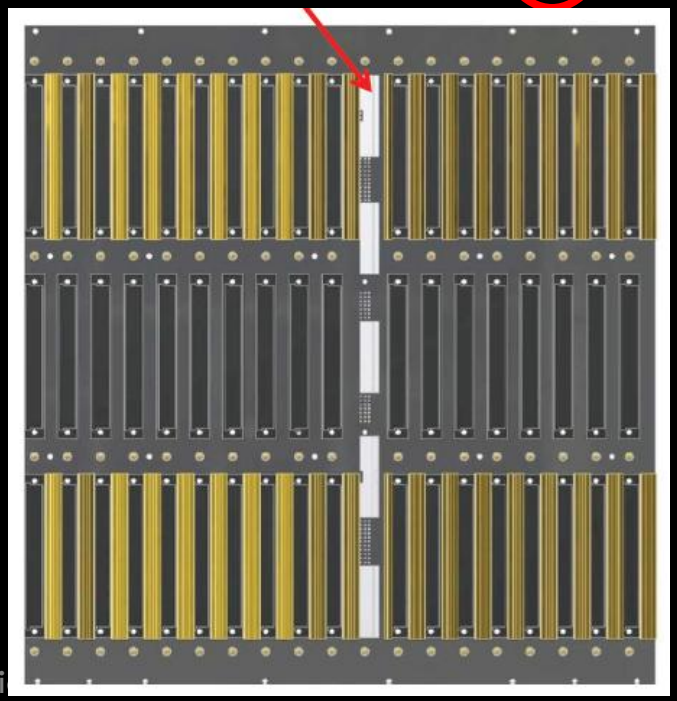




Lar: Milano contributions

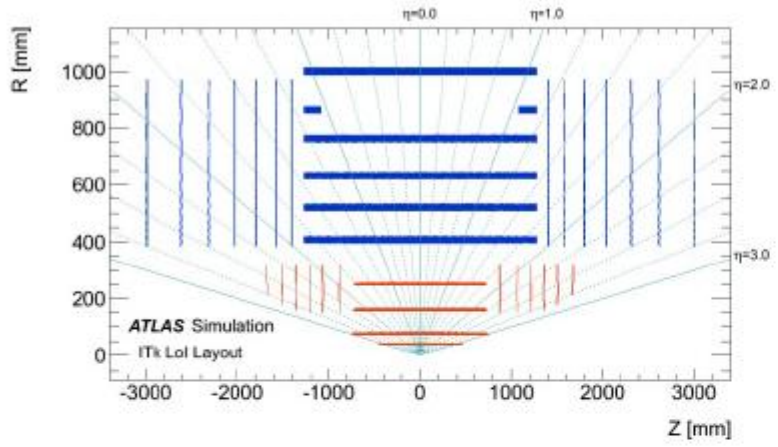
- Baseplanes:
  - redesign
  - ~1/3 of the production in Italy
- On-detector new Lar Trigger Digitizer Board (LTDB):
  - design and prototyping of power distribution
  - POL instead of LVDS (extension of the Gruppo V - APOLLO project)
- Data formatting on LTDB:
  - design of algorithms for data multiplexing/serialization using FPGA as a test bench
  - Collaboration with BNL on radiation tests

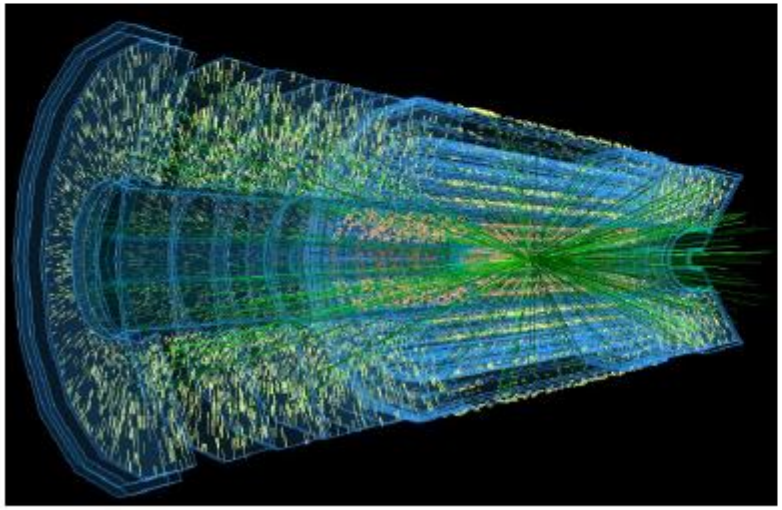
HFEC Type	Baseplane	LTDB	LDPB
EMB	64	64	64
EMEC Std	32	32	32
EMEC Special	8	8	16
HEC	8	8	8
FCAL	2	4	4
Total	114	116	124



Phase II

Phase II (ITK)





- 'Classical' tracker layout
  - 4/6 pixel layers/disks
  - 5/7 strip layers/disks + 'stub' cylinders
  - 50x250 μm^2 pixels (25x150 for inner layers)
  - 24/48 mm strips in barrel (inner/outer layers) with various different lengths in disks
- Full coverage up to $|\eta|=2.5$
  - limited coverage up to $|\eta|=2.7$
- Assumptions on HL-LHC conditions
  - $<\mu>=140$
  - Beam spot size 7.5 cm (luminous region in z)

Phase II (ITK)

- Sensors and bump bonding:
  - Continue (together with CMS) R&D with Selex
  - First step: development with IBL FE-I4 chip at 100 micron
  - Gruppo V call on bump-bonding techniques (and pixel)?
- Mechanical an thermal studies:
  - Extensions of studies done on IBL staves
  - ITK mechanical structures and thermal issues.

Phase II (LAr)

- Apart of the possibility of replacing FCAL and HEC electronics (still under discussion), the main change to LAr will be the replacement of all the 1524 Front End Boards (FEBs)
- New FEBs (FEB2s) will be designed with fully digital free running readout, i.e. avoiding trigger signal receivers and data buffering on the FEB
  - signals from all calorimeter cells are digitized at 40 MHz and sent off-detector
- Milano interest in exploiting the possibilities offered by the new readout to design a much more flexible trigger at LVL1:
  - Use of full granularity data, fast pattern recognition algorithm implemented in FPGA
- Some of us have presented a PRIN 2013 related to these studies

Tier2

- Milano e' uno dei 4 Tier2 italiani
- Le risorse richieste sono determinate dalla volontà di conservare il ruolo significativo nel computing di ATLAS acquisito negli ultimi anni conservando gli share di risorse pledged per le attività centrali e di garantire la competitività agli utenti italiani mediante l'uso di risorse dedicate nei Tier2
  - Tier2 italiani: 9% CPU e 7% Disco
- Per il 2014 solo sostituzione di materiale oboleto:
  - Le CPU obsolete sono le macchine con più di 3 anni di vita
  - Lo storage obsoleto comprende le SAN con più di 5 anni di vita

Tier2

	CPU 2014 (HS06)	CPU 2015 (HS06)	Disco 2014 (TBn)	Disco 2015 (TBn)
Frascati	1187	2304	0	120
Milano	4979	3735	192	176
Napoli	5312	3415	184	180
Roma	4707	3072	92	180
Tot	**16185**	**12526**	**468**	**656**

- Quota per Milano: 86.3 kEUR in totale
  - 33.1 kEUR (disco)
  - 43.5 kEUR (CPU)
  - 4.3 kEUR (rete)
  - 5.4 kEUR (server)

Anagrafica e richieste finanziarie

- 30 persone/24.5 FTE
  - 29 persone/24.6 nel 2013
  - Percentuali Call Gr. V e altri progetti?
- Metabolismo e missioni simili al 2013
  - Ripresa turni fine 2014: 1.5 mesi
- MOFB LAr: 75 kCHF (RRB Aprile '13)
- Richieste Calcolo (tot.: 86.3 keuro)
- Phase I:
  - Lar: 15 keuro
  - FTK and AFP to be discussed in ATLAS-Italia
- Phase II: R&D for ITK; Call CSN5?
- Meeting with referee on July 9

Richieste ai servizi

- Progettazione e officina
  - 7 mu progettazione, 7 mu officina
  - 30% Coelli

  Attivita' tracking upgrade Phase II (ITK), Lar (FEA of power dissipation new boards)

- Servizio Elettronica
  - 12 mu per progettazione FTK
  - 9 mu Lar
  - 3 mu installazione/commisioning PP2 in IBL
  - ~50% Citterio

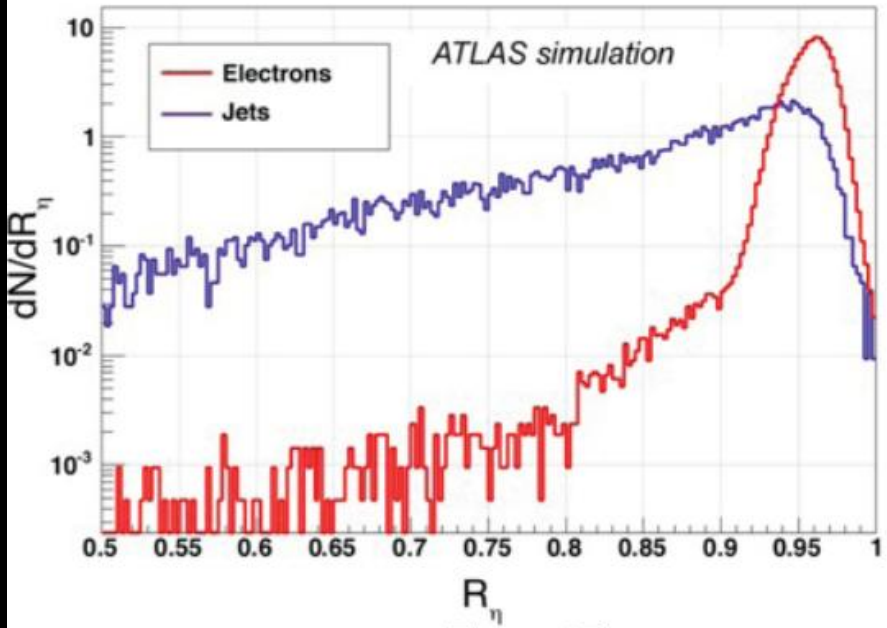
Back up

Lar Phase I upgrade

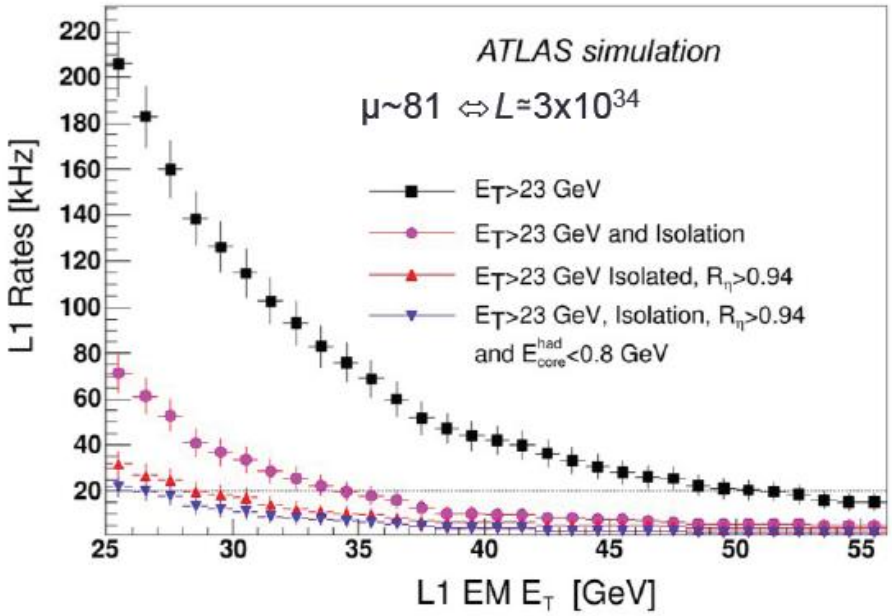
- Purposes:
  - maintain high efficiency for Level-1 triggering on low P_T objects (electrons and photons)
  - Improve jet, tau, MET triggers
  - Enable lower thresholds for multi-object triggers
  - Give more flexibility in trigger menu design and in operations
- In the LAr calorimeter this implies changes to the front-end electronics to allow greater granularity to be exploited at Level-1
  - finer segmentation in eta
  - depth information
- Enable use of more powerful LVL2 /offline-like variables/ techniques in the L1Calo selection:
  - Shower shapes

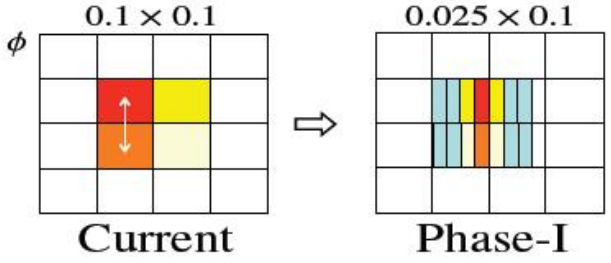
Improving electron ID → eFEX

Increase em trigger discrimination power by processing finer granularity LAr data



$$R_\eta = \frac{\sum_{3\times2} E_T}{\sum_{7\times2} E_T}$$

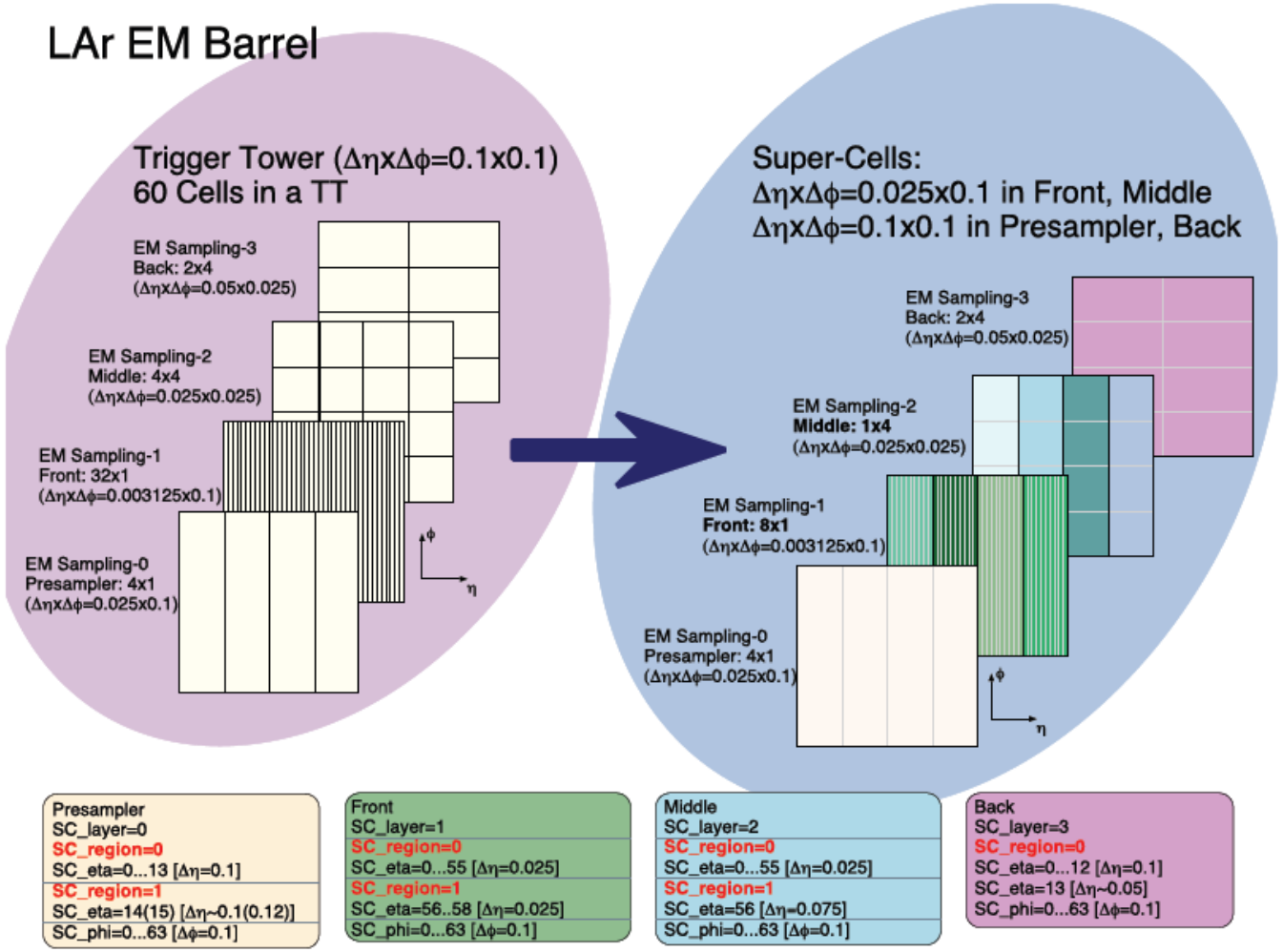


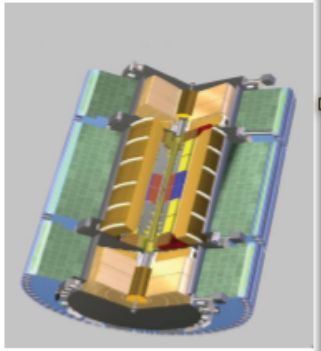


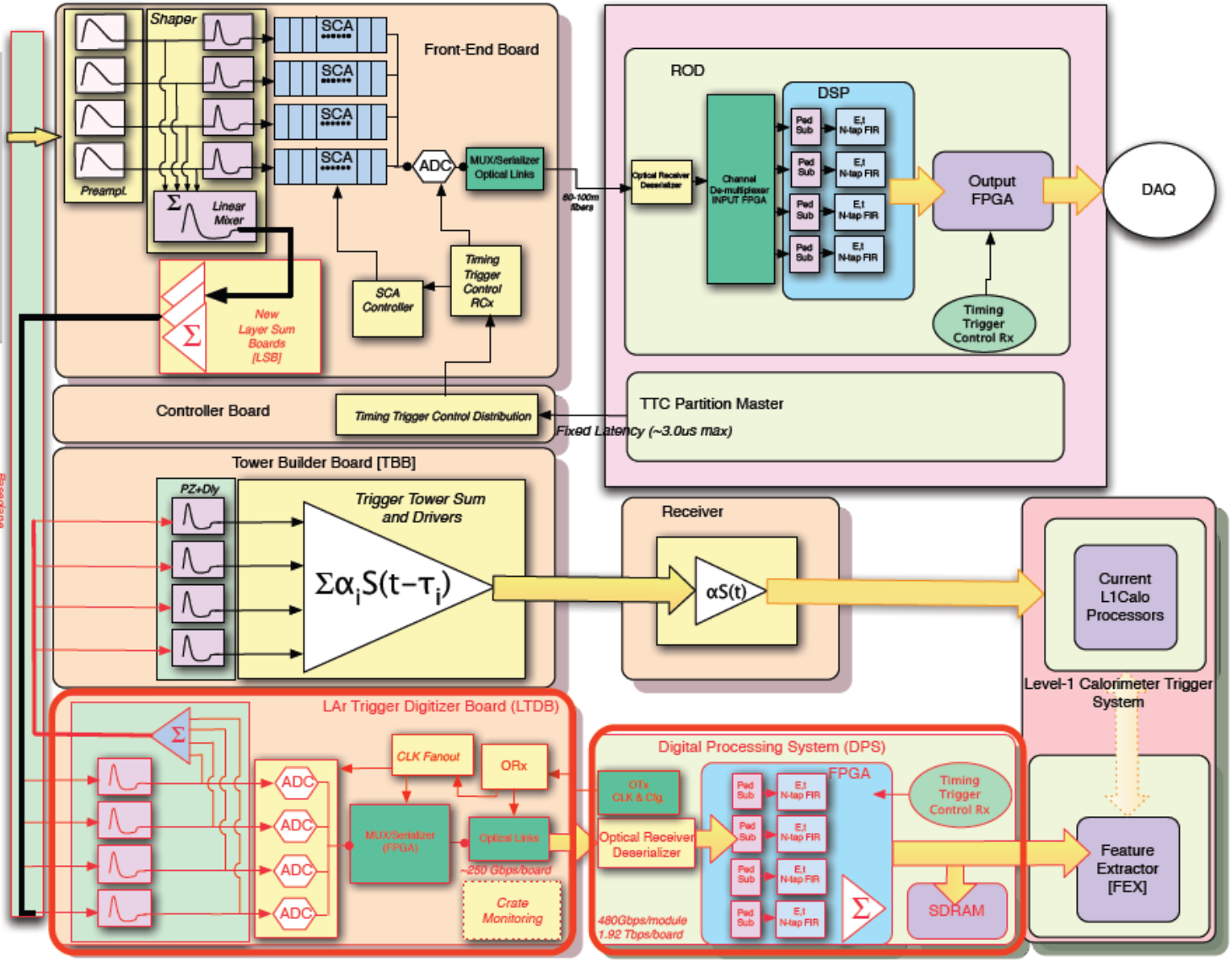
One Trigger Tower

↓

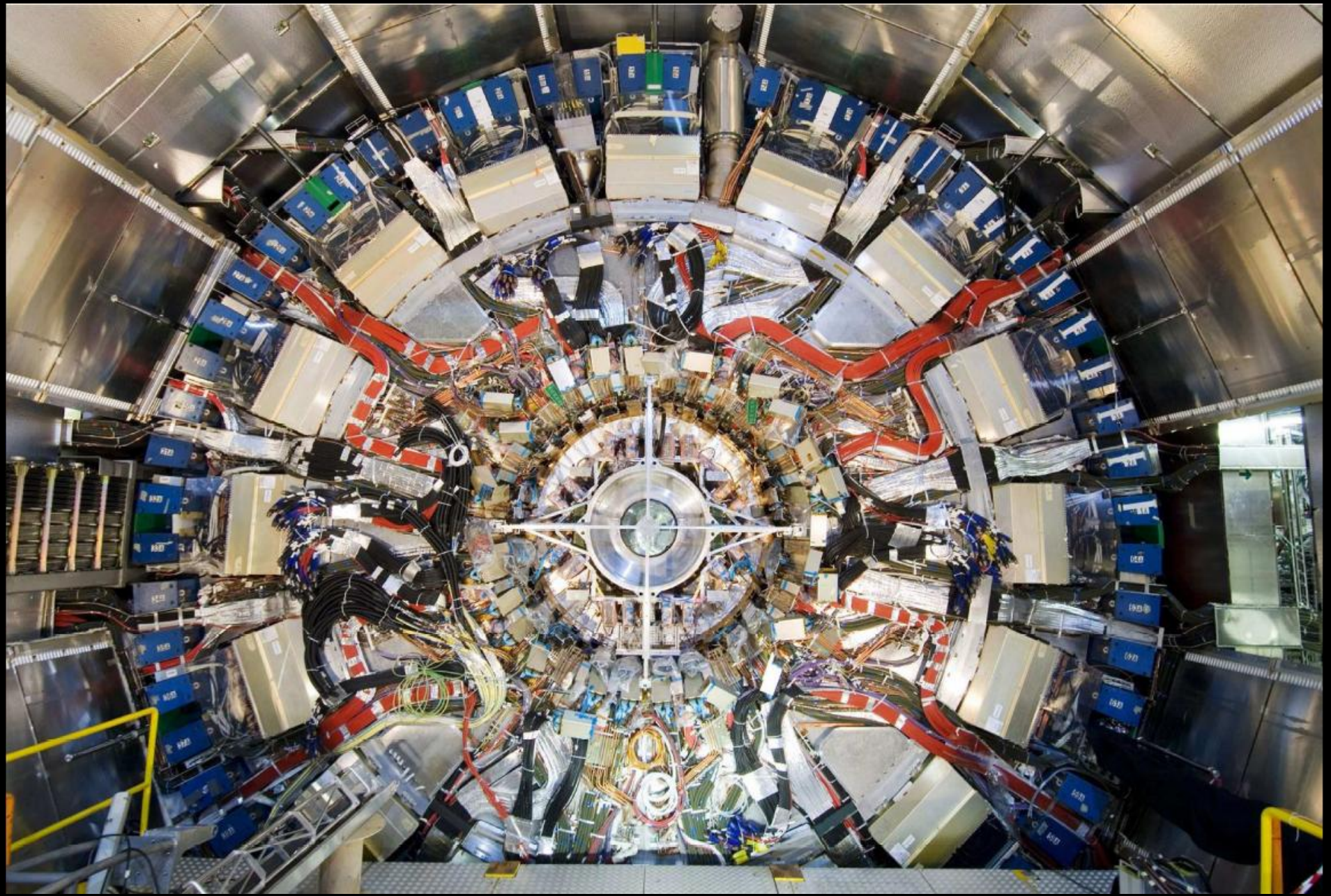
Ten Super-Cells
- 1 PS
- 4 Strips
- 4 Middle
- 1 Back

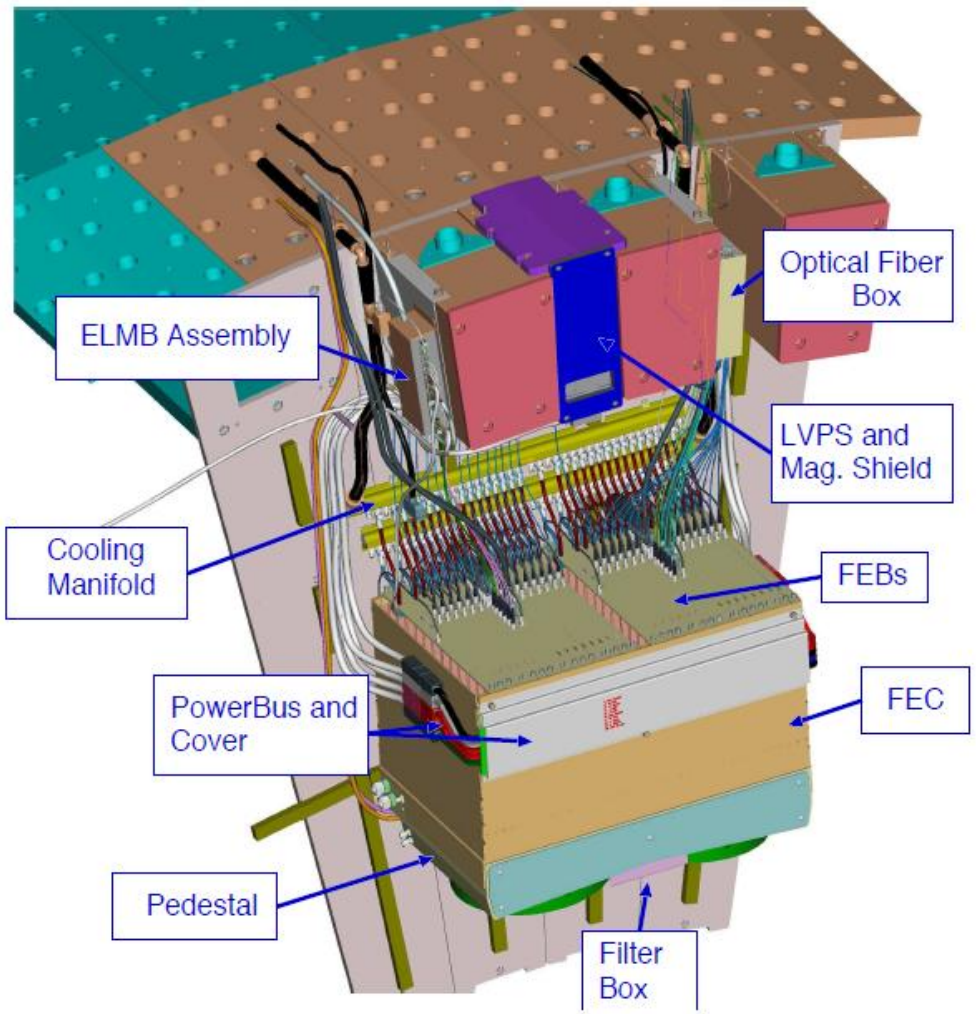


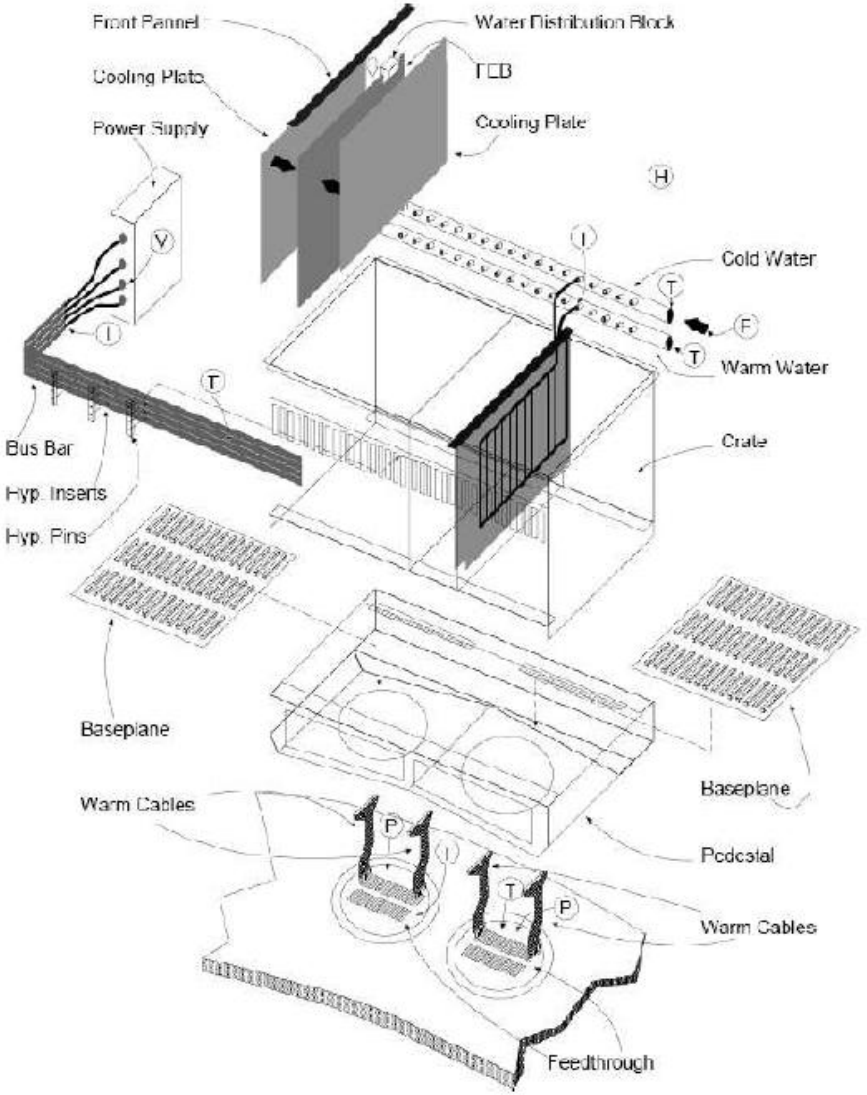


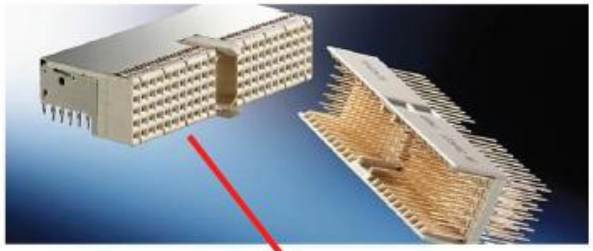


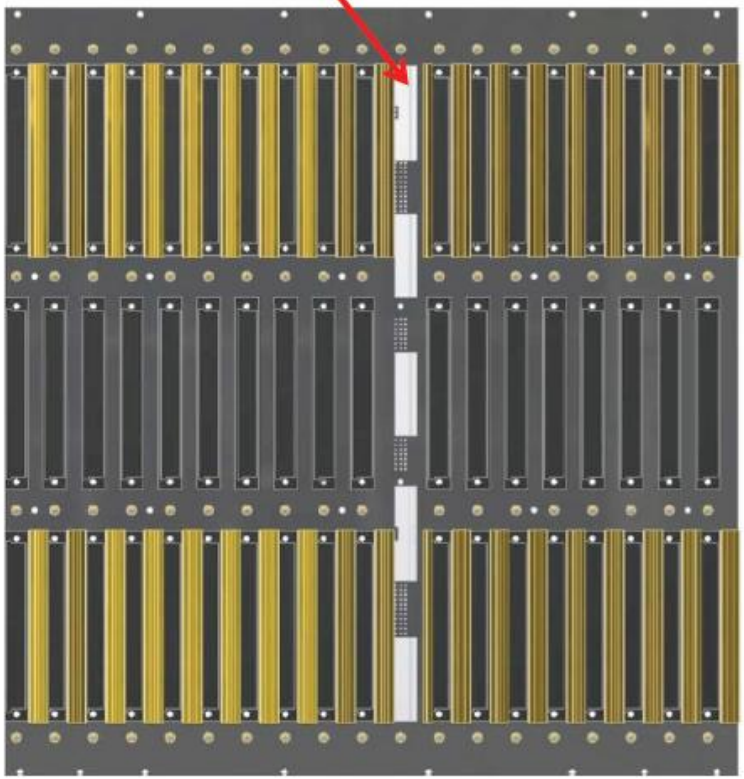
Possible implementation
$\Delta\eta\times\Delta\phi$=0.025x0.1 1st and 2nd layer EM
$\Delta\eta\times\Delta\phi$=0.1x0.1 elsewhere

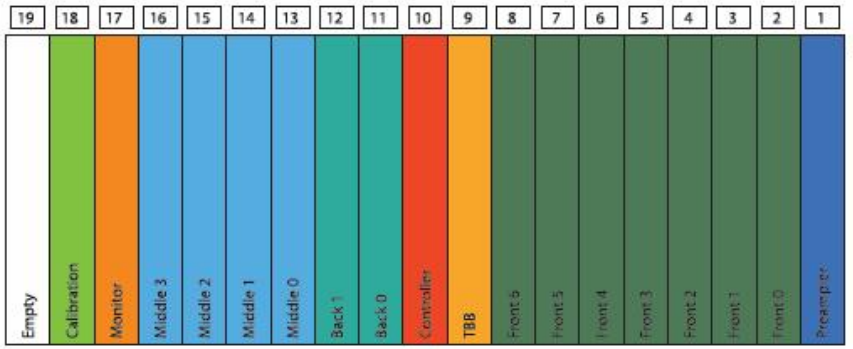


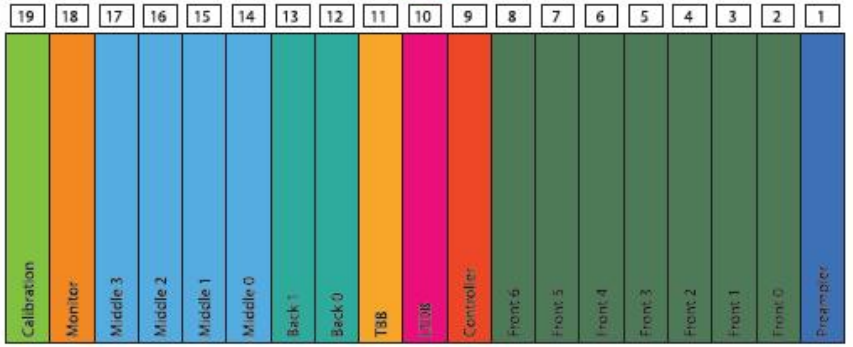

Optical Fiber Box
ELMB Assembly
LVPS and Mag. Shield
Cooling Manifold
FEBs
PowerBus and Cover
FEC
Pedestal
Filter Box


Front Pannel
Water Distribution Block
Cooling Plate
FEB
Power Supply
Cooling Plate
Cold Water
Warm Water
Crate
Bus Bar
Hyp. Inserts
Hyp. Pins
Baseplane
Baseplane
Warm Cables
Pedestal
Warm Cables
Feedthrough






19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
Slot #
Empty
Calibration
Monitor
Middle 3
Middle 2
Middle 1
Middle 0
Back 1
Back 0
Controller
TBB
Front 6
Front 5
Front 4
Front 3
Front 2
Front 1
Front 0
Preamplifier


19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
Calibration
Monitor
Middle 3
Middle 2
Middle 1
Middle 0
Back 1
Back 0
TBB
LTDB
Controller
Front 6
Front 5
Front 4
Front 3
Front 2
Front 1
Front 0
Preamplifier


EM Barrel

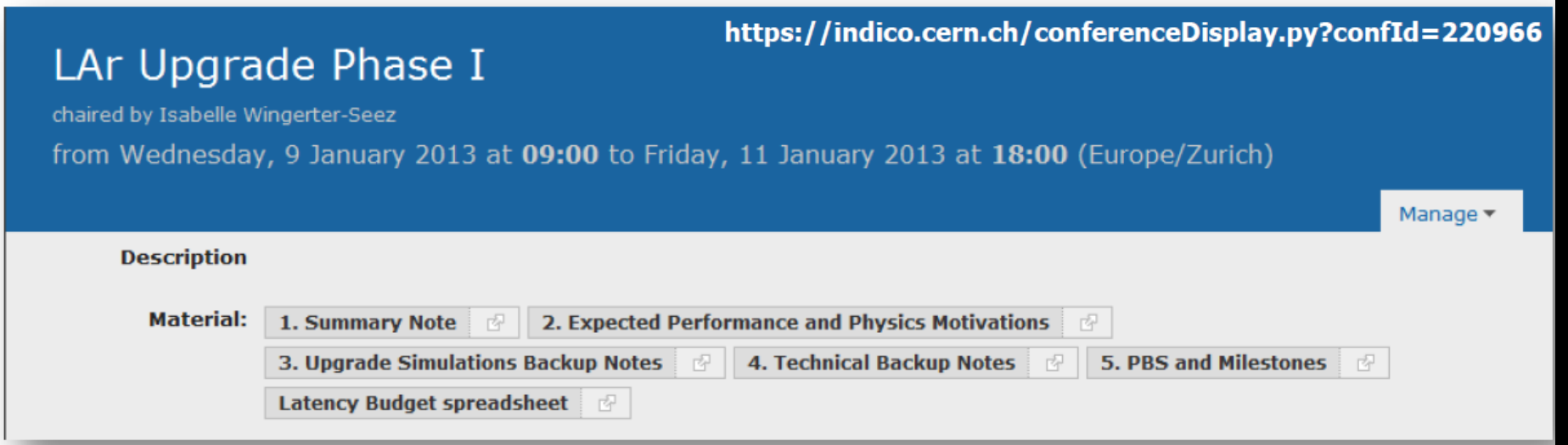
LAr electronic upgrade for Phase I

#	Project	Letter of Intent presented and approved by LHCC	Initial Design Review	Kick-off meeting	CB approval	TDR due	LHCC Session	I-MOU needed	MOU-due for signature (RRB)
1	FTK	21-Mar-12	2-Dec-10	3-Dec-10	24-Jun-11	30-Apr-13	11-Jun-13	yes	15-Oct-13
2	nSW	21-Mar-12	29-Aug-12	31-Aug-12	5-Oct-12	31-May-13	11-Jun-13	not clear	15-Oct-13
3	LAr	✓ 21-Mar-12	✓ 9-Jan-13	✓ 11-Jan-13	✓ 8-Feb-13	15-Sep-13	24-Sep-13	not clear	15-Oct-13
4	TDAQ	21-Mar-12	21-Jan-13	23-Jan-13	8-Feb-13	15-Sep-13	24-Sep-13	not clear	15-Oct-13
5	AFP	21-Mar-12	17-Sep-12	19-Sep-12	2014	2014	2014	yes	14-Oct-14

Project is on schedule:

- IDR passed on January 9-11, 2013
- CB approval on February 8, 2013
- Next step is TDR due September 15, 2013

Outcome of the LAr Phase-I Initial Design Review



- ✓ Reviewers:
  - Giulio Aielli, Michael Begel, Philippe Farthouat, Claudia Gemme (chair), Murrough Landon, Steve McMahon, Christoph Rembser, Stefano Veneziano

General comments of the reviewers

- ✓ The reviewers have looked at the physics case, the required hardware upgrade and the proposed structure of the organization for the project.
- ✓ The upgrade of the LAr electronics is a high priority project for the ATLAS experiment in Phase-I in order to keep an optimal trigger system as the luminosity increases beyond LHC nominal luminosity.
- ✓ We have paid particularly attention that there are no showstoppers in the proposed technical implementation and that the proposal is compatible with Phase-II.
- ✓ We congratulate the LAr community on the information provided and the very clear presentations and discussion during the review.
- ✓ A set of recommendations is made for the next steps of the project, mainly concerning the preparation of the Technical Design Report scheduled for Fall 2013.
  - ATU-TC-MR-0012: https://edms.cern.ch/document/1262820/1
  - Short term recommendations (details on TDR milestones, schedule, demonstrator program, etc..) done just after the review have already been included in the IDR documentation.

Recommendations – Physics case

- ✓ While the EM and Jet trigger studies are well advanced, more work on MET and tau studies is still needed and we recommend to
  - settle on a single set of simulation samples that are common with other Phase I and II efforts;
  - establish common benchmarks and definitions used to define the performance of the system.
  - It is mandatory to establish good contact with other upgrade groups who need validation studies on the same timescale.
- ✓ In the results of the studies a clearer factorization of benefits of issues like dynamic range and granularity and algorithm should be given.
- ✓ A clearer demonstration how the optimal working points (in terms of identification of bunch crossing, saturation and energy resolution) will be chosen needs to be given.

Both items might have implications on the hardware choices.

- ✓ A complete estimate of the important physics rates when this system is used during LHC Phase-II should be given.

Rec.: Technical Implementation-I

- ✓ Identify key failure mechanisms and ensure adequate redundancy is built into every aspect of the design, even based on the current detector operation.
- ✓ Front-End
  - Choice of ADC: COTS vs custom designs. It is recommended to pursue the three current options, even in view of future developments for Phase-II, but, in case all of them meet the requirements, to consider the commercial one.
  - Optical Links: if possible we recommend that the LAr community explores the possible use of the developments in the versatile link project (VTTX, dual transmitter).
  - We recommend the proponents to explore the possibility of using the serializer GBTx in parallel with other custom developments. In the case that FPGAs are demonstrated to work reliably in the environment (radiation), we recognize that this is also a valid solution.
  - Validate services (cooling, power supplies) and mechanics of the new LTDB with new connectors.

Rec.: Technical Implementation-II

- ✓ Back-End
  - A more detailed description of the readout (i.e. ROD) functionality. A more detailed description of the monitoring and what goes into the data stream.
  - Continue to consider implications for Phase-II as this part of the system will be kept.
- ✓ Installation
  - A detailed understanding of the risks involved in the installation of the new electronics in the pit.
  - A more detailed evaluation of the crate refurbishment schedule and timetable. Including a complete ALARA study of the radiation risks involved in the installation in the pit, implications on the scope of work activities and schedule impact. The schedule seems tight and therefore we recommend to develop it in strong contact with TC.
  - Finalize the initial study concerning the installation of the fibers, in particular in the flexible chains.

Conclusions

- ✓ The reviewers would like to thank the proponents for the significant amount of work done preparing for the review, the very clear documentation and presentations.
- ✓ The case for the LAr upgrade was very well made and we endorse the plan as presented.
- ✓ We cannot see any significant technical problems with the proposed solution as it is presented at this time and would recommend that you proceed to the TDR.
  - In our summary we have given various recommendations which we believe the proponents should consider as they move towards a TDR.

Milano possible contributions

- Baseplanes:
  - redesign
  - ~1/3 of the production in Italy [collaboration with BNL, Orsay]

- Layer Summing Boards:
  - redesign
  - ~1/3 of the production in Italy [collaboration with BNL, Saclay]

- On-detector new Lar Trigger Digitizer Board (LTDB):
  - design and prototyping of power distribution
  - POL instead of LVDS, extension of the Gruppo V - APOLLO Project [collaboration with BNL]

- Data formatting on LTDB:
  - design of algorithms for data multiplexing/serialization using FPGA as a test bench
  - Collaboration with BNL on radiation tests

- Simulazioni:
  - Simulazioni: sviluppo di algoritmi che utilizzino le supercelle a L1

- Interessi in vari aspetti del progetto con simulazioni, design e prototyping di componenti,…

Link to complete Product Breakdown Structure

Item	# units	Prod end	Prod start	PRR	FDR
Frontend					
Baseplane	124	5-2017	11-2016	9-2016	2-2016
LSBs	1664	9-2017	9-2016	7-2017	12-2015
LTDB:	124	9-2017	3-2017	1-2017	6-2016
Analog Mezzanines	124*4	1-2017	1-2016	10-2015	4-2015
Optical pigtails	124*4	1-2017	7-2016	5-2016	10-2015
Cooling plates	124*2	1-2017	7-2016	5-2016	10-2015
Mainboards					
ADC	124*80	1-2017	1-2016	11-2015	4-2015
ASIC Serializer	124*160	1-2017	1-2016	11-2015	4-2015
ASIC Laser Driver	124*160	1-2017	1-2016	11-2015	4-2015
VCSEL mezzanine (TOSA)	124*160	1-2017	1-2016	11-2015	4-2015
DC Powering	124	1-2017	1-2016	11-2015	4-2015
Base PCB	124	1-2017	1-2016	11-2015	4-2015
Long Fibers	58	7-2017	1-2017	11-2016	4-2016
Backend					
ATCA shelves	3	12-2016	9-2016	7-2016	-
LDPB/GBTD	34	9-2017	3-2017	1-2017	6-2016
AMC	34*4	1-2017	1-2016	11-2015	4-2015
IPMC	34*1	1-2017	1-2016	11-2015	4-2015
MMC	34*4	1-2017	1-2016	11-2015	4-2015
Optical pigtails	34*4	1-2017	1-2016	11-2015	4-2015
MicroPod Cooling block	34*4*4	1-2017	1-2016	11-2015	4-2015
Carrier Board	34	1-2017	1-2016	11-2015	4-2015
TTC Optical Couplers	3	7-2017	1-2017	10-2016	-
In shelf switches	3*2	7-2017	1-2017	10-2016	-
Receiver PCs	3	7-2017	1-2017	10-2016	-
Controlling PCs	2	7-2017	1-2017	10-2016	-

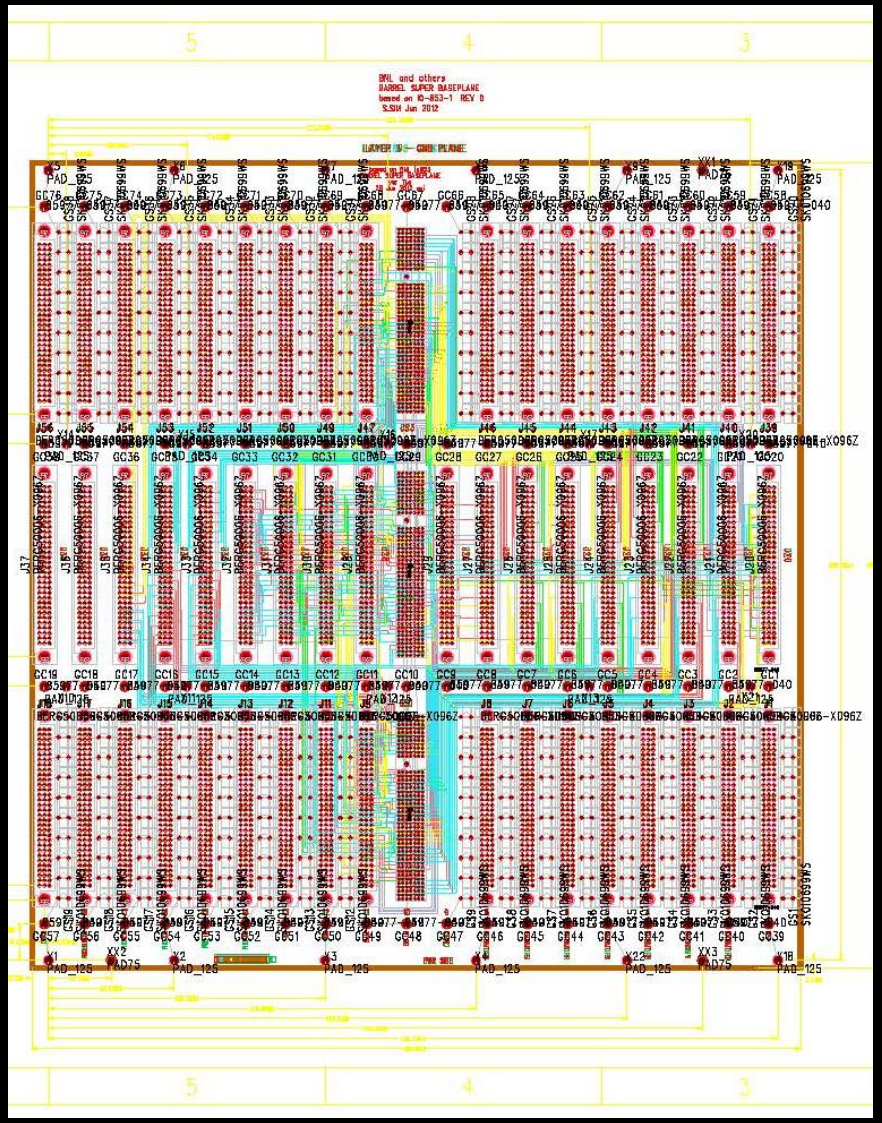
Barrel baseplane

- La scheda e' stata progettata usando:

- Solo stripline con impedenza controllata (50 ohm, tracce di 150 μm)
- Usando 5 layers, uno in piu' della scheda esistente, per migliorare il routing
- Non introducendo "via" per avere migliore signal integrity.
- Per il connettore della LTDB (fila centrale della figura) e' stato scelto un connettore Hard Metric a 2mm con shielding integrato.
- Lo spazio fra le traccie e' ~300 μm per avere basso crosstalk (< 1 %)

- Ulteriori verifiche sul layout:

- Simulazione a piena scheda con Hyperlinx dell'integrita' del segnale
- Simulazione dei segnali ottenuta con Spice e generazione dei modelli IBIS
- Eventuale ottimizzazione del layout in accordo con il produttore del prototipo della scheda



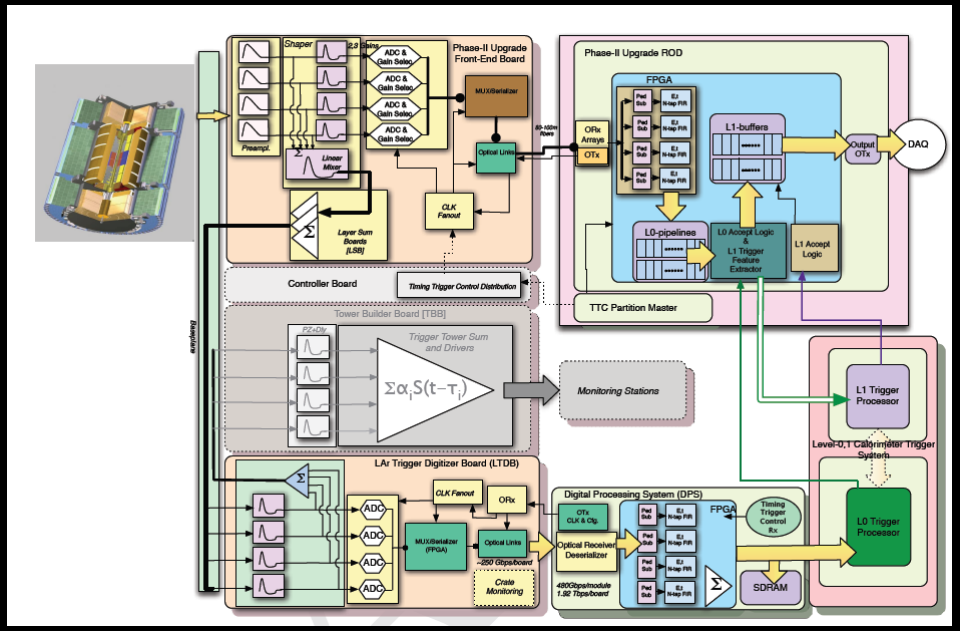
Institution	Interest	
Arizona	WG1	WG5 WG6
Triumf+Canada	WG1	WG3
LAPP	WG4	WG5 WG6
LAL	WG1	WG3
Milano	WG1	WG3
LPSC	WG2	
Dubna	WG1	WG3
Nevis	WG2	
SMU	WG2	
Dresden	WG5	WG6
CERN	WG2	WG4
SUNYSB	WG4	WG5
Saclay	WG1	WG3
BNL	WG1	WG2 WG3 (WG4) WG5 (WG6)
PITT	WG1	
CPPM	WG4	WG5
Lebedev	WG1	WG3
Novosibirsk	WG2	WG5
Montreal		
TOTAL	20 Institutions	48 FTE 103 names

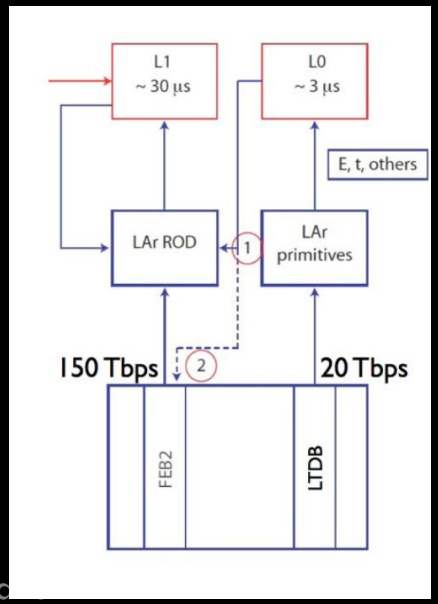
Phase II

- Apart of the possibility of replacing FCAL and HEC electronics (still under discussion), the main change to LAr will be the replacement of all the 1524 Front End Boards (FEBs):
  - the total dose for an integrated luminosity of 3000 fb-1 exceeds the FEB specifications
  - the Level-1 trigger latency may exceed the depth of the analog pipeline memories installed on the FEBs
  - natural ageing of electronic components
- New FEBs (FEB2s) will be designed with fully digital free running readout, i.e. avoiding trigger signal receivers and data buffering on the FEB
  - signals from all calorimeter cells are digitized at 40 MHz and sent off-detector

Phase II

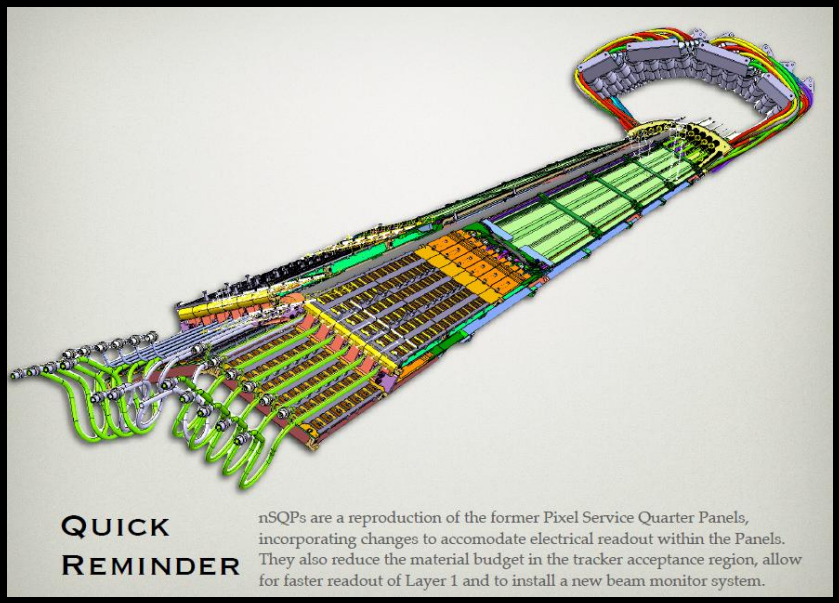
- The Phase I upgrade is compatible with the Phase II
- New FEB2s will be fitted in the existing Front End Crates and will use the same baseplanes built for Phase I:
  - Lar has already acquired all connectors needed for the FEB2s before they disappear from market
- Phase I LTDBs will also stay
  - Can be used to provide a low latency L0 trigger using the supercell granularity
- The full LAr calorimeter granularity will be available to the L1 trigger to further refine the trigger decision, possibly based on refined reconstruction in a region-of-interest determined by L0.





Milano interests for Phase II

- Continue involvement with power distribution architecture and with new front-end (for the current calo FE we have realized the preamps):
  - Powering distribution: power architecture with main converters and point-of-load converters (POL) close to the front-end
  - New Front-End: analog preamplification and shaping stages will be integrated in a single ASIC: Liquid Argon Preamp and Shaper (LAPAS)
    - Implementation of a wide dynamic range single ended preamp followed by low power differential shaping stages with multiple gains
    - SiGe technology (IBM, IHP)


QUICK
REMINDER
nSQPs are a reproduction of the former Pixel Service Quarter Panels, incorporating changes to accomodate electrical readout within the Panels. They also reduce the material budget in the tracker acceptance region, allow for faster readout of Layer 1 and to install a new beam monitor system.

IBL

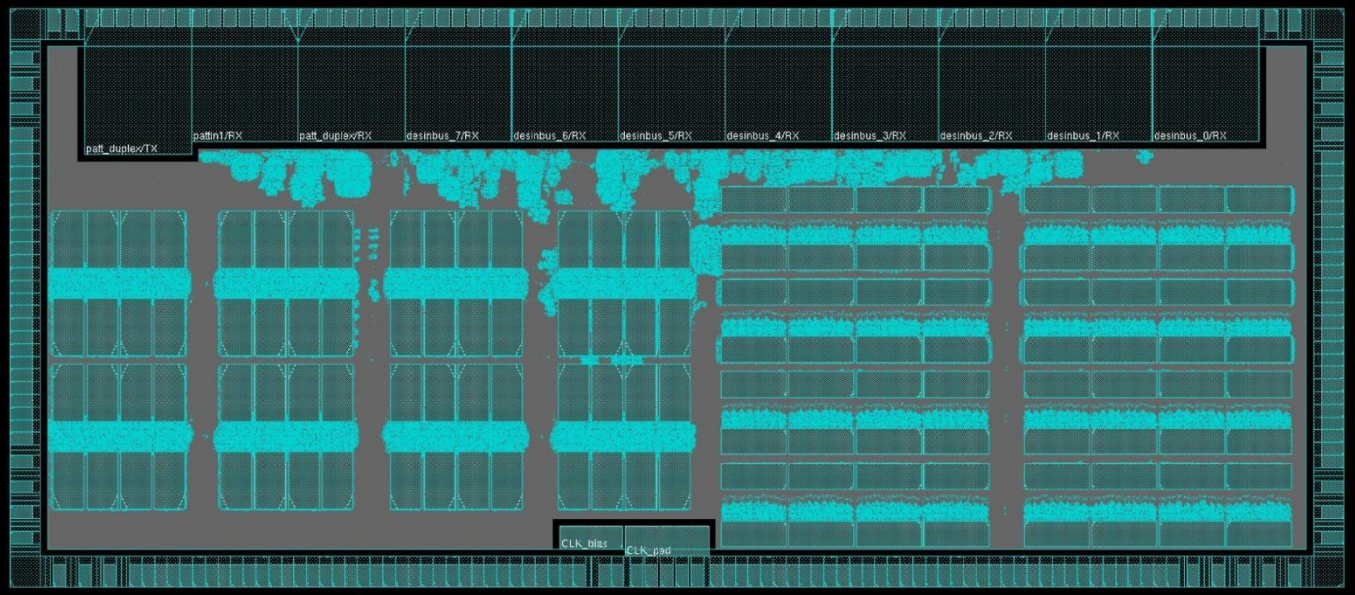
- Pixel is currently being disassembled inside the SR-1 radiation lab (Point 1):
  - All cables were disconnected from old service panels
  - All Service panels are removed
- Preparing for re-testing all non-functional modules inside the Pixel Detector
- remove the Beampipe support system
- Installation of the Inner Support Tube
  - Allows later insertion of IBL
  - Remounting of the Beampipe support system with new fixations
- Start of nSQP mounting

AMCHIP04 characterization

- Large number of exaustive characterization test demonstrate the **complete** functionality!
  - Development of a dedicated test system based on:
    - FPGA evaluation board used as a linux machine with the aim to generate stimuli and collect data
      - Linux driver
      - VHDL firmware
    - Daughter board with a compatible zero insertion force connector for the AMCHIP04

AMCHIP05mpw

- Large architecture (4k patterns)
  - multi-power supplies inside the core (1.2 V, 1.0 V, 0.7 V)
  - new low power cell working at 0.7 mV
    - power consumption minimization
- 23 x 23 Ball Grid Array (BGA) package



AMCHIP06

- Final Chip
  - It will be used for the final fabrication and installed in FTK
- 128 kpatterns
- Flip chip with the same BGA package used for the AMCHIP05mpw
- Reduce as much as possible power consumption

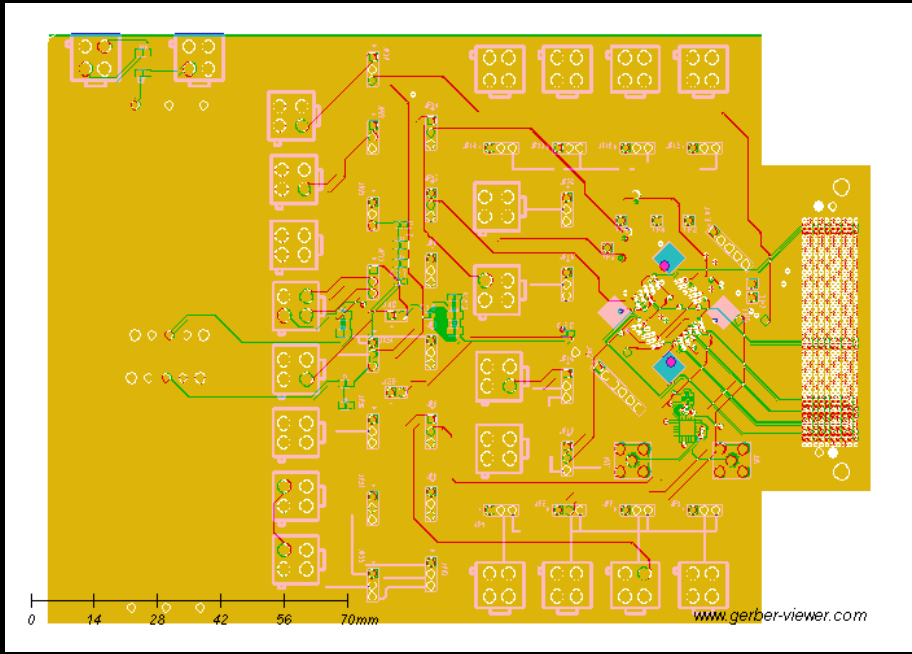
Power consumption trend

AMCHIP04	1.872 W
AMCHIP05miniasic (XORAM cells)	1.185 W
AMCHIP05mpw (700 mV cells)	0.836 W

PCB for the AMCHIP05miniasic test

Design completed

Test planned for July 2013



Upgrades (LAr)

- IDR now passed, endorsed at CB 8.Feb.2013
- TDR is next milestone:
  - Draft 0.1 by end June, after baseline decisions in June LAr week
  - End July: finish technical chapters
  - Motivations and Physics studies August
  - Final revision 1-7th September
- Converging on key choices and a way to progress in design
  - FE and BE groups in full function
  - Lots of progress on FE, ASICs, BE, Links….
  - Finalize Demonstrator design in next months. Produce 2-3 units
- System tests being prepared
  - Agreed to hold an ATLAS review before the installation of Demonstrator

- Purposes:
  - maintain high efficiency for Level-1 triggering on low P_T objects (electrons and photons)
  - Improve jet, tau, MET triggers
  - Enable lower thresholds for multi-object triggers
  - Give more flexibility in trigger menu design and in operations
- In the LAr calorimeter this implies changes to the front-end electronics to allow greater granularity to be exploited at Level-1
  - finer segmentation in eta
  - depth information
- Enable use of more powerful LVL2 /offline-like variables/ techniques in the L1Calo selection:
  - Shower shapes

Upgrades (AFP)

#	Project	Letter of Intent presented and approved by LHCC	Initial Design Review	Kick-off meeting	CB approval	TDR due	LHCC Session	I-MOU needed	MOU-due for signature (RRB)
1	FTK	21-Mar-12	2-Dec-10	3-Dec-10	24-Jun-11	30-Apr-13	11-Jun-13	yes	15-Oct-13
2	nSW	21-Mar-12	29-Aug-12	31-Aug-12	5-Oct-12	31-May-13	11-Jun-13	not clear	15-Oct-13
3	LAr	21-Mar-12	9-Jan-13	11-Jan-13	8-Feb-13	15-Sep-13	24-Sep-13	not clear	15-Oct-13
4	TDAQ	21-Mar-12	21-Jan-13	23-Jan-13	8-Feb-13	15-Sep-13	24-Sep-13	not clear	15-Oct-13
5	AFP	21-Mar-12	17-Sep-12	19-Sep-12	2014	2014	2014	yes	14-Oct-14

- The detector baseline will be decided before the next ATLASWEEK
- The group aims to be prepared for a review on the low/medium luminosity physics program latest for this Summer
- Test Beam for validating the Timing+Tracker combination is planned for Spring 2014

Phase II (ITK)

- Work going on in a number of directions to develop baseline layout beyond what was presented in the LoI
  - Adding realism
  - Bringing software description of sensor and structural elements closer to what is actually envisaged
  - Debugging and optimising performance
- Framework changes can also help development of new (and existing) alternatives
  - For software changes relating to ITK, aim should be more towards 'generalised' than 'specialised' – ie avoid (and try to remove existing) use of 'special cases' or hard-coded assumptions
- Alternative layouts being studied with various tools, at various levels of detail
  - Alpine layout, not mentioned here, also of great interest
  - Establish which ones are worth taking forward for further study
  - Likely that baseline will evolve by time of TDR – studying this at level of detail required for TDR will take a lot of time and effort, therefore decision needs to be made sufficiently early for this work to be done

Phase II (LAr)

- *LAr will need to upgrade the read-out electronics for Phase-II*
  - *new LAr front-end electronics*
  - *new LAr back-end electronics*
  - *new HEC power supplies*
- In addition, a LAr detector upgrade in the endcap region may be required:
  - replacement of HEC cold electronics
  - new sFCal or additional MiniFCal detector in front of current FCal

Phase II (Lar)

- LAr has developed four options to progress towards a decision whether to open or not the cryostat:
- **Option 0: No change neither of the HEC cold electronics nor of the FCal detectors.**
- **Option 1: If the HEC cold electronics have to be replaced, the large cold cryostat cover would have to be opened and the irradiated FCal would have to be removed. A newly built cold FCal (sFCal) would then be inserted before closing the cryostat.**
- **Option 2: If the HEC cold electronics do not have to be replaced, the cold FCal would be replaced by a new one of the sFCal type. It is anticipated that only the small cover of the cold vessel, the FCal bulkhead, would have to be removed.**
- **Option 3: If the HEC cold electronics do not have to be replaced, the cold FCal would stay in place and a new small calorimeter (Mini-FCal) would be placed in front of it. In this case only the cryostat warm vessel would have to be opened.**