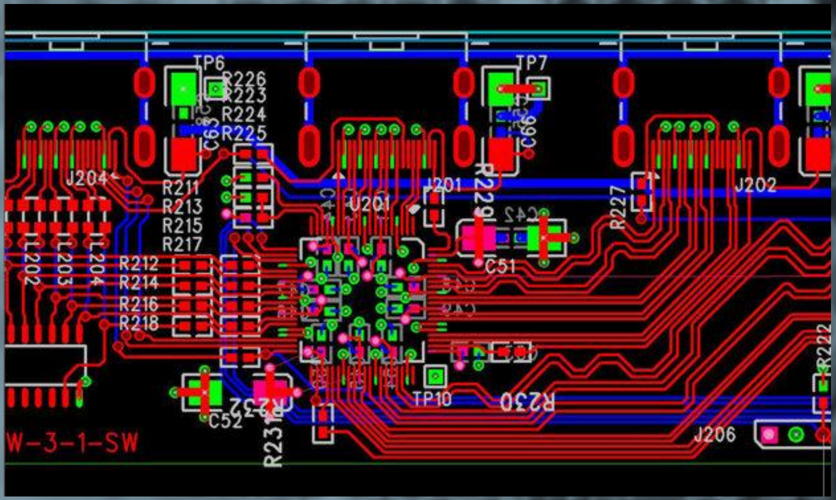
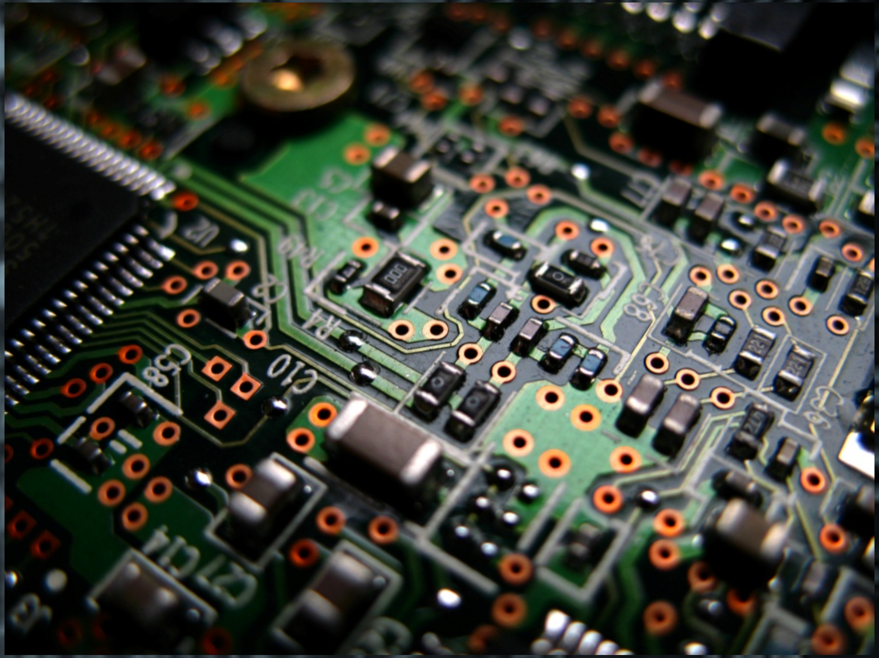
Attività del Laboratorio di Elettronica


TP6
R226
R223
R224
R225
C63
TP7
C66
J204
R211
R213
R215
R217
U201
J201
R229
C42
R227
J202
L202
L203
L204
R212
R214
R216
R218
C51
C52
R232
R231
TP10
R230
R222
J206
W-3-1-SW


C58
C10
R1
C14

Esperimenti in cui è coinvolto il Laboratorio di Elettronica

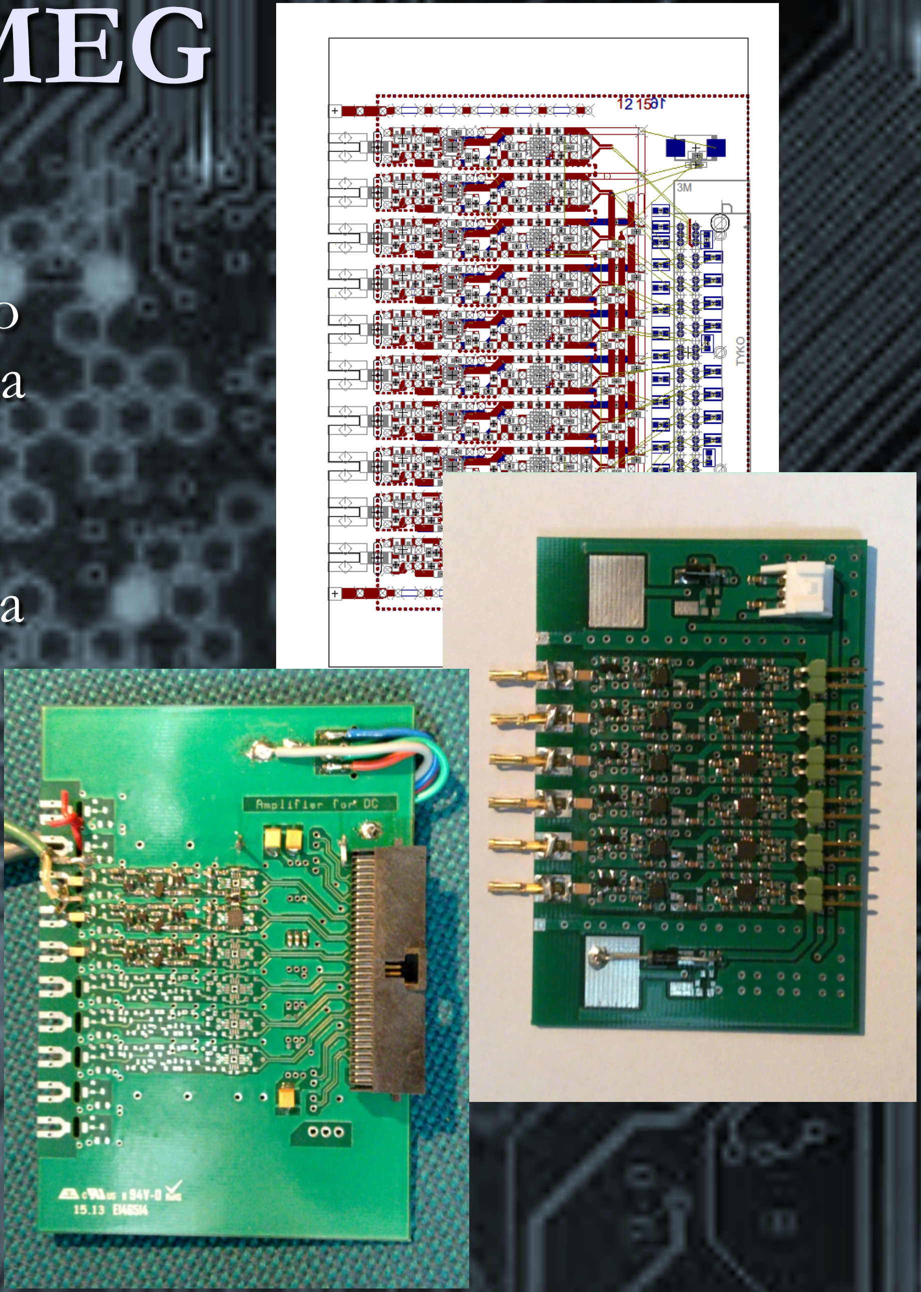
- **Esperimento MEG:** Ricerca del decadimento $\mu \rightarrow e + \gamma$, non previsto dal modello standard delle particelle elementari presso il Paul Scherrer Institut di Zurigo (Svizzera).
- **Esperimento CLUCOU/CLUTIM/MU2E:** Definizione di un modello di cella di drift e della sua elettronica di lettura per l'ottimizzazione delle risoluzioni spaziali e della misura di dE/dx in un rivelatore di particelle ionizzanti.
- **Esperimento AUGER:** Studio dei raggi cosmici di altissima energia presso Malargue (Argentina).
- **Esperimento EEE:** Sviluppo di una rete in Italia per la rivelazione di raggi cosmici di elevata energia in collaborazione con le Scuole secondarie di secondo grado.

Esperimenti in cui è coinvolto il Laboratorio di Elettronica

- **Esperimento AMY:** Misura e caratterizzazione dell'emissione di microonde (1-25 GHz) da parte del plasma creato da sciami atmosferici. Le misure sono state effettuate alla Beam Test Facility (BTF) dei Laboratori Nazionali di Frascati
- **Esperimento CORAM:** Realizzazione di un esperimento simile a quelli di **G. Pfotzer** utilizzando un setup sperimentale sufficientemente semplice ma al tempo stesso in grado di fornire diversi tipi di informazione, variando la soglia di energia minima delle particelle considerate e il range angolare considerato.
- **Esperimento CosMic:** Rivelazione dei raggi cosmici nelle microonde tramite un self-triggering radiotelescopio nella banda di alcuni GHz
- **Esperimento DIAPIX:** Realizzazione di un rivelatore a pixel ibrido di diamante policristallino prodotto per Chemical Vapor Deposition (CVD) ultra resistente alla radiazione.

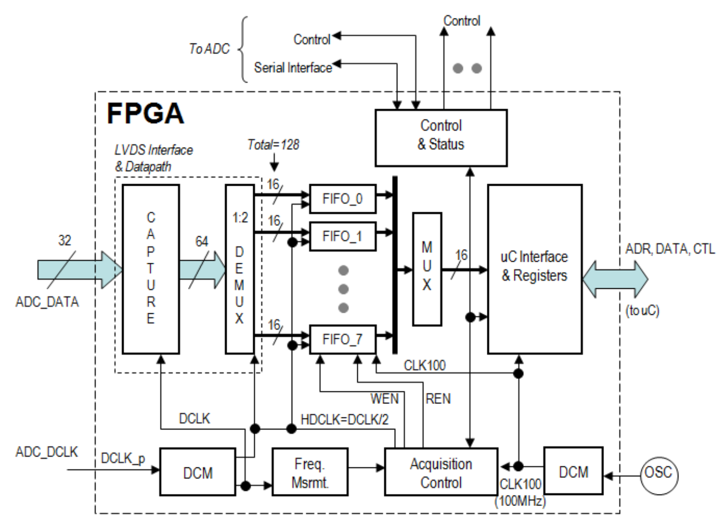
Esperimento MEG

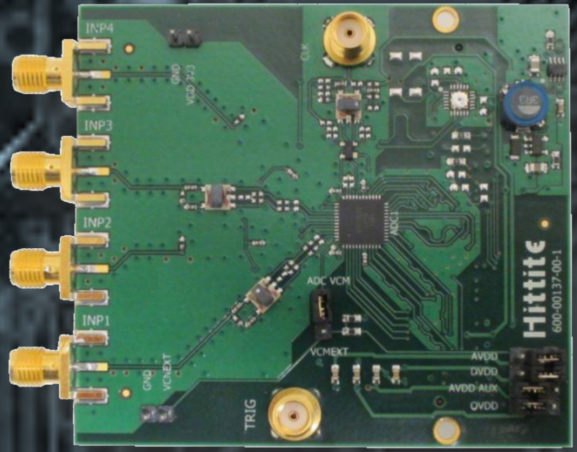
- Sviluppo del Front End con caratteristi che di basso rumore ed elevata larghezza di banda passante.
- Supporto per la messa a punto del sistema di filatura della nuova camera a fili.



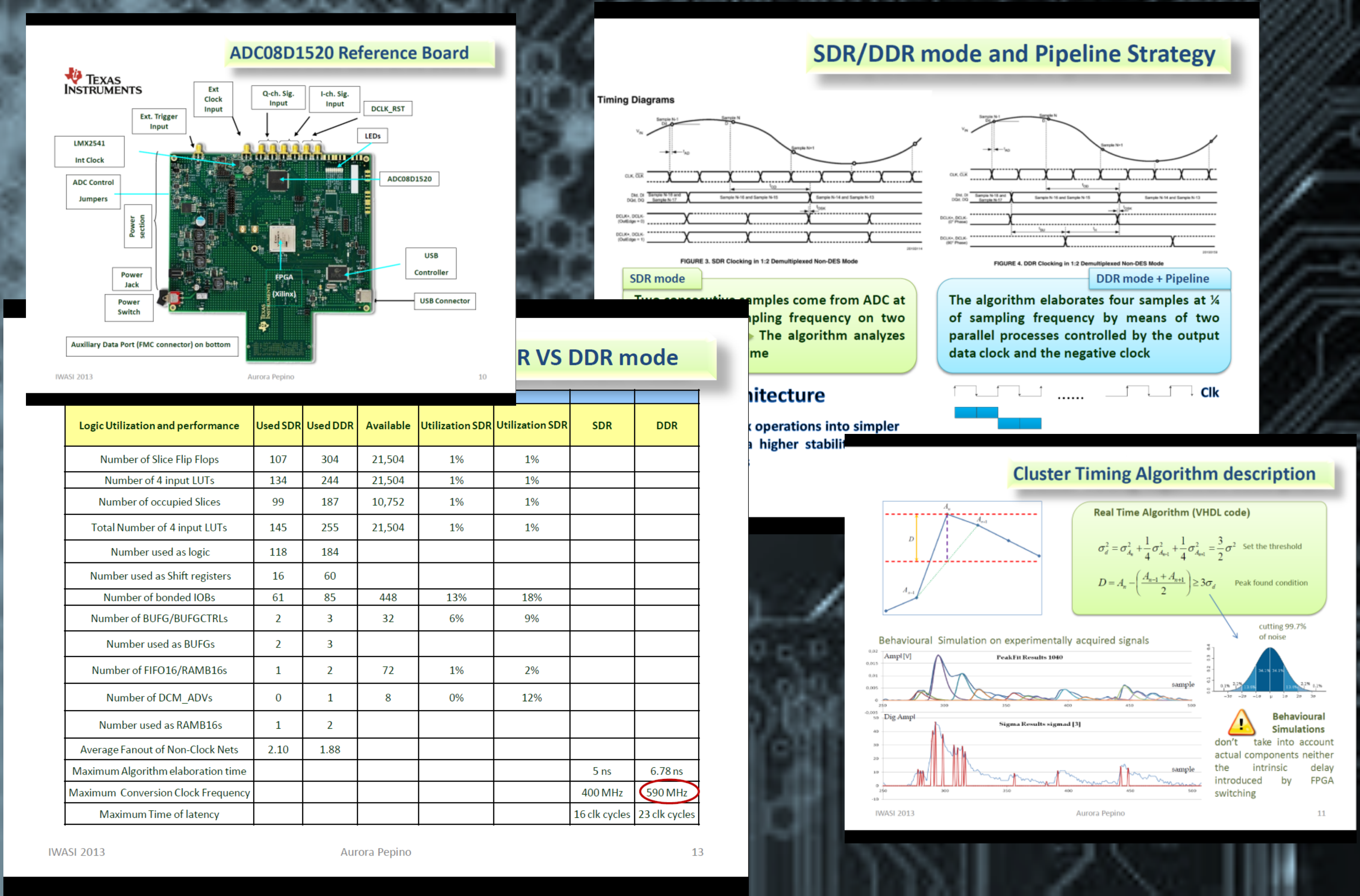
Esperimento CLUCOU/CLUTIM/MU2E

- Utilizzo di sistemi con ADC commerciali per la verifica dell'algoritmo di ricerca dei picchi implementato in FPGA.


To ADC
Control
Serial Interface
Control
FPGA
Control & Status
LVDS Interface & Datapath
Total=128
16
16
16
CAPTURE
1:2
DEMUX
FIFO_0
FIFO_1
FIFO_7
MUX
16
uC Interface & Registers
ADR, DATA, CTL
(to uC)
32
ADC_DATA
64
CLK100
WEN
REN
DCLK
HDCLK=DCLK/2
ADC_DCLK
DCLK_p
DCM
Freq. Msrmt.
Acquisition Control
CLK100 (100MHz)
DCM
OSC


INP4
INP3
INP2
INP1
TRIG
CLK
ADC VCM
VCMEXT
AVDD
DVDD
AVDD AUX
OVDD
Hittite
600-00137-00-1

Esperimento CLUCOU/CLUTIM/MU2E



ADC08D1520 Reference Board

Texas Instruments
Ext. Trigger Input
Ext Clock Input
Q-ch. Sig. Input
I-ch. Sig. Input
DCLK_RST
LEDs
LMX2541 Int Clock
ADC Control Jumpers
ADC08D1520
Power section
FPGA (Xilinx)
USB Controller
Power Jack
Power Switch
USB Connector
Auxiliary Data Port (FMC connector) on bottom

IWASI 2013 Aurora Pepino 10

SDR/DDR mode and Pipeline Strategy

Timing Diagrams

FIGURE 3. SDR Clocking in 1:2 Demultiplexed Non-DES Mode

FIGURE 4. DDR Clocking in 1:2 Demultiplexed Non-DES Mode

SDR mode

Two consecutive samples come from ADC at …pling frequency on two … The algorithm analyzes …me

DDR mode + Pipeline

The algorithm elaborates four samples at ¼ of sampling frequency by means of two parallel processes controlled by the output data clock and the negative clock

…itecture

…operations into simpler …a higher stabilit…

…R VS DDR mode

Logic Utilization and performance	Used SDR	Used DDR	Available	Utilization SDR	Utilization SDR	SDR	DDR
Number of Slice Flip Flops	107	304	21,504	1%	1%		
Number of 4 input LUTs	134	244	21,504	1%	1%		
Number of occupied Slices	99	187	10,752	1%	1%		
Total Number of 4 input LUTs	145	255	21,504	1%	1%		
Number used as logic	118	184					
Number used as Shift registers	16	60					
Number of bonded IOBs	61	85	448	13%	18%		
Number of BUFG/BUFGCTRLs	2	3	32	6%	9%		
Number used as BUFGs	2	3					
Number of FIFO16/RAMB16s	1	2	72	1%	2%		
Number of DCM_ADVs	0	1	8	0%	12%		
Number used as RAMB16s	1	2					
Average Fanout of Non-Clock Nets	2.10	1.88					
Maximum Algorithm elaboration time						5 ns	6.78 ns
Maximum Conversion Clock Frequency						400 MHz	590 MHz
Maximum Time of latency						16 clk cycles	23 clk cycles

IWASI 2013 Aurora Pepino 13

Cluster Timing Algorithm description

Real Time Algorithm (VHDL code)

$$\sigma_d^2 = \sigma_{A_n}^2 + \frac{1}{4}\sigma_{A_{n-1}}^2 + \frac{1}{4}\sigma_{A_{n+1}}^2 = \frac{3}{2}\sigma^2$$ Set the threshold

$$D = A_n - \left(\frac{A_{n-1} + A_{n+1}}{2}\right) \geq 3\sigma_d$$ Peak found condition

cutting 99.7% of noise

Behavioural Simulation on experimentally acquired signals

Ampl [V]
PeakFit Results 1040
sample
Dig Ampl
Sigma Results sigmad [3]
sample
34.1% 34.1%
13.6% 13.6%
2.1% 2.1%
0.1% 0.1%

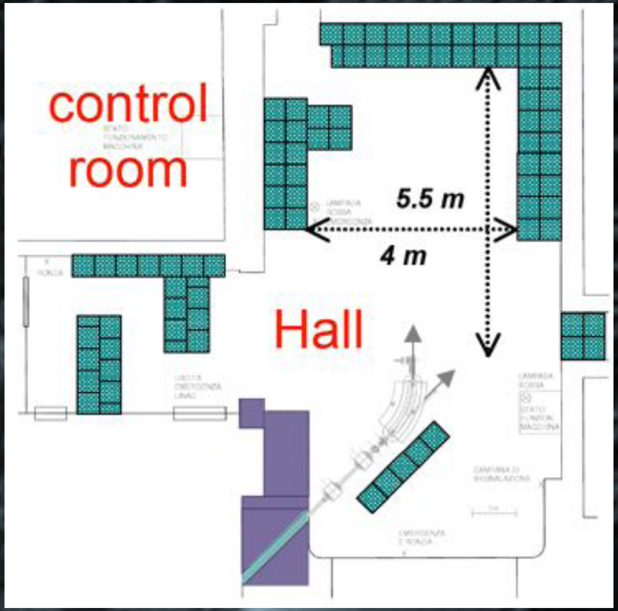
Behavioural Simulations don't take into account actual components neither the intrinsic delay introduced by FPGA switching

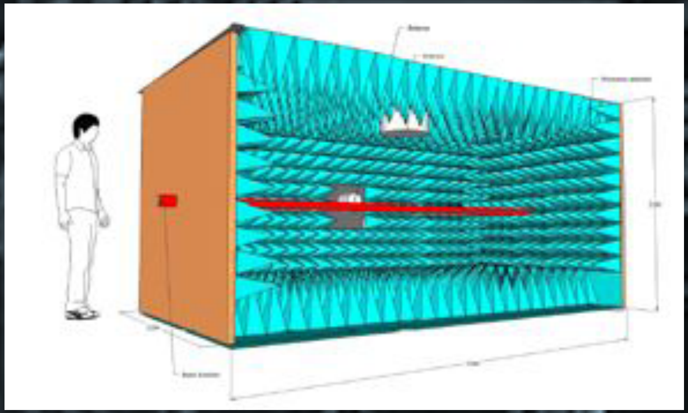
IWASI 2013 Aurora Pepino 11

Esperimento AMY

- Messa a punto del setup da utilizzare per l’acquisizione dati realizzata tramite oscilloscopio LeCroy Wave Master nei test beam effettuati presso la BTF dei Laboratori Nazionali di Frascati.

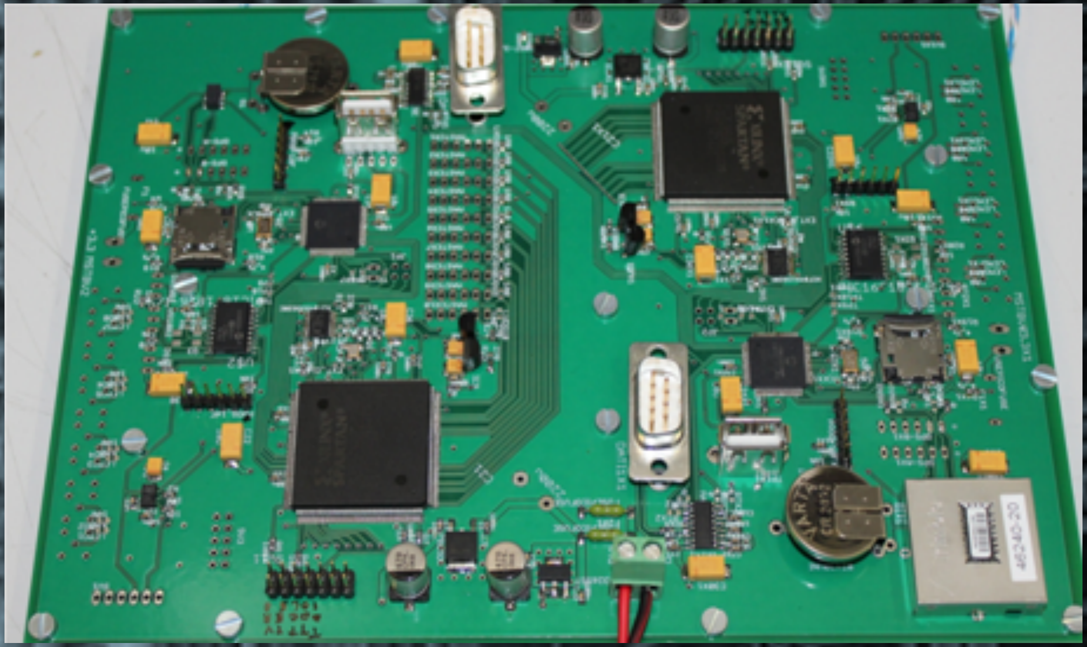
be mechanicall
R&S*AC090 to
systems.


control room
STATO FUNZIONAMENTO MACCHINA
LAMPADA ROSSA
5.5 m
4 m
Hall
LAMPADA ROSSA
CAMPANA DI SEGNALAZIONE



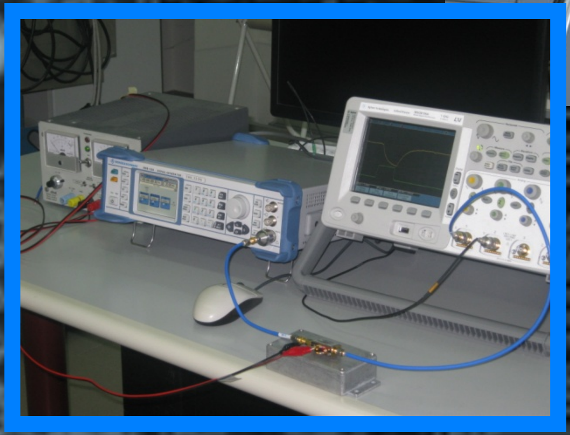
Esperimento CORAM

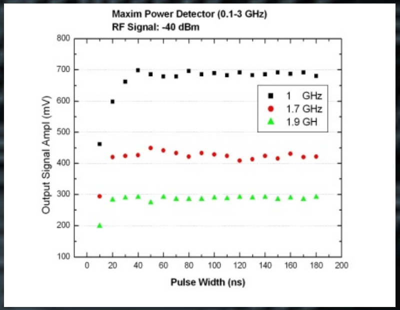
- Realizzazione del sistema di acquisizione basato su FPGA Xilinx Spartan 3E 500K che comunica con un µC (PIC 18F87J50) che raccoglie anche i dati provenienti da un modulo GPS (timestamps)



Esperimento CosMic

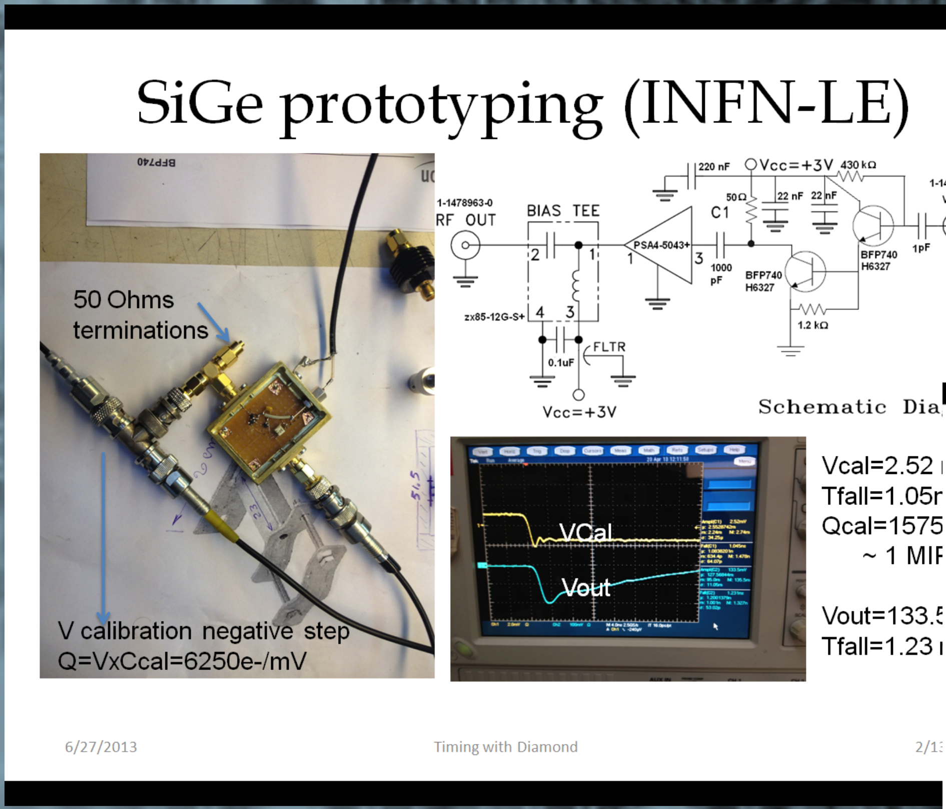
- Costruzione di un prototipo di Power detector basato sul Maxim MAX 2015 EUA
- Acquisiti tutti i Power Detector e pronti per la realizzazione della scheda finale che li alloggia.





Esperimento DIAPIX

Realizzazione di un prototipo di Amplificatore a basso rumore (Carlo Pinto)



SiGe prototyping (INFN-LE)

50 Ohms terminations

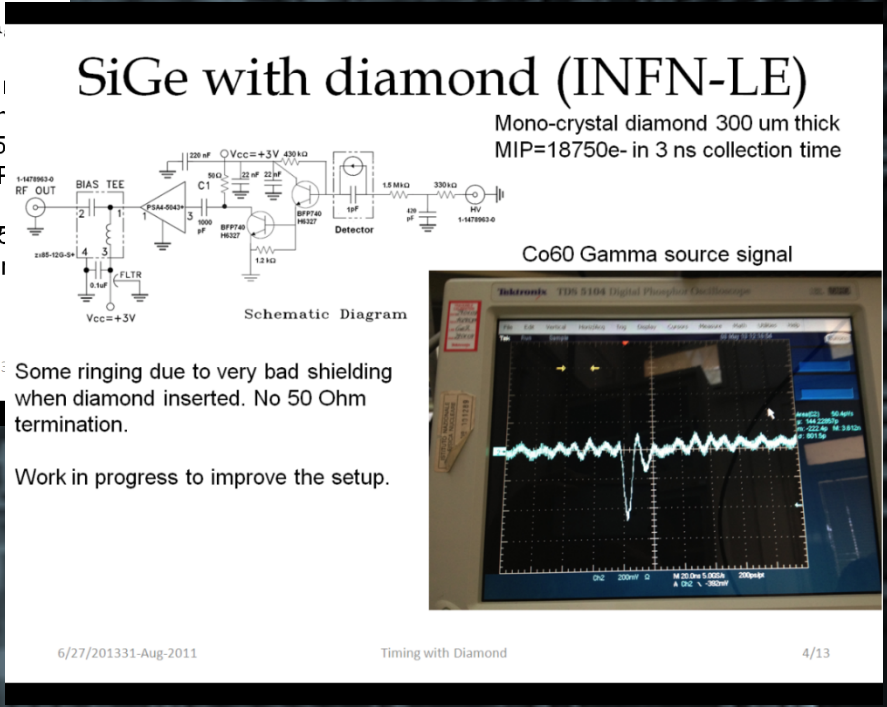
V calibration negative step
Q=VxCcal=6250e-/mV

1-1478963-0
RF OUT
BIAS TEE
2
1
4
3
zx85-12G-S+
0.1uF
FLTR
Vcc=+3V
PSA4-5043+
1
3
C1
1000 pF
220 nF
Vcc=+3V
430 kΩ
50Ω
22 nF
22 nF
BFP740 H6327
BFP740 H6327
1.2 kΩ
1pF
1-1478963-0
Vpulse
Schematic Dia
VCal
Vout

Vcal=2.52
Tfall=1.05
Qcal=1575
~ 1 MI

Vout=133.
Tfall=1.23

6/27/2013 Timing with Diamond 2/1



SiGe with diamond (INFN-LE)

Mono-crystal diamond 300 um thick
MIP=18750e- in 3 ns collection time

1-1478963-0
RF OUT
BIAS TEE
2
1
4
3
zx85-12G-S+
0.1uF
FLTR
Vcc=+3V
PSA4-5043+
1
3
C1
1000 pF
220 nF
Vcc=+3V
430 kΩ
50Ω
22 nF
22 nF
BFP740 H6327
BFP740 H6327
1.2 kΩ
1pF
Detector
1.5 MkΩ
330 kΩ
420 pF
HV
1-1478963-0
Schematic Diagram
Tektronix TDS 5104 Digital Phosphor Oscilloscope

Co60 Gamma source signal

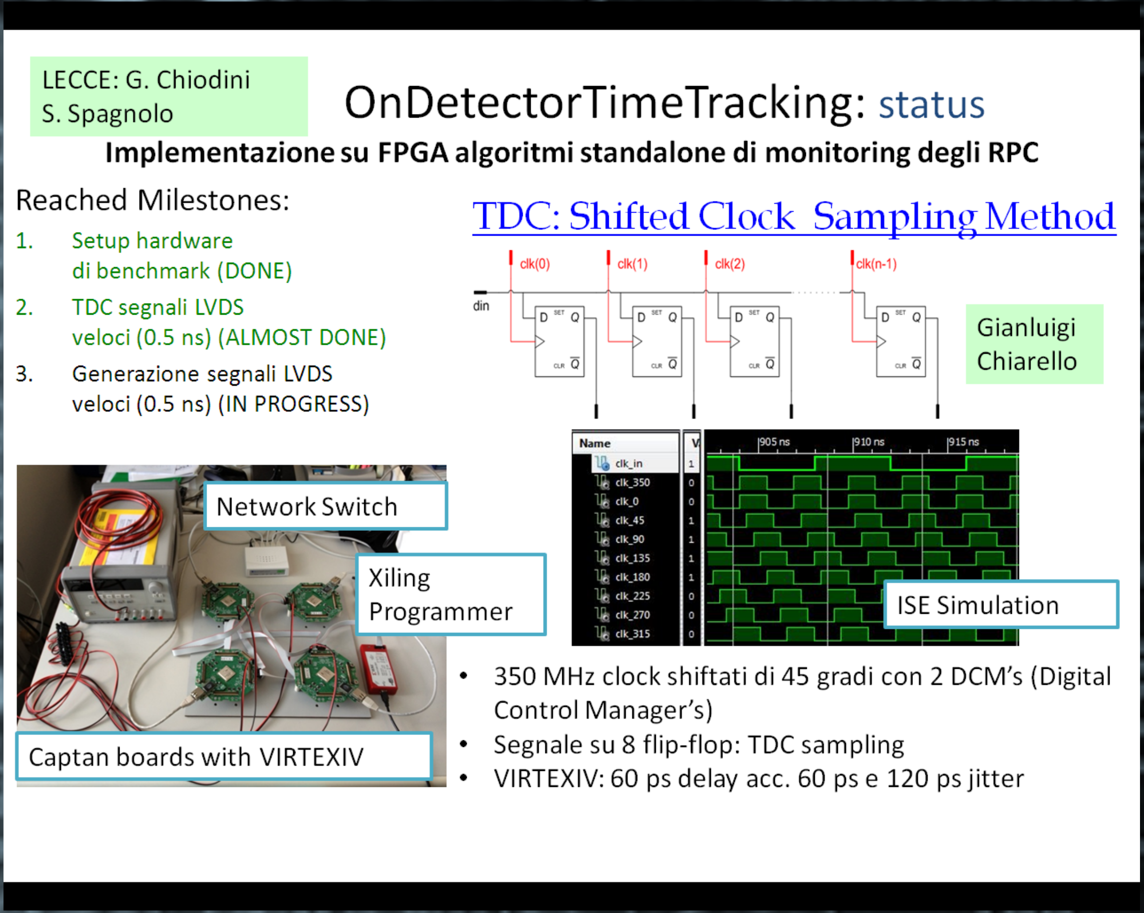
Some ringing due to very bad shielding when diamond inserted. No 50 Ohm termination.

Work in progress to improve the setup.

6/27/201331-Aug-2011 Timing with Diamond 4/13

Esperimento Atlas (RPC)

- Implementazione su FPGA Virtex di un TDC con tecniche di sfasamento di clock


clk(0)
clk(1)
clk(2)
clk(n-1)
din
D
SET
Q
CLR
$\overline{Q}$
Name
V
clk_in
clk_350
clk_0
clk_45
clk_90
clk_135
clk_180
clk_225
clk_270
clk_315
905 ns
910 ns
915 ns

LECCE: G. Chiodini
S. Spagnolo

OnDetectorTimeTracking: status

Implementazione su FPGA algoritmi standalone di monitoring degli RPC

Reached Milestones:

1. Setup hardware di benchmark (DONE)
2. TDC segnali LVDS veloci (0.5 ns) (ALMOST DONE)
3. Generazione segnali LVDS veloci (0.5 ns) (IN PROGRESS)

TDC: Shifted Clock Sampling Method

Gianluigi Chiarello

Network Switch

Xiling Programmer

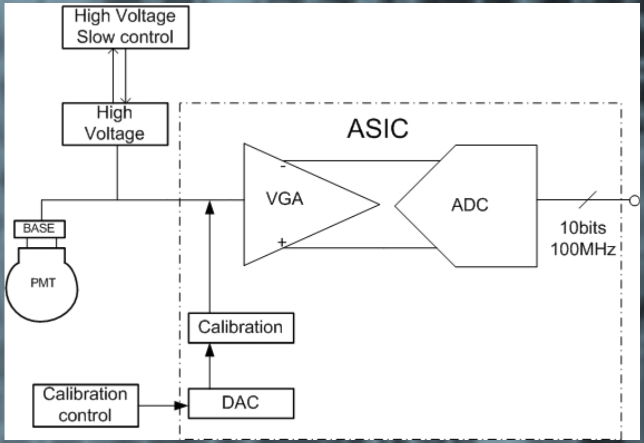
Captan boards with VIRTEXIV

ISE Simulation

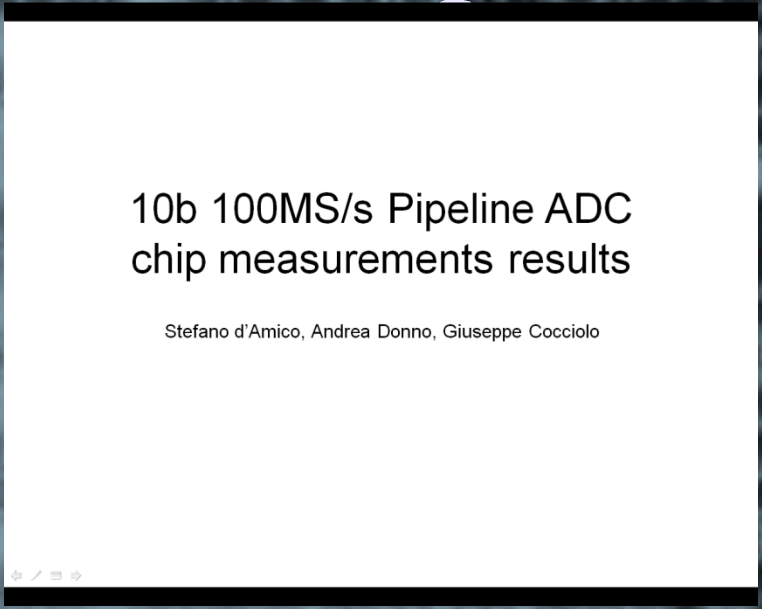
- 350 MHz clock shiftati di 45 gradi con 2 DCM’s (Digital Control Manager’s)
- Segnale su 8 flip-flop: TDC sampling
- VIRTEXIV: 60 ps delay acc. 60 ps e 120 ps jitter

Esperimento AUGER

- Sviluppo di un circuito integrato (Flash ADC a 10 bit) per l’acquisizione del segnale dal rivelatore di superficie dell’esperimento.

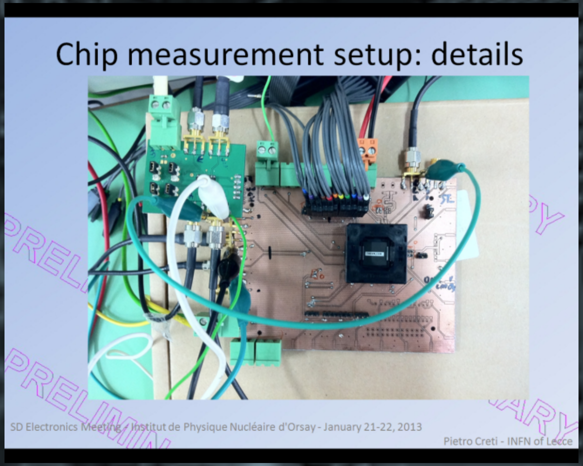

High Voltage
Slow control
High
Voltage
ASIC
VGA
-
+
ADC
10bits
100MHz
BASE
PMT
Calibration
Calibration
control
DAC

Esperimento AUGER



10b 100MS/s Pipeline ADC
chip measurements results

Stefano d'Amico, Andrea Donno, Giuseppe Cocciolo

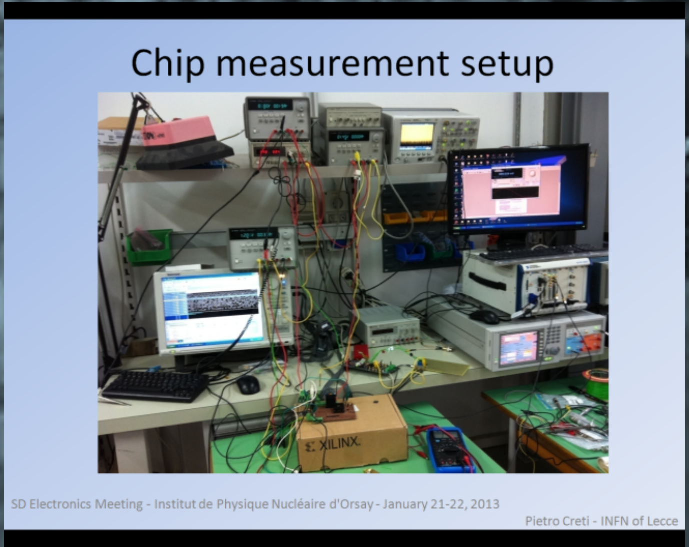


Chip measurement setup: details

PRELIMINARY

SD Electronics Meeting - Institut de Physique Nucléaire d'Orsay - January 21-22, 2013

Pietro Creti - INFN of Lecce

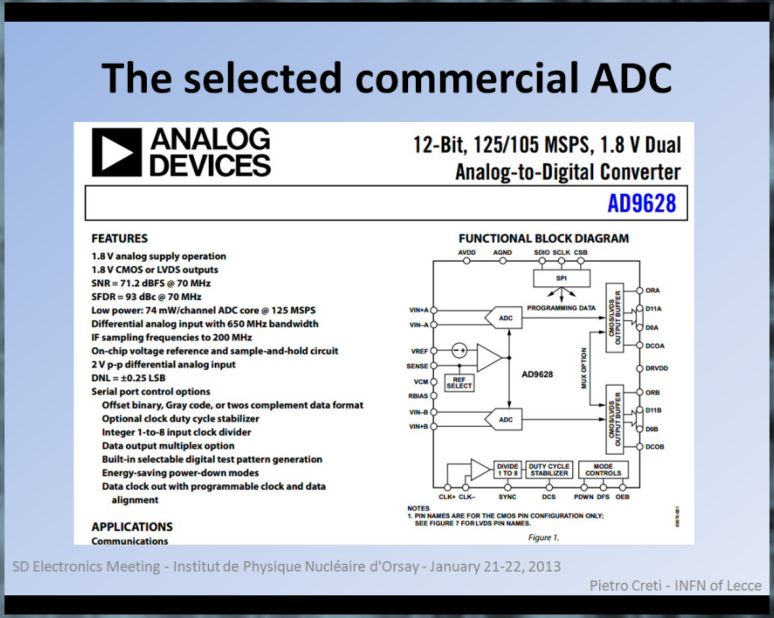


Chip measurement setup

SD Electronics Meeting - Institut de Physique Nucléaire d'Orsay - January 21-22, 2013

Pietro Creti - INFN of Lecce

Esperimento AUGER



The selected commercial ADC

ANALOG DEVICES

12-Bit, 125/105 MSPS, 1.8 V Dual
Analog-to-Digital Converter

AD9628

FEATURES

- 1.8 V analog supply operation
- 1.8 V CMOS or LVDS outputs
- SNR = 71.2 dBFS @ 70 MHz
- SFDR = 93 dBc @ 70 MHz
- Low power: 74 mW/channel ADC core @ 125 MSPS
- Differential analog input with 650 MHz bandwidth
- IF sampling frequencies to 200 MHz
- On-chip voltage reference and sample-and-hold circuit
- 2 V p-p differential analog input
- DNL = ±0.25 LSB
- Serial port control options
  - Offset binary, Gray code, or twos complement data format
  - Optional clock duty cycle stabilizer
  - Integer 1-to-8 input clock divider
  - Data output multiplex option
  - Built-in selectable digital test pattern generation
  - Energy-saving power-down modes
  - Data clock out with programmable clock and data alignment

APPLICATIONS

Communications

FUNCTIONAL BLOCK DIAGRAM

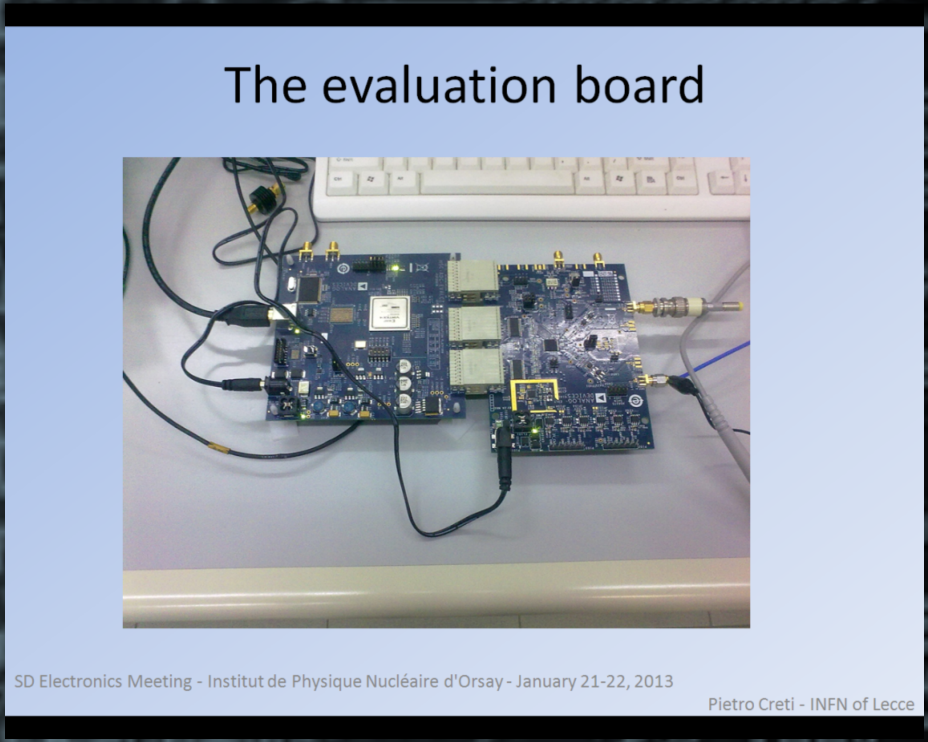
AVDD
AGND
SDIO
SCLK
CSB
SPI
PROGRAMMING DATA
VIN+A
VIN–A
ADC
VREF
SENSE
VCM
RBIAS
VIN–B
VIN+B
REF SELECT
AD9628
MUX OPTION
CMOS/LVDS OUTPUT BUFFER
ORA
D11A
D0A
DCOA
DRVDD
ORB
D11B
D0B
DCOB
DIVIDE 1 TO 8
DUTY CYCLE STABILIZER
MODE CONTROLS
CLK+
CLK–
SYNC
DCS
PDWN
DFS
OEB

NOTES
1. PIN NAMES ARE FOR THE CMOS PIN CONFIGURATION ONLY; SEE FIGURE 7 FOR LVDS PIN NAMES.

Figure 1.

SD Electronics Meeting - Institut de Physique Nucléaire d'Orsay - January 21-22, 2013

Pietro Creti - INFN of Lecce



The evaluation board

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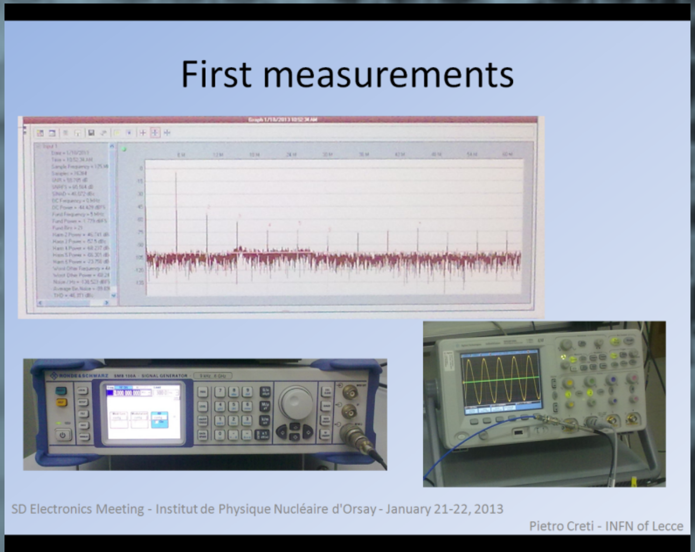


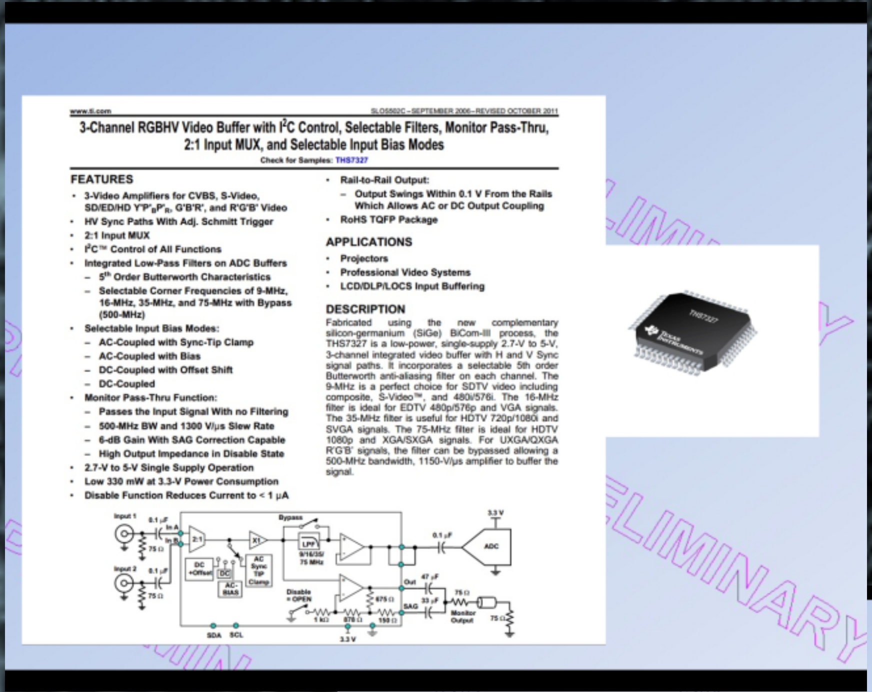
First measurements

SD Electronics Meeting - Institut de Physique Nucléaire d'Orsay - January 21-22, 2013

Pietro Creti - INFN of Lecce

Esperimento AUGER

- Front End Upgrade: Very low noise Splitter with 2 channel per each PMT , 60 MHz 6° order Bessel Filter and 15 bit dynamic range.



www.ti.com SLOS502C – SEPTEMBER 2006 – REVISED OCTOBER 2011

3-Channel RGBHV Video Buffer with I²C Control, Selectable Filters, Monitor Pass-Thru, 2:1 Input MUX, and Selectable Input Bias Modes

Check for Samples: THS7327

FEATURES

- 3-Video Amplifiers for CVBS, S-Video, SD/ED/HD Y'P'$_B$P'$_R$, G'B'R', and R'G'B' Video
- HV Sync Paths With Adj. Schmitt Trigger
- 2:1 Input MUX
- I²C™ Control of All Functions
- Integrated Low-Pass Filters on ADC Buffers
  - 5th Order Butterworth Characteristics
  - Selectable Corner Frequencies of 9-MHz, 16-MHz, 35-MHz, and 75-MHz with Bypass (500-MHz)
- Selectable Input Bias Modes:
  - AC-Coupled with Sync-Tip Clamp
  - AC-Coupled with Bias
  - DC-Coupled with Offset Shift
  - DC-Coupled
- Monitor Pass-Thru Function:
  - Passes the Input Signal With no Filtering
  - 500-MHz BW and 1300 V/µs Slew Rate
  - 6-dB Gain With SAG Correction Capable
  - High Output Impedance in Disable State
- 2.7-V to 5-V Single Supply Operation
- Low 330 mW at 3.3-V Power Consumption
- Disable Function Reduces Current to < 1 µA
- Rail-to-Rail Output:
  - Output Swings Within 0.1 V From the Rails Which Allows AC or DC Output Coupling
- RoHS TQFP Package

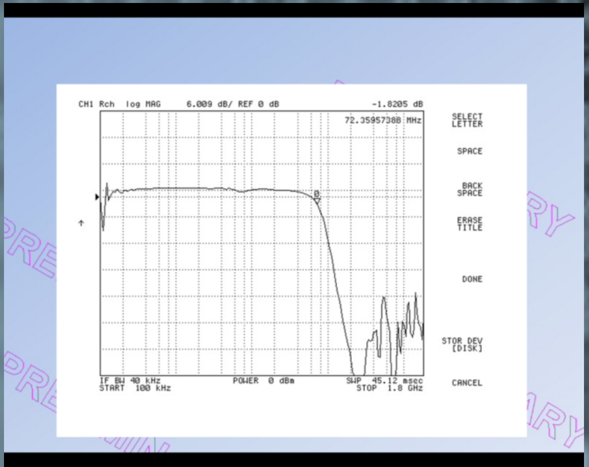
APPLICATIONS

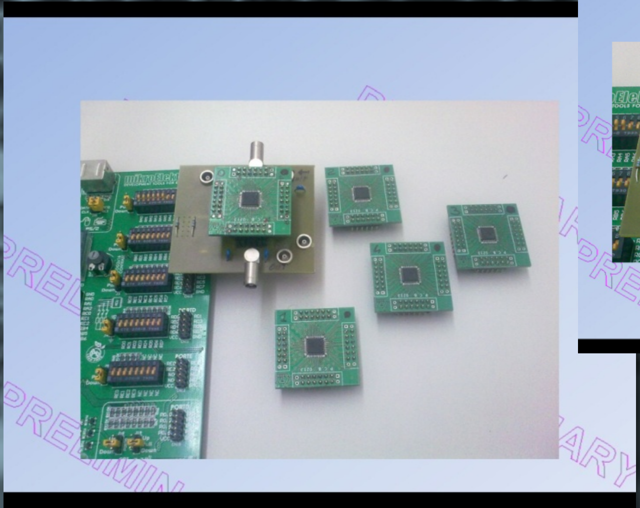
- Projectors
- Professional Video Systems
- LCD/DLP/LOCS Input Buffering

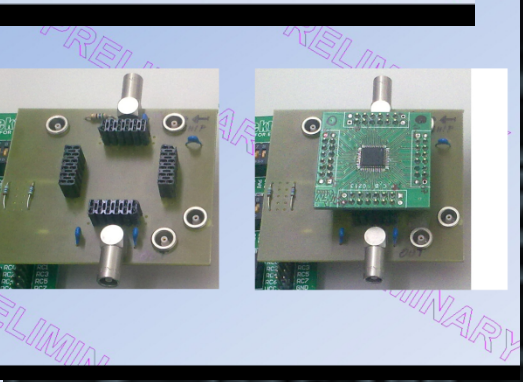
DESCRIPTION

Fabricated using the new complementary silicon-germanium (SiGe) BiCom-III process, the THS7327 is a low-power, single-supply 2.7-V to 5-V, 3-channel integrated video buffer with H and V Sync signal paths. It incorporates a selectable 5th order Butterworth anti-aliasing filter on each channel. The 9-MHz is a perfect choice for SDTV video including composite, S-Video™, and 480i/576i. The 16-MHz filter is ideal for EDTV 480p/576p and VGA signals. The 35-MHz filter is useful for HDTV 720p/1080i and SVGA signals. The 75-MHz filter is ideal for HDTV 1080p and XGA/SXGA signals. For UXGA/QXGA R'G'B' signals, the filter can be bypassed allowing a 500-MHz bandwidth, 1150-V/µs amplifier to buffer the signal.

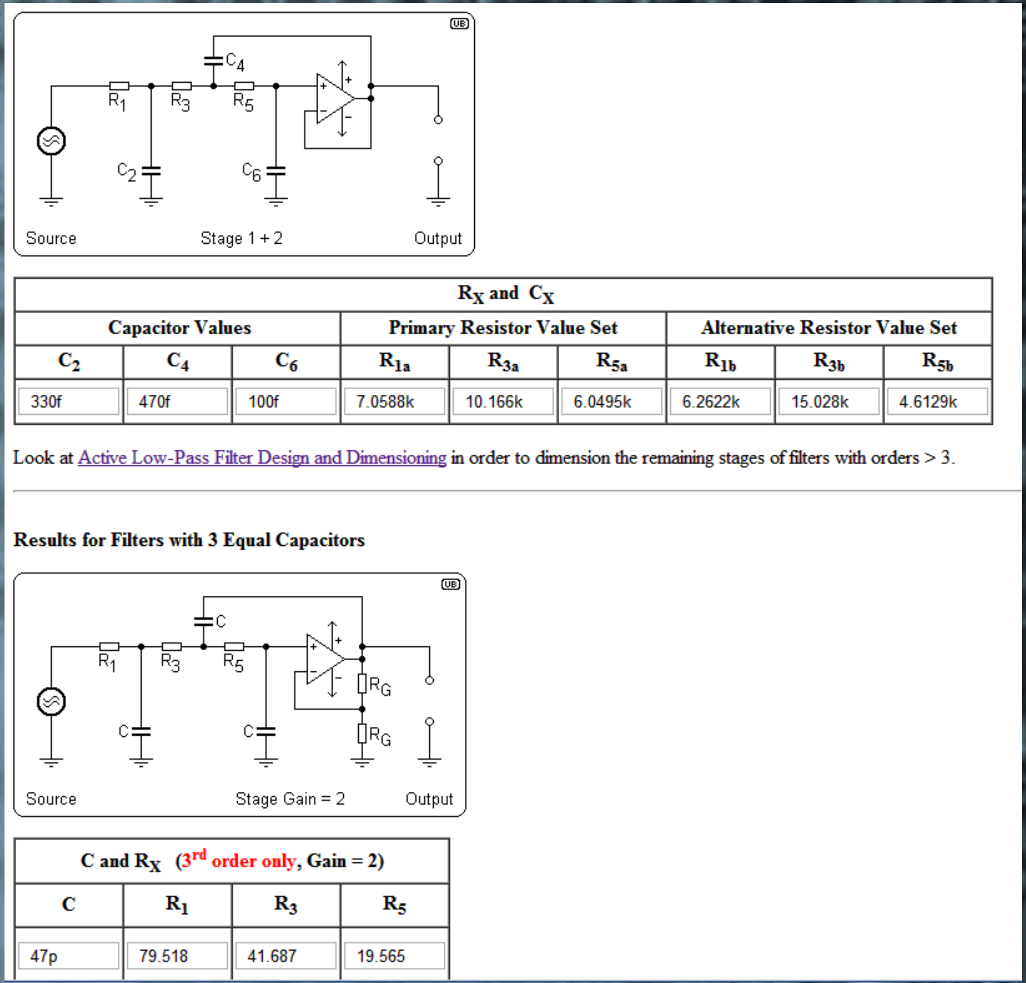
PRELIMINARY







Esperimento AUGER

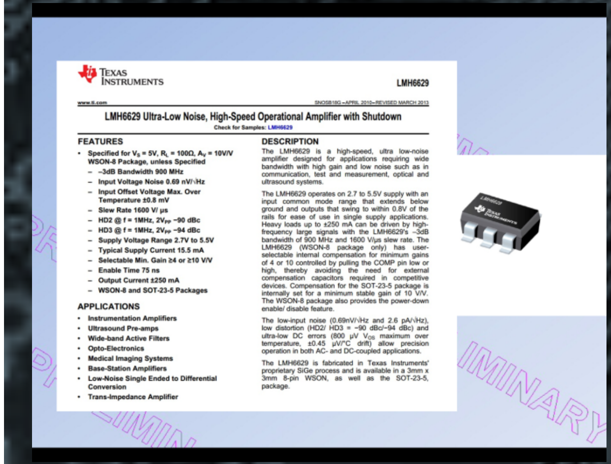


R_X and C_X								
Capacitor Values			**Primary Resistor Value Set**			**Alternative Resistor Value Set**		
C_2	C_4	C_6	R_{1a}	R_{3a}	R_{5a}	R_{1b}	R_{3b}	R_{5b}
330f	470f	100f	7.0588k	10.166k	6.0495k	6.2622k	15.028k	4.6129k

Look at Active Low-Pass Filter Design and Dimensioning in order to dimension the remaining stages of filters with orders > 3.

Results for Filters with 3 Equal Capacitors

C and R_X (3^{rd} order only, Gain = 2)			
C	R_1	R_3	R_5
47p	79.518	41.687	19.565



TEXAS INSTRUMENTS

LMH6629

www.ti.com

SNOSB18G – APRIL 2010 – REVISED MARCH 2013

LMH6629 Ultra-Low Noise, High-Speed Operational Amplifier with Shutdown

Check for Samples: LMH6629

FEATURES

- Specified for V_S = 5V, R_L = 100Ω, A_V = 10V/V WSON-8 Package, unless Specified
  - –3dB Bandwidth 900 MHz
  - Input Voltage Noise 0.69 nV/√Hz
  - Input Offset Voltage Max. Over Temperature ±0.8 mV
  - Slew Rate 1600 V/ µs
  - HD2 @ f = 1MHz, $2V_{PP}$ −90 dBc
  - HD3 @ f = 1MHz, $2V_{PP}$ −94 dBc
  - Supply Voltage Range 2.7V to 5.5V
  - Typical Supply Current 15.5 mA
  - Selectable Min. Gain ≥4 or ≥10 V/V
  - Enable Time 75 ns
  - Output Current ±250 mA
  - WSON-8 and SOT-23-5 Packages

APPLICATIONS

- Instrumentation Amplifiers
- Ultrasound Pre-amps
- Wide-band Active Filters
- Opto-Electronics
- Medical Imaging Systems
- Base-Station Amplifiers
- Low-Noise Single Ended to Differential Conversion
- Trans-Impedance Amplifier

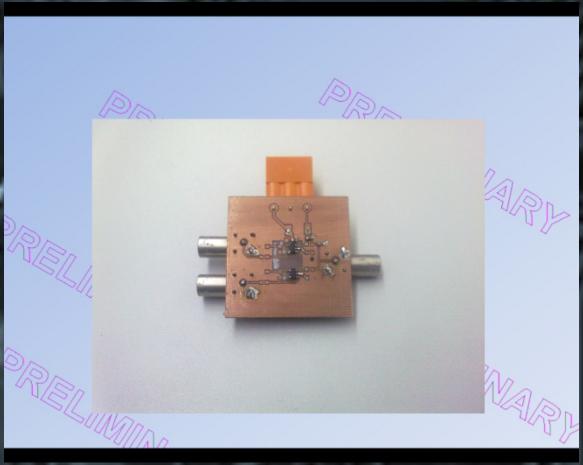
DESCRIPTION

The LMH6629 is a high-speed, ultra low-noise amplifier designed for applications requiring wide bandwidth with high gain and low noise such as in communication, test and measurement, optical and ultrasound systems.

The LMH6629 operates on 2.7 to 5.5V supply with an input common mode range that extends below ground and outputs that swing to within 0.8V of the rails for ease of use in single supply applications. Heavy loads up to ±250 mA can be driven by high-frequency large signals with the LMH6629's –3dB bandwidth of 900 MHz and 1600 V/µs slew rate. The LMH6629 (WSON-8 package only) has user-selectable internal compensation for minimum gains of 4 or 10 controlled by pulling the COMP pin low or high, thereby avoiding the need for external compensation capacitors required in competitive devices. Compensation for the SOT-23-5 package is internally set for a minimum stable gain of 10 V/V. The WSON-8 package also provides the power-down enable/ disable feature.

The low-input noise (0.69nV/√Hz and 2.6 pA/√Hz), low distortion (HD2/ HD3 = −90 dBc/−94 dBc) and ultra-low DC errors (800 µV V_{OS} maximum over temperature, ±0.45 µV/°C drift) allow precision operation in both AC- and DC-coupled applications.

The LMH6629 is fabricated in Texas Instruments' proprietary SiGe process and is available in a 3mm x 3mm 8-pin WSON, as well as the SOT-23-5, package.



Esperimento AUGER

- Realizzato nuovo circuito per impulsatore a Led per segnali di qualsiasi durata temporale (entro i parametri del led) fino a circa 30 Volt di ampiezza
- Realizzato alimentatore lineare da 35 a 70 Volt da utilizza con APD e, contemporaneamente, sviluppo di un elevatore step-up di tensione a basso rumore sempre per APD
- I primi test hanno mostrato un corretto funzionamnto sia dell'impulsatore che dell'alimentatore.