



DEPARTMENT OF
INFORMATION
ENGINEERING
UNIVERSITY OF PADOVA



Chip Irradiation per l'Industria

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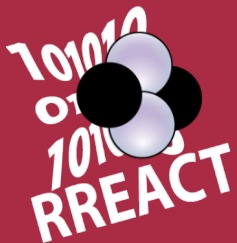
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and INFN – Sezione di Padova



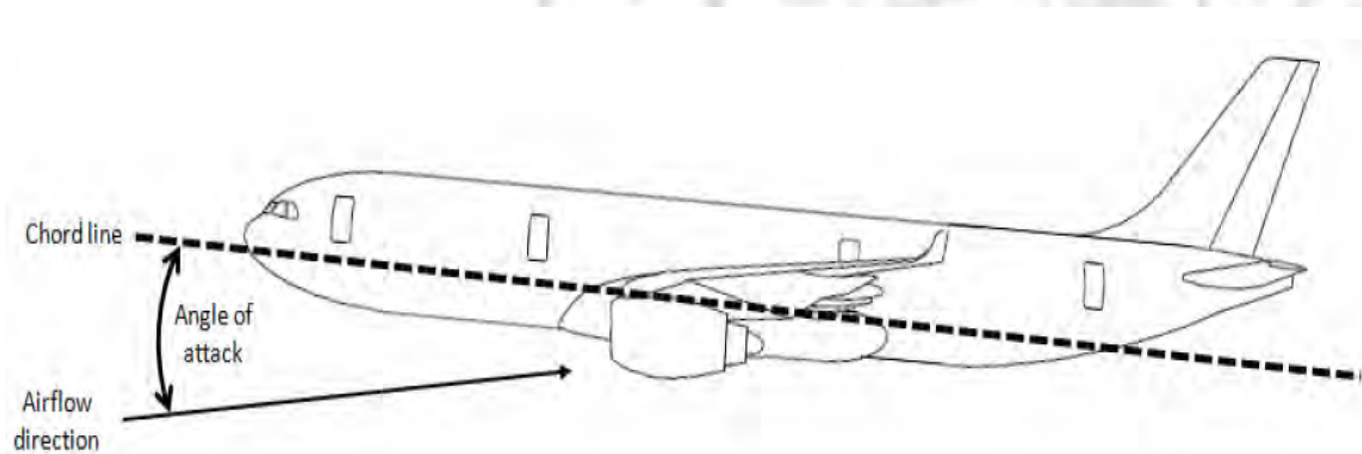
- An Abrupt Introduction to Radiation Effects: the Qantas Flight 72 Incident
- Radiation Environments
 - Terrestrial, Artificial
- Radiation Effects in Electronic Devices
 - Single Event Effects (SEE)
- Industrial Concern over SEE
- SEE Testing
- Conclusions

Qantas Flight 72 (QF72) was a scheduled flight from Singapore [...] to Perth [...] on 7 October 2008 that made an emergency landing [...] following an inflight accident featuring a pair of sudden **uncommanded pitch-down manoeuvres** that resulted in serious injuries to many of the occupants



From Wikipedia

“There was a limitation in the algorithm used by the A330/ A340 [...] for processing angle of attack (AOA) data. This limitation meant that, in a very specific situation, **multiple AOA spikes from only one of the three air data inertial reference units could result in a nose-down** elevator command.”



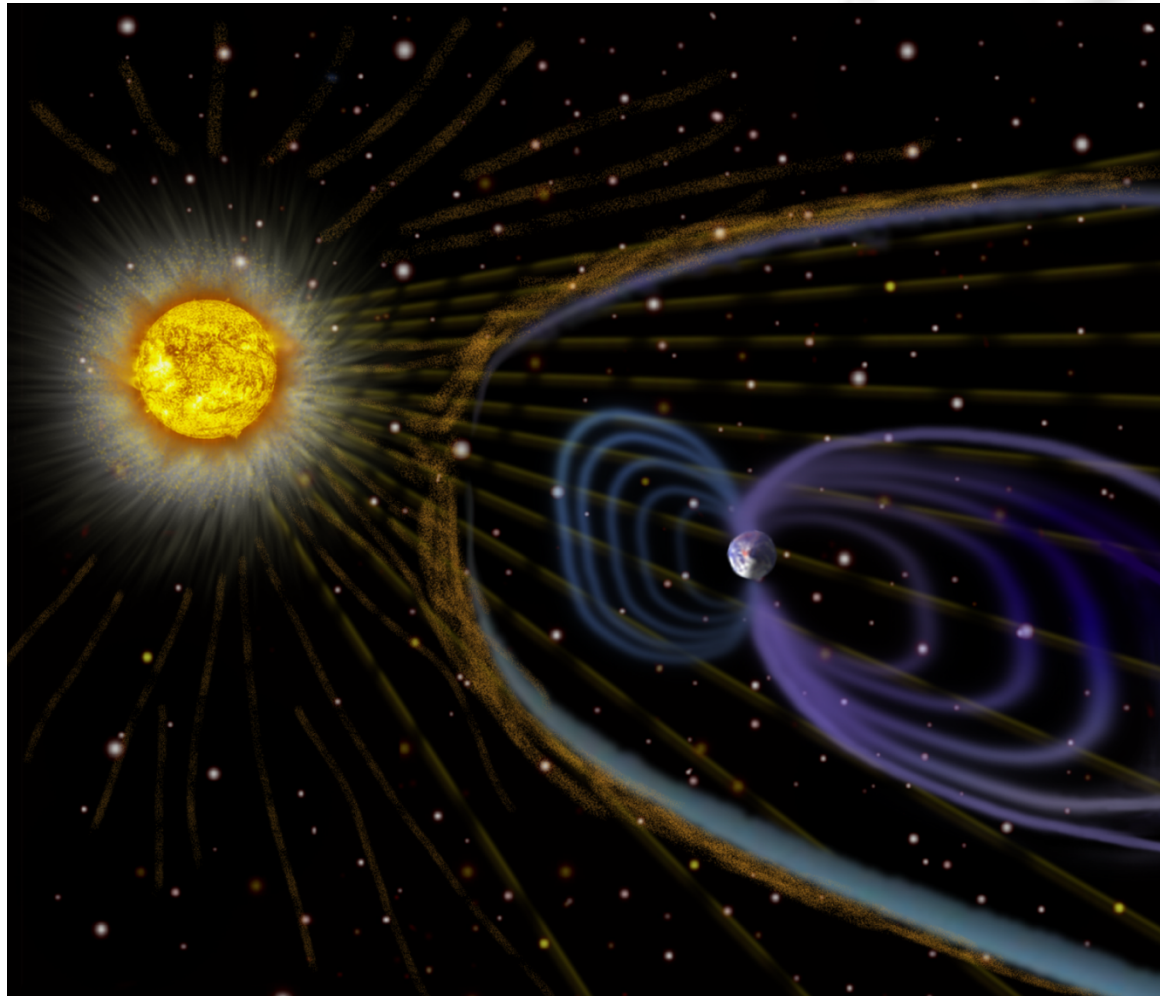
From ATSB TRANSPORT SAFETY REPORT Aviation Occurrence Investigation AO-2008-070 “In-flight upset 154 km west of Learmonth, WA 7 October 2008VH-QPA Airbus A330-303”

“One of the aircraft’s three air data inertial reference units (ADIRU 1) exhibited a **data-spike failure mode**, during which it transmitted a significant amount of incorrect data on air data parameters to other aircraft systems, without flagging that this data was invalid.”

“The LTN-101 **air data inertial reference** unit (ADIRU) model had a demonstrated **susceptibility to single event effects** (SEE). “

From ATSB TRANSPORT SAFETY REPORT Aviation Occurrence Investigation AO-2008-070 “In-flight upset 154 km west of Learmonth, WA 7 October 2008VH-QPA Airbus A330-303“

The Space Radiation Environment

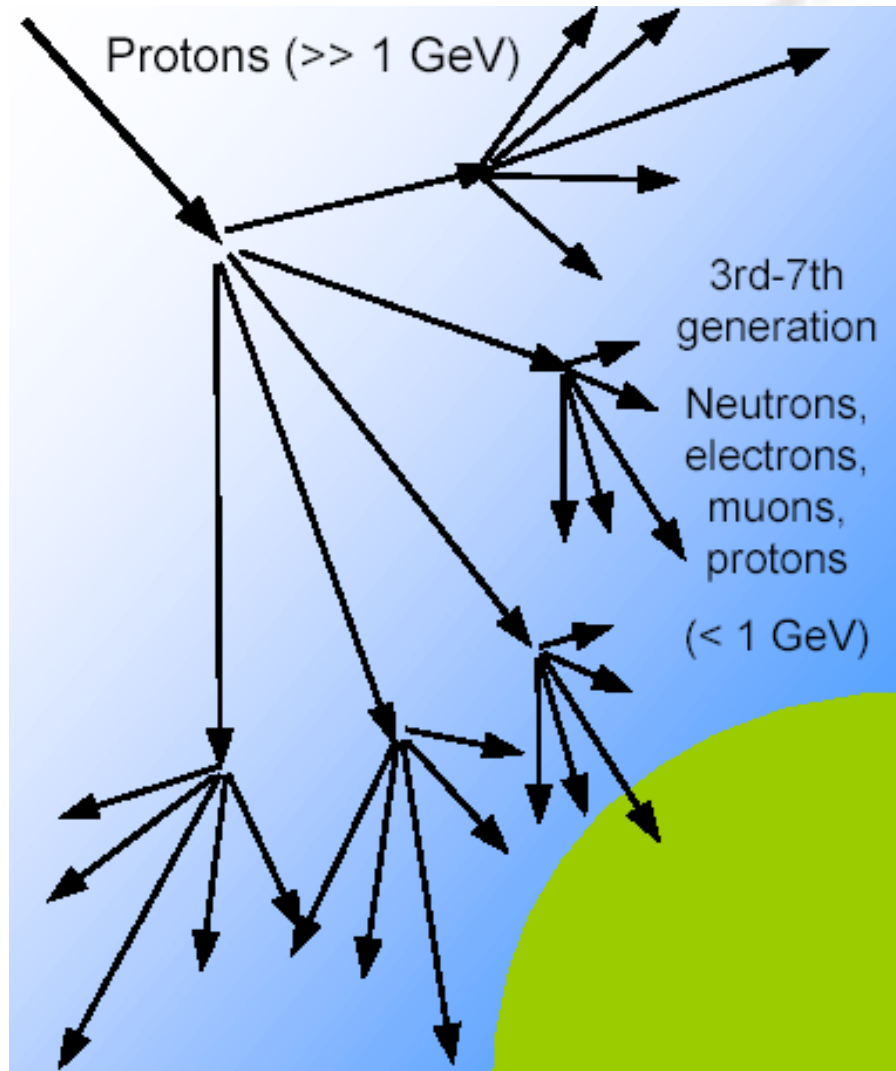


Artistic render courtesy of NASA

Space was the first community that had to deal with radiation effects on electronics (Telstar incident)

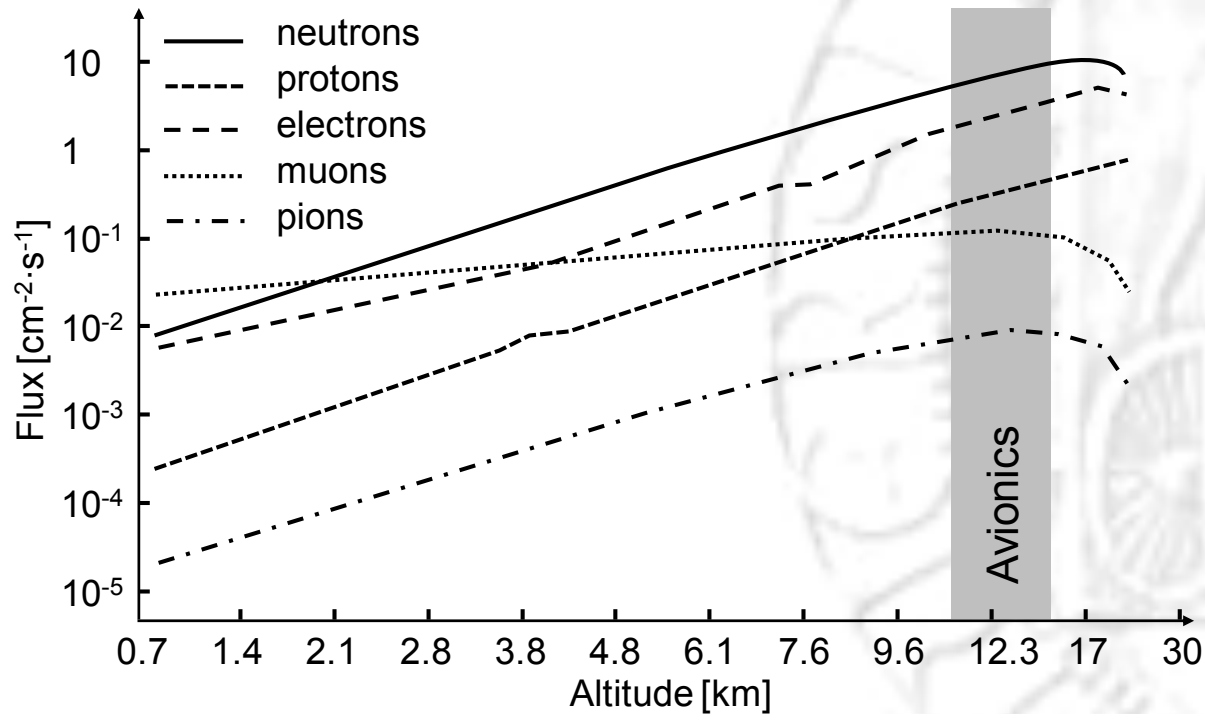
Electronics onboard satellites must cope with:

- Trapped Particles
- Solar Particle Events
- Galactic Cosmic Rays



Issues at sea level:

- Alpha-emitting radioactive contaminants in dice and packages
- Recently concern on muon-induced soft errors has surfaced
- The biggest threat: **atmospheric neutrons** (high-energy and thermal). Actually, the whole energy spectrum is capable of generating effects in electronic chips

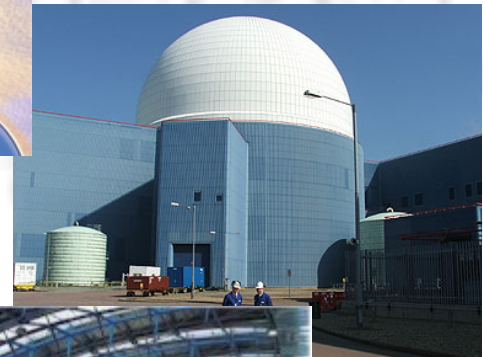
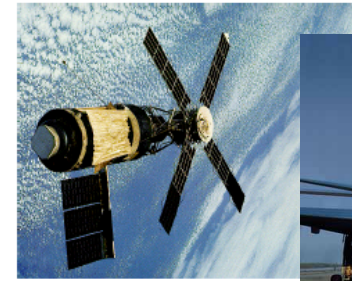


Avionics

- Neutron flux is $\sim 300\times$ at commercial airplane altitudes, compared to sea level
- Airplanes have many critical systems

- Artificial sources of radiation
 - Radiation therapy and diagnostic facilities
 - Industrial accelerators and sources
 - Nuclear power plants
 - High-energy physics experiments

- All makers of systems needing **high-reliability**
- Aerospace
 - Satellites
 - Civilian and military aircrafts
- Medical
 - Implanted electronic devices (pacemakers, defibrillators...)
- Nuclear Industry
 - Instrumentation and control in proximity to reactors
- Transport
 - Electronics in cars and trains
 - Signalling and traffic control networks
- IT Networks and Telecommunication



➤ Total Ionizing Dose

- affects **dielectric layers** (e.g., gate, isolation, and passivation oxides)
- causes **parametric shifts** in transistors/device parameters
- **cumulative effect**, usually reported as a function of ionizing dose

➤ Displacement Damage

- affects bulk materials (e.g. crystalline Silicon)
- **cumulative effect**, usually reported as a function of equivalent neutron fluence or displacement dose

➤ Single Event Effects

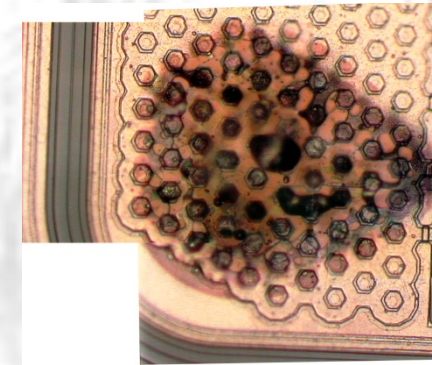
- **stochastic effects**: caused by a single ionizing particle impinging randomly on a sensitive device volume
- cause a variety of different effects: **memory corruption**, **burn-out**, etc.

Terrestrial

Space/Artificial

Classifications of Single Event Effects

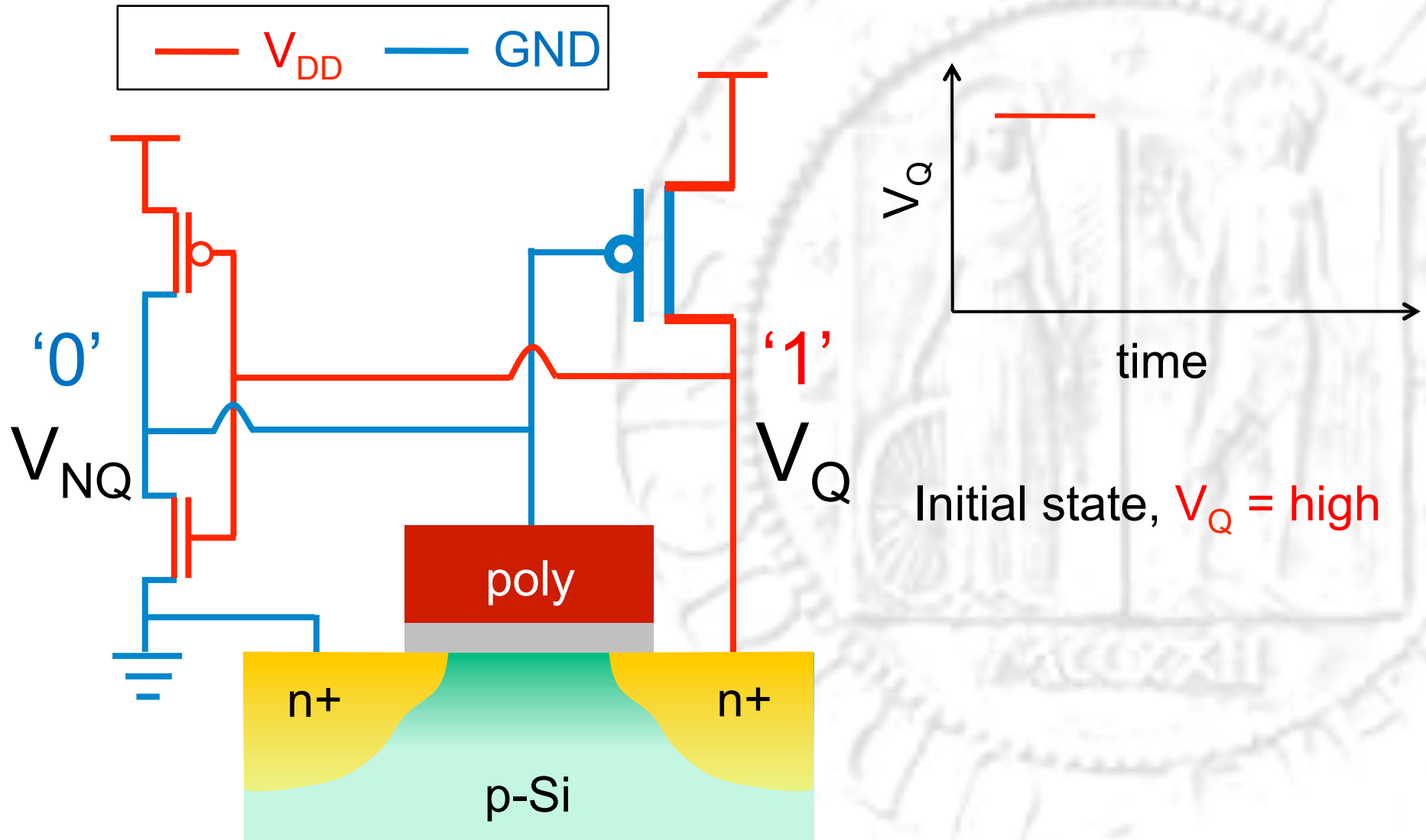
- **Single Event Effect (SEE):** perturbation of the behavior of electronic (optoelectronic) devices, circuits and/or systems produced by a single ionizing particle
- **Non-destructive (soft errors):**
 - Single Event Upset (SEU)
 - Single Bit Upset (SBU)
 - Multiple Bit Upset (MBU)
 - Single Event Transient (SET)
 - Single Event Functional Interrupt (SEFI)
 - Single Event Latchup (SEL)... *may be destructive*
- **Destructive (hard errors):**
 - Single Event Burnout (SEB)
 - Single Event Gate Rupture (SEGR)
 - Stuck Bits



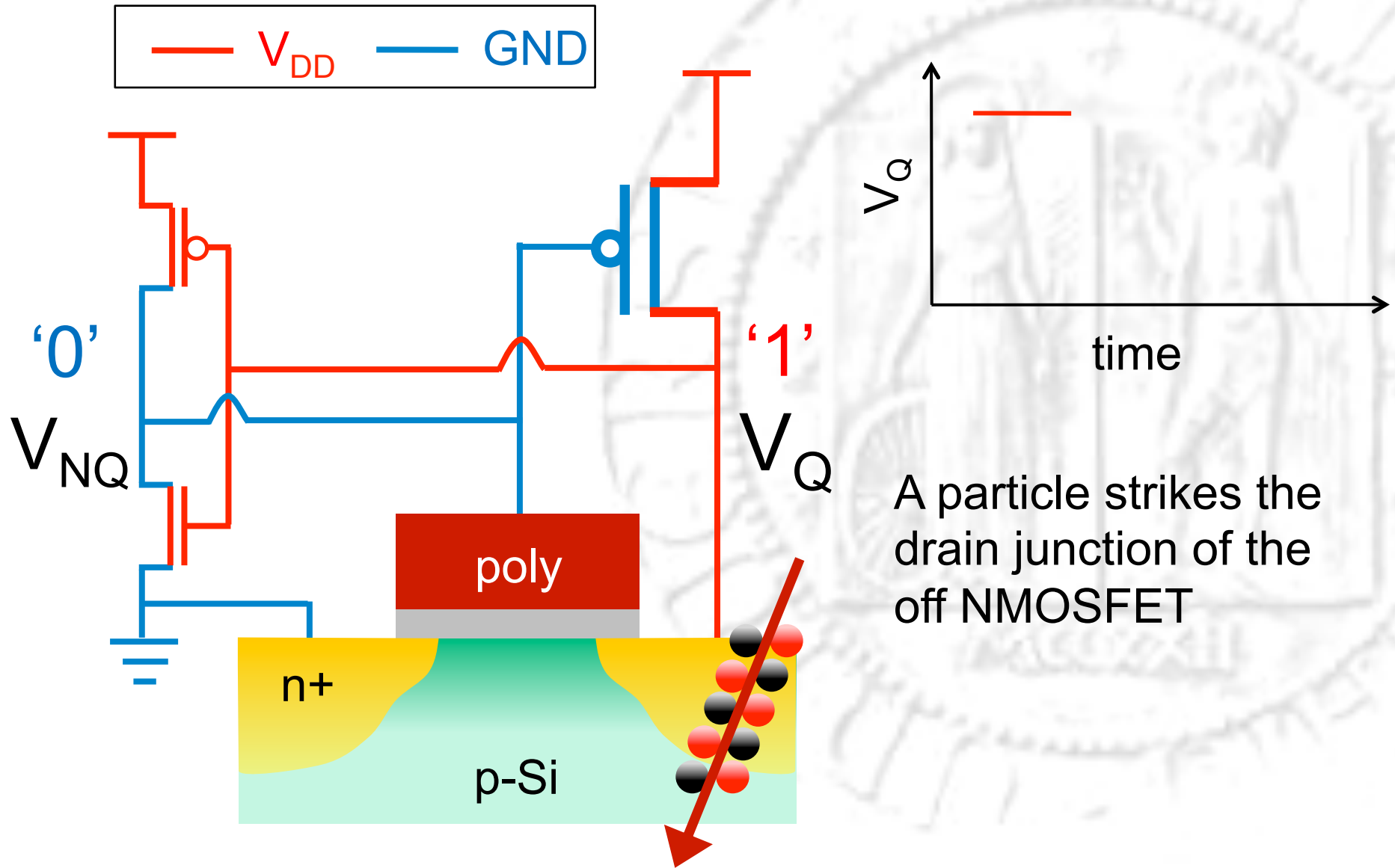
*Destructive event
in a COTS 120V
DC-DC Converter*

*K. LaBel,
EWRHE
2004*

An Example: Single Event Upsets in SRAMs

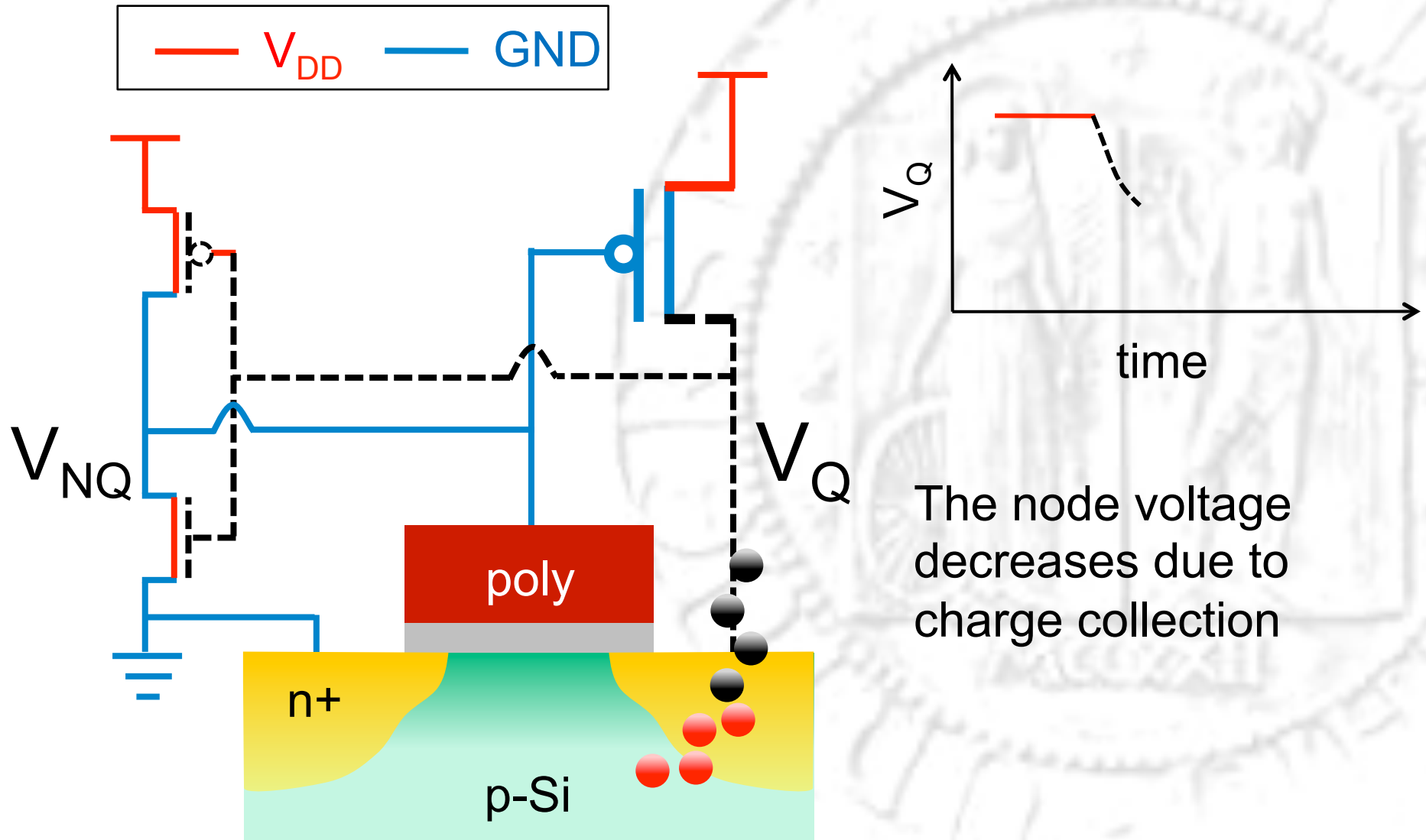


An Example: Single Event Upsets in SRAMs

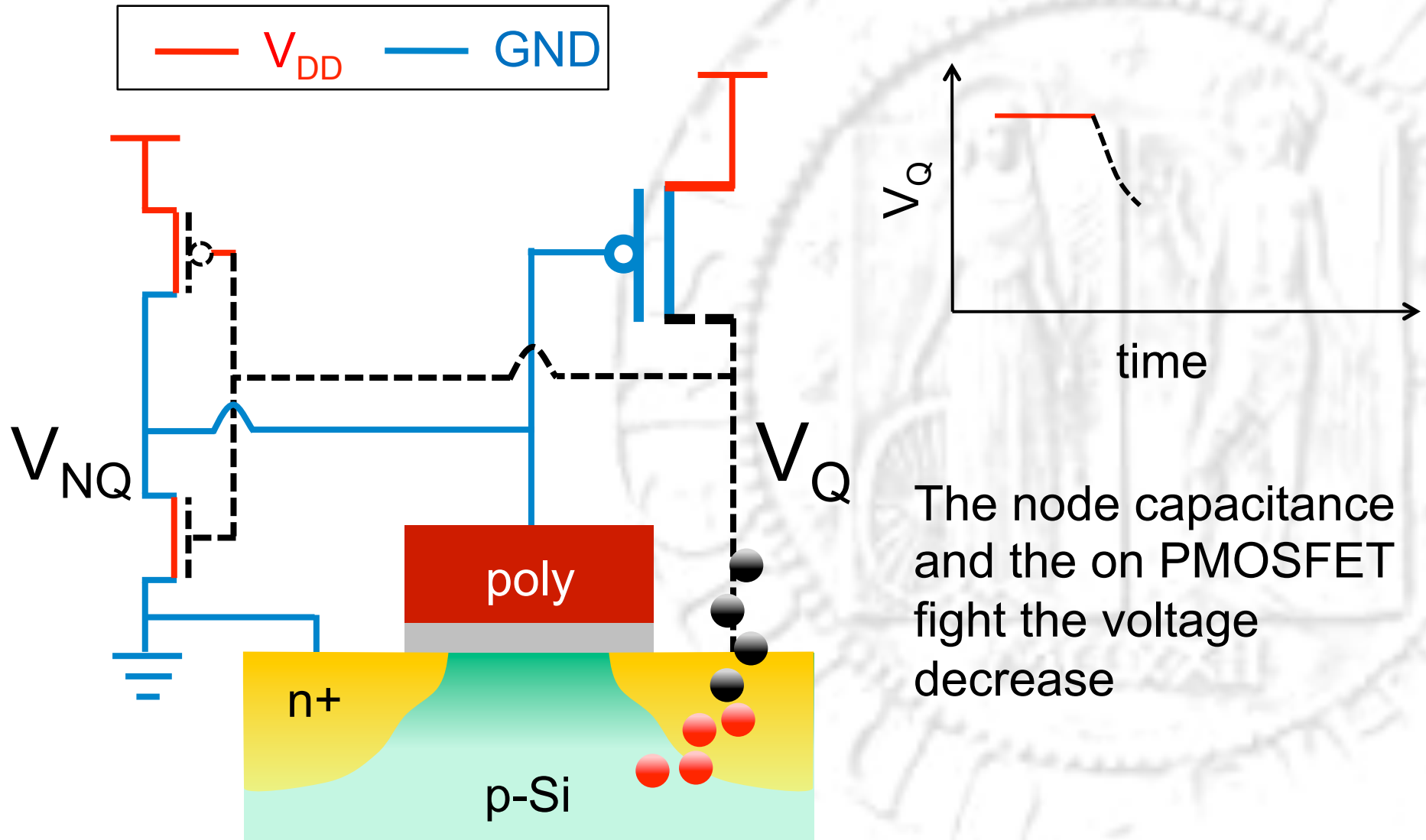


A particle strikes the drain junction of the off NMOSFET

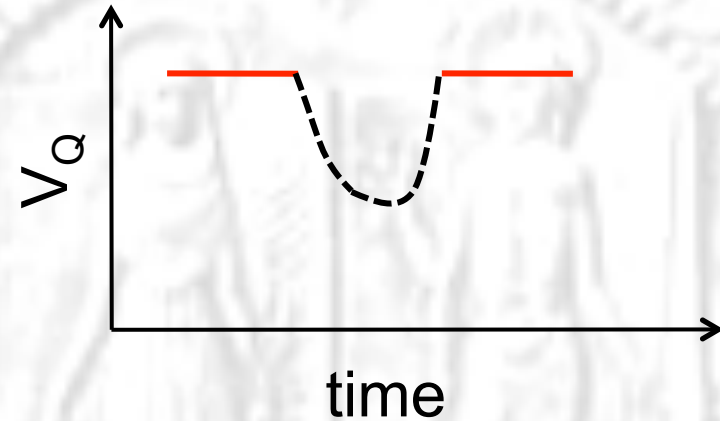
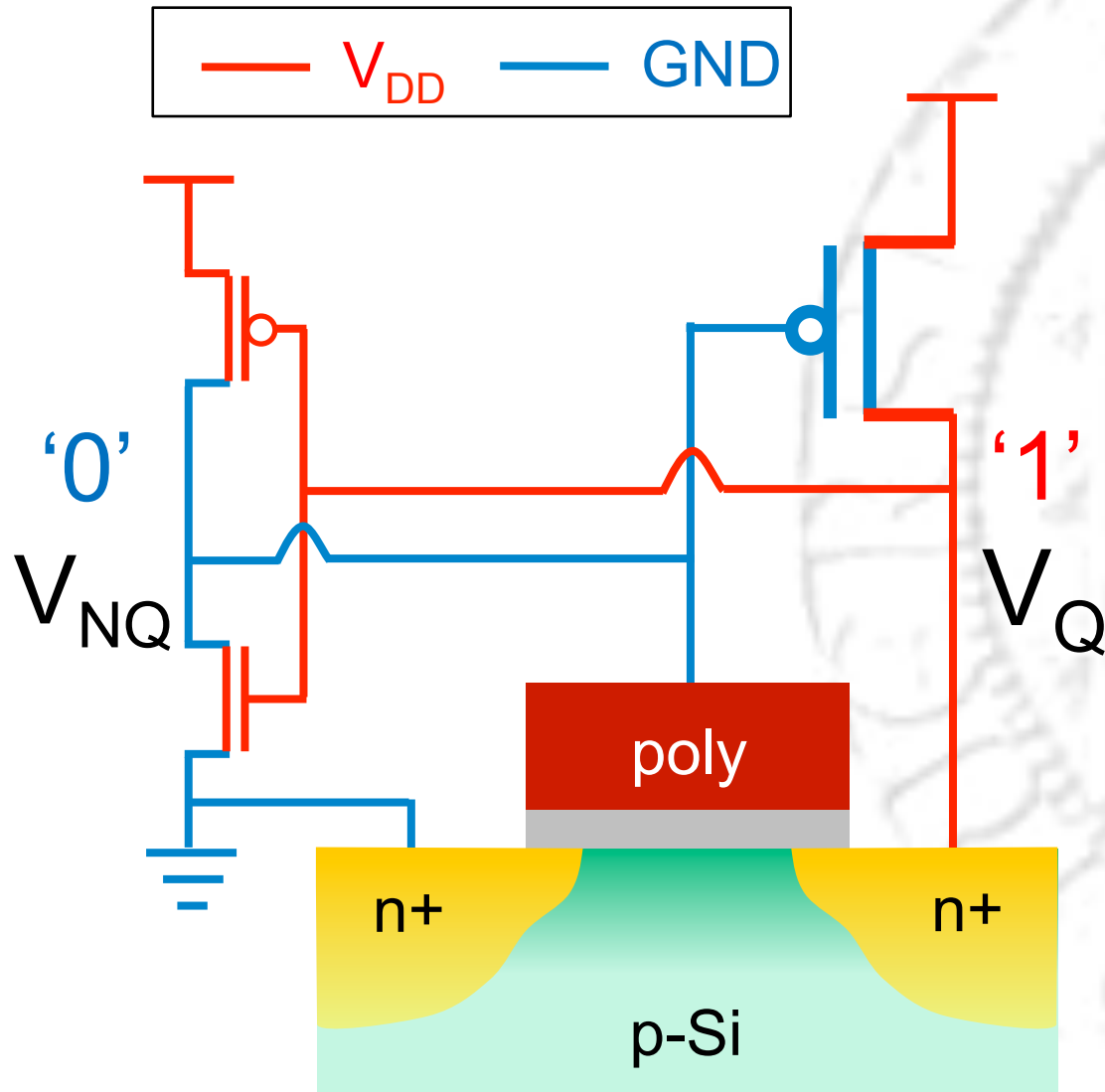
An Example: Single Event Upsets in SRAMs



An Example: Single Event Upsets in SRAMs

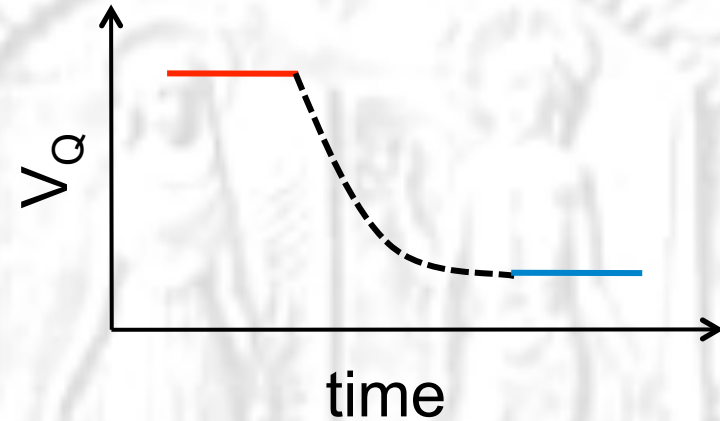
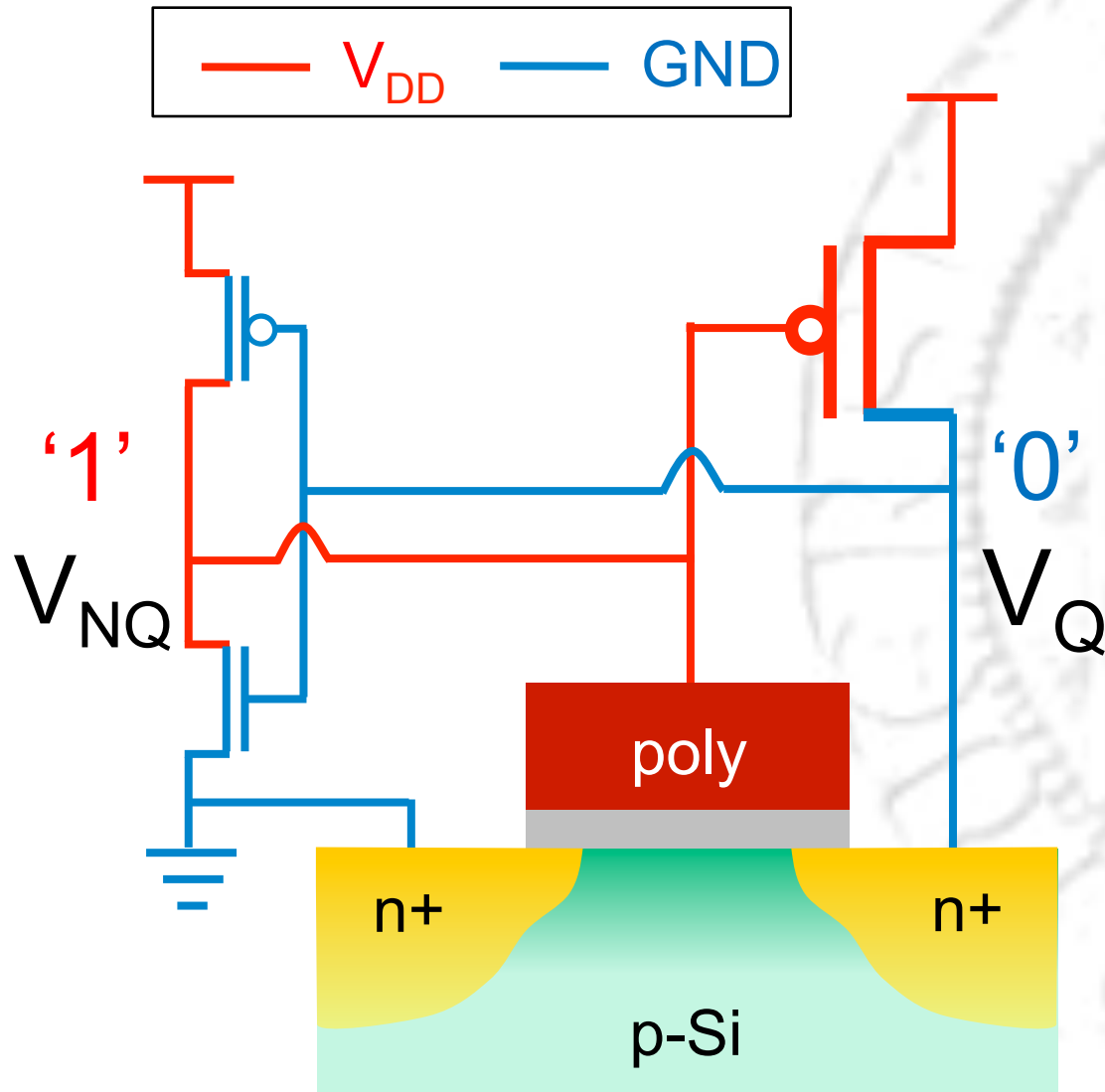


An Example: Single Event Upsets in SRAMs



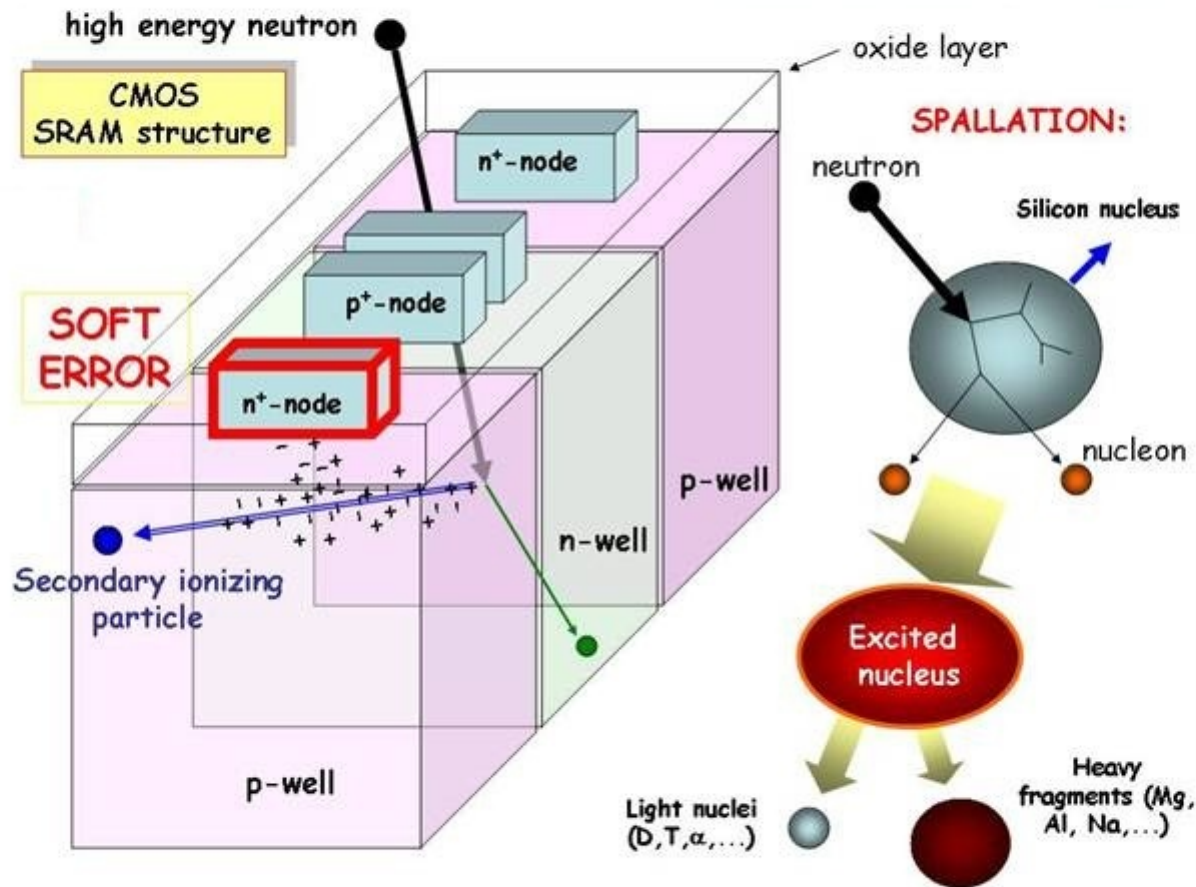
If the voltage transient is below the switching threshold or is too short, no change occurs

An Example: Single Event Upsets in SRAMs



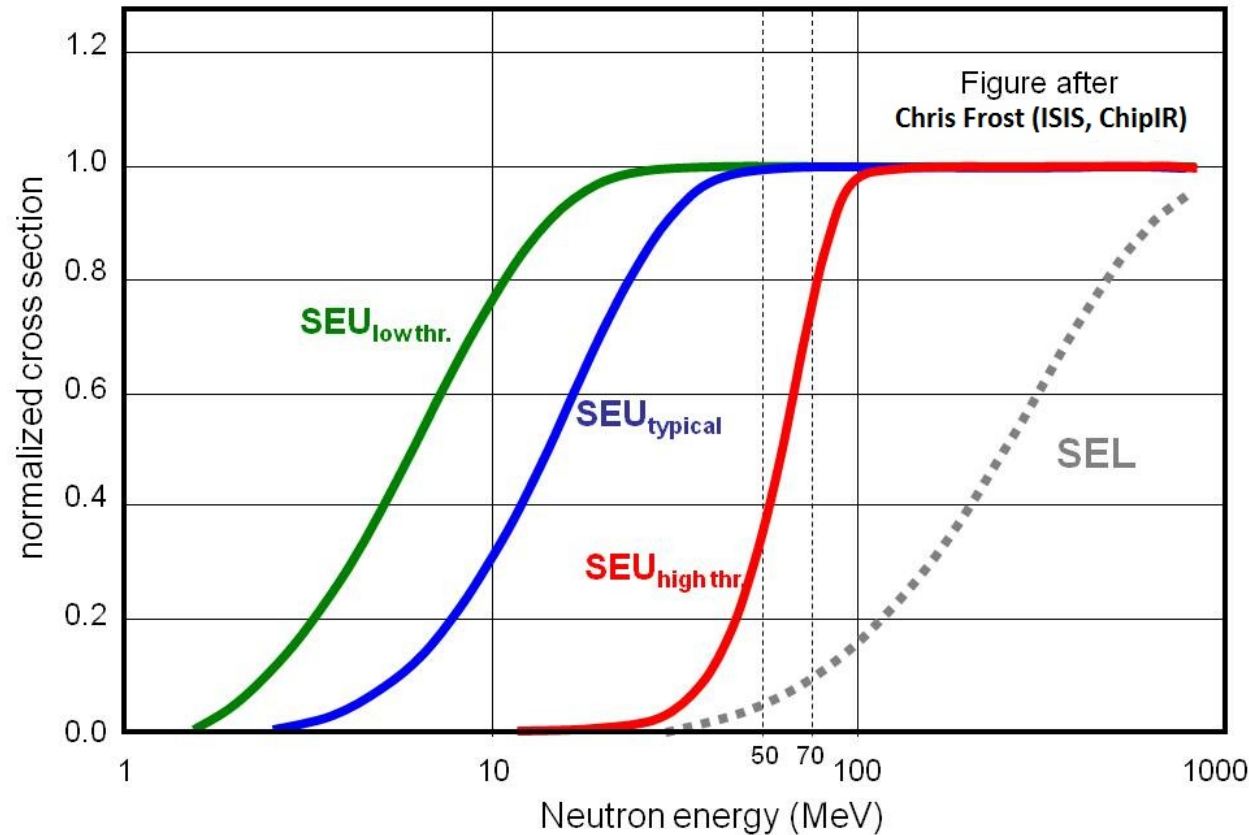
But if the voltage transient is **long** and **ample** enough (in other terms, if the collected charge is larger than the critical charge), the cell flips

Neutron-induced Single Event Effects

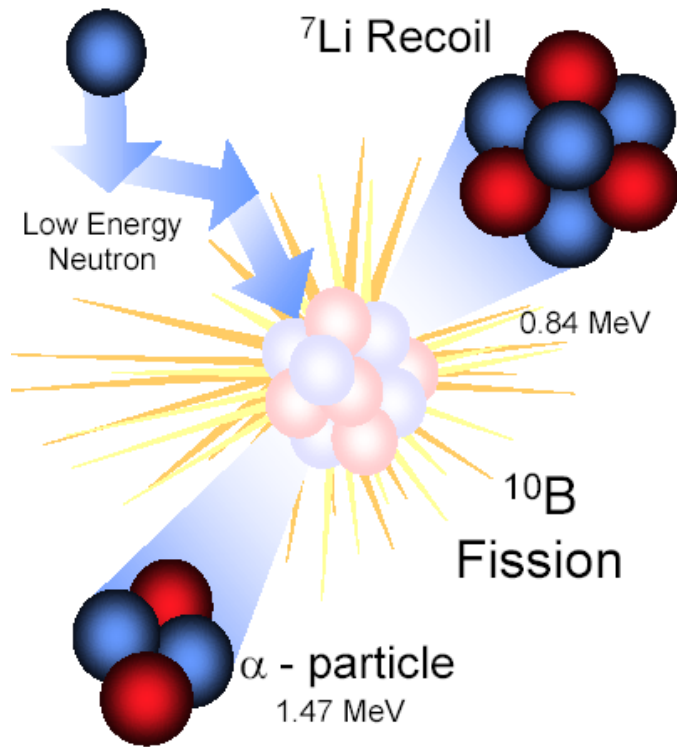


n-induced SEEs are due to secondary ionizing particles, generated by the interaction of n with the chip materials

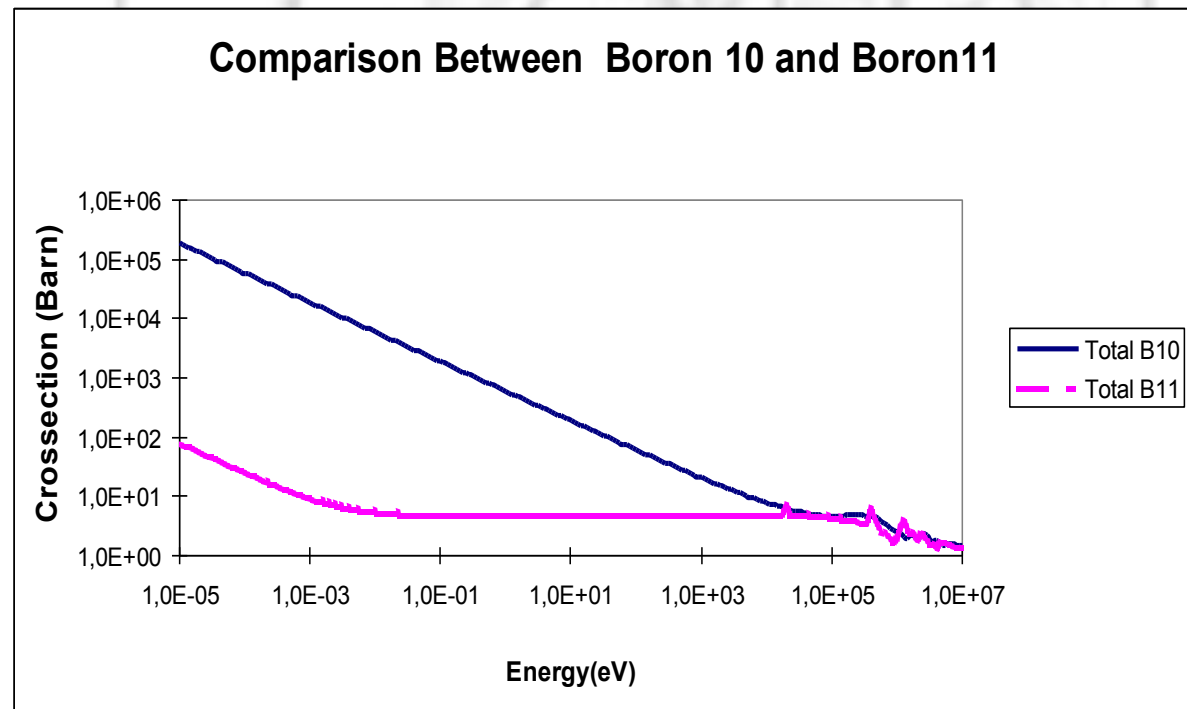
neutron-induced SEE cross-sections vs energy



n-induced SEEs occur when the energy of the impinging neutron is above a minimum **threshold value**



Boron 10 is extensively used by the semiconductor industry. It has a very high interaction cross section with thermal neutrons



“**Soft errors** have become a huge concern in advanced computer chips because, uncorrected, they produce a failure rate that is **higher than all the other reliability mechanisms combined!**”

R. Baumann, Fellow, IEEE (was with Texas Instruments)

“Since chip SER is viewed by many as a **legal liability** (selling something that you know may fail), the public literature in this field is sparse and always makes management nervous”

J. Ziegler and H. Puchner, “SER-History, Trends and Challenges”, Cypress Semiconductors, 2004

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Radiation Effects

Documentation

Ionizing radiation can cause unwanted effects in semiconductor devices. Energetic Protons, Neutrons, Heavy Ions, and Alpha particles can strike

Defense QPro Data Sheets

AEC - Q100 - REV-G
May 14, 2007

Automotive Electronics Council
Component Technical Committee

Appendix 6: Part Design Criteria to Determine Need for SER Testing

A6.1 Use the following criteria to determine if a part is a candidate for SER Testing:

- The part use application will have a significant radiation exposure such as an aviation application or extended service life at higher altitudes.
- SER testing is needed for devices with large numbers of SRAM or DRAM cells (≥ 1 Mbit). For example: Since the SER rates for a 130 nm technology are typically near 1000

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Single Event Upsets

Ionizing radiation can cause unwanted effects in semiconductor devices, such as flipping the state of memory

IBM Journal of Research and Development

Volume 52, Number 3
April-May 2008

Soft Errors in Circuits and Systems

FPGAs

- Stratix IV (E and GX)
- Stratix III
- Stratix II/Stratix II GX
- Stratix/Stratix GX
- Arria GX
- Cyclone III
- Cyclone II
- Cyclone

CPLDs

- MAX II
- MAX 3000A
- MAX 7000

ASICs

- HardCopy III
- HardCopy II
- HardCopy Stratix
- HardCopy APEX 20K

Downloads

- Device Pin-Outs
- Gerber Files
- IBIS Models
- BSDLBST
- PCB Symbols

Configuration/Programming

- Configuration
- Programming
- Programming Tools

Power

- Power Management
- Early Power Estimators
- Certified Power Solutions

I/O

- Features

Low Graphics | Accessibility help

BBC

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Microsoft says PCs may need DRAM upgrade

Rick Merritt
EE Times
(05/17/2007 11:04 PM EDT)

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LOS ANGELES — Desktop and notebook computers may need to adopt error-correcting code (ECC) memory to combat rising system crashes from single-bit memory errors, according to a confidential white paper written by Microsoft Corp. The software giant raised the issue in a panel discussion on [memory](#) at the Windows Hardware Engineering Conference here although it admits its data on system failures is still inconclusive.

For about four years Microsoft has been collecting data through its Online Crash Analysis (OCA) tool that reports system crashes to a Microsoft Web site. About 18 months ago it began sharing OCA data and the white paper with



Industrial Concern over Soft Errors (3)

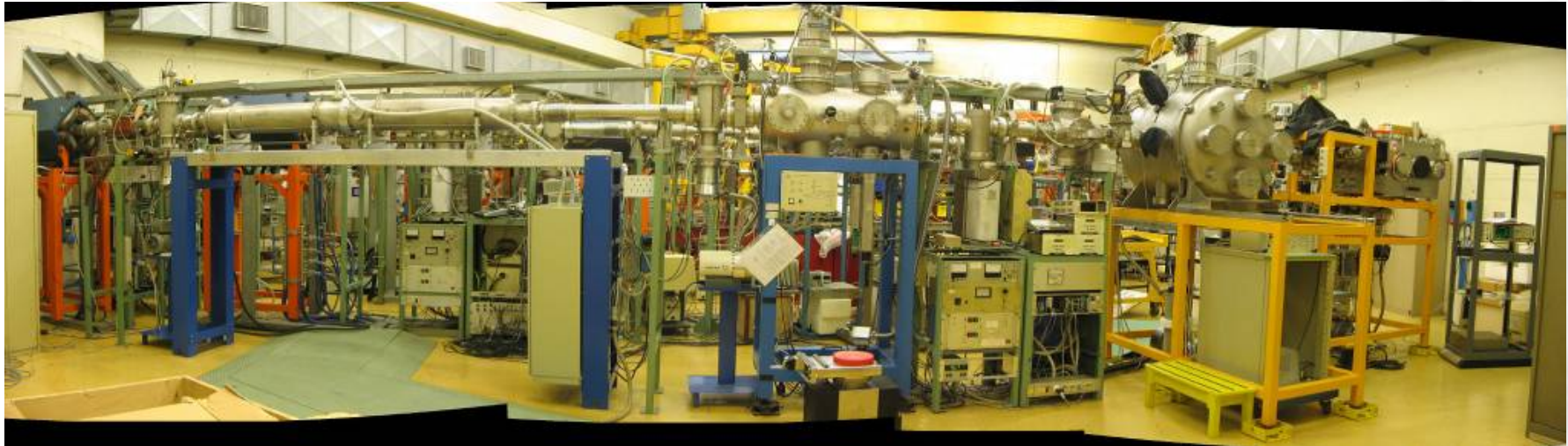
- “Timely testing avoids cosmic ray damage to critical auto electronics”,
John Wood and Earl Caustin, MOSAID Systems, 15/6/2006
- “Cosmic rays damage automotive electronics”,
Martin Mason, Actel Corporation, 31/5/2006
- “Alpine lab enters rarified air of soft-error test”,
Junko Yoshida, 25/9/2006
- “SEU mitigation in Stratix III Devices”, *May 2007*





- Semiconductor companies make soft error tests **at the component level**, but **results are confidential** (arbitrary units are typically used in publications) and disclosed only to very large customers
- **System-level** error rates are difficult to derive from component data or may be too overestimated
- Failure rates can be as high as **10^5 FIT**

For terrestrial applications, a **neutron source** reproducing the terrestrial spectrum, with some orders of magnitude of acceleration is desirable to test components and systems



- **SIRAD** line at the TANDEM accelerator of the Legnaro Labs
 - Heavy ions and protons
 - Ion Electron Emission Microscope : unique SEE micro-mapping capability!
- Plans for a **SEE neutron facility**
 - Uses the new high-current, variable-energy 70-MeV Cyclotron
 - Three different targets under consideration

- **Radiation effects are a very serious threat** for high-reliability applications, even at sea level, mainly due to atmospheric neutrons
- **Sensitivity** of chips **is increasing** with each generation, due to feature size scaling
- **Component- and system-level radiation testing is necessary** to avoid issues, such as those occurring in the Qantas 72 flight