FTK: HW status

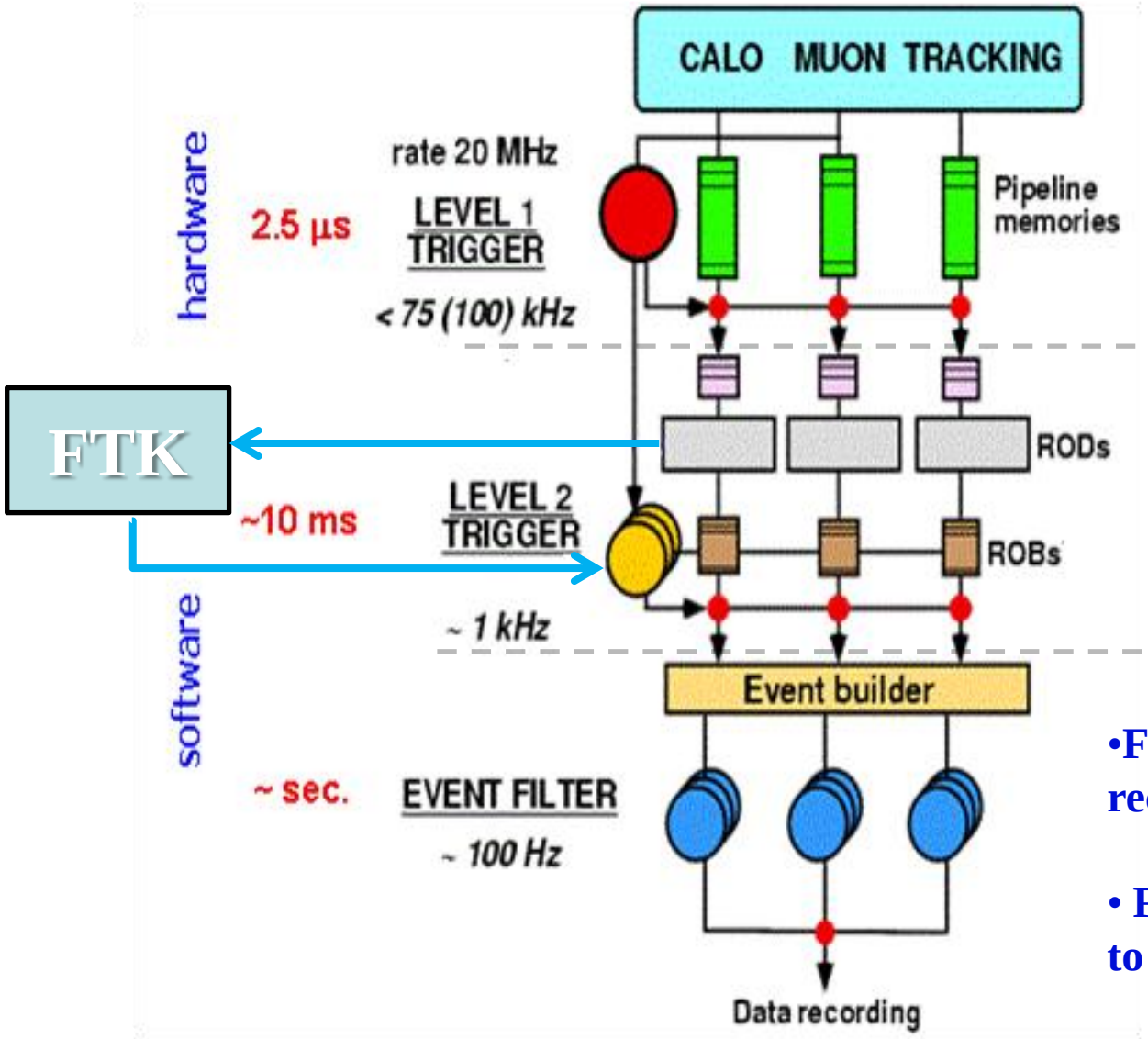
Marco Piendibene for the FTK team

Atlas Italia – Pisa - April 12, 2013

OUTLINE

- For each board: Status – future schedule for 2015
- Summary of timescales
- Milestones & Conclusions

Atlas trigger system: where is FTK?

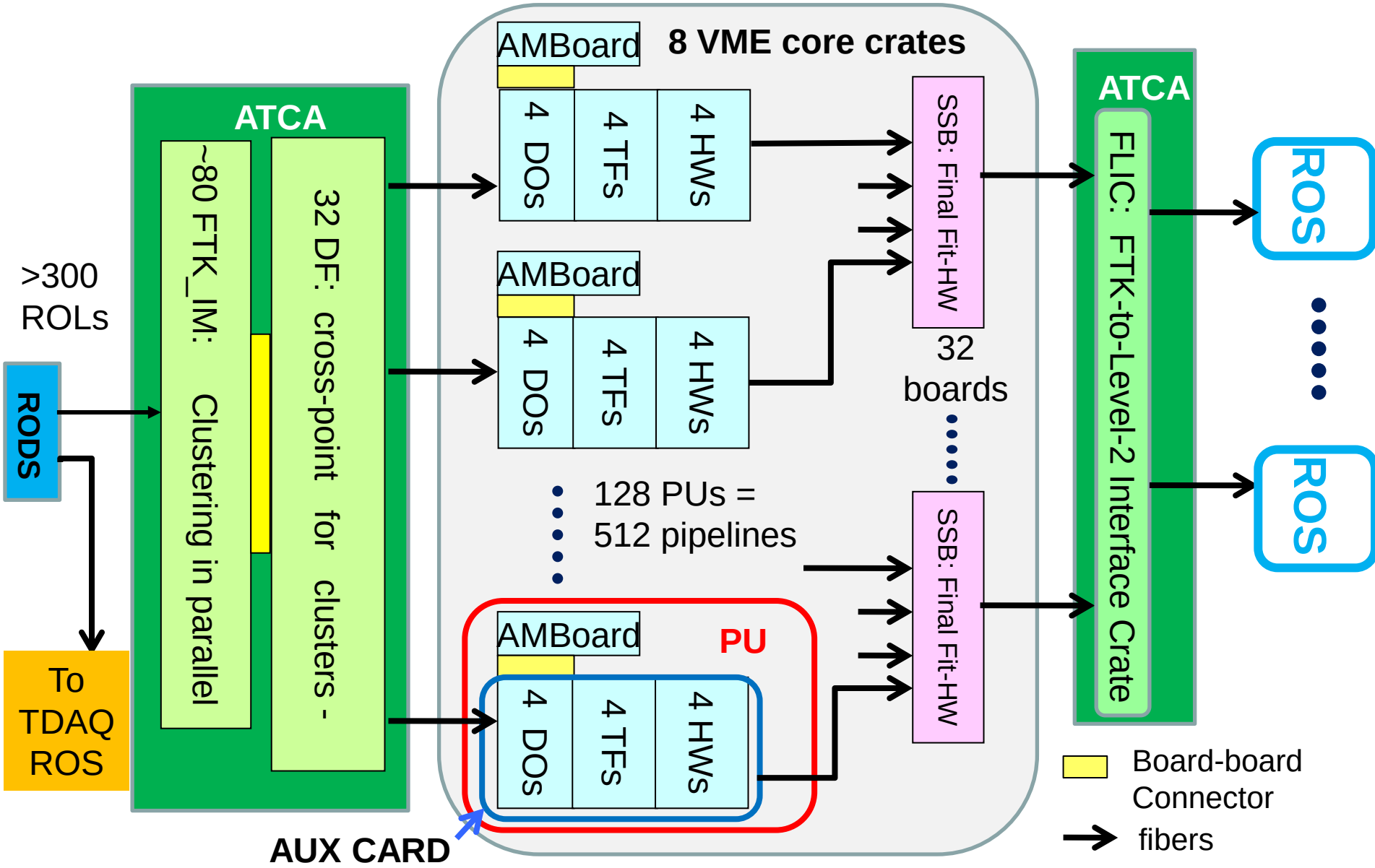


- We need to reduce the amount of data
- Atlas 3 levels trigger

- **FTK is an hardware system to reconstruct the particles tracks**
- **FTK gives tracks information to Level2 trigger.**

FTK global view

16400 AMchips
~2000 FPGAs
Thousands of serial links



Dual-output HOLA (U. of Chicago)

RODS

To DAQ ROS

ATCA

FTK_IM: Clustering in parallel

32 DF: cross-point for clusters -

STATUS

- Sends SCT & pixel data to DAQ & FTK.
- All required boards produced and tested.
- 32 boards installed at P1.
- More SCT RODs→ produce 40 more **HOLAs**.
- IBL RODs have it built in.

  We will pay for ½ of the QSFPs.

Schedule:

Production of additional DO-HOLAs:

Spring. '13

Installation of DO-HOLAs/fibers:

when fibers from all ROD-BOCs will be disconnected for new RODs installation

Test of installation

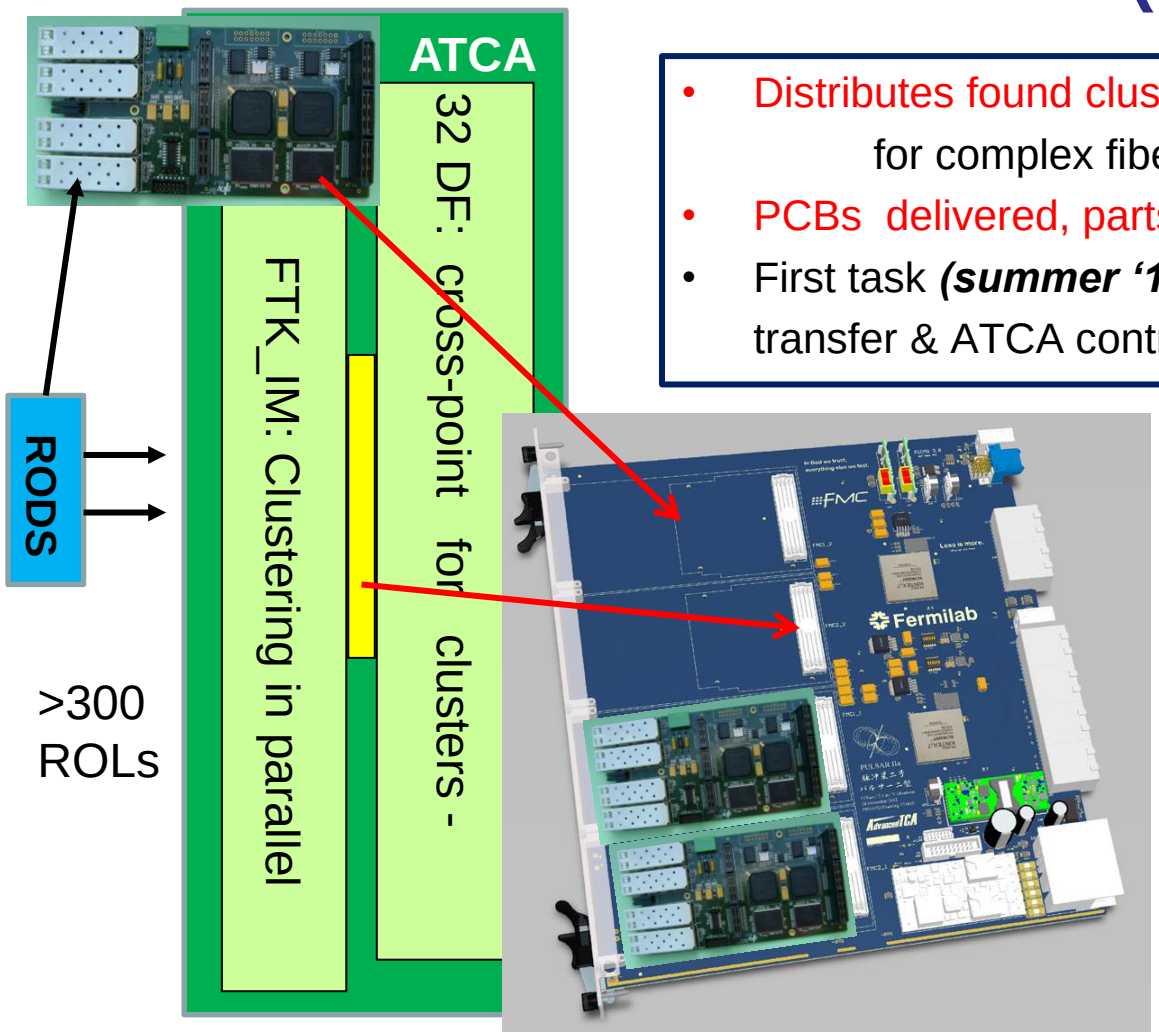
when ROS will be available

FTK input mezzanine (FTK_IM Frascati Waseda)

- Receive ROD's data and do cluster finding.
- Prototypes produced, tested, and used @P1.
- Few changes needed for DF compatibility.
- New prototype: now under stand-alone test

STATUS

Data Formatter (DF, Fermilab, UofC)



- Distributes found clusters to 64 FTK η-ϕ towers. ATCA for complex fiber-to-tower mapping.
- PCBs delivered, parts assembly is on-going
- First task ***(summer '13)*:** test high speed serial data transfer & ATCA control functionality. Firmware test.

STATUS

Schedule:

Test FTK_IM-IBL BOC: ***Sum. '13***

Integrated tests w DF: ***Aut. '13***

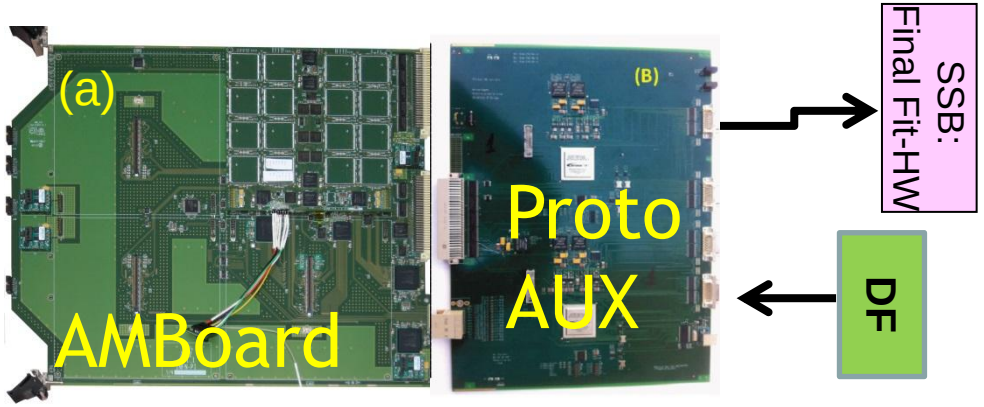
Global Integration ***Spr.-Sum. '14***

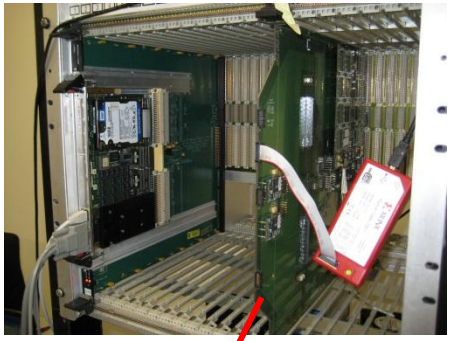
Production FTK_IM: ***Sum. '14***

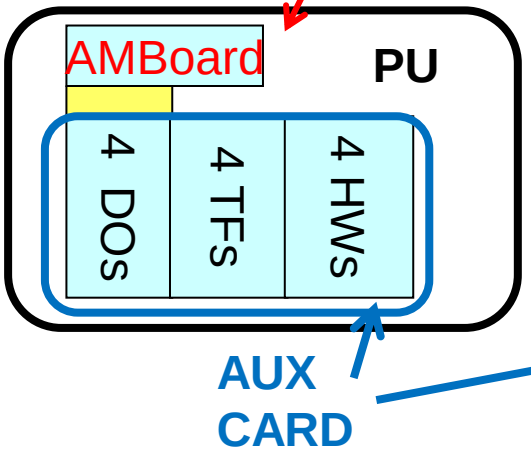
DF Production ***Sum. '14***

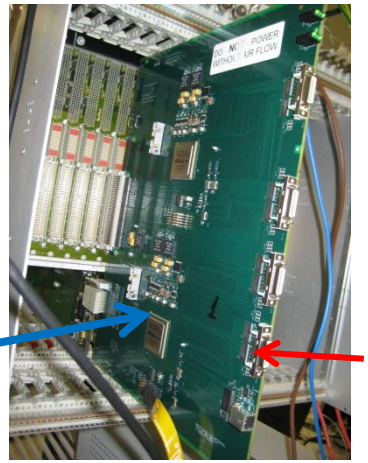
DF-FTK_IM Installation ***Aut. '14***

FTK Processor Unit (PU) - Status









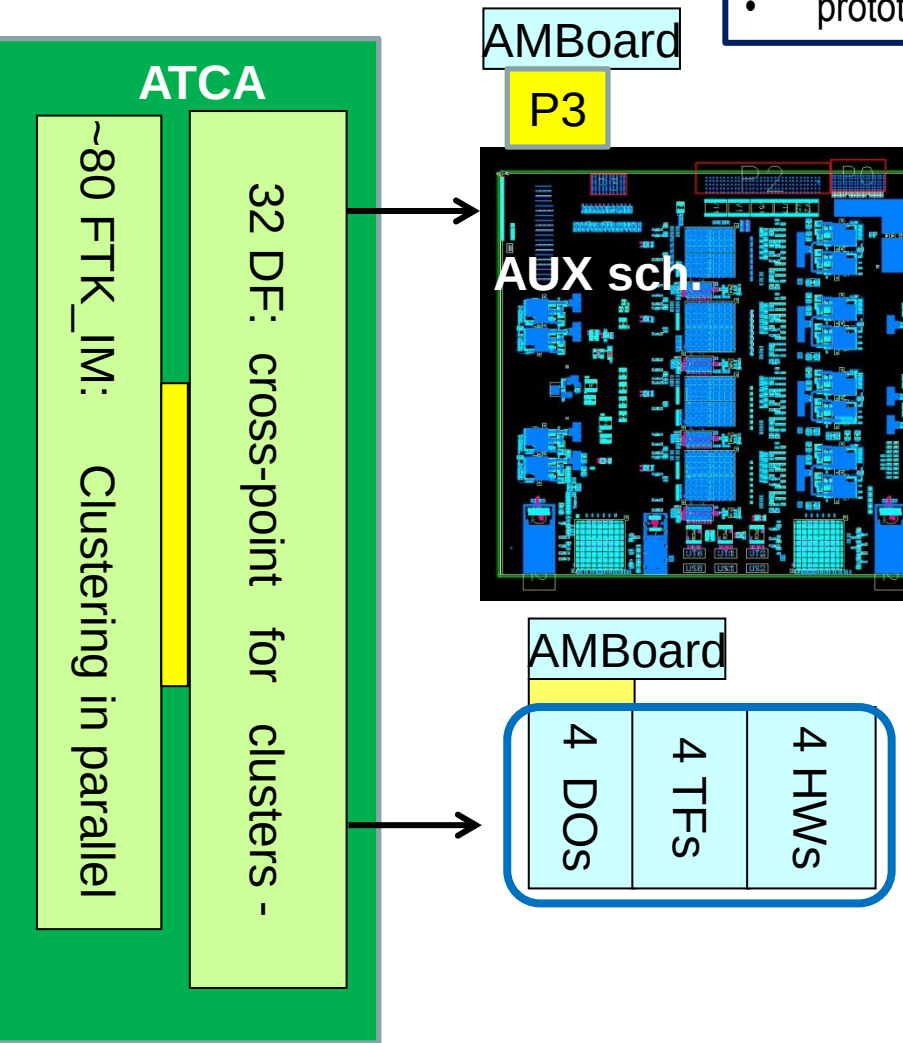
- 128 PUs do pattern matching and the 1st stage track fitting.
- A PU consists of an
  - ***Associative Memory*** VME board (a) (AMB-Europe)
  - a large ***Auxiliary Card*** (b) (AUX-UoChicago) behind it.

We tested them successfully together in the Pisa test stand for Data Transfer & VME functions

The final AUX (U. of Chicago)

- Receives DF data, sends coarse hits to AMB, receives back roads, and does the 1st-stage fitting (8 layers).
- Final board design completed
- Firmware ready for data processing (under optimization), but error handling, monitoring tasks to be added.
- Engineering review in March successful
- prototype PCB ordered

STATUS



Schedule:

Standalone test: ***Summer '13***

Integrated Test DF/AUX : ***Aut. '13***

Integrated Test AMB/AUX : ***next Winter***

Integrated 1st stage: ***Spring '14***

Global Integration: ***Spr.-Sum '14***

AUX Production ***Sum-Aut. '14***

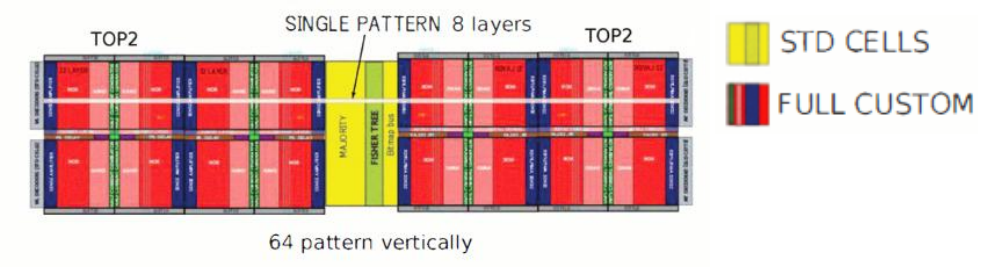
AUX Installation ***Aut. '14-Winter '15***

AM System (1): - Status

DOI:10.1109/ANIMMA.2011.6172856

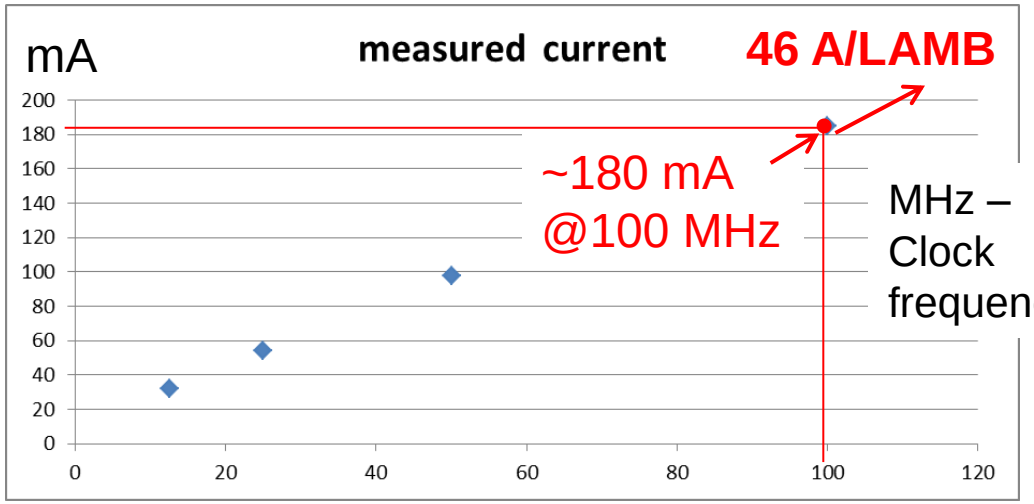
AM chip04: TMSC 65 nm with Variable Resolution

- custom cell to reduce pattern size: 8k patterns in 14 mm^2.



- Yield>80% - tests successful
- 64kpatt power consumption lower than AMchip03

AMchip03 (5 kpat, 180 nm): 1 A → **1,8 W**
AMchipnew (64 kpatt): 1,45 A → **1,7 W**
expected **1,6 W**



EXTREMELY GOOD RESUSLTS, BUT:
we need Serialized I/O whose consumption is high *(many SL fanouts)*.

TWO possibilities:

(1) Dilute boards in more crates

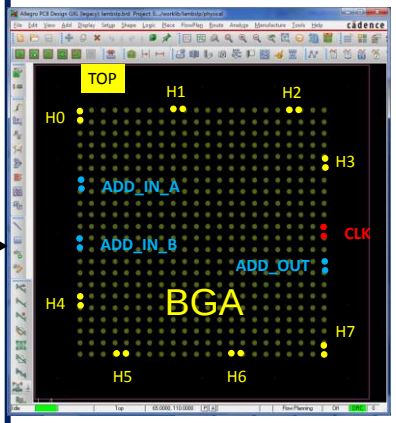
(2) *Reduce further* AMchipnew core consumption: down from 1.2 v to 0.6 v: ***new LP custom cell.***

AM System (2): Why Serialized I/O

TSMC-65 nm:
Too many GND/VCC pads needed

Reaction:

AMchipnew⟶ all buses **serialized** ⟶ recently **purchased IP**.
use 23x23 mm^2 **BGA** instead of **LQ208**



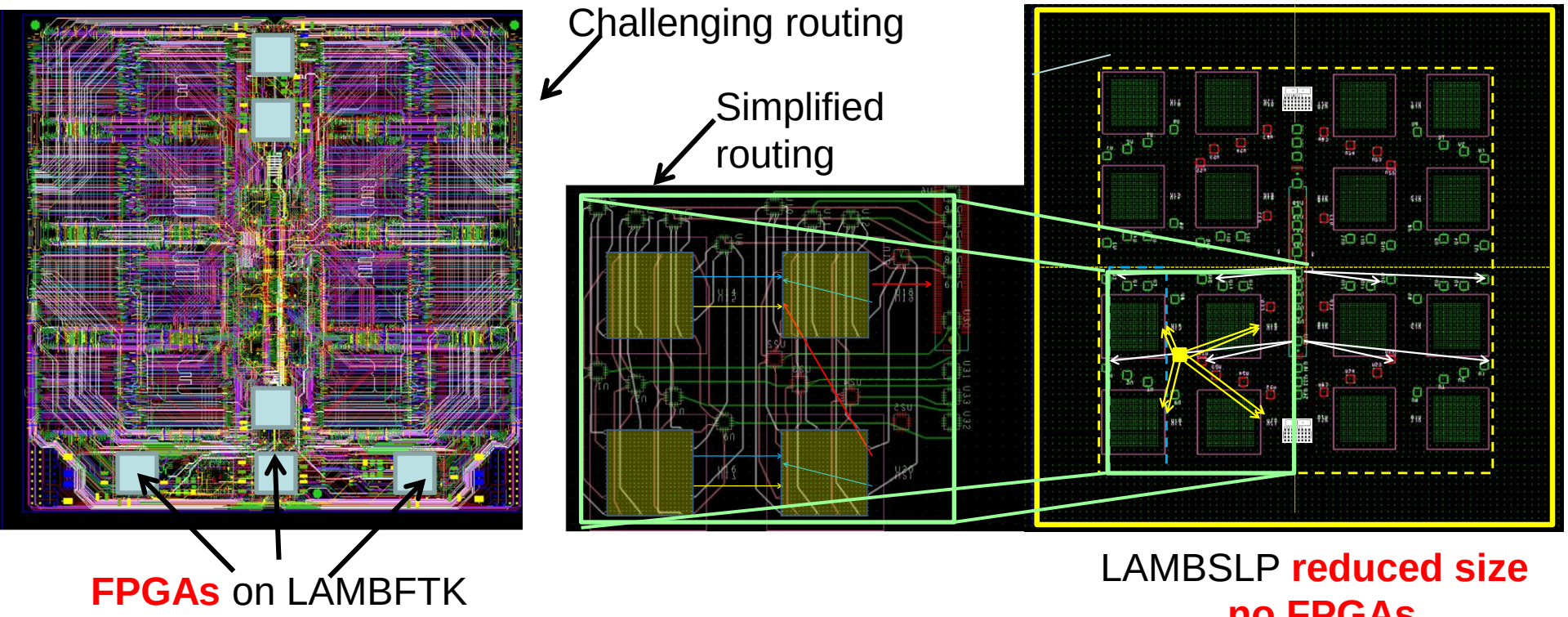
Status:

Miniasic ⟶ taped out **March 2013,** expected **middle of June**. Package QFN64
Test stand for miniasic: under design, should be **ready for June**
Small MPW (amchip05) complete of all functions & **new LP custum cell** ⟶ **under design**
AMchip06: 64 or 128 kpatt chip, w **new custum cell** ⟶ **under study**

Schedule:

Miniasic test: ***Summer '13***
AMchip05 (Small MPW) ⟶ ***tape out July 26 or August 10 ('13)***
AMchip05 delivery: ***Nov-Dec '13***
AMchip05 test: ***Next Winter***
AMchip06,⟶ ***tape out late Spring '14 - pilot run (expected new funds for this)***
AMchip06 delivery: ***early Autumn '14***
AMchip06 tests: ***Autumn '14- Winter '15***

AM System (3): A new LAMB for AM chip05: all buses on serial links



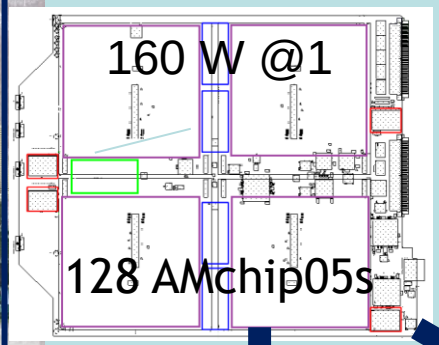
BGA with **Flip chip** technique:

(1) high frequency solution for 2.5 Gb/s links
(2) Caps included in the package to be able to solder BGA on both sides **(32 BGA/LAMB)**
(3) Possibility of **multi-packaging**
(4) ***AMchip05 more expensive*** *than expected (IP, flip chip BGA, multipackaging)*
INFN budget insufficient → the ***AM system*** *try to become* ***EUROPEAN***

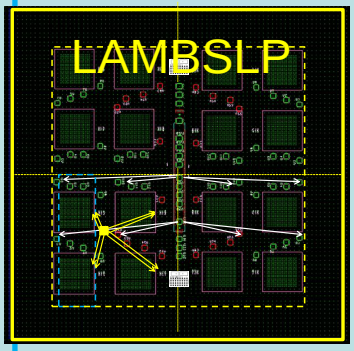
AM System (5) new version of AMB

AMBFTK for AMC04(PI-MI-PV))

AMBSLP for AMC05 (Europe)



Miniasic
Test-LAMB
QFN64
1.92 x 1.92
mm^2



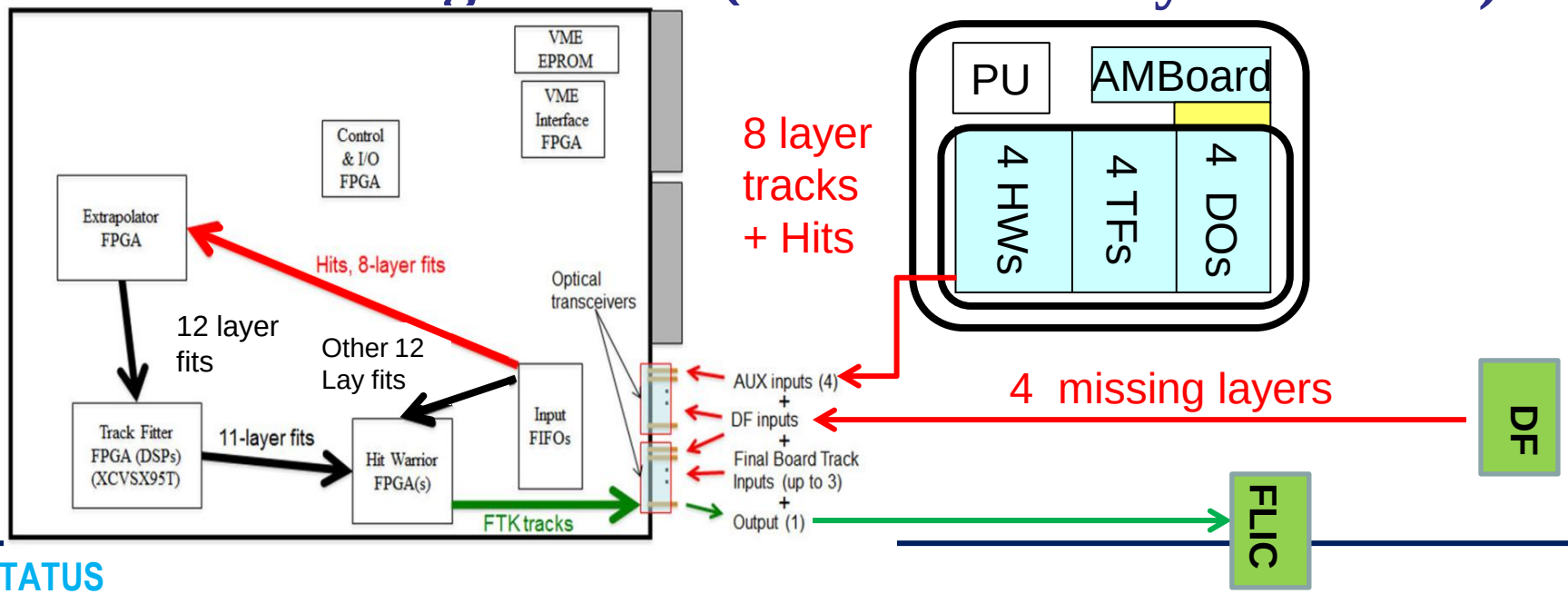
SCHEDULE

AMBSLP: PCB expected ***Summer. '13***
LAMBminiasic: PCB expected ***June. '13***
Tests w minisic: ***Summer '13***
LAMBSLP: PCB expected ***Aut. '13***
Tests w AMCHIP05: ***Autumn '13-Winter '14***
Integration AMB (AMchip05)/AUX: ***next winter***
Integration w AMCHIP06: ***Autumn '14***
Small Production/Install. PUs : ***Wint.-Spr. '15***

STATUS

- **AMBFTK** consistent with **AMchip04** - **tested** with the Proto-AUX.
- VME communication and the high speed serial links are OK even on long distances and through connectors.
- New Serial Link Processor under design: **AMBSLP** and **LAMBSLP for QFN64 (miniasic) and BGA**

Second Stage Board (SSB-University of Illinois)



STATUS

- SSB: **full 12-layer fit**: (a) receives 8-layer good tracks from the PU (b) find hits in the missing 4 silicon layers, (c) fit tracks with 12 lay, (d) removes duplicates.
- basic firmware functions written, testing in progress.
- After that, board design will be finalized.
- An engineering review is planned for April, with a prototype to be built shortly after.

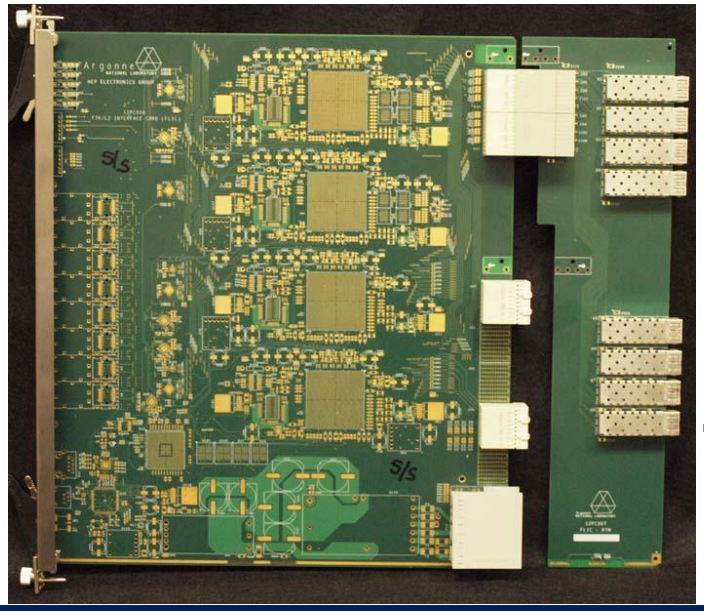
SCHEDULE

- Stand-alone test **Summer '13**
- Integration with FLIC ***Autumn '13***
- Integration with AUX **Autumn '13**

Global Integration: ***Spring –Summer '14***
Small Production: ***Summer '14***
Installation: ***Autumn '14***

FTK-to-Level-2 Interface Crate (FLIC-Argonne)

SSB: Final Fit - HW



ROS

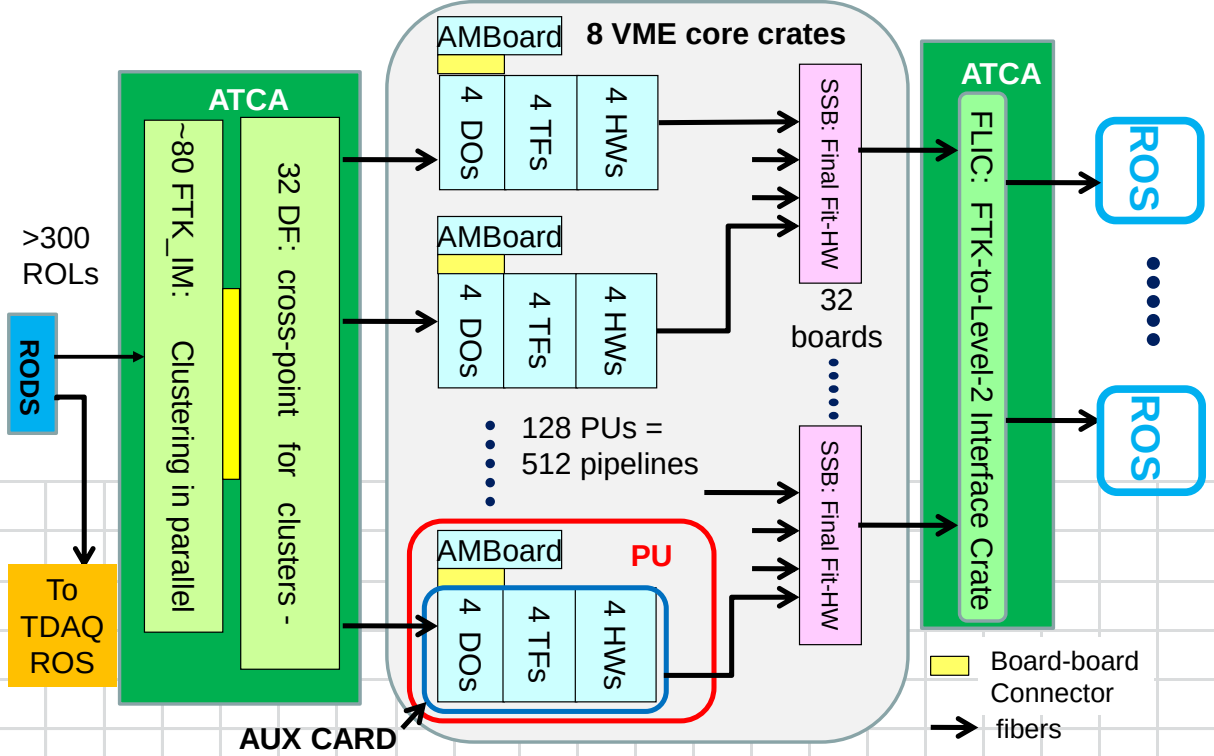
- FLIC sends tracks to ROS's
- ATCA favors communication for global functions like primary vertex finding.
- As with the DF, an early prototype is needed to start exercising the new (to us) ATCA standards.
- first prototype board ready and under test

STATUS

Schedule

- first prototype tested standalone ***Spring '13***
- Integration and test w SBB ***Autumn '13***
- Global Integration: ***Spring-Summer '14***
- Production: ***Summer '14***
- Installation: ***Autumn '14***

Schedule Summary for 2015 8-16 PUs



Legenda
Asic submission
Stand-alone test
Integrated test
Global Integration test
Production - Installation

Months	7	8	9	10	11	12	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3	4	5	6
Tasks	2013						2014												2015					
Dual Output HOLA												test												
FTK Input Mezzanine	w IBL			w DF/RODs						Global Int.														
Data Formatter	test			w AUX						Global Int.														
Miniasic	test																							
AMchip05	tapeout				test																			
AMchip06											tapeout					test								
AMBSLP-Mini-LAMBSLP		test																						
AMBSLP-LAMBSLP					w AM05		w AUX			Global Int.							w AM06		8-16 PUs					
AUX CARD	test			w DF			w AMBSLP			Global Int.			8-16 PUs											
Second Stage Board (SSB)	test			w FLIC/AUX						Global Int.														
FTK Level-2 Interface Crate (FLIC)	test			w SSB - ROS						Global Int.														

Many activities in FTK lab – Pisa (april 2013)

Paola Giannetti
(INFN) Pisa
FTK Project leader

Marco Piendibene
(University of Pisa & INFN)
Engineer, HW/FW expert
Hardware responsible

Saverio Citraro
(University of Pisa & INFN)
HW/FW engineer

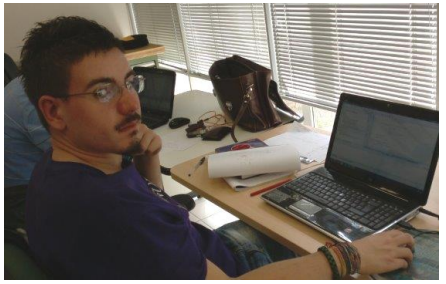
Daniel Magalotti
(University of Modena and Reggio Emilia – INFN Perugia)
Engineer, HW/FW expert
Firmware responsible

Andreas Sakellariou
*(Prisma Electronics, Greece – **IAPP collaboration**)*
Engineer, HW/FW expert

Pierluigi Luciano
(University of Pisa & INFN)
HW/FW engineer (student)

Calliope-Louisa Sotiropoulou
*(Aristotle University of Thessaloniki , Greece – **IAPP collaboration**)*
Physicist, HW/FW expert

Riccardo Cipriani
(University of Pisa & INFN)
HW/FW engineer (student)



Milestones & Conclusions

Milestones

- Before August ‘14: Global integration with AMchip05 (small AM bank)
- Autumn ’14: Production and Installation of all boards except AMBSLP+ that will come later (waiting AM06)

Conclusion

- All the prototypes are in advanced status and soon we will know test results
- The schedule is tight, especially for the AMBSLP board. No contingency

Crate needed Power

LAMB power for **AMchip** (from AM04 measur.) **~57*4=230 W** as expected

AUX power **~75 W**

Crate Power ~ (75+57*4) * 16 = **4850 W** **was OK**

BUT **Serial links** add a not negligible contribution:

~ **30 W** for each LAMB and **24 W** for AMBSLP: Tot~ (4*30+24)*16 = **2300 W**

TOO MUCH

FURTHER REDUCTION of *AMCHIP CONSUMPTION* and *LARGER BANK* (128 Kpatterns) will *RENORMALIZE* THE TOTAL CONSUMPTION

~5 KWATT

AM System (4) IAPP and STREP FP7 applications for extra funds

People Manpower
Funded 1.5 Meuros
Starts Feb 2013

ICT - funds for Amchip – **requested to EC 3 Meuros**
(**in March the result**)

UniPisa (Pisa) Dell'Orso - **AM system boards**
LPNHE (Paris) Calderini - **AMchip** (applied also to its funding agency)
AUTH (Tessaloniki) Kordas **board firmware – simulation**
CERN (TE-MPE-EM section) Formenti **board design**
CAEN (Viareggio) Petrucci - **Integration**
Prisma Electronics (Alexandroupolis) Mermigli
board development, assembly, test – firmware

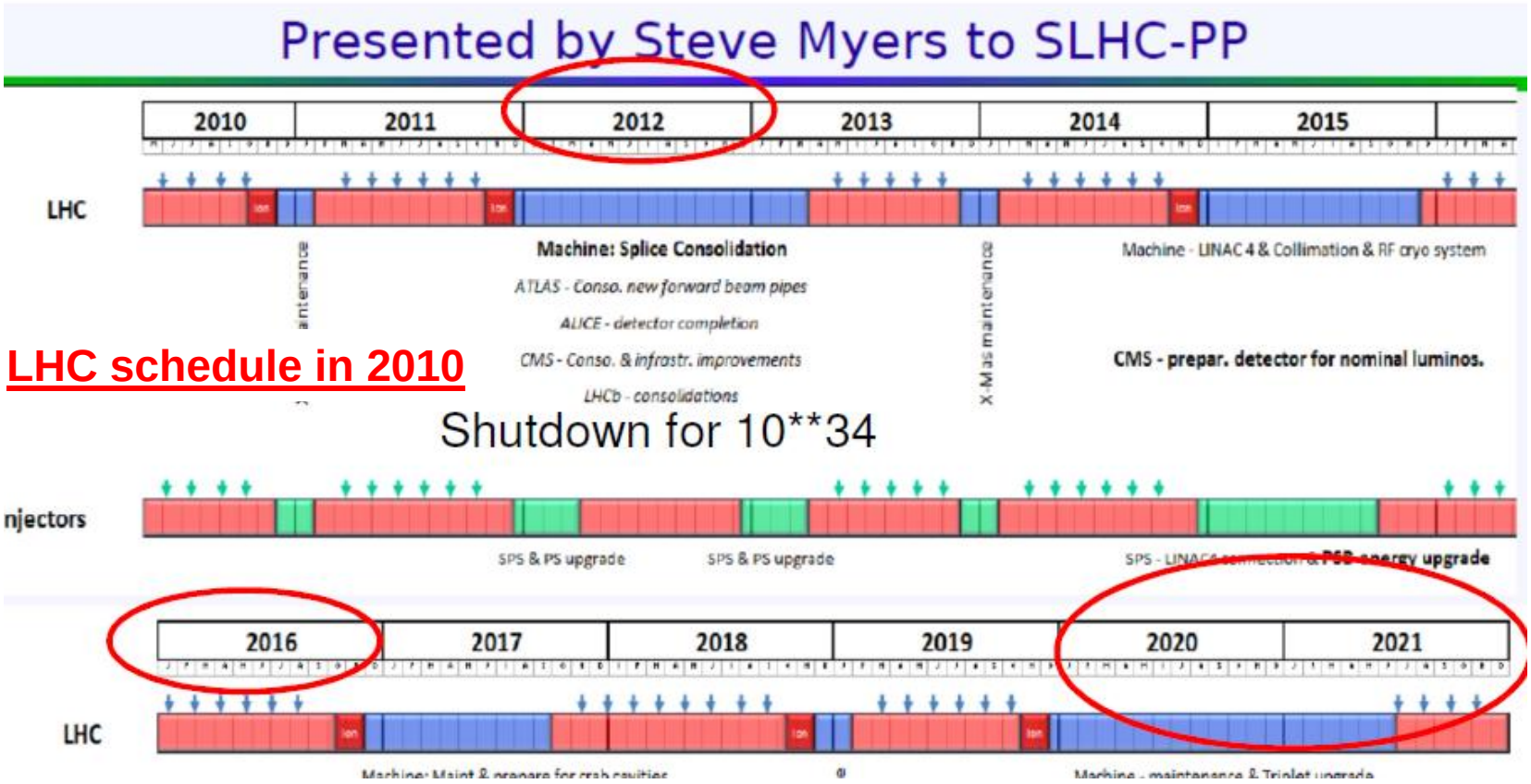
IAPP consortium

Strong technical support

STREP (coordinator INFN) would add for FTK:
University of Geneva on **AM system Boards** (applied also to its funding agency)
……

IMEC for **flip chip multi-packaging** and AMchip submissions to TSMC
MICROTEST - **test setup** for AMchip massive production tests

Strong technical support



LHC schedule in 2010

Workplan at review time (Dec. 2010)

- 2012 or 2013 installation of all Hola2 during long shutdown
  Substitute them in small bunches, reconnect to TDAQ & test;
  FTE: 2 months, may be more. Procedure to be established with ID people
- 2013 enlargement of vertical slice to cover the barrel first (8 or 16 PUs)
  FTE: 4x8 months?
- 2013-2014 data taking
- 2015 extension to the forward/backward detector regions *FTE: 3x5 months?*
- 2015-2016-2017 increase computing power as needed *FTE: 3x4 months?*

LHC Time-line (CERN DG at ICHEP 2012)

(See also DG New Year Presentation on 6th Jan 2013)

https://indico.cern.ch/getFile.py/access?resId=0&materialId=slides&confId=219327

2009 — Start of LHC

Run 1: 7 and 8 TeV centre of mass energy, luminosity ramping up to few 10^{33} cm^{-2} s^{-1}, few fb^{-1} delivered

2013/14 — LHC shut-down to prepare machine for design energy and nominal luminosity

Run 2: Ramp up luminosity to nominal (10^{34} cm^{-2} s^{-1}), ~50 to 100 fb^{-1}

20**18** — Injector and LHC Phase-I upgrades to go to ultimate luminosity

Run 3: Ramp up luminosity to 2.2 x nominal, reaching ~100 fb^{-1} / year accumulate few hundred fb^{-1}

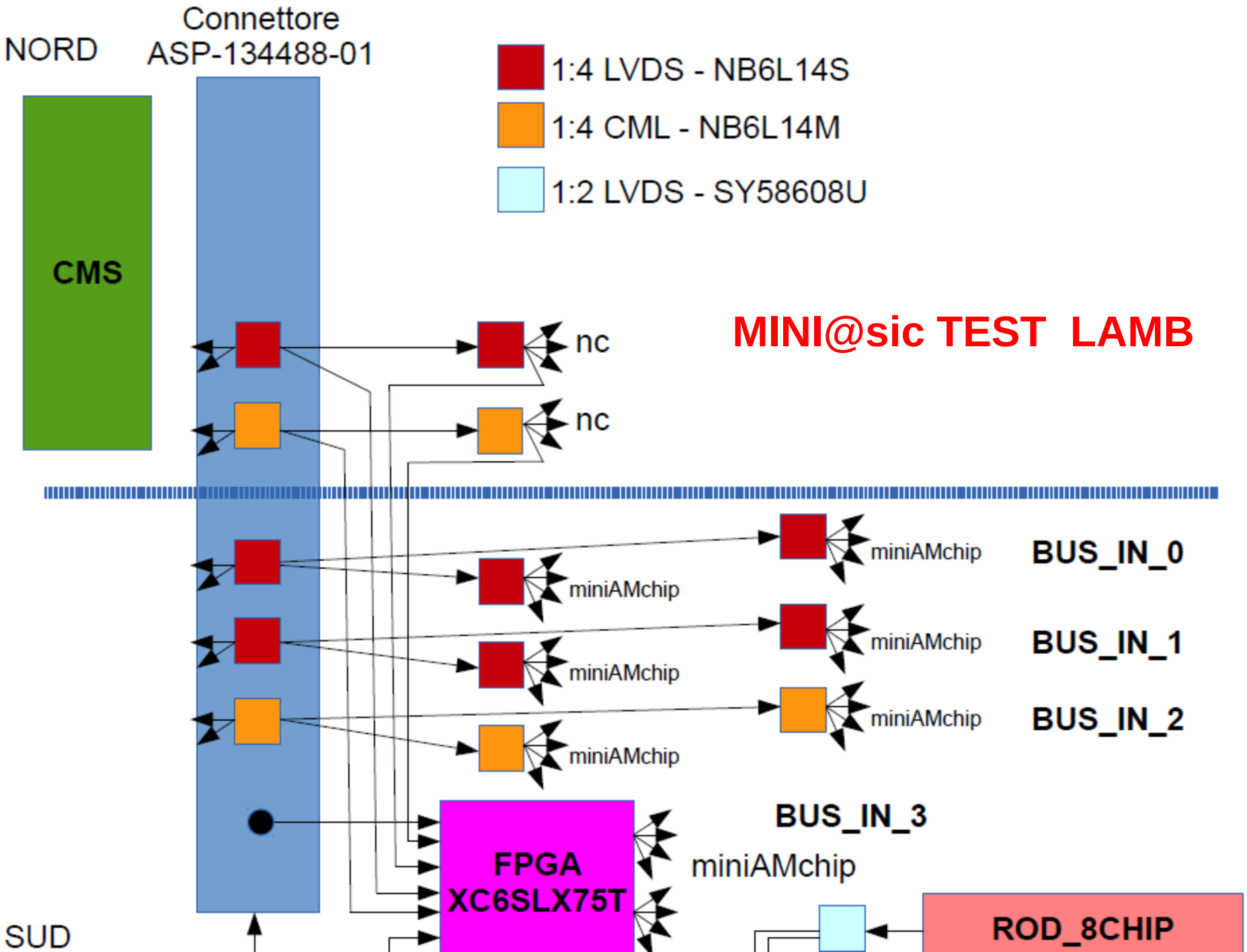
~20**22** — Phase-II: High-luminosity LHC. New focussing magnets for very high luminosity with levelling

Run 4: Collect data until > 3000 fb^{-1}

2030

(Could go further and need to worry about high μ before going to 25ns)

(We assume up to $3\times10^{34}cm^{-2}s^{-1}$ and 25ns, so should plan for μ up to 81)


NORD
Connettore
ASP-134488-01
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1:4 CML - NB6L14M
1:2 LVDS - SY58608U
CMS
MINI@sic TEST LAMB
nc
nc
miniAMchip
miniAMchip
miniAMchip
miniAMchip
BUS_IN_0
BUS_IN_1
BUS_IN_2
BUS_IN_3
miniAMchip
FPGA
XC6SLX75T
ROD_8CHIP
SUD