Cylindrical GEM Inner Tracker for BESIII

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Present ASIC designs at TO-INFN and future perspectives for BESIII CGEM

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Torino Group

Torino Univ./INFN group:

- **hardware and electronics**
  - Michela Greco (researcher)
  - Simonetta Marcello (full professor)

- **software and analysys**
  - Fabrizio Bianchi (associate professor)
  - Marco Destefanis (senjor post-doc)
  - Luciano Fava (researcher)
  - Marco Maggiora (associate professor)
  - Stefano Spataro (researcher)

Torino MicroElectronics Laboratory

Experienced senjor researchers:

- Giovanni Mazza
- Angelo Rivetti

Full design and implementation of ASICs since many years

TOFPET ASIC for PET applications (available today):

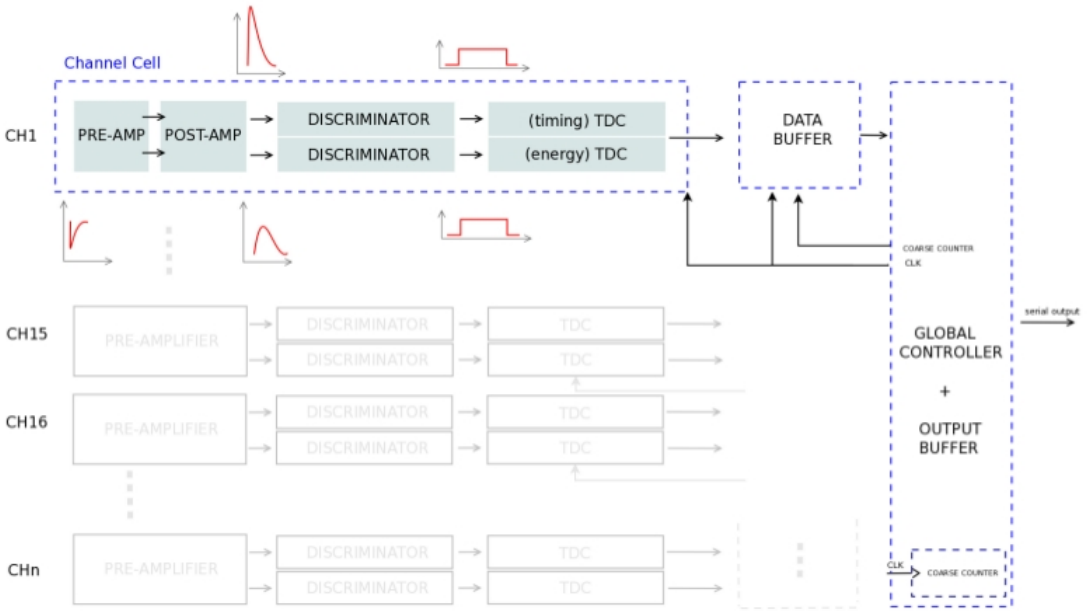
- developed also by a full time Ph.D. student (M.D. Rolo)
- total man power: 1.5y * 2FTE (experienced)
- technology: IBM 130nm
- proceedings:
  - “TOFPET ASIC for PET applications“
    14th INTERNATIONAL WORKSHOP ON RADIATION IMAGING DETECTORS,
    http://iopscience.iop.org/1748-0221/8/02/C02050

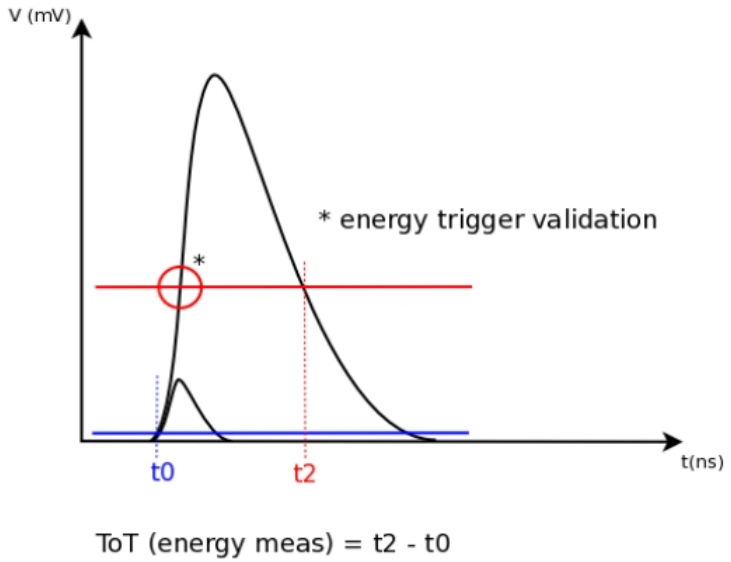
Features of an ASIC for SiPM readout in PET applications

Parameter	Value
Number of channels	64
Clock frequency	80 – 160 MHz
Dynamic range of input charge	**300 pC**
SNR (Q_{in} = 100 fC)	> 20-25 dB
Amplifier noise (in total jitter)	< 25 ps (FWHM)
TDC time binning	**50 ps**
Coarse gain	G_0, $G_0/2$, $G_0/4$
Max. channel hit rate	100 kHz
Max. output data rate	320 Mb/s (640 w/ DDR)
Channel masking	programmable
SiPM fine gain adjustment	**500 mV (5 bits)**
SiPM	up to 320pF term. cap., 2MHz DCR
Calibration BIST	internal gen. pulse, 6-bit prog. amplitude
Power	**< 10 mW per channel**

How these specs impact the choice of the readout chip architecture?

Overview of the channel architecture



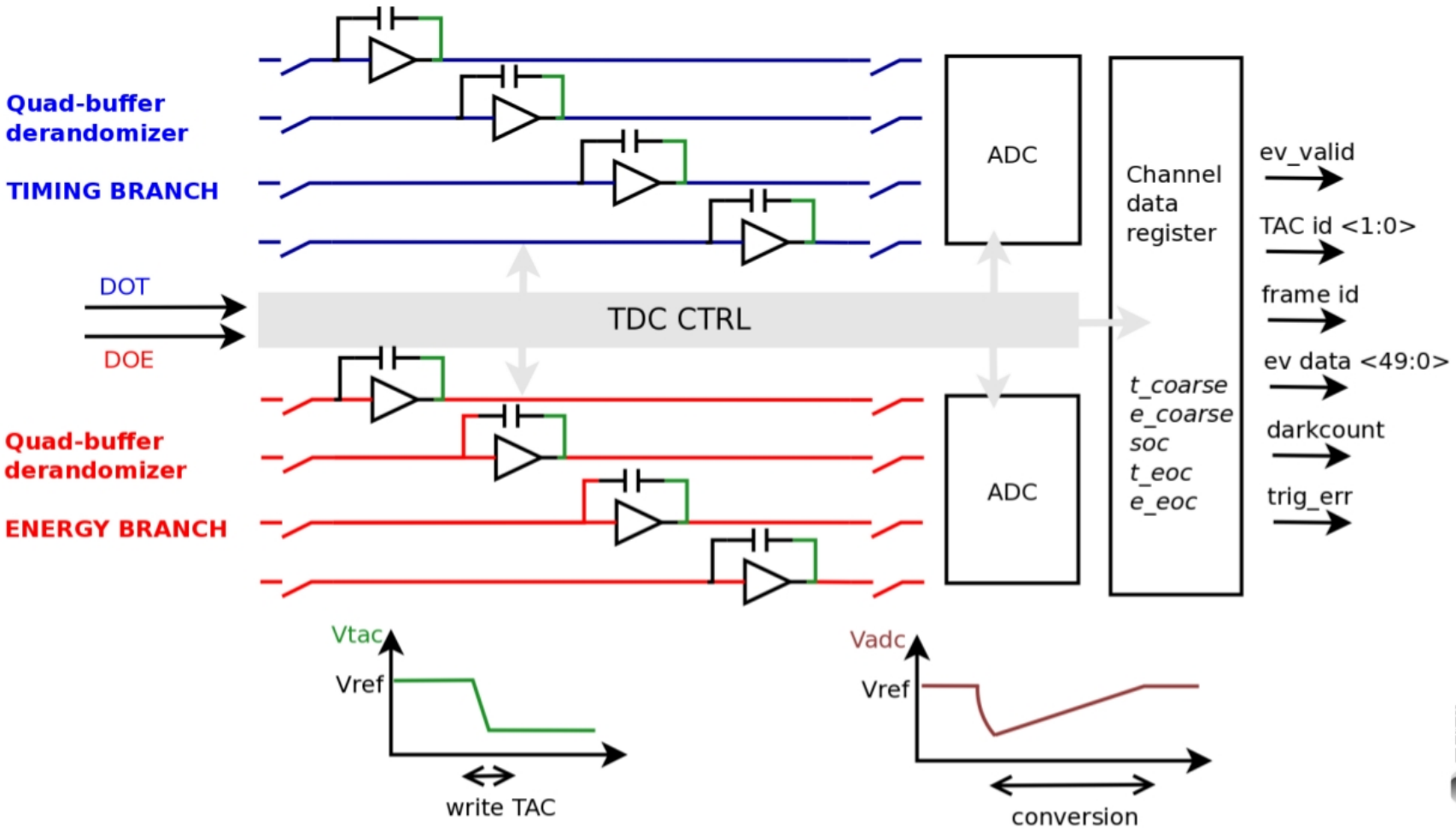


- Time and charge measurements with independent TDCs
- TDC time binning 50 ps
- Charge measured with Time-over-threshold
- Typ. power consumption is 7mW p/channel (**trigger 0.5 p.e.** w/ $SNR > 23dB$ for 9 mm^2 MPPC, 40 KHz event rate, 1MHz DCR)

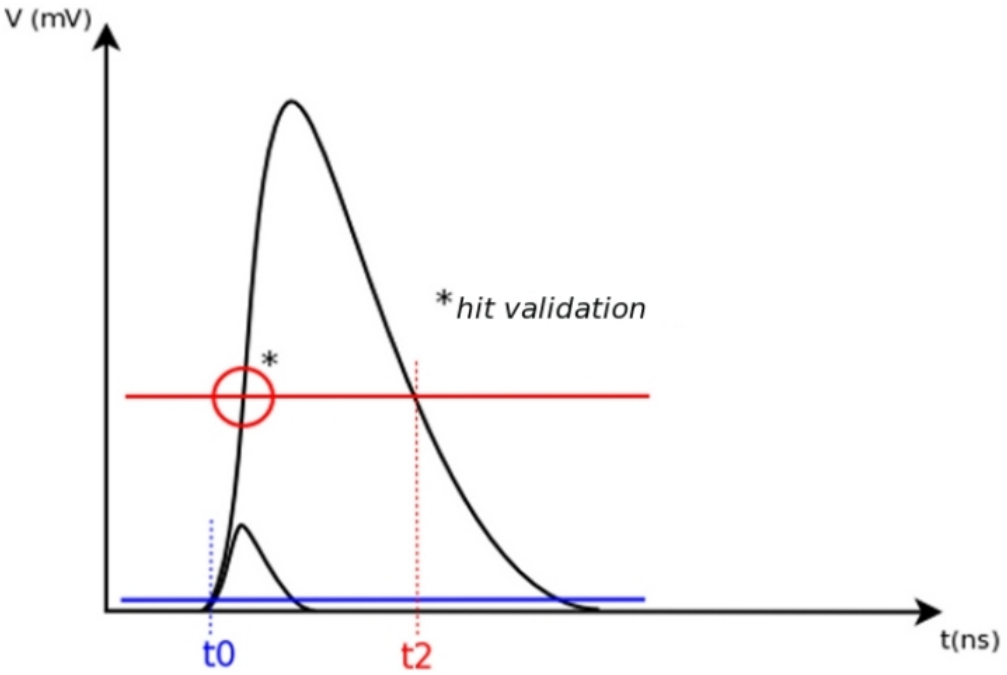
Time-to-Digital Converter

Analogue TDC with 50 ps time binning - based on Time-to-Amplitude Conversion [Stevens89, Rivetti09]

- TDC Control: switching, hit validation, buffer allocation, data reg.
- Time stamp: 10-bit master clock count + Fine time measurement

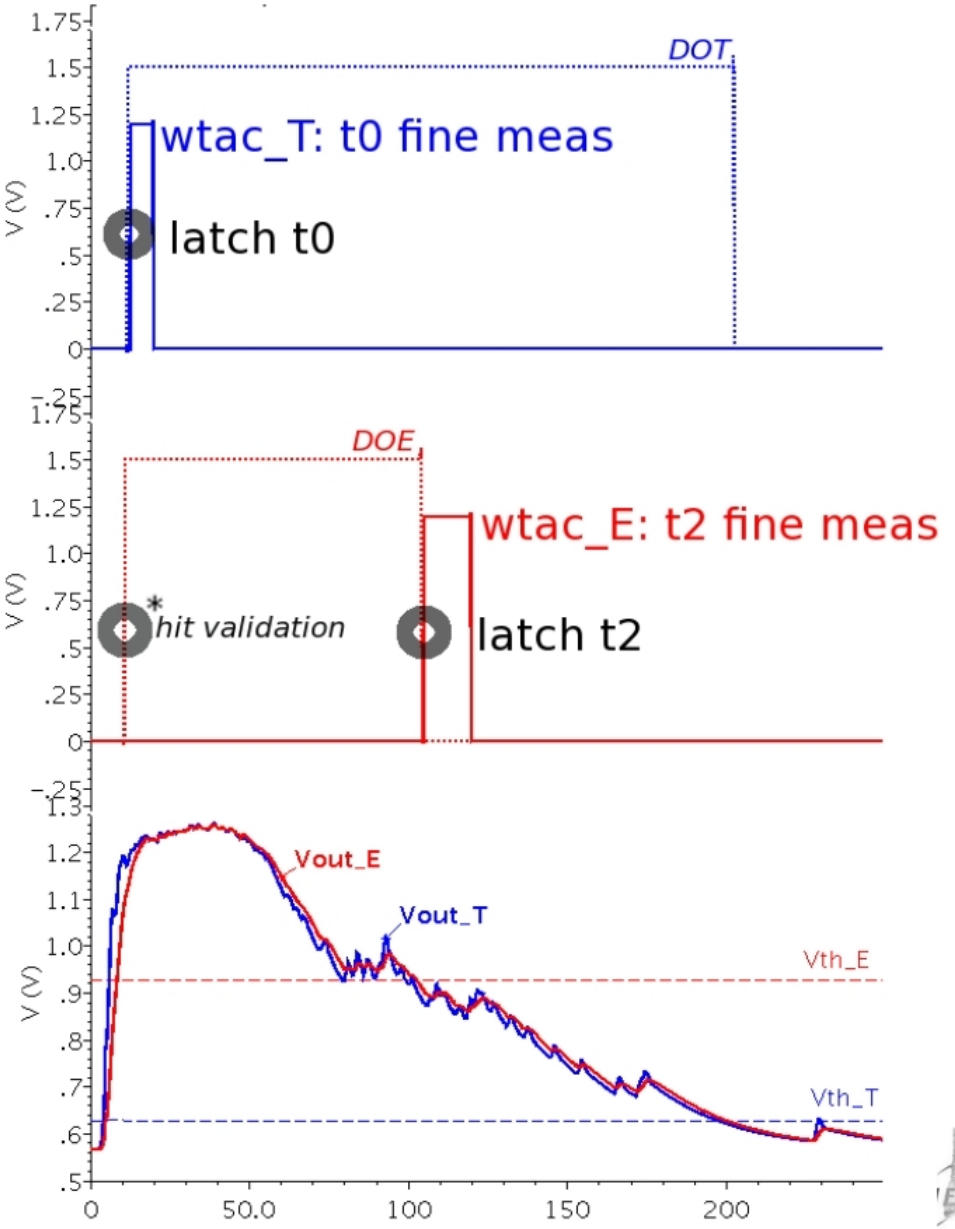


TDC operation for a valid event



ToT (energy meas) = t2 - t0

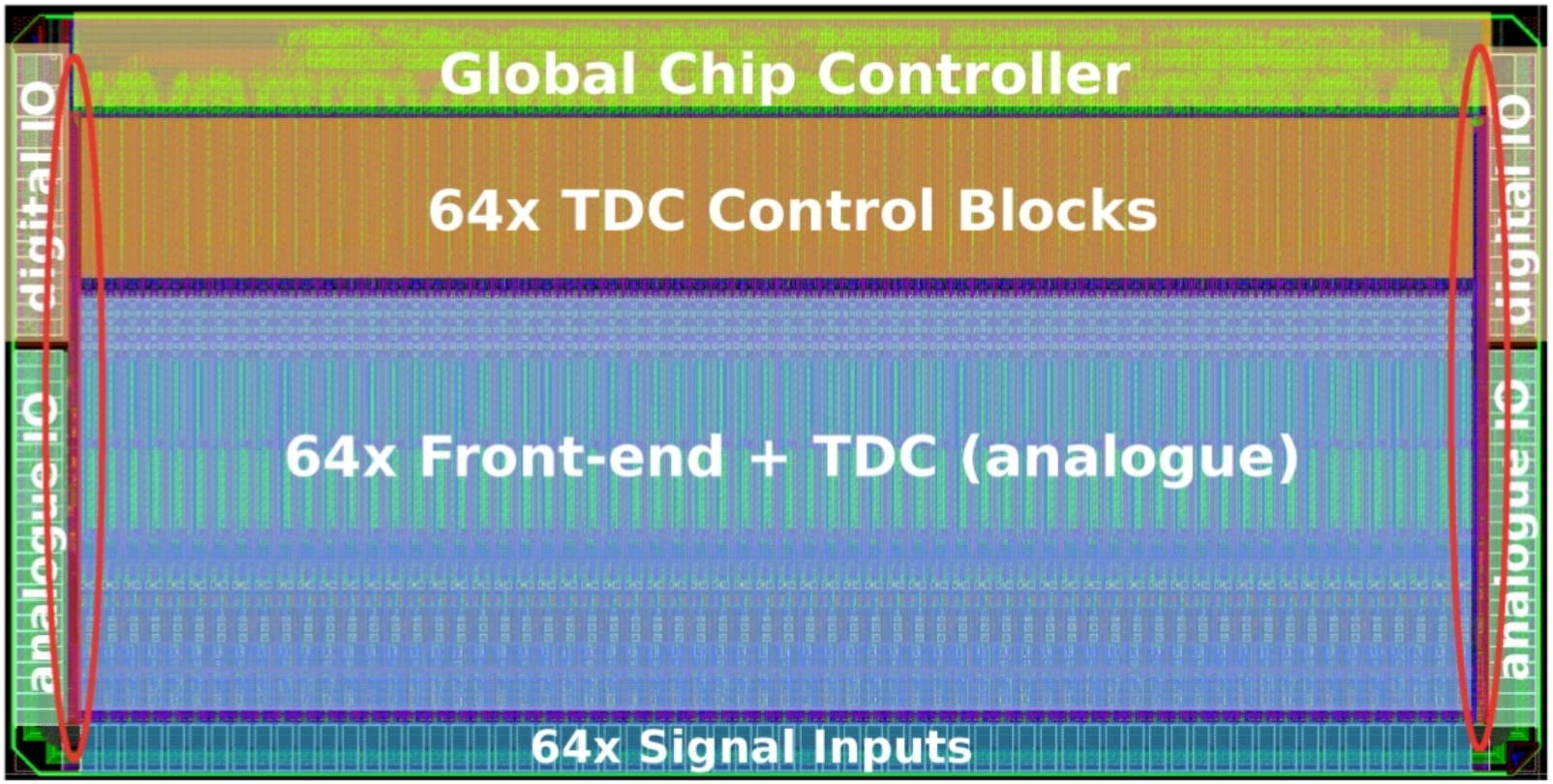
a)



b)

Floorplan of the 64-channel mixed-mode chip

- CMOS 130nm 25mm^2 64-channel ASIC
- Highlight shows the allocated area for bias and calibration circuitry.
- One pad-free edge to allow abutting two twin chips into a 128-channel BGA package.



Future perspectives for BESIII

Torino MicroElectronics Laboratory:

- migration to a newer and cheaper technology:
  - IBM 130nm → UMC 110nm
  - t.o.t. approach
  - lower consumption (4mW/ch)
  - triggerless (FPGA needed to include trigger)
  - should be exportable to P.R.C. (complete implementation in I)
  - tunable gains
  - signals at PANDA:
    - up to 40pF, 2-50 fC
    - data rate: up to 40 kHz/ch (ASIC up to 300 kHz/ch)
    - time resolution: 30 ps
    - FE adapted to silicon micro-strips (PANDA GEM?)
- perspectives for BESIII:
  - mantain BE
  - FE could be redesigned
  - testbed and testing manpower crytical issues

PANDA FE and workshop April, 29th-30th @ ALBA!

Needed information!

Parameters	Min Value	Max value
Input signal (fC)		
Detector capacitance		
Event rate per channel		
Desired number of channel per chip		
Time resolution		
Input referred noise (rms electrons)		
Power consumption per channel		
Radiation load (TiD)		
Radiation load (NIEL)		

Additional important information:

- Polarity of the input signal (positive, negative, either)
- Detailed sensor model with terminal capacitances and resistance
- Information on the signal shape and its fluctuation
- The presence of tails or other artifact in the signal is of primary importante.
- Trigger requirements
- Snapshot of KLOE2 CGEM signal

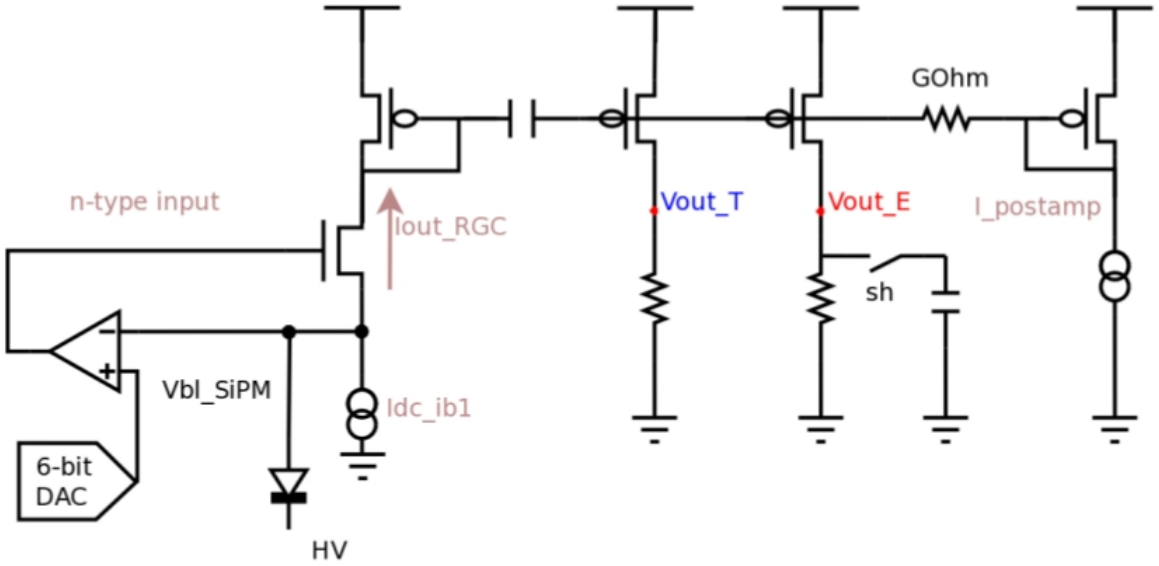
Main goal of this workshop! (for us from Turin..)

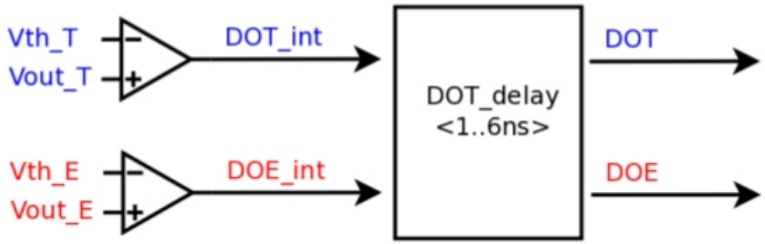
Can CGEM ASIC for BESIII inherit the UMC PANDA design?

QUESTION TIME

Front-End

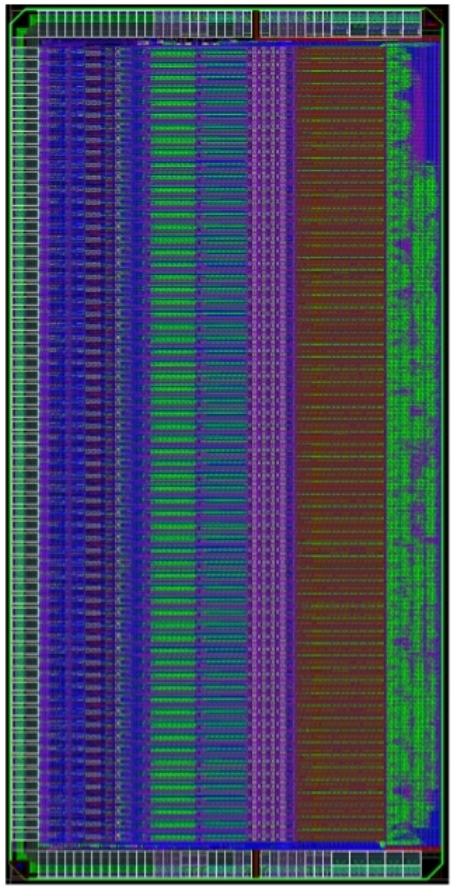
- Low-Zin pre-amplifier, 2 independent TIA branches for Timing and Energy triggers
- Fine adjustment of the HV bias (6-bit over 500mV range) of the SiPM
- Selectable shaping function for Vout_E to avoid re-triggering and correct eventual loss of ToT vs. Qin monotonicity
- Selectable delay line for dark count filtering
- Usable for p-type or n-type (hole, electron collection) devices





Packaging of a 128-channel SiP

- The TOFPET ASIC has one pad-free edge
- That allows a second (rotated) chip to be abutted
- The compact 7x7 mm SiP can be packaged into a BGA



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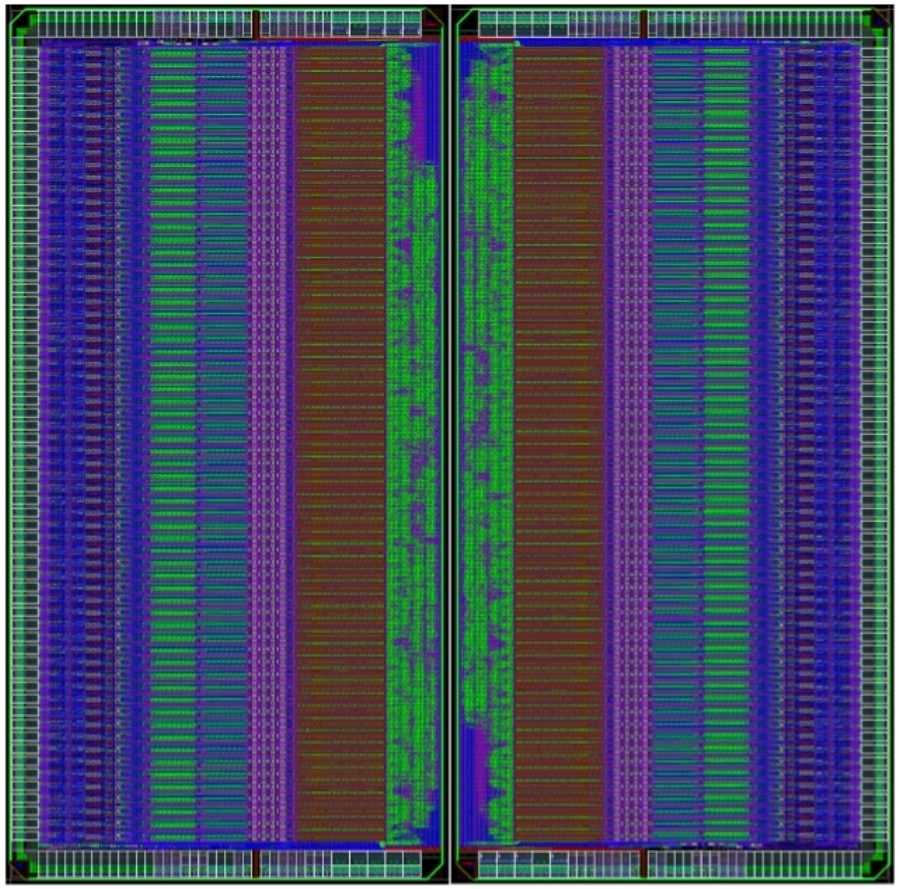

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