



GASTONE64

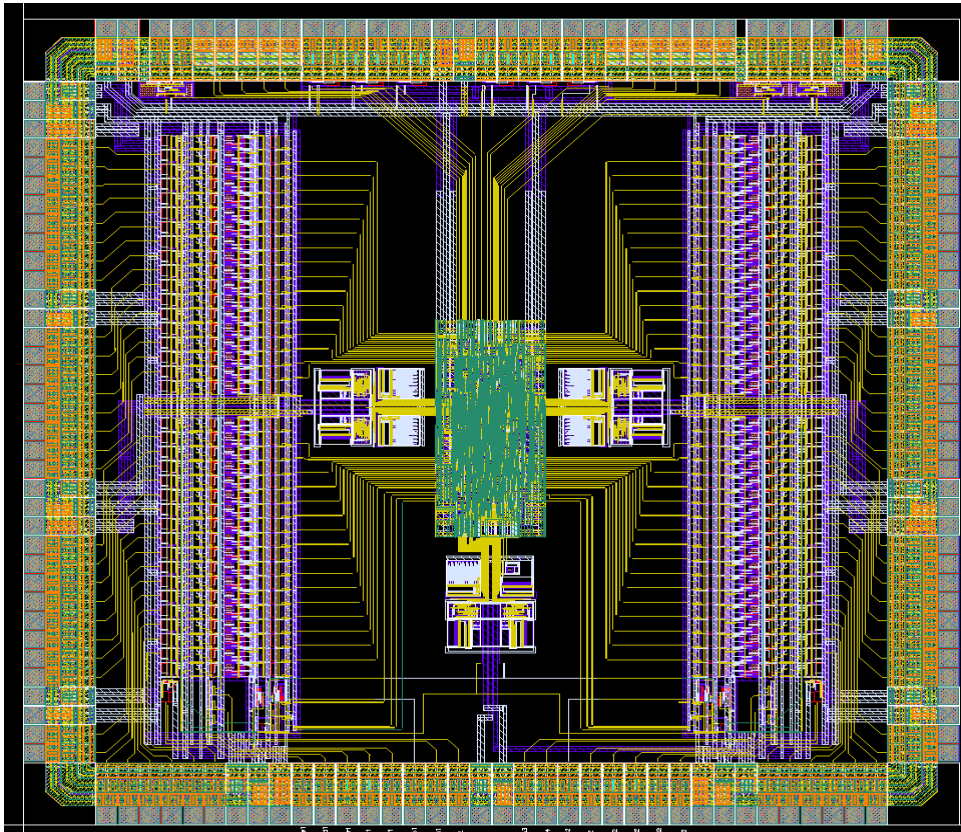
The KLOE IT Front-End Electronics

F. Loddo
INFN Bari

On behalf of KLOE2 IT Sub-group



GASTONE64 layout

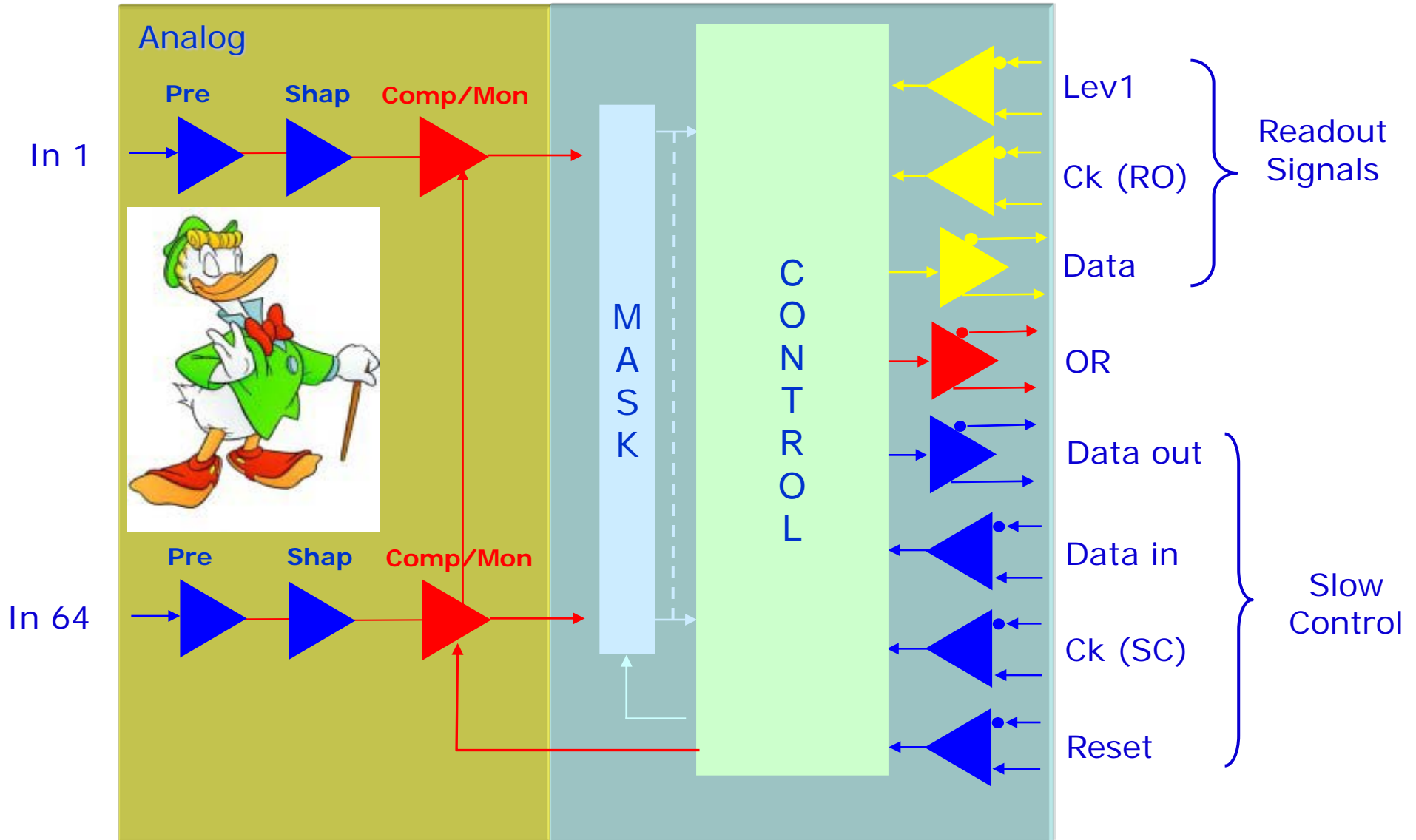


- Technology: CMOS 0.35 μm
- #Channels: 64
- Die area: $\sim 4.5 \times 4.5 \text{ mm}^2$
- Power: $\sim 6 \text{ mW/channel}$
- Package: plastic QFP144
 - $20 \times 20 \text{ mm}^2$
 - pitch: 0.5 mm
 - thickness: 1.4 mm

GASTONE (Gem Amplifier Shaper Tracking ON Events)



Block diagram





Analog Section

- 1 a charge preamplifier to integrate the input strip current into a voltage
- 2 a shaper circuit providing noise filtering and semi-gaussian shaping

Preamp gain	4 mV/fC @ $C_{\text{det}} = 100$ pF
Input impedance	120 Ω
Preamp supply current	~ 280 μ A
Shaper gain	4
Shaper supply current	~ 150 μ A
Peaking time	90 ns
ENC	800 e^- + 40 e^- /pF
Overall charge sensitivity	16 mV/fC @ $C_{\text{det}} = 100$ pF
Crosstalk	< 3%

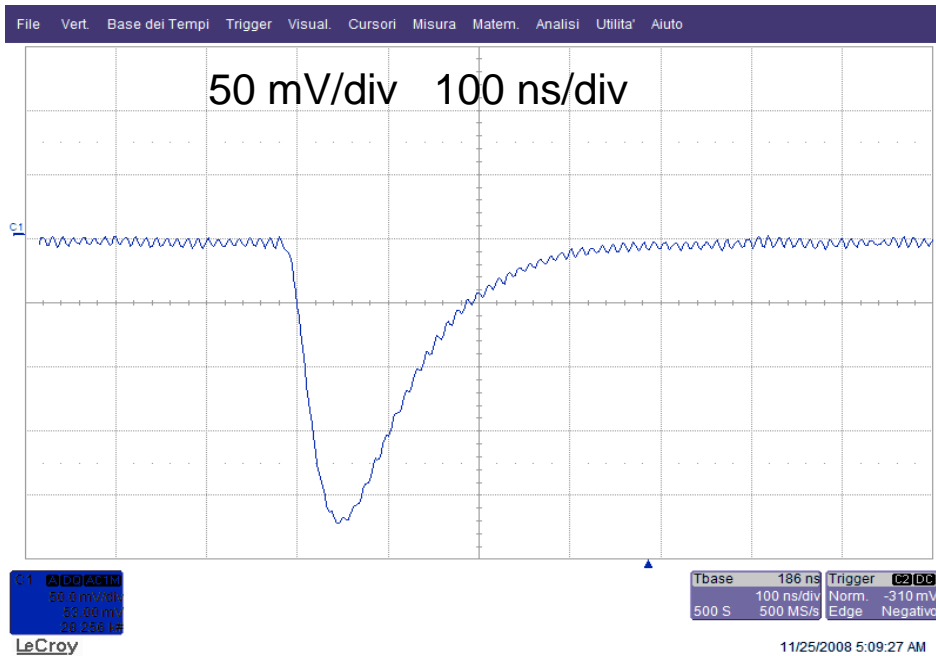
- 3 A leading-edge discriminator

DISCRIMINATOR MAIN SPECS	
Threshold	0 - 30 fC
Offset (rms)	~ 2.2 mV
Supply current	~ 180 μ A

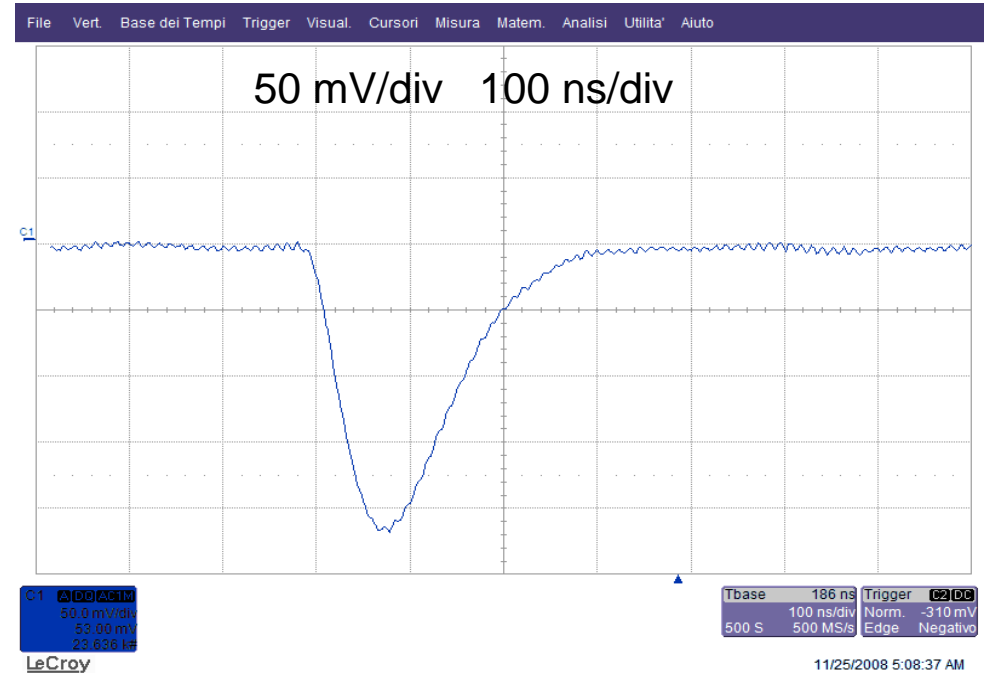


Analog Section

Shaper output ($Q_{in} = 10 \text{ fC}$)



$C_{in} = 10 \text{ pF}$

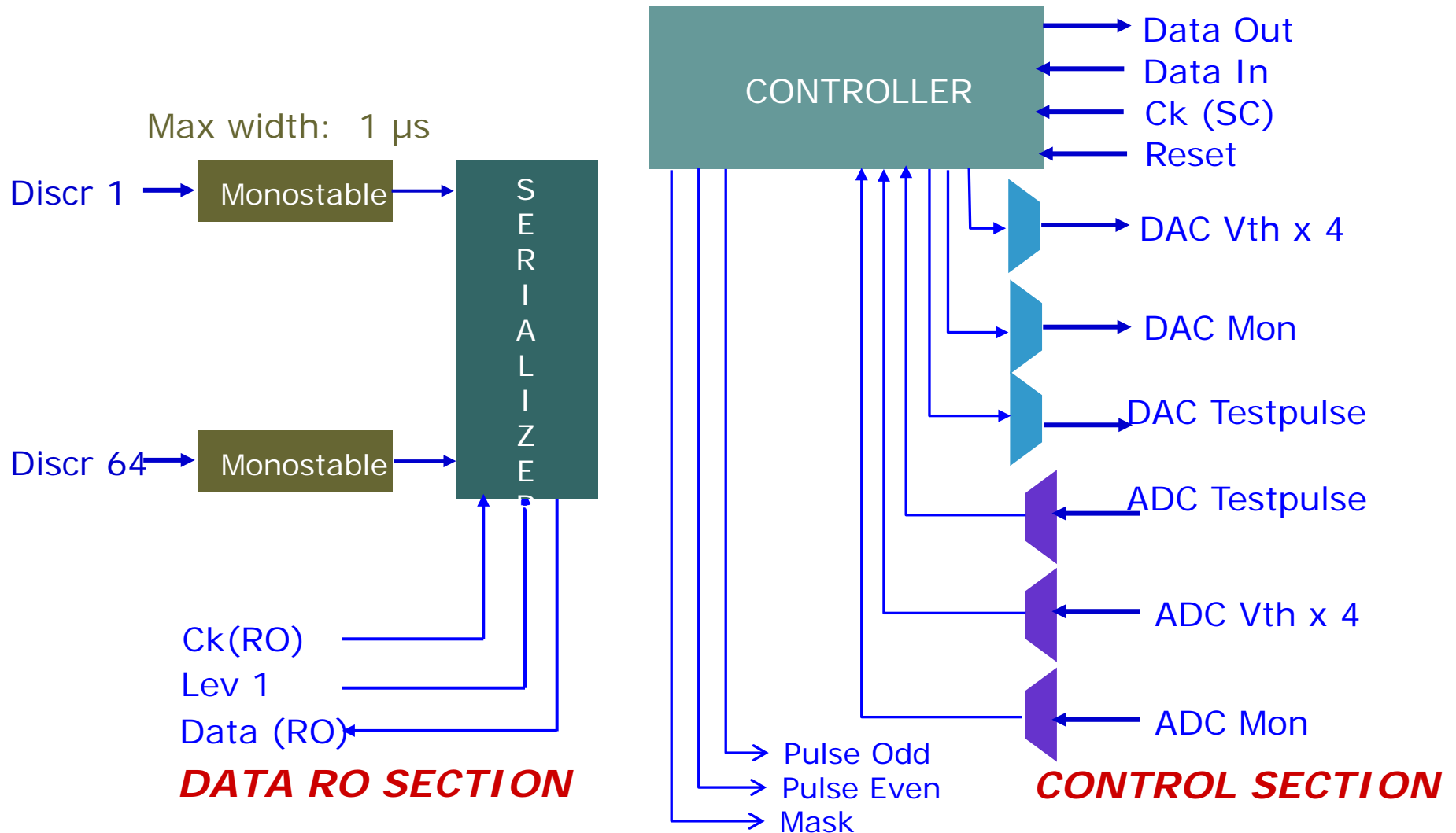


$C_{in} = 50 \text{ pF}$



Digital Section

The digital section contains a **slow-control logic** and a **data readout logic**





Digital Section (Readout)

- Upon the arrival of the trigger signal, the signals coming from the analog section are stored into a 96-bit register
- Each event word contains:
 - 10 bits header
 - 5 bits identifying the trigger number
 - 9 bits for ID chip
 - 64 bits for data
 - 8 bits at '0' ending the data-frame
- The readout clock (50 MHz) is active only during the readout
- Using both clock edges → Serial readout **100 Mbit/s** on LVDS
- The chip also produces a global OR signal to be used for self-triggering applications

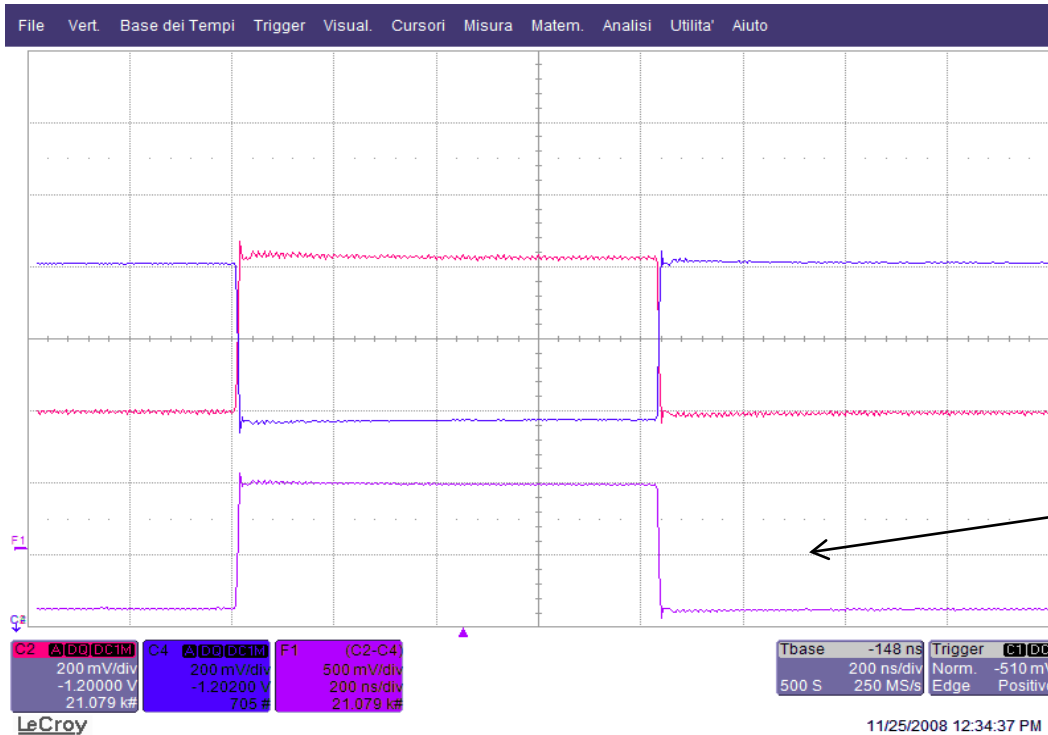


Digital Section (Slow-control)

- 28 **8-bit registers** for configuring the chip functionalities
 - 4 10-bit DACs (1 DAC/16 channels)
 - 1 8-bit DAC for Pulse Width setting
 - 1 10-bit DAC for Test Pulse setting
 - 6 8-bit ADCs for monitoring
- Controlled by a SPI interface port running at 1 MHz.



LVDS driver



LVDS signals

Differential signal

- Common mode: 1.2 V
- Voltage swing: 400 mV
- Differential signal voltage swing: 800 mV
- Capable to drive long lines (20 m)
- Power consumption: 12 mW



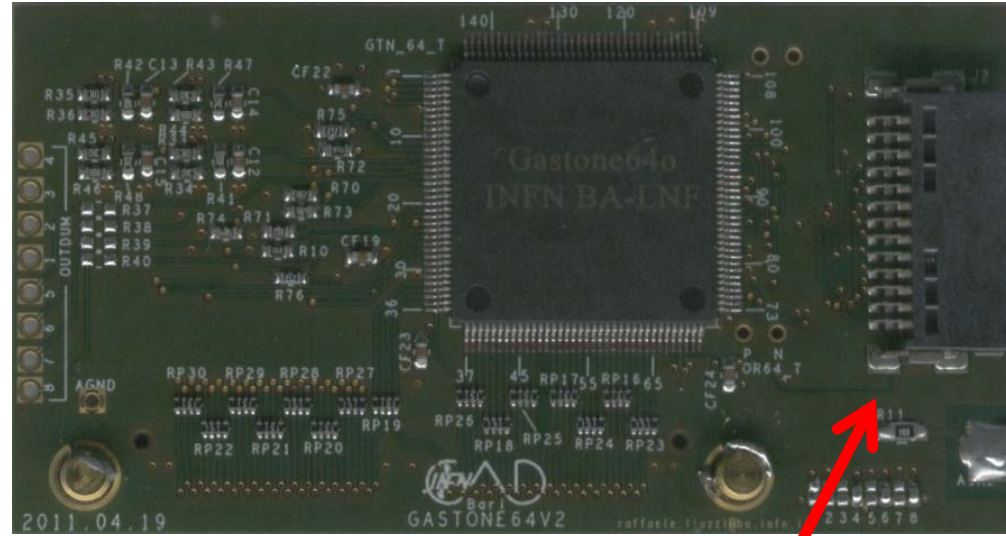
Front-end board (120 channels)

Dimensions: 75x40 mm²



Input connector (GEM)

- 120 strips
- GND



I/O connector

- Power supplies
- SPI slow control bus
- Readout bus

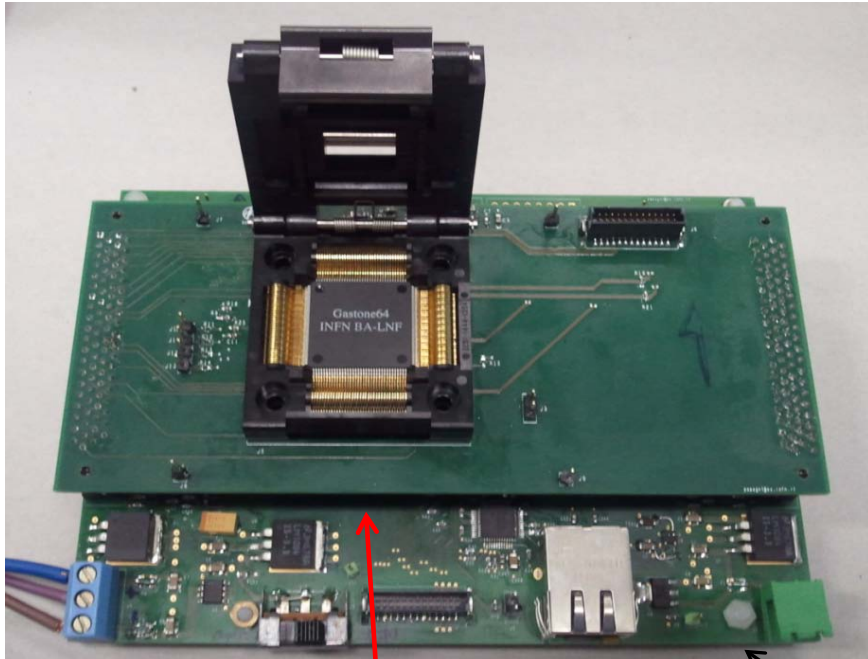


GASTONE64 quality control

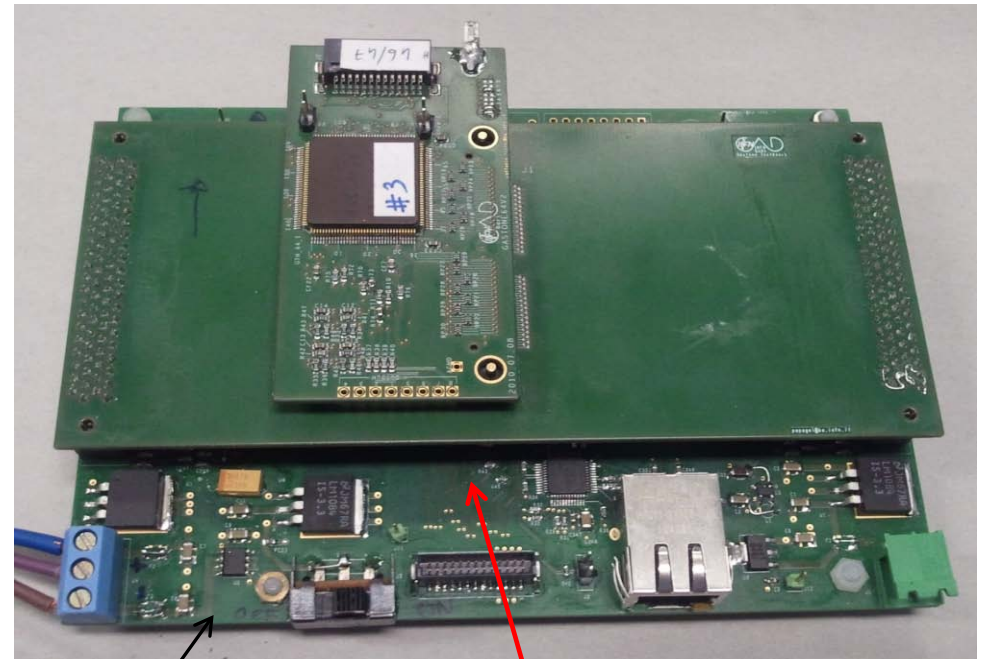
Test bench:

Single mother board Ethernet controlled

- **Piggy-back board housing socket for chip testing (64 channels)**
- **Piggy-back board for FEB testing (120 channels)**



Piggy-socket board

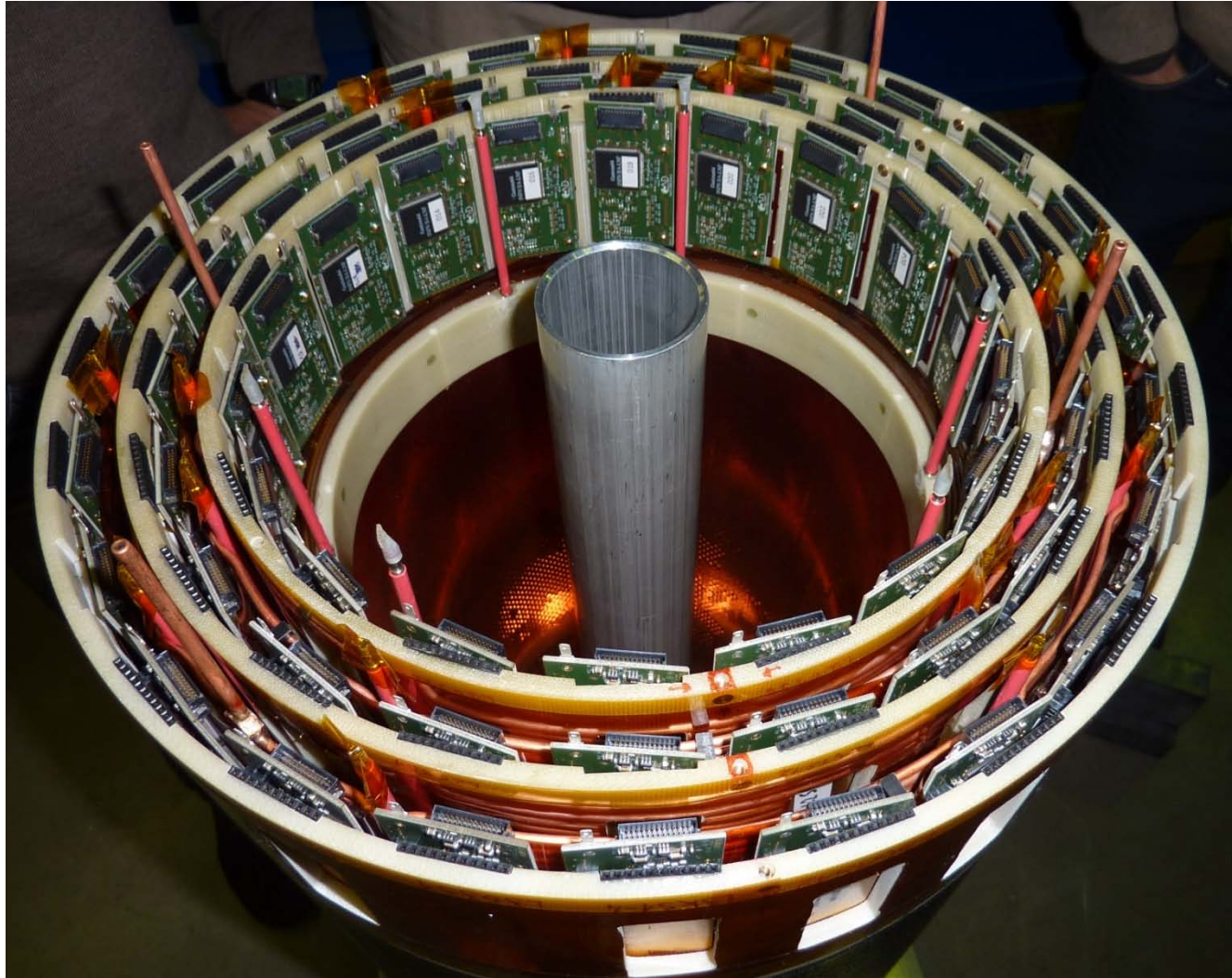


Piggy-FEB board

Mother board



Front-end board installation





Conclusions

- Gastone64 fulfils all the design specifications
- The chips as well the front-end boards have been fully produced and installed in KLOE2 IT
- We are ready to install KLOE2 IT in KLOE apparatus