High Performance Vertexing Devices at the ILC

M. Winter IPHC-Strasbourg)

INFN-LC workshop – Como – 16-17 May 2013

Outline

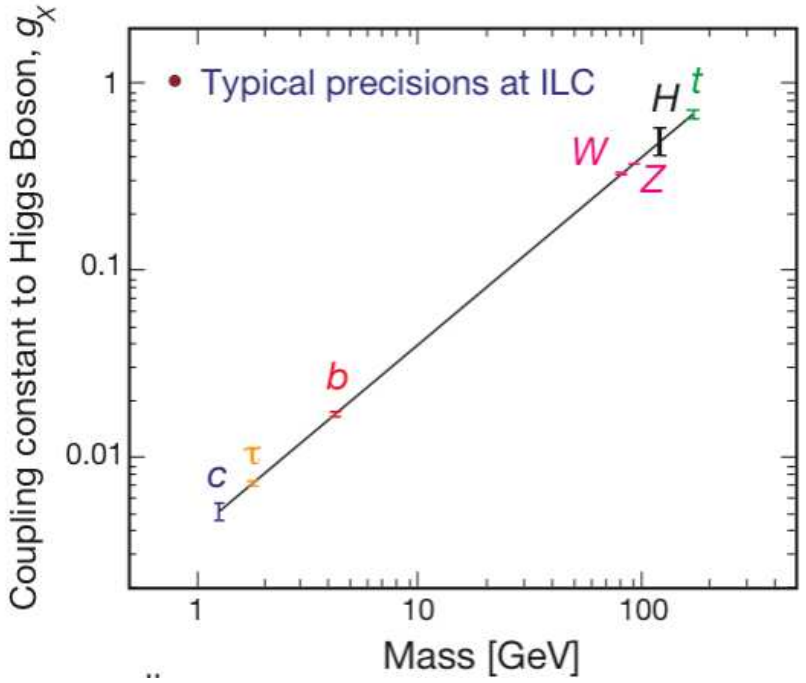
- *Main (conflicting) specifications:*
  - Physics driven specs
  - Running condition driven specs
- *Accelerator related aspects:*
  - Beam related background
  - Time structure
- *R&D goals and on-going activities:*
  - Pixel sensors
  - System integration
- *Summary complemented with poorly covered WP*

Linear Collider Specificities

- VERTEX DETECTOR NEEDED TO :
  - ⁕ reconstruct decay vertex of short lived particles
    decaying (mostly) near beam IP (typically at O(100) μm)
  - ⁕ reconstruct low momentum tracks barely reaching
    the - high resolution - main tracker (B $\sim$ 3.5 - 5 T)

    $\hookrightarrow$ achieve high efficiency & purity flavour tagging

    $\Rightarrow$ charm & tau !!!



- VERTEX DETECTOR SPECS : Ex: Couplings (SM-Higgs-like) particle to elementary bosons & fermions
  - ⁕ unprecedented granularity & material budget (very low power)
  - ⁕ much less demanding running conditions than at LHC (at least up to $\sim$ 1 TeV)

    $\Rightarrow$ · alleviated read-out speed & radiation tolerance requests

    · possibility of coming very close to the IP

The Central Conflict of Vertexing

- A COMPLEX SET OF STRONGLY CORRELATED ISSUES :

  ⁕ **Charged particle sensor technology :**

  · highly granular, thin, low power, swift pixel sensors

  ⁕ **Micro-electronics :**

  · highly integrated, low power, SEE safe, r.o. μcircuits

  ⁕ **Electronics :**

  · high data transfer bandwith (no trigger), some SEE tol.

  · low mass power delivery, allowing for power cycling

  ⁕ **Mechanics :**

  · rigid, ultra-light, heat but not electrical conductive, mechanical supports, possibly with $C_{\Delta t} \simeq C_{\Delta t}^{Si}$

  · very low mass, preferably air, cooling system

  · micron level alignment capability

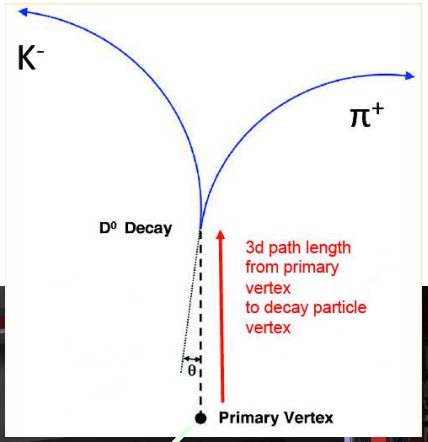
  ⁕ **EM compliance :**

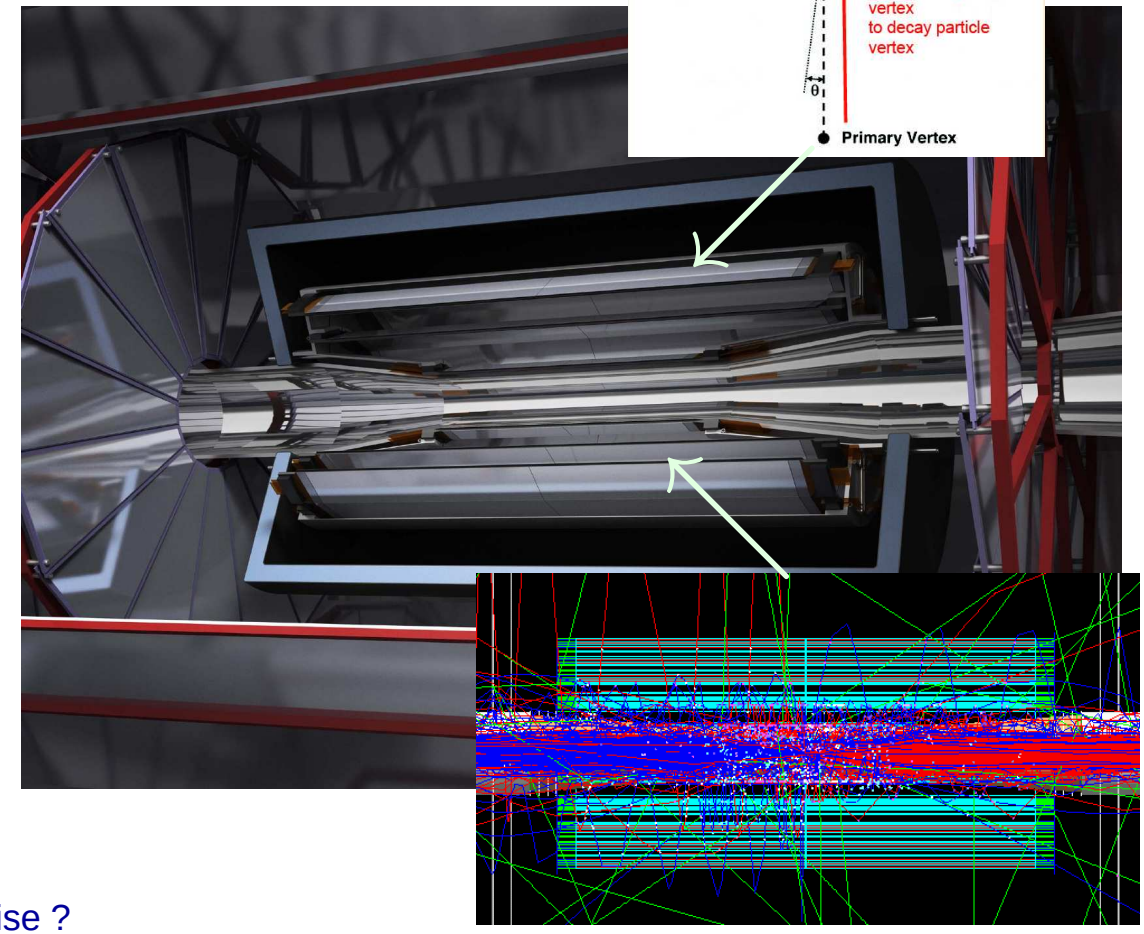
  · power cycling in high B field ⇛ F(Lorentz)

  · higher mode beam wakefield disturbance ⇛ pick-up noise ?

  ⁕ **Radiation load and SEE compliance at T_{room}**

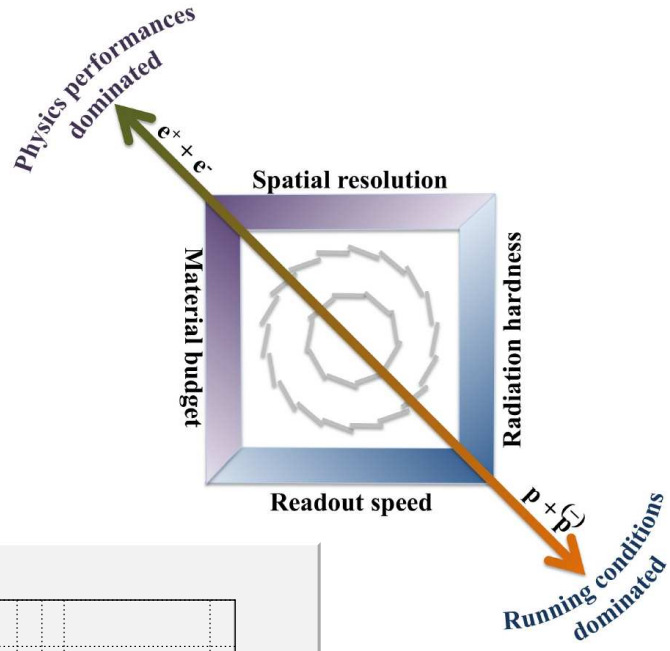
  ⇛ reduced material budget



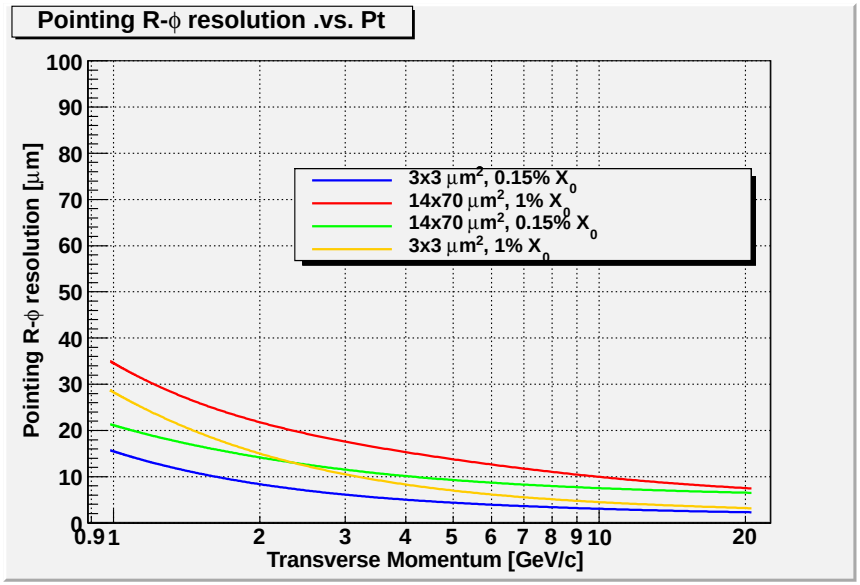


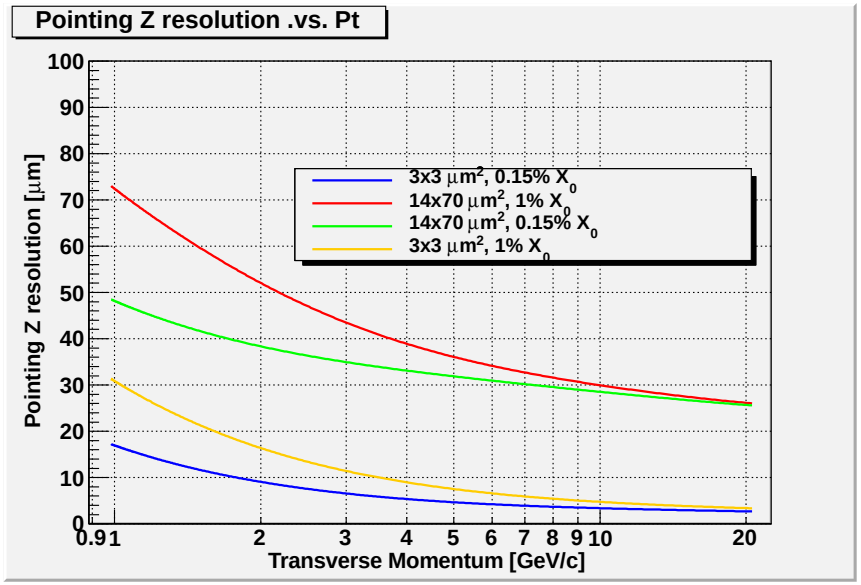
Linear Collider Precision Goal

- SPECIFIC BALANCE BETWEEN CONFLICTING REQUIREMENTS
  - ⁕ Privilege is given to physics driven specifications (esp. $\leq$ 1 TeV)
  - ⁕ R&D rather performed to match running condition driven specifications
- LC VERTEXING GOAL : $\sigma_{R\phi,Z} \leq 5 \oplus 10 - 15/p \cdot sin^{3/2}\theta \ \ \mu m$
  - ▷ LHC: $\sigma_{R\phi} \simeq 12 \oplus 70/p \cdot sin^{3/2}\theta$



▷ Compare $\sigma_{R\phi,Z}$(ILD) with VXD made of ATLAS-IBL or ILD-VXD pixels

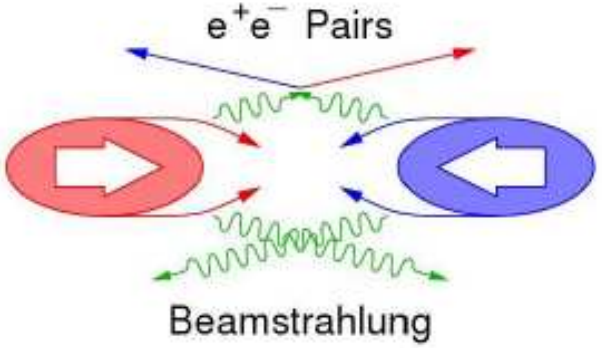




⇒ Significant improvement required wrt present LHC techno: GRANULAR (ϕ, z), THIN, LOW POWER

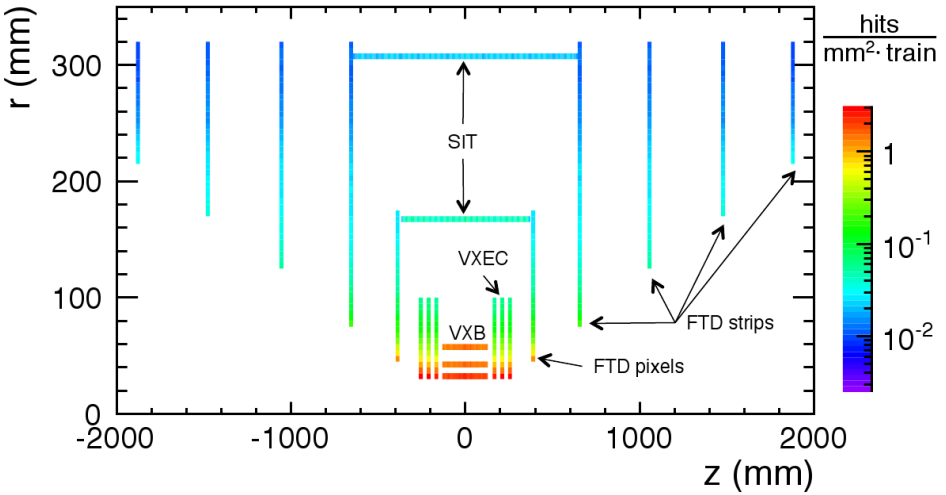
Machine Related Issues

- 2 DIFFERENT MACHINE PROJECTS DRIVEN BY THE LC COMMUNITY :
  - ILC ($\gtrsim$ 2026/27 Japanese roadmap) : $\sim$ 0.2–0.5 $\longmapsto$ 1 TeV
  - CLIC : $\sim$ 0.5 – 3 TeV



- TWO MAIN ASPECTS GOVERN THE DETECTOR SPECIFICATIONS :
  - beam related backgrounds :
    - e^+e^- pairs and $\gamma\gamma$ collisions (CLIC)
    - drive occupancy & radiation load
      - $\hookrightarrow$ annual load: O(100) kRad & O(10^{11}) n_{eq}/cm^2 **($< 10^{-3}$ LHC load !!!)**
  - beam time structure $\Rightarrow$ $<$ 1% duty cycle

    - short bunch trains separated by ”long” beamless periods
    - influences occupancy & allows substantial power saving



- IMPACT OF DIFFERENT ILC AND CLIC RUNNING CONDITIONS :
  - different vertex detector specification hierarchy
    - $\Rightarrow$ different vertex detector geometry and sensor optimisations

Time Resolution Considerations

- TIMING REQUESTS ARE CENTRAL TRACKING AND COLLIDER DEPENDENT :

- OCCUPANCY MANAGEMENT:
  - aim for pixel occupancy $\lesssim$ few 10^{-2} - 10^{-3} (tracking strategy dependent)

    $\Rightarrow$ optimise read-out time $\times$ pixel size (density) $\times$ inner radius

Linear Collider	Bunch train Duration [μs]	N(BX)/train	Inter-bunch Duration [ns]	Inter-train Duration [ms]	Duty Cycle
ILC (500 GEV)	727	1312	554	200	0.36 %
ILC (1 TEV)	897	2450	366	200	0.45 %
CLIC (3 TEV)	0.156	312	0.5	20	0.00031 %

- POWER MANAGEMENT :
  - 2 options for ILC :
    - signal read out continuously during train and detector $\sim$ switched of inbetween trains

      $\Rightarrow$ target read-out time depends on tracking strategy: track seed in main tracker or vertex detector
    - charge stored in pixel during train & processed+transfered slowly inbetween trains (immune to potential EMI)

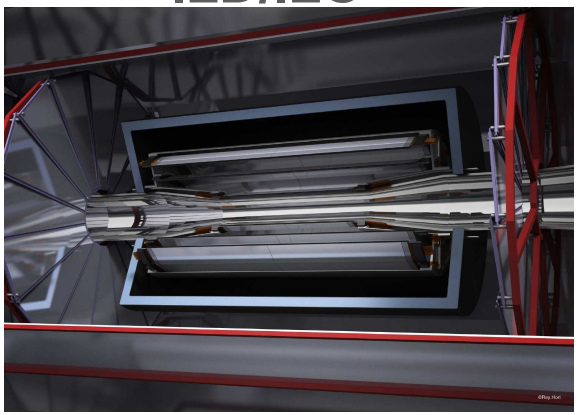
      $\Rightarrow$ constrains pixel size or/and in-pixel circuitry (timestamp)
  - CLIC (3 TeV) : $\lesssim$ 10 ns time (20 BX) resolution required $\Rightarrow$ continuous read-out

    $\Rightarrow$ strong impact on (fast) sensor technology
  - **General goal :** O(10) mW/cm^2 average power to allow air flow cooling (mat. budget !)

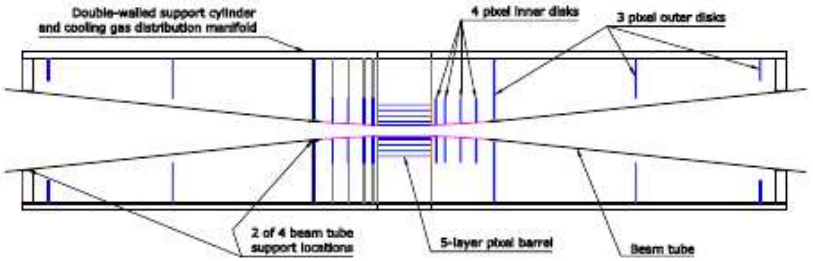
LC Vertexing Devices

- MAIN CHARACTERISTICS OF ILC VERTEX DETECTORS:
  - ⁕ **Geometry :**
    - S $\sim$ 0.5 m^2; coverage: $\cos\theta \lesssim 0.98$
    - SiD : short barrel complemented by 3 end-cap disks
    - ILD : long barrel geometry
    - R_{in} - $R_{out} \simeq$ 15–60 mm
    - 3 double-sided or 5 single-sided layers $\longmapsto$ 0.1–0.15 % X_0/sgle-layer !
  - ⁕ **Sensors :**
    - $\sigma_{R\phi,z} \lesssim 3\ \mu m$ (20μm pitch), 50 μm thin, O(10)mW/cm^2 (mean)
    - $\Delta t \sim 10\ \mu s$ (ILD) or $\ll 10\ \mu s$ (SiD) depending on tracking strat.
    - 2 r.o. alternatives : during or inbetween trains (option: 5$\times$5 μm^2 pixels)
    - R&D on various sensor techno. & r.o. architectures: exploit t $<$ construct.
- MAIN CHANGES NEEDED FOR CLIC VERTEX DETECTORS:
  - **Sensors :** $\Delta t \lesssim 10\ ns$!!!
  - **Geometry :** R_{in} - $R_{out} \simeq$ 30–60/80 mm; S $\sim$ 0.7–1.1 m^2
- MAIN R&D TOPICS ADDRESSED :
  - high precision low power pixel sensors $\longmapsto$ various optimisations
  - mechanics and cooling
  - power delivery and pulsing

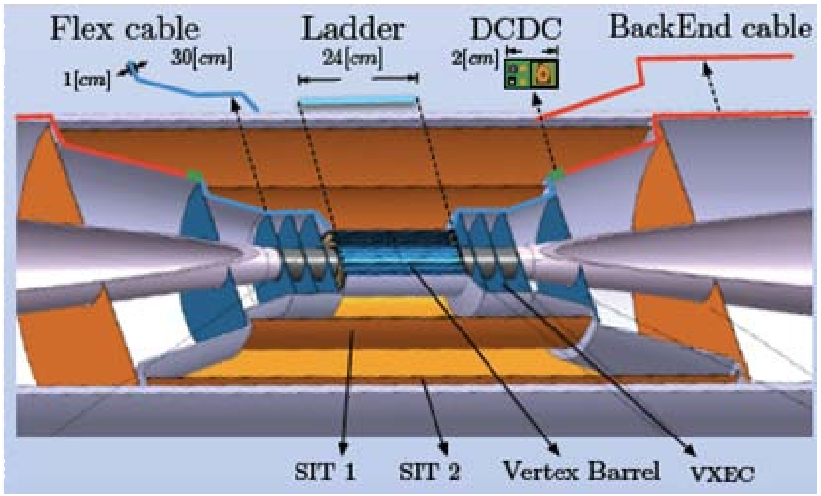
ILD/ILC



SiD/ILC

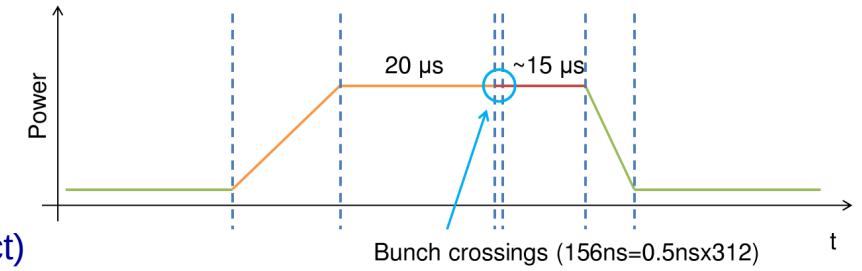


CLIC



Power Delivery & Cycling

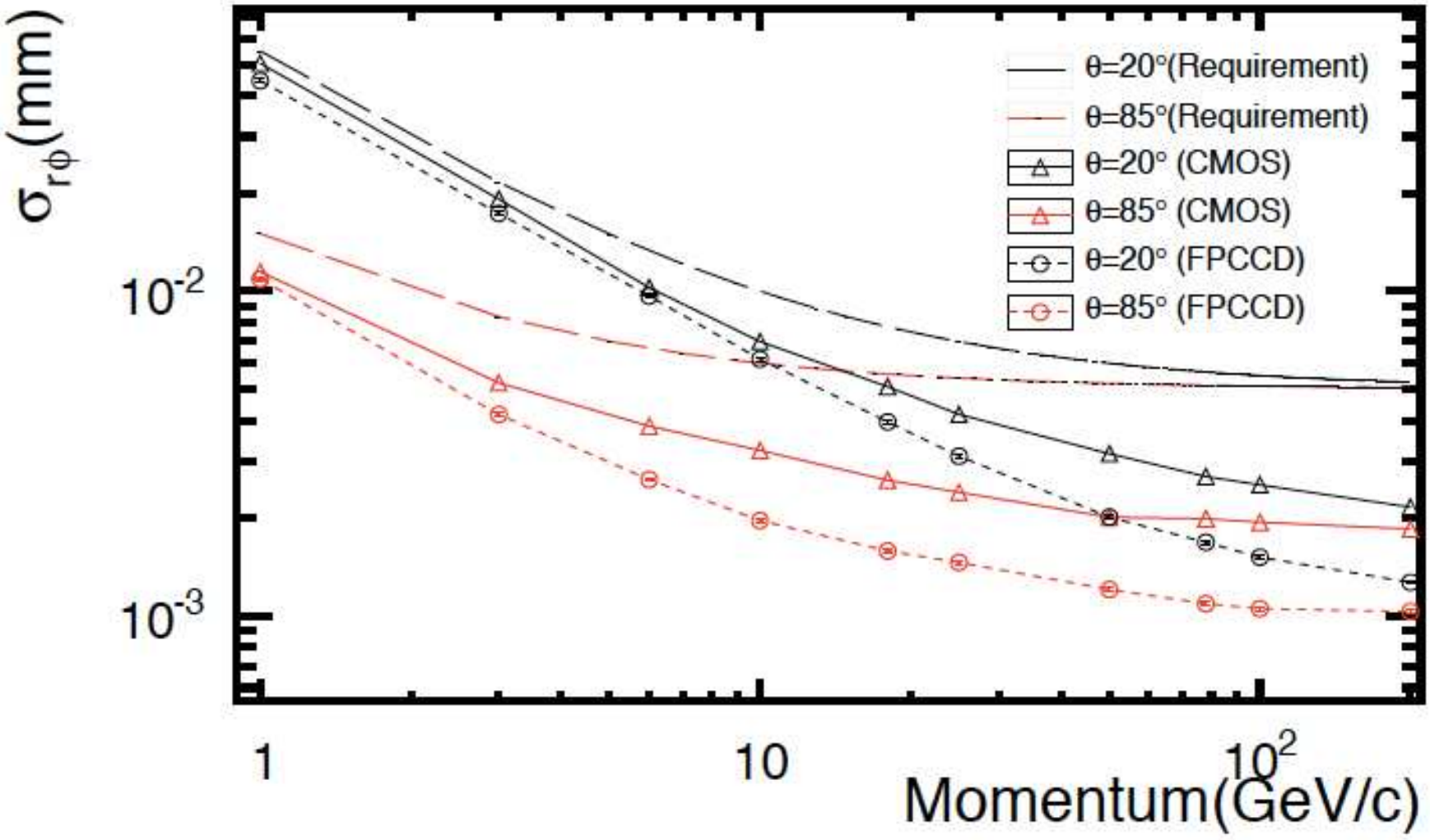
- PIXEL SENSORS : $\sim$ 0.1–1 W/cm^2 $\Rrightarrow$ 1-10 kW/m^2
  - $\hookrightarrow$ would require active cooling, generating material budget overheads
- EXPLOIT THE VERY LOW DUTY CYCLE OF THE ACCELERATOR : · ILC : few 10^{-3} · CLIC : few 10^{-6}
  - ⁕ EITHER very slow ($\equiv$ low power) signal processing $\Rrightarrow$ postponed read-out inbetween trains
  - ⁕ OR fast signal processing during train (occupancy !) & detectors switched off between trains $\equiv$ power pulsing/cycling
- SUBSTANTIAL DIFFICULTIES :
  - ⁕ Low power slow read-out imposes :
    - · either $\sim$ 5 μm pitch against occupancy $\Rrightarrow$ large Nb(pixels) read out in 200 ms
      $\Rrightarrow$ long serial read-out fitting inbetween trains (// read-out tends to break power limit)
    - · or in-pixel circuitry to timestamp consecutive hits in same (larger) pixel
      $\Rrightarrow$ conflict between pixel dimensions fitting spatial resolution (small) and those fitting timing resolution (larger)
  - ⁕ Continuous read-out with power cycling leads to :
    - · switching on & off a few grams light ladders in a high B field (3.5 - 5 T) $\Rrightarrow$ F(Lorentz) up to several tens of grams ...
    - · distributing several hundreds of Amperes shortly before each train arrival
    - · heat cycle the ladders ...
- TESTS ALREADY STARTED :
  - ⁕ DEPFETS: power cycling test outside of magnet sucessful
  - ⁕ CMOS pixel sensor power cycling test foreseen in 2T magnet (AIDA project)
  - ⁕ CLIC inner tracking system test bench



CLIC power pulsing scheme

ILC oriented Pixel Sensor R&D

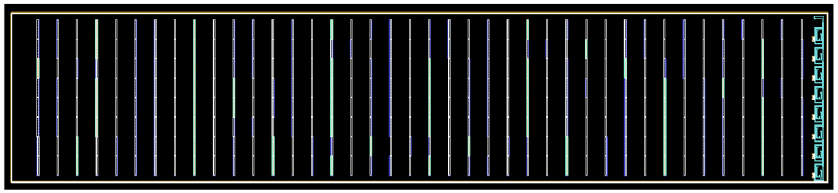
Fine versus High Precision Pixels

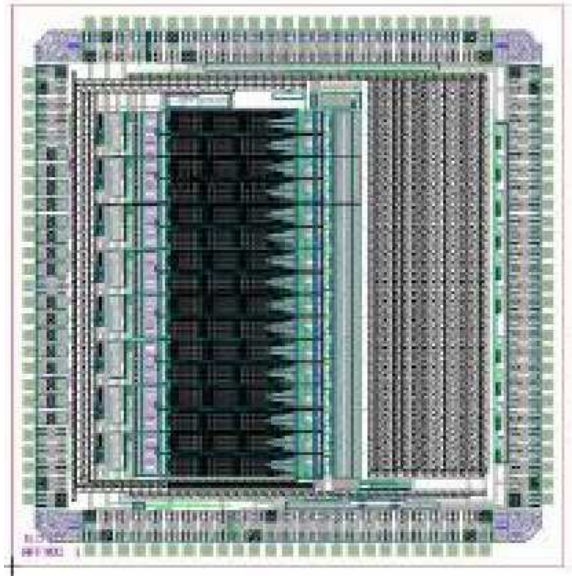


Fine Pixel CCDs: Main Features

- PROMINENT FEATURES OF FPCCDS:
  - Signal charge created in a fully depleted $\sim$ 15 μm thin epitaxial layer
    $\Rightarrow$ limited charge spread
  - Very small pixels (5$\times$5 μm^2):
    - $\sigma_{sp} \lesssim 1\ \mu m$
    - beam related BG rejected by pattern recognition
  - High-res epi and small pixels (occupancy/BX $\sim$ few ppm) used to integrate over full train duration
    $\Rightarrow$ devt addresses very low power ADCs
  - Can be thinned down to 50 μm
  - Need -40°C cooling for radiation tolerance purposes
    $\Rightarrow$ impact on material budget (modest ?)

62.4 mm long prototype



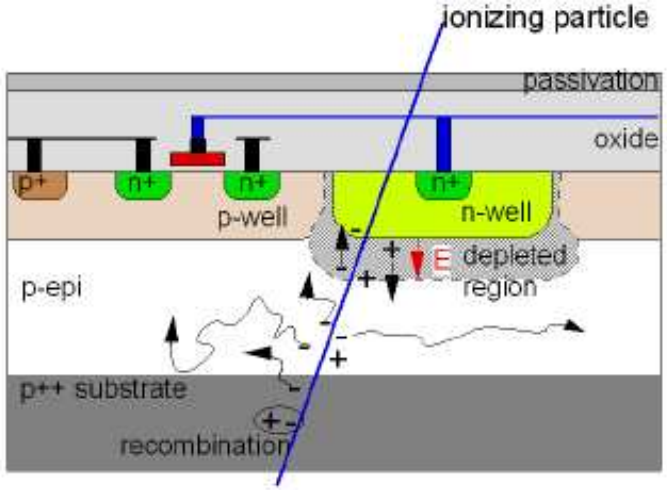


- SEVERAL ESSENTIAL R&D TOPICS ADDRESSED :
  - 5$\times$5 μm^2 pixel matrix detection performances
  - Low power, large bandwidth, r.o. electronics (e.g. 8-bit? ADC)
  - Low mass CO_2 cooling

- Approach not limited to CCDs: expected to work with CMOS sensors (cost effective, smaller pixels, cooling)

CMOS Pixel Sensors: Main Features

- PROMINENT FEATURES OF CMOS PIXEL SENSORS:
  - high granularity ⇛ excellent (micronic) spatial resolution
  - very thin (signal generated in 10-20 μm thin, high-res, epitaxial layer)
  - signal processing μ-circuits integrated on sensor substrate
    ⇛ impact on downstream electronics and syst. integration (⇛ cost)
  - MIMOSA series based on rolling shutter read-out ⇛ low power

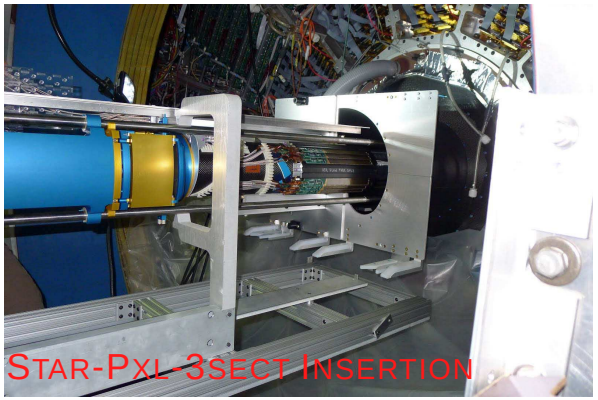


- CMOS PIXEL SENSOR TECHNOLOGY HAS A VERY HIGH POTENTIAL

⇛ R&D largely consists in trying to exploit potential at best with accessible industrial processes

↪ manufacturing parameters not optimised for particle detection:

epitaxy characteristics, feature size, N(ML), ... ⇛ breakthrough with 0.18 μm TJSC


STAR-PXL 3SECT INSERTION

- TECHNOLOGY ALREADY UNDER PROD/DEVT FOR UPCOMING DETECTORS:

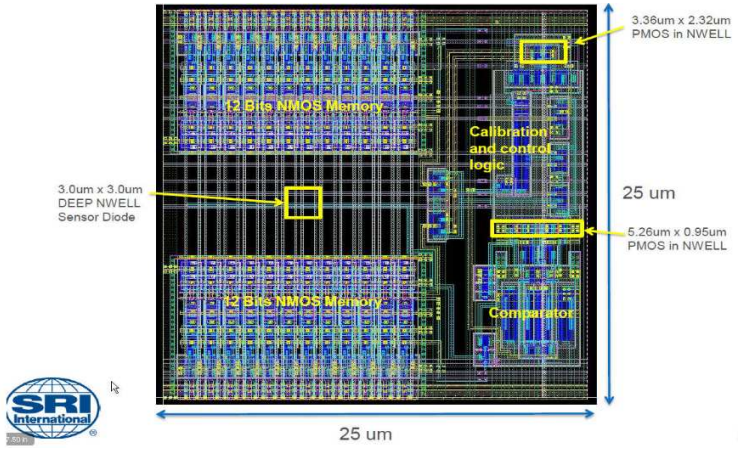
Experiment -Detector	**Pitch** [μm]	σ_{sp} [μm]	$t_{r.o.}$ [μs]	**ladder** X_0 [%]	**Dadiation load** [MRad]	n_{eq}/cm^2	**Area** [m^2]
STAR-PXL **'13**	20.7	3.5	200	0.37%	0.15	$3{\cdot}10^{12}$ (30°C)	.16
ALICE-ITS **'18**	20-30	~ 5	10-30	0.3%	0.7	10^{13} (30°C)	0.5-10
CBM-MVD **'19**	20-30	~ 5	10-30	0.3-0.5%	$\leq$10	$\leq 10^{14}$ ($\ll$ 0°C)	~ 0.5
ILD-500	16-80	<3	10-100	<0.15	0.1	10^{11} (30°C)	0.35
ILD-1000	16-80	<3	2-100	<0.15	> 0.3	few 10^{11} (30°C)	0.35


ALICE-ITS INNER BARREL

  - option for BESS-3, ATLAS/Phase-2 tracker, ...

Chronopixel Sensors: Main Features

- PROMINENT FEATURES OF CMOS PIXEL SENSORS:
  - CMOS Pixel Sensor with in-pixel (sgle BX) 12-bit time stamping
    $\Rrightarrow$ tracking based on Vx detector seed (SiD option)
  - Read-out delayed inbetween consecutive bunch trains (power saving)
  - Double-hit timestamping possibility ($25 \times 25\ \mu m^2$ pixels)



- REQUIRES A VERY ADVANCED (MIXED ?) CMOS TECHNOLOGY :
  - VDSM ($\leq$ 90 nm, with deep P-well), for high μcircuitry density
    $\hookrightarrow$ trade-off: pixel size (occupancy) vs in-pixel circuitry complexity
  - Epitaxial layer: thick and resistive enough for cluster spread and SNR

- CUSTOMISED DESIGN IN INDUSTRY (SARNOFF)
  $\Rrightarrow$ cost, design optimisation possibility, devt timeline, ...

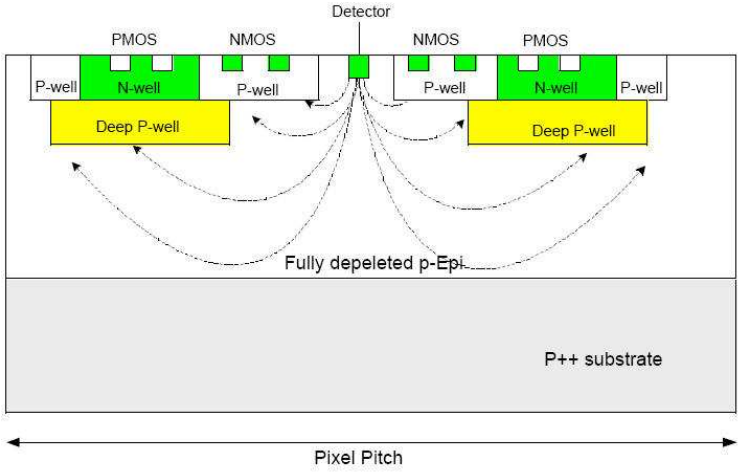
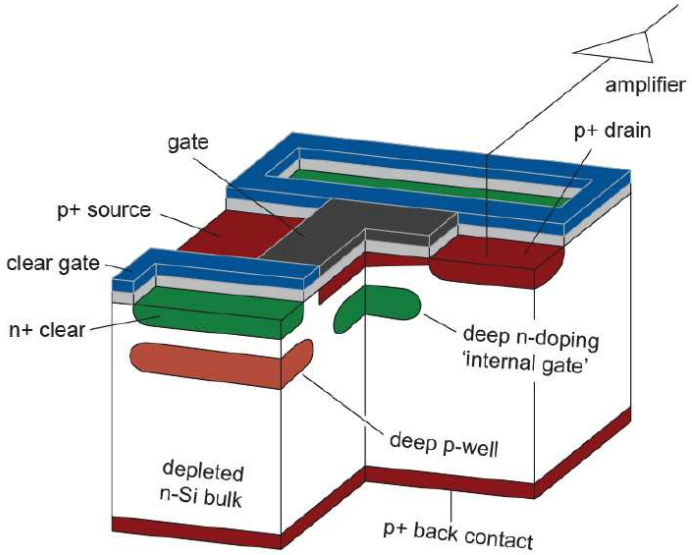
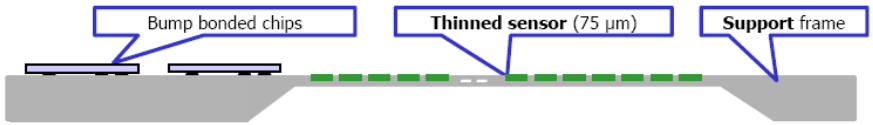


Figure 11.1 Proposed pixel architecture employing the deep p-well layer

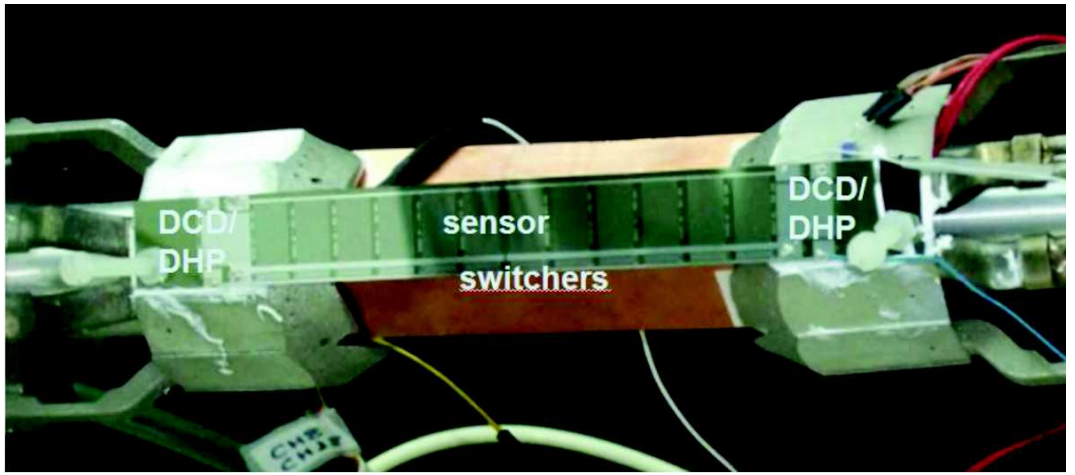
DEPFET Sensors: Main Features

- PROMINENT FEATURES OF DEPFET PIXEL SENSORS:
  - Signal charge created in a fully depleted Si substrate and collected by a n-type node (”internal gate”) burried under a p-channel FET, delivering a current modulated ($\propto$) by the charge collected on the node
  - External gate to enable read-out $\Rightarrow$ r.o. chips
  - Clear contact removes charge from internal gate $\Rightarrow$ switcher chip
  - Steering and signal processing ASICs bonded on ladder edge & end
  - Read-out based on rolling shutter mode $\Rightarrow$ low power
  - High granularity $\Rightarrow$ micronic spatial resolution
  - Can be thinned down to 50 μm
  - Sensors are embedded in Si mechanical support
    $\Rightarrow$ low material budget





- TECHNOLOGY UNDER PROD/DEVT FOR THE BELLE-II VERTEX DETECTOR:
  - $\hookrightarrow$ Several specs close to those of the ILD-VXD inner layer (e.g. $< 0.2\%\ X_0$)
    - $\hookrightarrow$ granularity$\times$speed still to improve



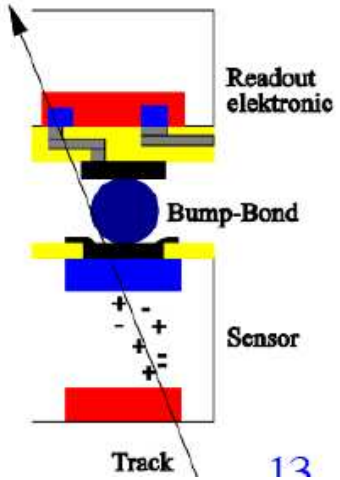
CLIC oriented Pixel Sensor R&D

(See also CLIC talk)

CLIC Motivated R&D: Hybrid Approach

- MOTIVATED BY THE $\lesssim$ 10 NS TIME RESOLUTION NEEDED AT CLIC

- AS COMPARED TO EXISTING/FORTHCOMING DEVICES, THE R&D ADDRESSES :
  - $\lesssim$ 10 times smaller pixels
  - $\lesssim$ 10 times smaller material budget

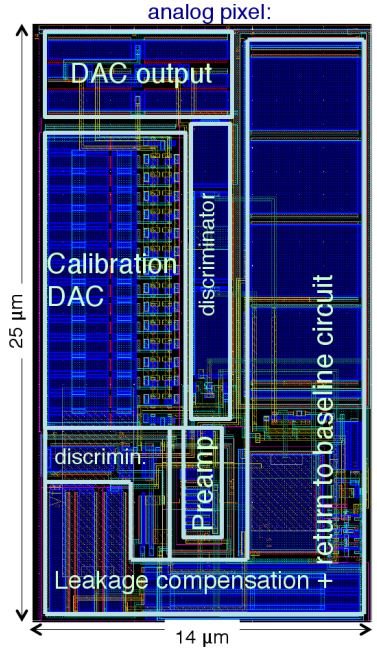


- SOME MAJOR R&D LINES :
  - Thinned high-resistivity fully depleted substrates available commercially

    $\Rightarrow$ develop handling and bonding procedures
  - R&D on fast, low-power r.o. ASICs in VDSM CMOS processes
    - TimePix3 (2013) : 130 nm IBM, 55 μm pitch
    - SmallPix (2013) : 130 nm IBM, $\lesssim$ 40 μm pitch
    - $\triangleright$ **ClicPix ($\sim$ 2015) : 65 nm process, 25 μm pitch**

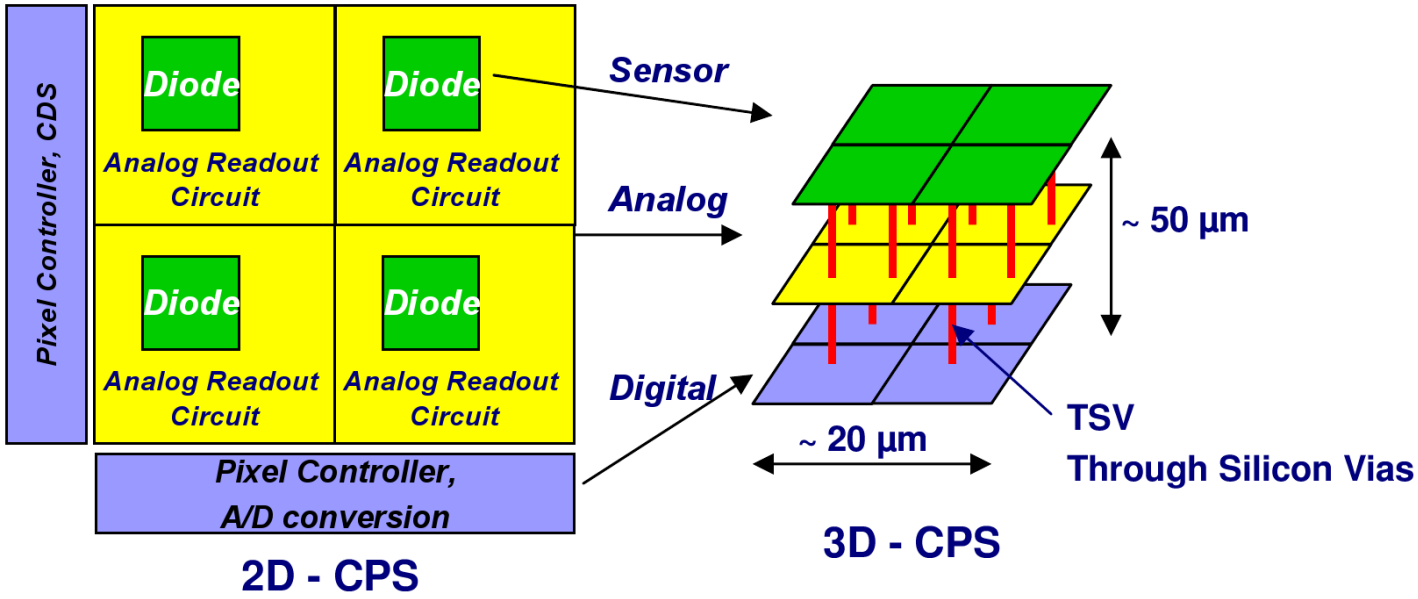
      $\hookrightarrow$ **demonstrator prototype (2013) : 64$\times$64 pixel array** $\longrightarrow$
  - R&D on low-mass, high-density interconnects :

    TSV, μbump bonding, Cu pillars, ...

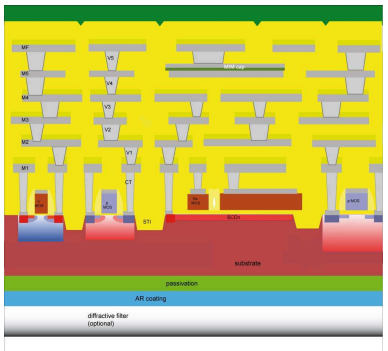


CLIC Motivated R&D : 3DIT

- HIGH POTENTIAL APPROACH CONSISTING IN STACKING CHIPS INTERCONNECTED AT PIXEL LEVEL
- MAJOR R&D ISSUES :
  - ⁕ Investigate 3D Integrated technologies
    - ⟷ Through Silicon Vias (TSV)
  - ⁕ Allows combining thin tiers dedicated to specific & complementary functionalities:
    charge sensing, analog r.o., digital proc., ...
  - ⁕ Allows integrating high density signal processing μcircuits in small pixels !

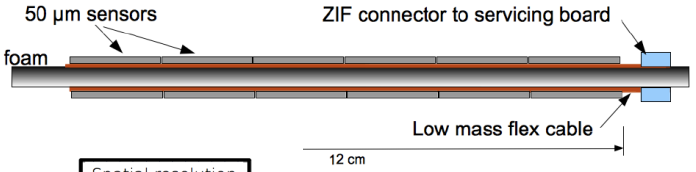


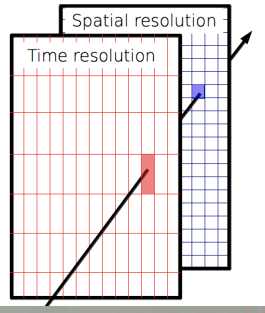
- DEVELOPMENT STARTED IN 2009 (3DIC CONSORTIUM) from various sensing technologies (hybrid, CMOS, ...)
  - ⁕ facing interconnectivity difficulties ⟼ 2-tier chips back recently: 1st test results satisfactory ⇛ devt can continue
  - ⁕ R&D also of interest for ILC (1 TeV) and for LHC/Phase-2
- EMERGING PERSPECTIVE: VDSM PROCESSES ON THIN (50 μm) FULLY DEPLETED SUBSTRATE ⇛
  (commercial cameras, X-ray imagers)
  ⇛ STAY TUNED

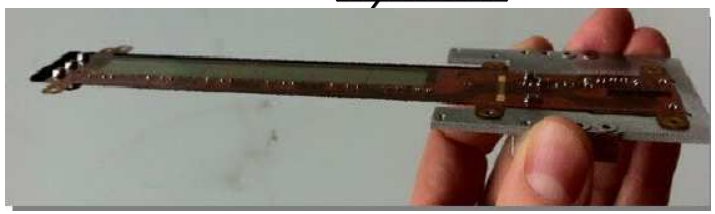


Sensor Integration in Ultra Light Devices

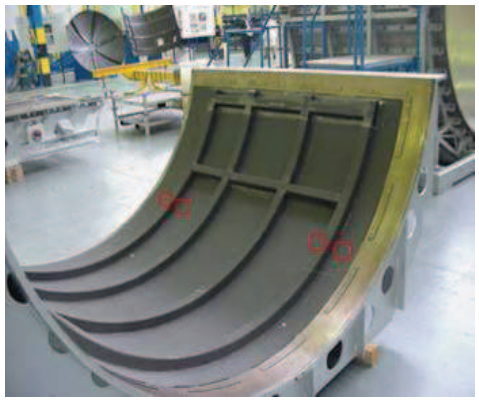
- **2-sided ladders with combined spatial & time resolutions :**
  - ⁜ manyfold bonus expected from 2-sided ladders:
    compactness, alignment, pointing accuracy (shallow angle), redundancy, etc.
  - ⁜ studied by PLUME coll. (Oxford, Bristol, DESY, IPHC) & AIDA (EU)
    ↪ **P**ixelated **L**adder using **U**ltra-light **M**aterial **E**mbedding
  - ⁜ square pixels for single point resolution on beam side
  - ⁜ elongated pixels for 4-5 times shorter r.o. time on other side
  - ⁜ correlate hits generated by traversing particles
  - ⁜ expected total material budget $\sim$ 0.3 % X_0
    ↪ 1st proto. (0.6 % X_0) fabricated & operationnal
    ▷ validated on beam at CERN-SPS (traversing m.i.p.)

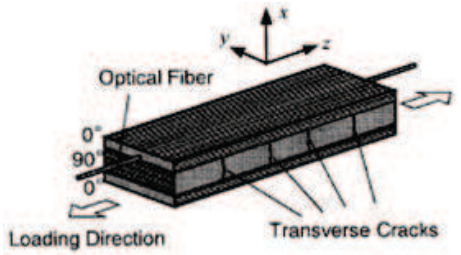


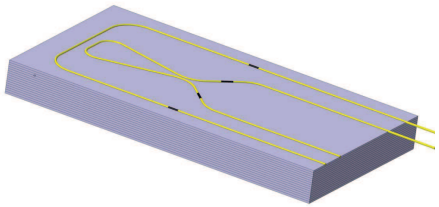




- **Optical fiber based alignment monitoring :**
  - ⁜ Embedded Fiber Bragg Grating sensors on carbon fiber struct. (CFRP)
    for deformation & T monitoring used in aeronautics & civil engineering
  - ⁜ Precise online measurement of mecha. support deformations
    ⇒ optimise material budget of mechanical supports
  - ⁜ Pple: measure shift in reflected Bragg wavelength due to change
    in refraction index & periodicity of index variation







SUMMARY

- LC vertex detectors drive a specific/innovative R&D on highly pixelated position sensitive devices :
  - **Sensors:** $20\times20\mu m^2$ pixels $\Rrightarrow$ $\sigma_{sp} \lesssim 3\ \mu m$, $50\mu m$ thin, low power, 3DIC (VDSM), 2-sided ladders, ..
  - **System integration:** ultra-light ladders (0.1–0.2 % X_0/layer), fast power cycling in magnetic field, ...
- Timelines :
  - **ILC (less demanding) :** main goals seem $\pm$ achievable by $\lesssim$ 2015 but quite so room for improvement
  - **CLIC-3TeV (more demanding) :** $>$ 100 times faster read-out speed required (granularity$\times$speed conflict)
    $\Rrightarrow$ R&D on chip interconnects and power saving $\longmapsto$ viable solutions by 2020 (?)
- Numerous spin-offs :
  - **Subatomic physics :** high-precision BT, STAR, Belle-II, ALICE, CBM, BESS-3, ..., LHC Phase-2 ?, ...
  - **Other areas :** hadrontherapy, light source infrastructure instrumentation, photon counting cameras, ...

$\Rrightarrow$ CONSIDERABLE PROGRESS ALREADY ACHIEVED IN LAST 10 YRS $\Rrightarrow$ EXPECT SIMILAR STEP UNTIL 2020 !

- Performance level achievable before detector construction will strongly depend on the importance of community efforts (striking lack of manpower at present)

$\Rrightarrow$ IMPORTANT MEETINGS: ECFA-LC WORKSHOP (END OF MAY), LCWS-2013 (NOVEMBRE)

Pending Instrumental Developments

- PIXELS :
  - Fine Pixel CPS : more granular, less expensive, more flexible than FPCCDs
  - fast sensors ($\gtrsim$ 1 μs) adapted to standalone tracking ($\leq$ 500 GeV) or 1 TeV running
- LADDERS :
  - material budget reduction, micro-channel cooling, alignment controls
- POWER CYCLING :
  - mechanical effect of high magnetic field
  - solutions to minimise the effect (sensor design, ladder design)
- POWER MANAGEMENT :
  - low mass P delivery design
  - **pulsed power distribution ($>$ 100 A) over the detector**

Pending Concept Optimisation Tasks

- PERFORMANCE OPTIMISATION :
  - ILD : inner tracker tracking using tracks extrapolated from TPC rather than standlone tracking
  - tracking using rolling shutter
- BACKGROUND HANDLING :
  - tracking strategy mitigating the effect of beamstrahlung electrons
  - effect of pile-up over several BX $\Rightarrow$ max occupancy allowed with continuous & power pulsed read-out
    (different pixel dimensions)
- PIXELATED VERSION OF SIT (ILD) :
  - compare pixel option with pile-up versus less accurate strip variant identifying each bunch
- ALTERNATIVE GEOMETRIES MERITS :
  - elongated barrel versus short barrel + disks
  - solutions to minimise the effect (sensor design, ladder design)

$\Rightarrow$ **Determine reliable vertex detector specifications:**
sensors, ladders, system integration, etc.

Japanese Roadmap

Possible Timeline

- July 2013
  - Non-political evaluation of 2 Japanese candidate sites complete, followed by down-selecting to one
- End 2013
  - Japanese government announces its intent to bid
- 2013~2015
  - Inter-governmental negotiations
  - Completion of R&Ds, preparation for the ILC lab.
- ~2015
  - Inputs from LHC@14TeV, decision to proceed
- 2015~16
  - Construction begins (incl. bidding)
- 2026~27
  - Commissioning

Fine versus High Precision Pixels