

Lar upgrade

F. Tartarelli

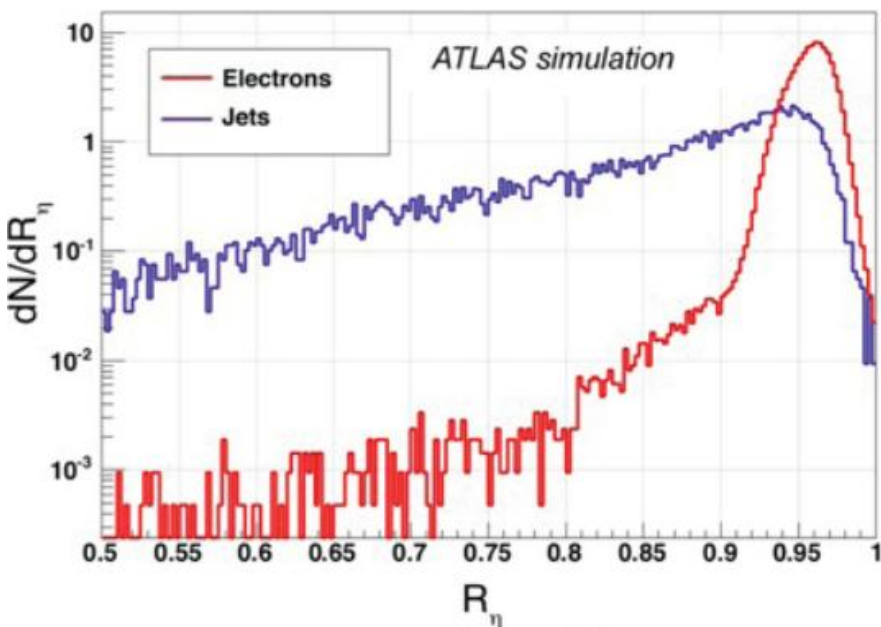
Incontro con i referee, 20/03/2012

LAr Phase I upgrade

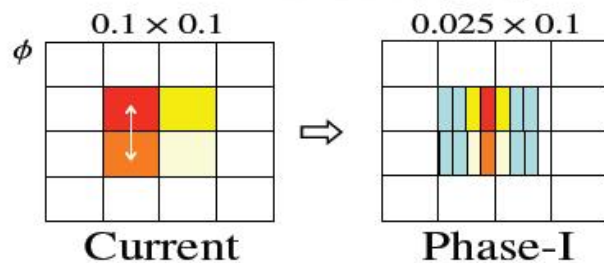
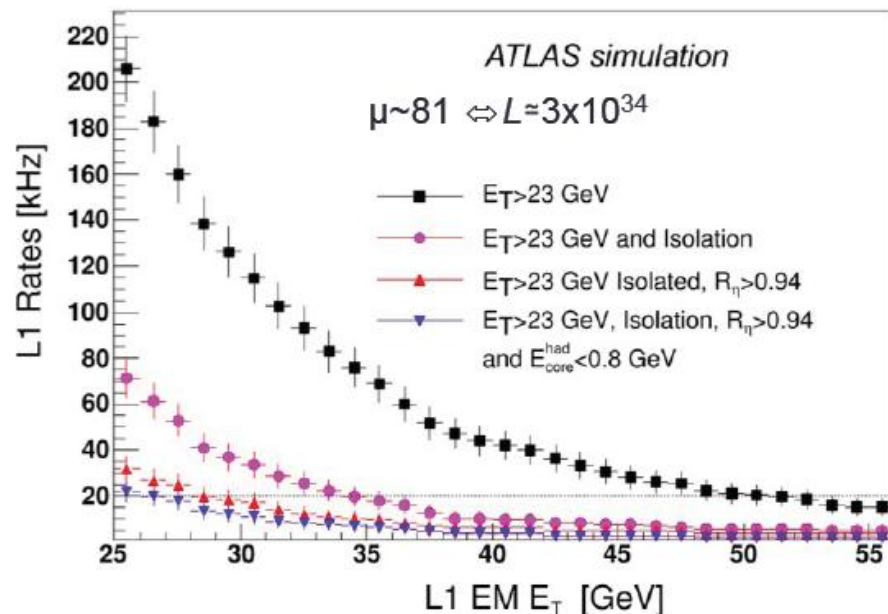
- Purposes:
 - maintain high efficiency for Level-1 triggering on low P_T objects (electrons and photons)
 - Improve jet, tau, MET triggers
 - Enable lower thresholds for multi-object triggers
 - Give more flexibility in trigger menu design and in operations
- In the LAr calorimeter this implies changes to the front-end electronics to allow greater granularity to be exploited at Level-1
 - finer segmentation in eta
 - depth information
- Enable use of more powerful LVL2 /offline-like variables/ techniques in the L1Calo selection:
 - Shower shapes

Improving electron ID → eFEX

Increase em trigger discrimination power by processing finer granularity LAr data



$$R_\eta = \frac{\sum_{3 \times 2} E_T}{\sum_{7 \times 2} E_T}$$



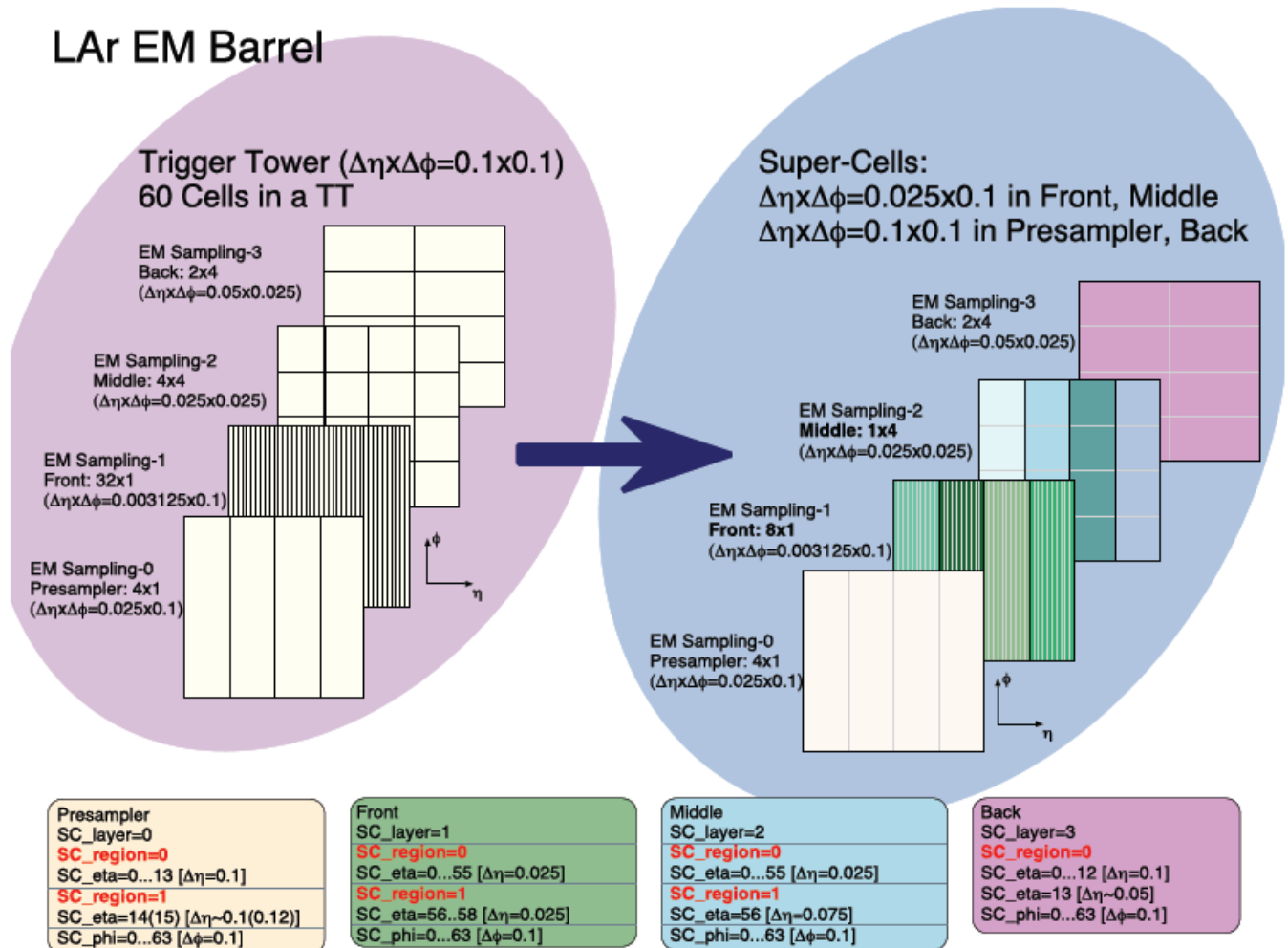
LAr EM Barrel

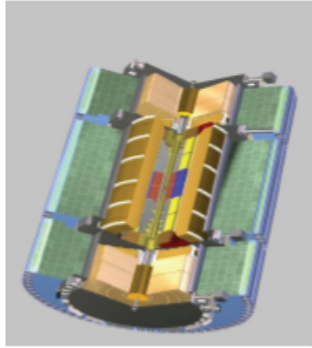
One Trigger Tower



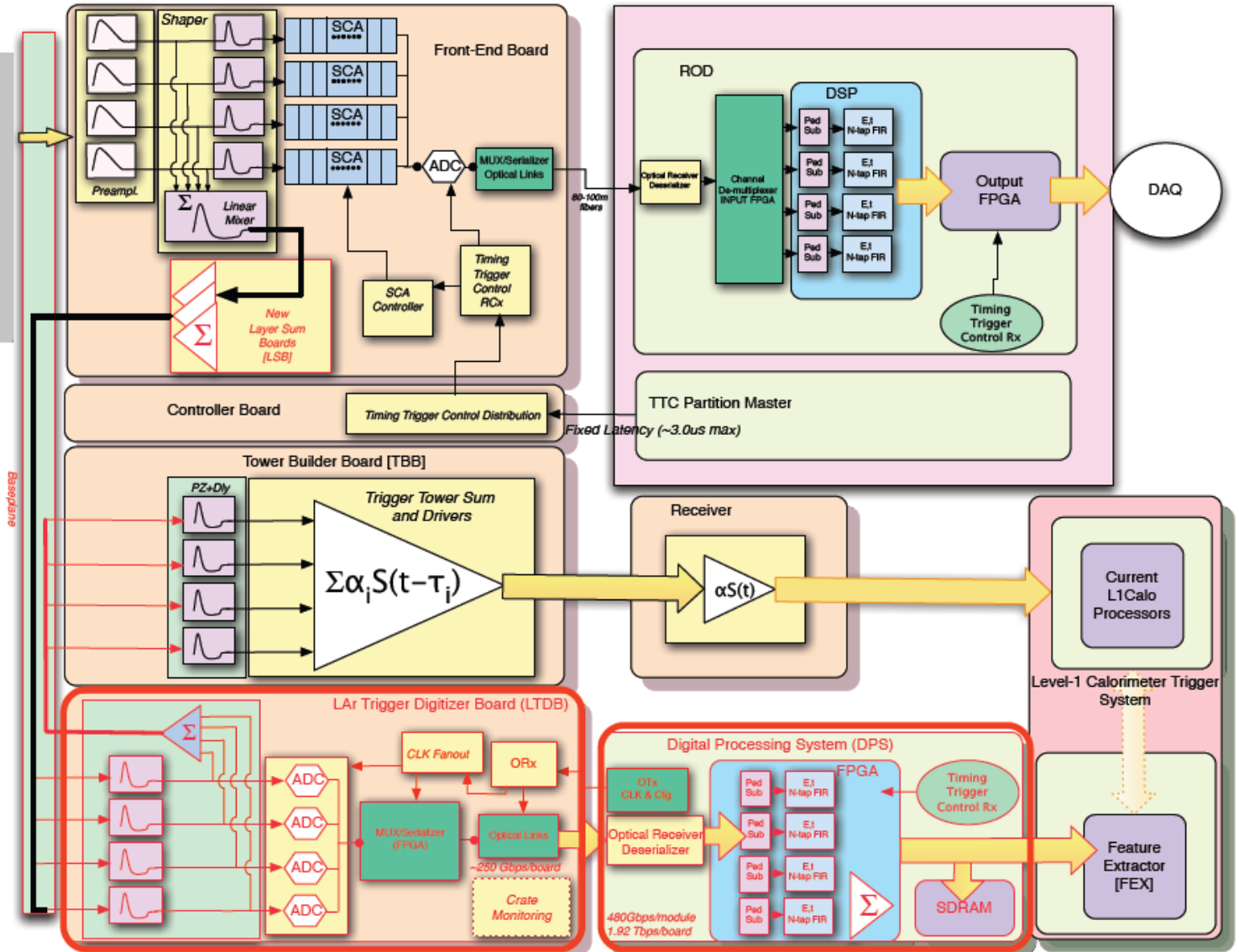
Ten Super-Cells

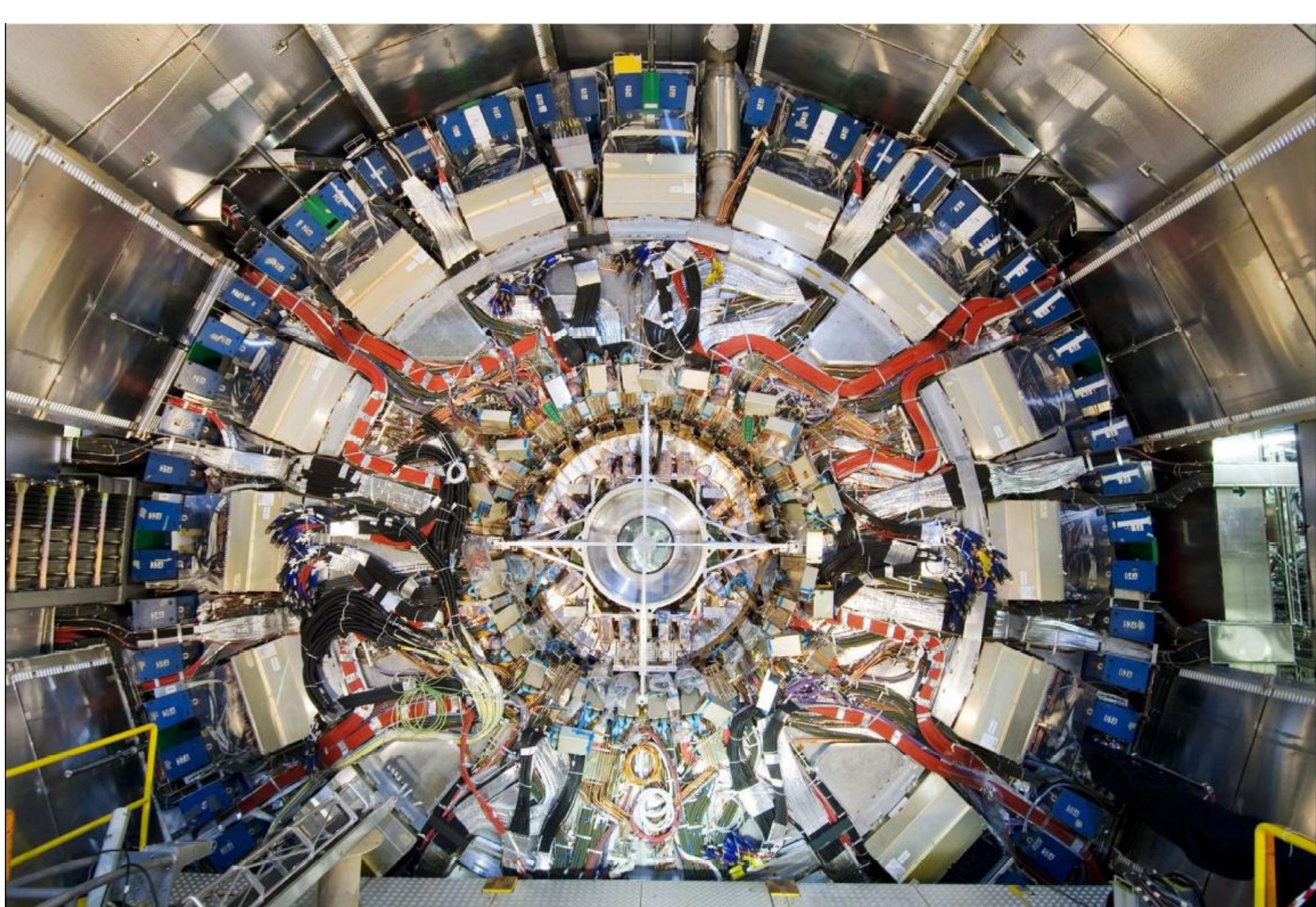
1 PS
4 Strips
4 Middle
1 Back

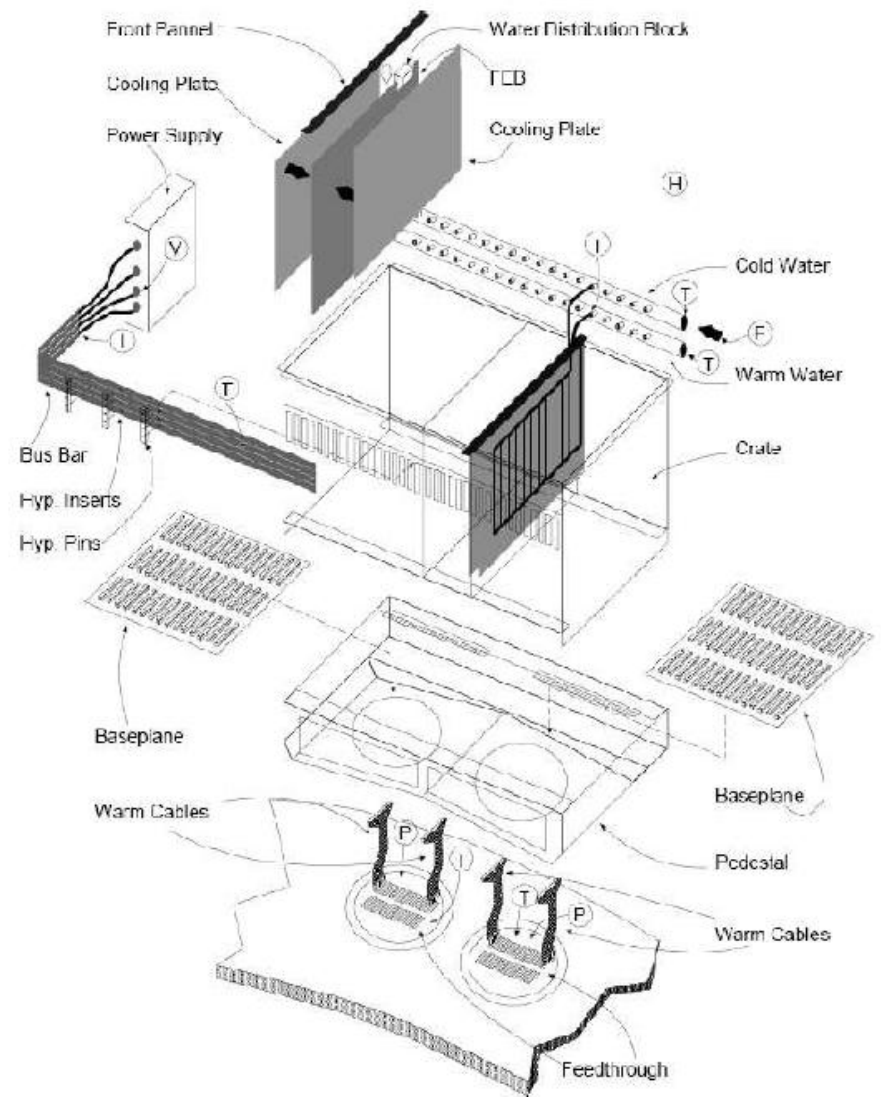
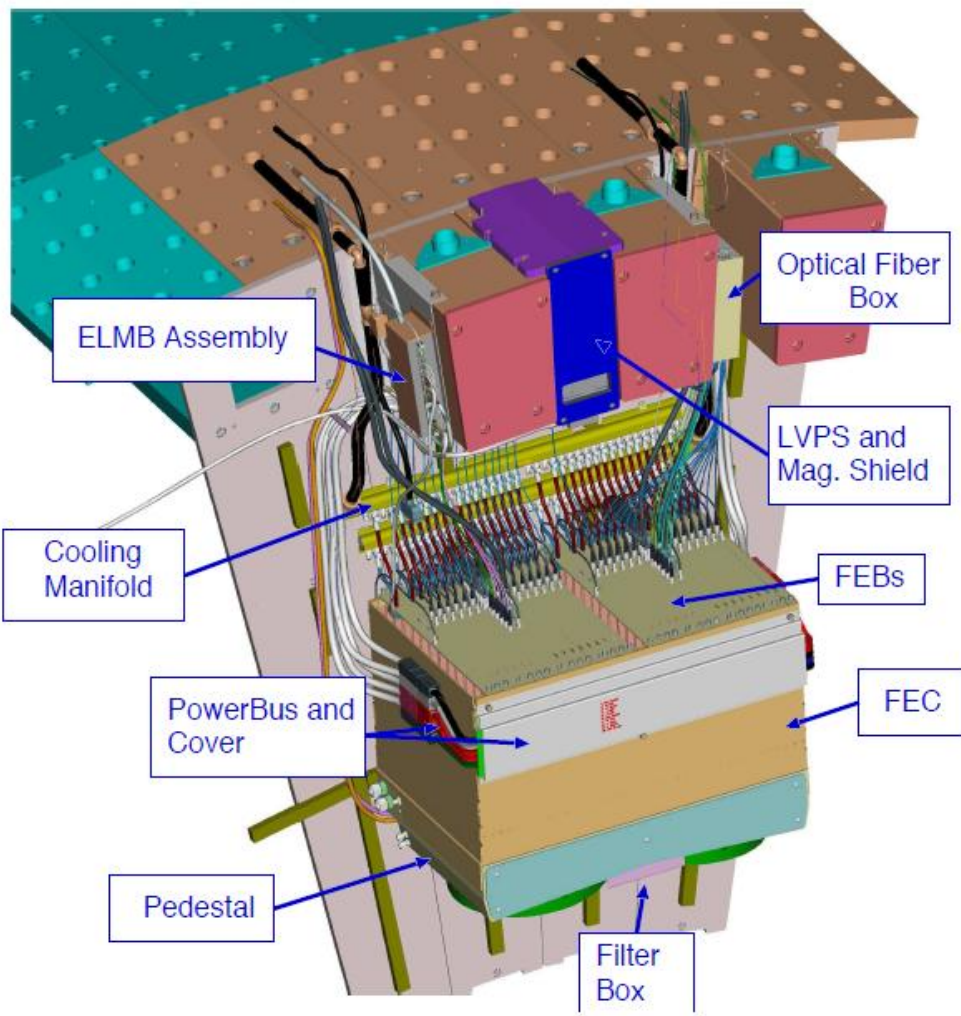


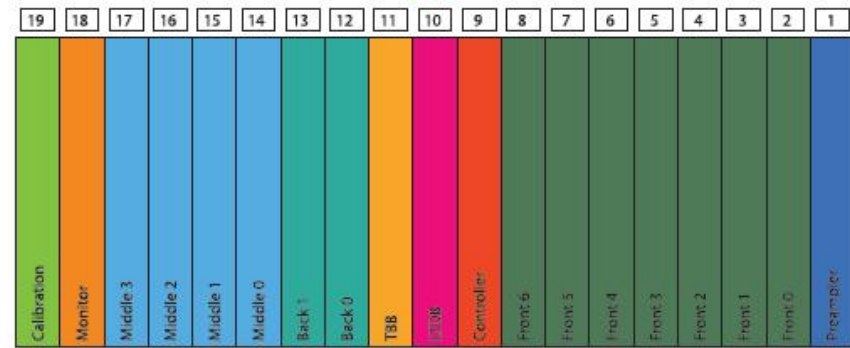
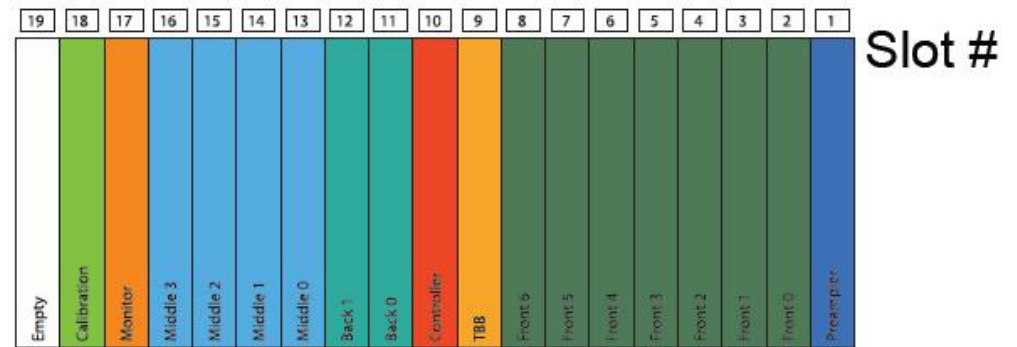
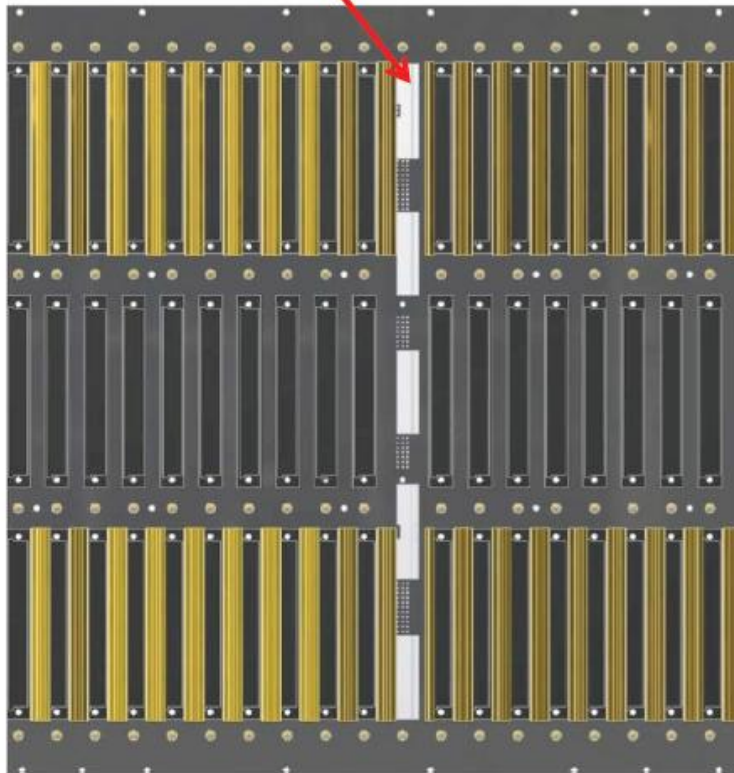
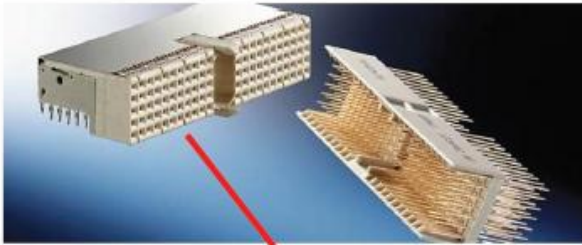


Possible implementation
 $\Delta\eta \times \Delta\phi = 0.025 \times 0.1$ 1st and 2nd layer EM
 $\Delta\eta \times \Delta\phi = 0.1 \times 0.1$ elsewhere









In-situ Demonstrator

- In order to test and commission the proposed upgrade for Phase-I before ATLAS operation:
 - Test of single elements
 - Full lab system tests at the LAr Electronic Maintenance Facility (EMF)
 - Installation of in-situ demonstrator during LS1
 - Test of production components
- The in-situ demonstrator plan is to equip one FEC with the read-out for the increased granularity :
 - Likely one barrel FEC ($\Delta\eta \times \Delta\phi = 1.4 \times 0.4$, about 2% of trigger acceptance)
 - 2 new baseplanes, all FEBs in the crate equipped with new LSBs, 2 LTDBOs, long fibers up to USA15 counting room, 2 LD
- The LTDBO will not have the components for the full series Phase-I boards, it will have a very similar functionality.

Demonstrator

- IDR review requested more details for In-situ demonstrator
 - They were worried it could be a major “disruption” of ATLAS operation
- More info added to the summary document of the review:
 - Well taken and, finally, very supportive:
- Agreed to hold an ATLAS review before the installation of Demonstrator
 - Show results of system test
 - Show installation plan with risks
 - 4 months prior to access end -> ~March 2014 (as of now)

LAr electronic upgrade for Phase I

#	Project	<i>Letter of Intent presented and approved by LHCC</i>	<i>Initial Design Review</i>	<i>Kick-off meeting</i>	<i>CB approval</i>	<i>TDR due</i>	<i>LHCC Session</i>	<i>I-MOU needed</i>	<i>MOU-due for signature (RRB)</i>
1	FTK	21-Mar-12	2-Dec-10	3-Dec-10	24-Jun-11	30-Apr-13	11-Jun-13	yes	15-Oct-13
2	nSW	21-Mar-12	29-Aug-12	31-Aug-12	5-Oct-12	31-May-13	11-Jun-13	not clear	15-Oct-13
3	LAr	✓ 21-Mar-12	✓ 9-Jan-13	✓ 11-Jan-13	✓ 8-Feb-13	15-Sep-13	24-Sep-13	not clear	15-Oct-13
4	TDAQ	21-Mar-12	21-Jan-13	23-Jan-13	8-Feb-13	15-Sep-13	24-Sep-13	not clear	15-Oct-13
5	AFP	21-Mar-12	17-Sep-12	19-Sep-12	2014	2014	2014	yes	14-Oct-14

- Project is on schedule:
 - IDR passed on January 9-11, 2013
 - CB approval on February 8, 2013
 - Next step is TDR due September 15, 2013
- Outcome very positive, a few things to follow towards TDR.
MOU soon after TDR:
 - Discussions on cost sharing just started

Outcome of the LAr Phase-I Initial Design Review



<https://indico.cern.ch/conferenceDisplay.py?confId=220966>

LAr Upgrade Phase I

chaired by Isabelle Wingerter-Seez

from Wednesday, 9 January 2013 at **09:00** to Friday, 11 January 2013 at **18:00** (Europe/Zurich)

Manage ▾

Description

Material:

1. Summary Note



2. Expected Performance and Physics Motivations



3. Upgrade Simulations Backup Notes



4. Technical Backup Notes



5. PBS and Milestones



Latency Budget spreadsheet



✓ Reviewers:

- Giulio Aielli, Michael Begel, Philippe Farthouat, Claudia Gemme (chair), Murrough Landon, Steve McMahon, Christoph Rembser, Stefano Veneziano

General comments of the reviewers



- ✓ The reviewers have looked at the **physics case**, the **required hardware upgrade** and the proposed structure of the **organization for the project**.
- ✓ The upgrade of the LAr electronics is a **high priority project for the ATLAS experiment in Phase-I** in order to keep an optimal trigger system as the luminosity increases beyond LHC nominal luminosity.
- ✓ We have paid particular attention that **there are no showstoppers** in the proposed technical implementation and that **the proposal is compatible with Phase-II**.
- ✓ We congratulate the LAr community on the information provided and the very clear presentations and discussion during the review.
- ✓ A set of **recommendations** is made for the next steps of the project, mainly concerning the preparation of the Technical Design Report scheduled for Fall 2013.
 - ATU-TC-MR-0012: <https://edms.cern.ch/document/1262820/1>
 - Short term recommendations (details on TDR milestones, schedule, demonstrator program, etc..) done just after the review have already been included in the IDR documentation.

Recommendations – Physics case



- ✓ While the EM and Jet trigger studies are well advanced, more work on MET and tau studies is still needed and we recommend to
 - settle on a single set of simulation samples that are common with other Phase I and II efforts;
 - establish common benchmarks and definitions used to define the performance of the system.
 - It is mandatory to establish good contact with other upgrade groups who need validation studies on the same timescale.
- ✓ In the results of the studies a clearer **factorization of benefits** of issues like dynamic range and granularity and algorithm should be given.
- ✓ A clearer demonstration how the **optimal working points** (in terms of identification of bunch crossing, saturation and energy resolution) will be chosen needs to be given.

Both items might have implications on the hardware choices.

- ✓ A complete estimate of the important physics rates when this system is used during LHC Phase-II should be given.

Rec.: Technical Implementation-I



- ✓ Identify key failure mechanisms and ensure **adequate redundancy** is built into every aspect of the design, even based on the current detector operation.
- ✓ Front-End
 - Choice of **ADC**: COTS vs custom designs. It is recommended to pursue the three current options, even in view of future developments for Phase-II, but, in case all of them meet the requirements, to consider the commercial one.
 - **Optical Links**: if possible we recommend that the LAr community explores the possible use of the developments in the versatile link project (VTTX, dual transmitter).
 - We recommend the proponents to explore the possibility of using the **serializer** GBTx in parallel with other custom developments. In the case that FPGAs are demonstrated to work reliably in the environment (radiation), we recognize that this is also a valid solution.
 - Validate services (cooling, power supplies) and mechanics of the new LTDB with new connectors.

Rec.: Technical Implementation-II



✓ Back-End

- A more detailed description of the readout (i.e. ROD) functionality. A more detailed description of the monitoring and what goes into the data stream.
- Continue to consider implications for Phase-II as this part of the system will be kept.

✓ Installation

- A detailed understanding of the **risks** involved in the installation of the new electronics in the pit.
- A more detailed evaluation of the **crate refurbishment schedule** and timetable. Including a complete **ALARA** study of the radiation risks involved in the installation in the pit, implications on the scope of work activities and schedule impact. The schedule seems tight and therefore we recommend to develop it in strong contact with TC.
- Finalize the initial study concerning the **installation of the fibers**, in particular in the flexible chains.

Conclusions



- ✓ The reviewers would like to thank the proponents for the significant amount of work done preparing for the review, the very clear documentation and presentations.
- ✓ The case for the LAr upgrade was very well made and we endorse the plan as presented.
- ✓ We cannot see any significant technical problems with the proposed solution as it is presented at this time and would recommend that you proceed to the TDR.
 - In our summary we have given various recommendations which we believe the proponents should consider as they move towards a TDR.

Milano possible contributions

Baseplanes:

- redesign
- ~1/3 of the production in Italy
[collaboration with BNL, Orsay]

~~Layer Summing Boards:~~

- ~~➤ redesign~~
- ~~➤ ~1/3 of the production in Italy
[collaboration with BNL, Saclay]~~

On-detector new Lar Trigger Digitizer Board (LTDB):

- design of power distribution scheme for demonstrator and Phase I LTDB's, considering also compatibility for Phase II upgrade
- POL instead of LVDS, extension of the studies done in the framework of the Gruppo V - APOLLO Project (which used LAr as use case)
[collaboration with BNL]

Data formatting on LTDB:

- design of algorithms for data multiplexing/serialization using FPGA as a test bench
- Collaboration with BNL on radiation tests

Simulazioni:

- Simulazioni: sviluppo di algoritmi che utilizzino le supercelle a L1

- Interessi in vari aspetti del progetto con simulazioni, design e prototyping di componenti,...

Costi (kCHF)

Deliverables	Total	2013	2014	2015	2016
Baseplanes: constr, assembly, conn,...	1.076	0.007	0.007	0.531	0.531
1/3 produzione in Italia →	0.360	0.07	0.07	0.177	0.177
Layer Sum Boards (Barrel, EM Endcap)	0.689	0.014	0.000	0.000	0.675
Total (MCHF):	1.765	0.021	0.007	0.531	1.206
Total (Italy):	0.600	0.014	0.007	0.177	0.402

- Rinunciando a design e produzione delle LSB e mantenendo la produzione di circa 1/3 della produzione dei baseplanes, il possibile contributo italiano si riduce di un fattore 2:
 - 360 kCHF (era 600 kCHF)
- Abbiamo chiesto ad una ditta italiana una stima piu' precisa del costo della produzione dei baseplanes e siamo in attesa di una risposta:
 - Elfes Technology srl, Cinisello Balsamo (MI)

Item	# units	Prod end	Prod start	PRR	FDR
Frontend					
Baseplane	124	5-2017	11-2016	9-2016	2-2016
LSBs	1664	9-2017	9-2016	7-2017	12-2015
LTDB:	124	9-2017	3-2017	1-2017	6-2016
Analog Mezzanines	124*4	1-2017	1-2016	10-2015	4-2015
Optical pigtails	124*4	1-2017	7-2016	5-2016	10-2015
Cooling plates	124*2	1-2017	7-2016	5-2016	10-2015
Mainboards					
ADC	124*80	1-2017	1-2016	11-2015	4-2015
ASIC Serializer	124*160	1-2017	1-2016	11-2015	4-2015
ASIC Laser Driver	124*160	1-2017	1-2016	11-2015	4-2015
VCSEL mezzanine (TOSA)	124*160	1-2017	1-2016	11-2015	4-2015
DC Powering	124	1-2017	1-2016	11-2015	4-2015
Base PCB	124	1-2017	1-2016	11-2015	4-2015
Long Fibers					
	58	7-2017	1-2017	11-2016	4-2016
Backend					
ATCA shelves	3	12-2016	9-2016	7-2016	-
LDPB/GBTD	34	9-2017	3-2017	1-2017	6-2016
AMC	34*4	1-2017	1-2016	11-2015	4-2015
IPMC	34*1	1-2017	1-2016	11-2015	4-2015
MMC	34*4	1-2017	1-2016	11-2015	4-2015
Optical pigtails	34*4	1-2017	1-2016	11-2015	4-2015
MicroPod Cooling block	34*4*4	1-2017	1-2016	11-2015	4-2015
Carrier Board	34	1-2017	1-2016	11-2015	4-2015
TTC Optical Couplers	3	7-2017	1-2017	10-2016	-
In shelf switches	3*2	7-2017	1-2017	10-2016	-
Receiver PCs	3	7-2017	1-2017	10-2016	-
Controlling PCs	2	7-2017	1-2017	10-2016	-

New baseplane design

HFEC Type	HFEC	FEB	CALIB	CONT	TBB	TDB
EMB	64	896	64	64	64	-
EMEC Std	32	416	32	32	32	-
EMEC Special	8	136	16	16	24	-
HEC	8	48	8	8	-	16
FCAL	2	28	2	2	-	4
Total	114	1524	122	122	120	20

Baseplane	LTDB	LDPB
64	64	64
32	32	32
8	8	16
8	8	8
2	4	4
114	116	124

- EMB (Milano/Orsay): ~finished
- EMEC standard (Orsay): ~finished
- EMEC special (Milano/Orsay): finalizing design
- HEC (Milano? Triumph?): not started
- FCAL (Canada/Arizona): not started

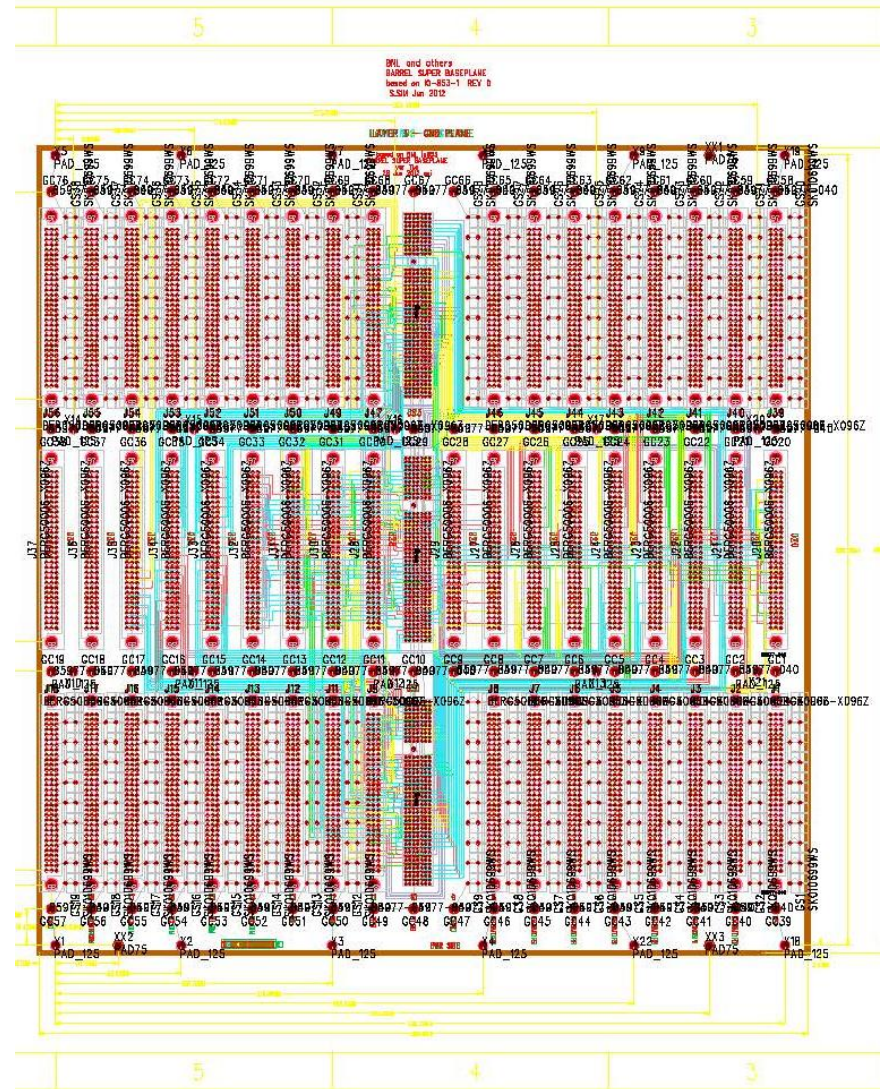
Finalizing studies on signal extraction at high-Z vs. double driver with respect to signal attenuation and delay

Produzione dei primi prototipi potrebbe cominciare in Aprile:

- Per il 2013 ci sono stati assegnati 5 keuro sj per questa produzione

Barrel baseplane

- La scheda e' stata progettata usando:
 - Solo stripline con impedenza controllata (50 ohm, tracce di 150 μ m)
 - Usando 5 layers, uno in piu' della scheda esistente, per migliorare il routing
 - Non introducendo "via" per avere migliore signal integrity.
 - Per il connettore della LTDB (fila centrale della figura) e' stato scelto un connettore Hard Metric a 2mm con shielding integrato.
 - Lo spazio fra le tracce e' $\sim 300 \mu$ m per avere basso crosstalk ($< 1 \%$)
- Ulteriori verifiche sul layout:
 - Simulazione a piena scheda con Hyperlinx dell'integrita' del segnale
 - Simulazione dei segnali ottenuta con Spice e generazione dei modelli IBIS
 - **Eventuale ottimizzazione del layout in accordo con il produttore del prototipo della scheda**



Milano involvement and responsibilities

- People involved (7 persone, ≈ 3 FTE al momento):
 - M. Citterio (DT): design nuovi baseplane, nuova distribuzione potenza
 - F. Tartarelli (PR): simulazione performance, tests
 - L. Carminati (RU): simulazione performance
 - M. Fanti (RU): simulazione performance
 - M. Lazzaroni (PA): nuova distribuzione potenza (in sinergia con APOLLO)
 - M. Alderighi (Ric. INAF): FPGA redundant code
 - R. Turra (AR): simulazione performance
 - + 1 progettista del servizio elettronica
- Attualmente il nostro l'involvement e' in linea con quanto disponibili presso gli altri istituti della collaborazione LAr

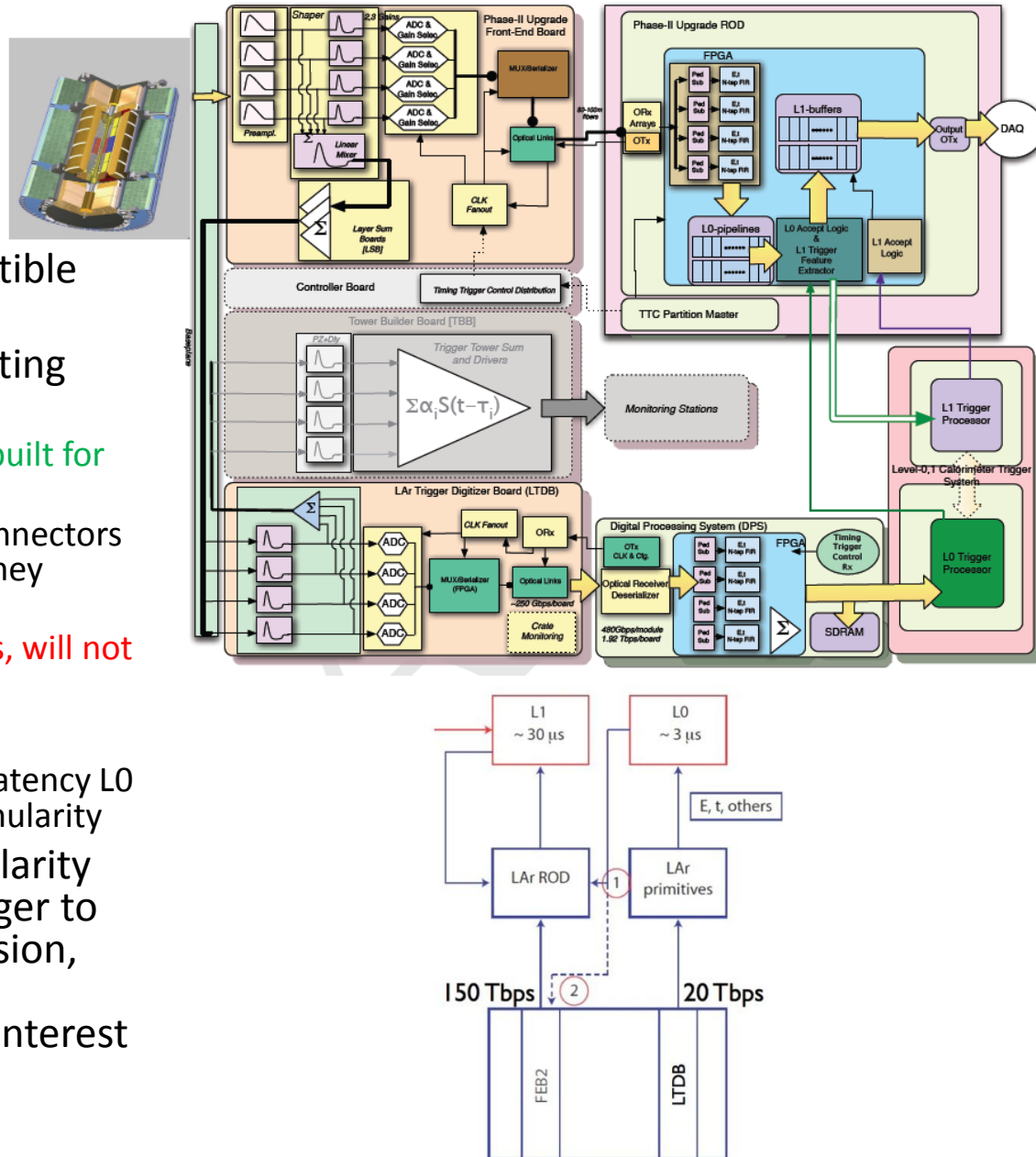
Institution	Interest	
Arizona	WG1	WG5 WG6
Triumpf+Canada	WG1	WG3
LAPP	WG4	WG5 WG6
LAL	WG1	WG3
Milano	WG1	WG3
LPSC	WG2	
Dubna	WG1	WG3
Nevis	WG2	
SMU	WG2	
Dresden	WG5	WG6
CERN	WG2	WG4
SUNYSB	WG4	WG5
Saclay	WG1	WG3
BNL	WG1	WG2 WG3 (WG4) WG5 (WG6)
PITT	WG1	
CPPM	WG4	WG5
Lebedev	WG1	WG3
Novosibirsk	WG2	WG5
Montreal		
20/03/2013	TOTAL 20 Institutions 48 FTE 103 names	

Phase II

- Apart of the possibility of replacing FCAL and HEC electronics (still under discussion), the main change to LAr will be the replacement of all the 1524 Front End Boards (FEBs):
 - the total dose for an integrated luminosity of 3000 fb⁻¹ exceeds the FEB specifications
 - the Level-1 trigger latency may exceed the depth of the analog pipeline memories installed on the FEBs
 - natural ageing of electronic components
- New FEBs (FEB2s) will be designed with fully digital free running readout, i.e. avoiding trigger signal receivers and data buffering on the FEB
 - signals from all calorimeter cells are digitized at 40 MHz and sent off-detector

Phase II

- The Phase I upgrade is compatible with the Phase II
- FEB2s will be fitted in the existing Front End Crates and
 - will use the same baseplanes built for Phase I
 - LAr has already acquired all connectors needed for the FEB2s before they disappear from market
 - LSBs, being FEB daughter cards, will not be kept
- Phase I LTDBs will also stay
 - Can be used to provide a low latency L0 trigger using the supercell granularity
- The full LAr calorimeter granularity will be available to the L1 trigger to further refine the trigger decision, possibly based on refined reconstruction in a region-of-interest determined by L0.



Milano interests for Phase II

- Continue involvement with:
 - power distribution architecture
 - new front-end (for the current calo FE we have realized the preamps)
- Powering distribution: power architecture with main converters and point-of-load converters (POL) close to the front-end
- New Front-End: analog preamplification and shaping stages will be integrated in a single ASIC: Liquid Argon Preamp and Shaper (LAPAS)
 - Implementation of a wide dynamic range single ended preamp followed by low power differential shaping stages with multiple gains
 - SiGe technology (IBM, IHP)

Demonstrator

- Demonstrate that we know how to make baseplane, install them and find possible problems on detector
- Show that analog signals are still OK and there are no faults in the digital functions
- Show waveforms of new super cells (and compare with legacy system)
- Front end electronics
 - How to power: switching regulator? Impact on noise
 - How to cool
 - How to reliably transmit data in a real environment
- Show the cell mapping is right for the new system and for the existing analog TBB
- Full integration:
 - at Board level and at Crate level
 - Back end electronics
 - Demonstrate data processing
- Steps
 - Step 1: use whatever available (COTS ADC, etc.)
 - Step 2: migrate towards final (ASIC based)

Phase II: detector upgrade options

- **Option 0:** No change neither of the HEC cold electronics nor of the FCal detectors.
- **Option 1:** If the HEC cold electronics have to be replaced, the large cold cryostat cover would have to be opened and the irradiated FCal would have to be removed. A newly built cold FCal (sFCal) would then be inserted before closing the cryostat.
- **Option 2:** If the HEC cold electronics do not have to be replaced, the cold FCal would be replaced by a new one of the sFCal type. It is anticipated that only the small cover of the cold vessel, the FCal bulkhead, would have to be removed.
- **Option 3:** If the HEC cold electronics do not have to be replaced, the cold FCal would stay in place and a new small calorimeter (Mini-FCal) would be placed in front of it. In this case only the cryostat warm vessel would have to be opened.
- Draft a document with selection process and tentative selection criteria. Decision process should conclude within LAr by end 2013/beginning 2014. Independent LAr review board

Motivations: MET

5.3 Improved MET Trigger Performance

Missing energy triggers are becoming more and more important in SUSY searches, for example for monojet signatures, and in stop and sbottom searches in the kinematic region where squark and neutralino mass are nearly degenerate [21].

The Super-Cell readout provides energy information from each layer in the LAr Calorimeter separately. Since the pile-up events contain a rather soft hadronic p_T spectrum, the pile-up particles are absorbed predominantly in the first layers of the calorimeter, seen from the interaction point. The E_T^{miss} reconstruction can thus become more robust against pile-up if energy thresholds for E_T^{miss} calculation are not applied on trigger towers as a whole, but layer-by-layer. Figure 11 demonstrates that after threshold optimisation the pile-up contribution can be nearly eliminated [6]. In particular in the high E_T^{miss} region, the background rates to physics signatures with high E_T^{miss} is significantly reduced.

