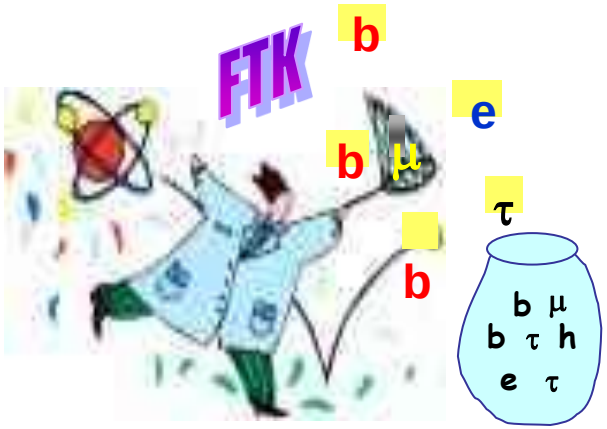
FTK Status – future developments

OUTLINE

HARDWARE

VERTICAL SLICE

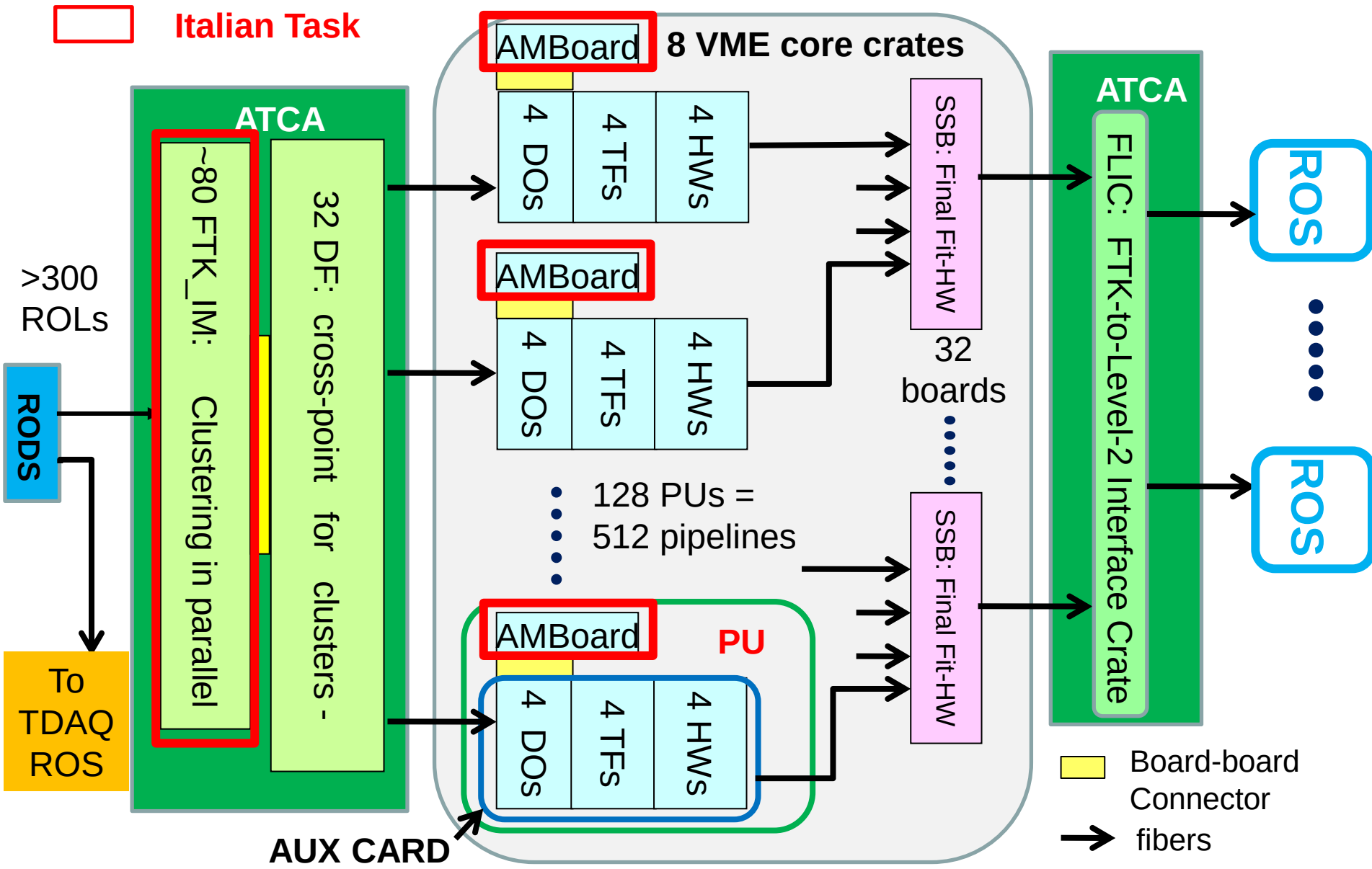
IMOU (sblocco SJ) – TDR – MOU schedule



Paola Giannetti for the FTK collaboration

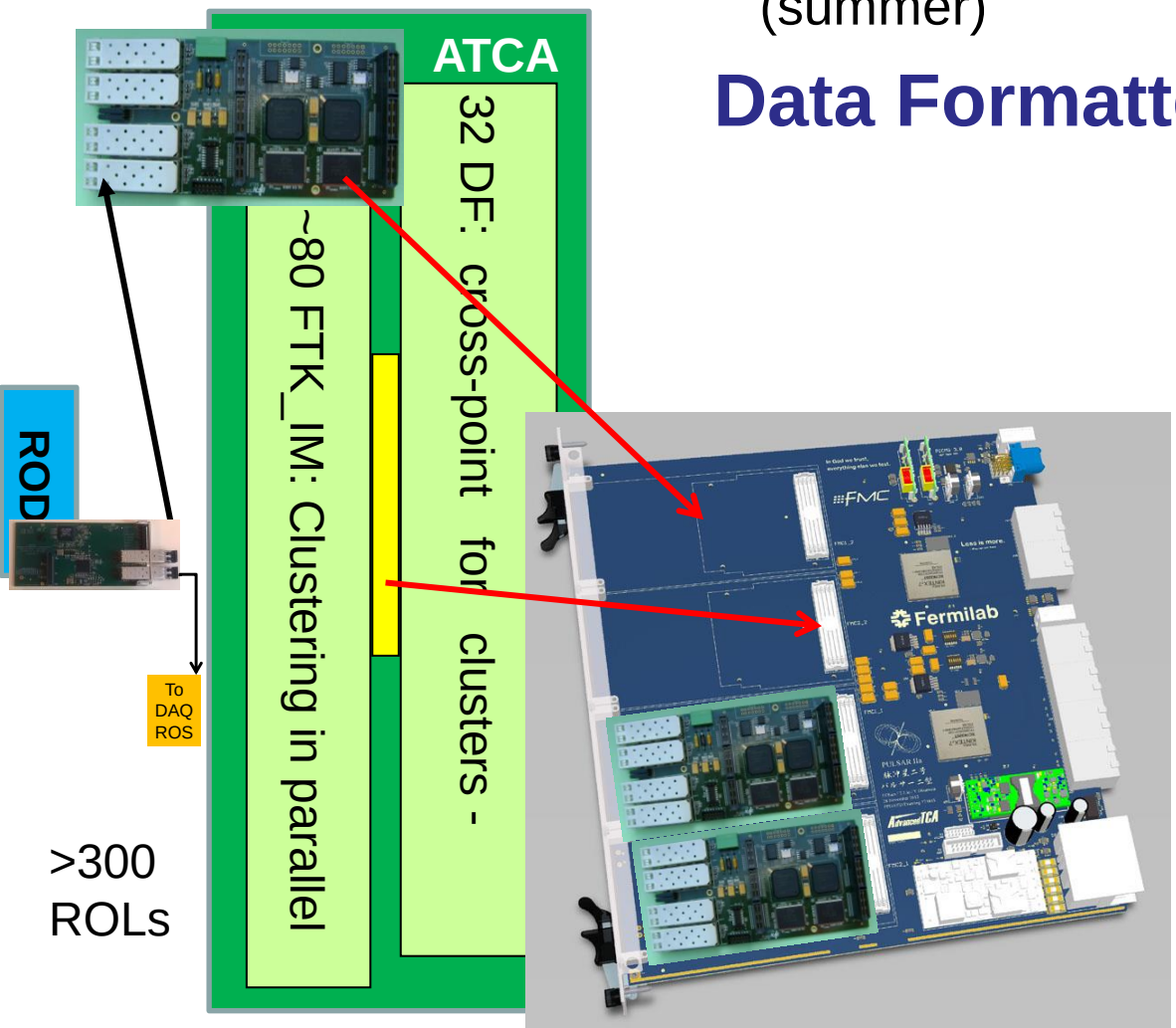
FTK global view

16400 AMchips
~2000 FPGAs
Thousands of serial links



FTK input mezzanine (FTK_IM Frascati Waseda)

- 4 FTK_IM/DF receive ROD's data and do cluster finding.
- Prototypes produced, tested, and used @P1.
- Few changes needed for DF compatibility.
- Final Production after tests with IBL BOC (summer)

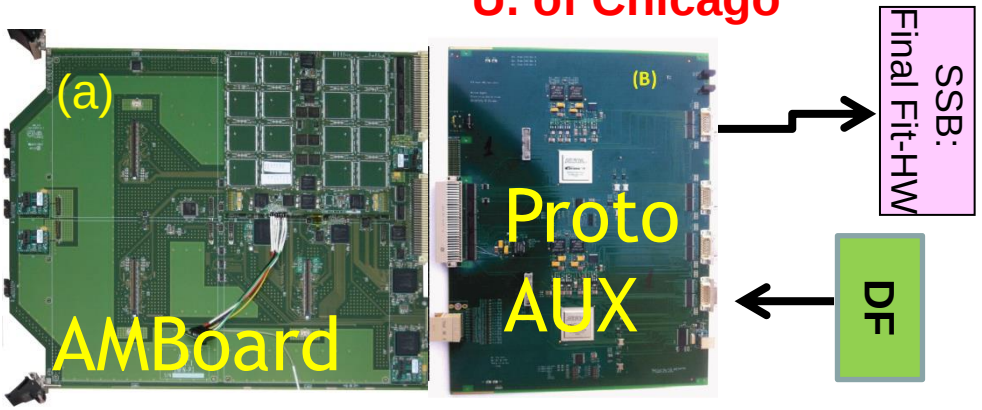


Data Formatter (DF - Fermilab)

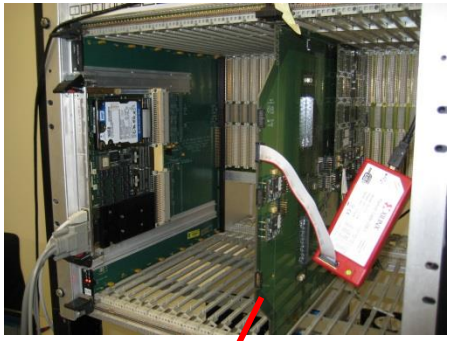
- Distributes found clusters to 64 FTK η-ϕ towers. ATCA for complex fiber-to-tower mapping.
- Designed and being manufactured
- Next Summer combined tests

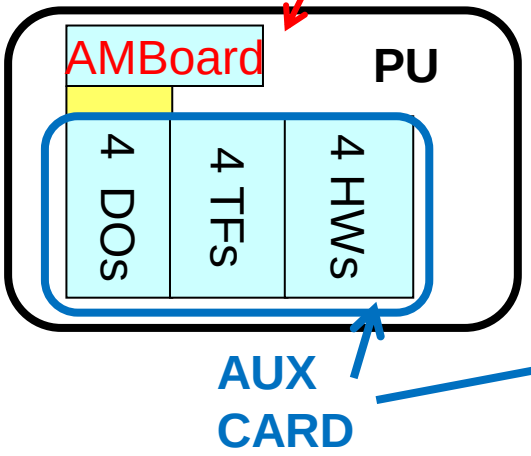
FTK Processor Unit (PU)

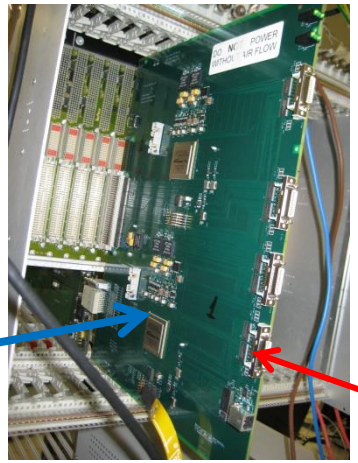
U. of Chicago



CDF Crate for tests (PISA-PERUGIA)







- 128 PUs do pattern matching and the 1st stage track fitting.
- A PU consists of an Associative Memory VME board (a)(AMB-Europe) and a large Auxiliary Card (b) (AUX-UoC) behind it.

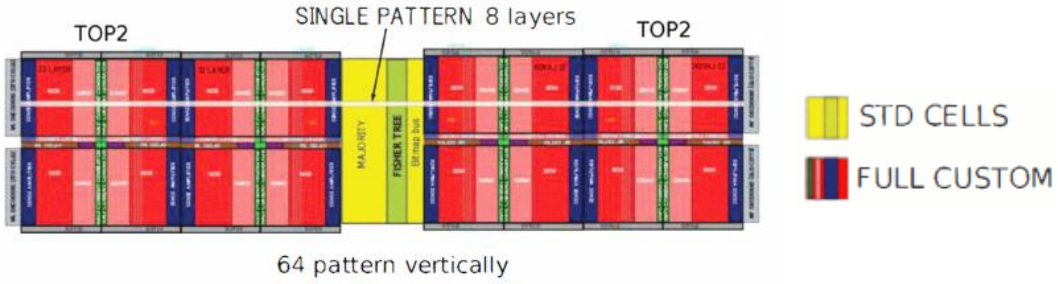
We have tested them together in the Pisa test stand:
long serial links OK

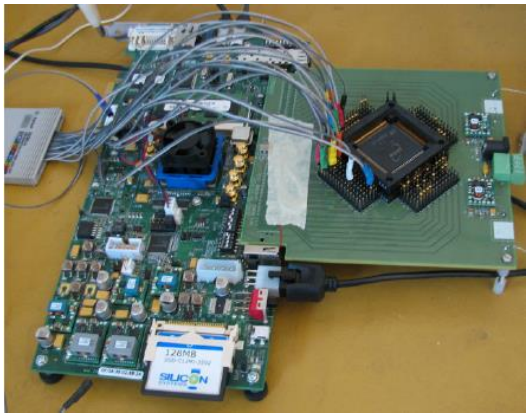
AM System MI-LNF-PI-LPNHE

DOI:10.1109/ANIMMA.2011.6172856

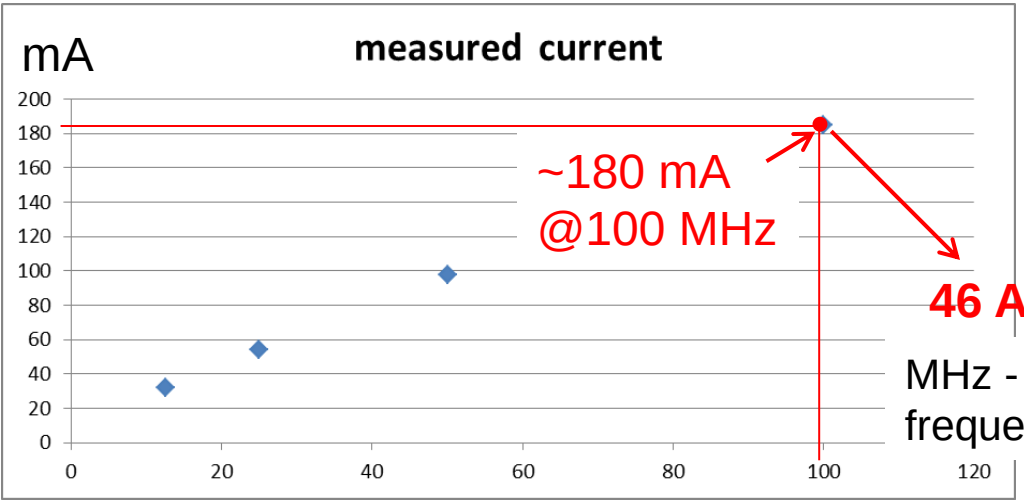
(1) AM chip04: TMSC 65 nm with Variable Resolution

- custom cell to reduce pattern size: 8k patterns in 14 mm^2.





- Yield>80% - tests successful
- 64kpatt power consumption lower than AMchip03 (180 nm)
- but slightly higher than desired.
- For AMchip05 core down from 1.2 v to 1.0 v to reduce further the power.

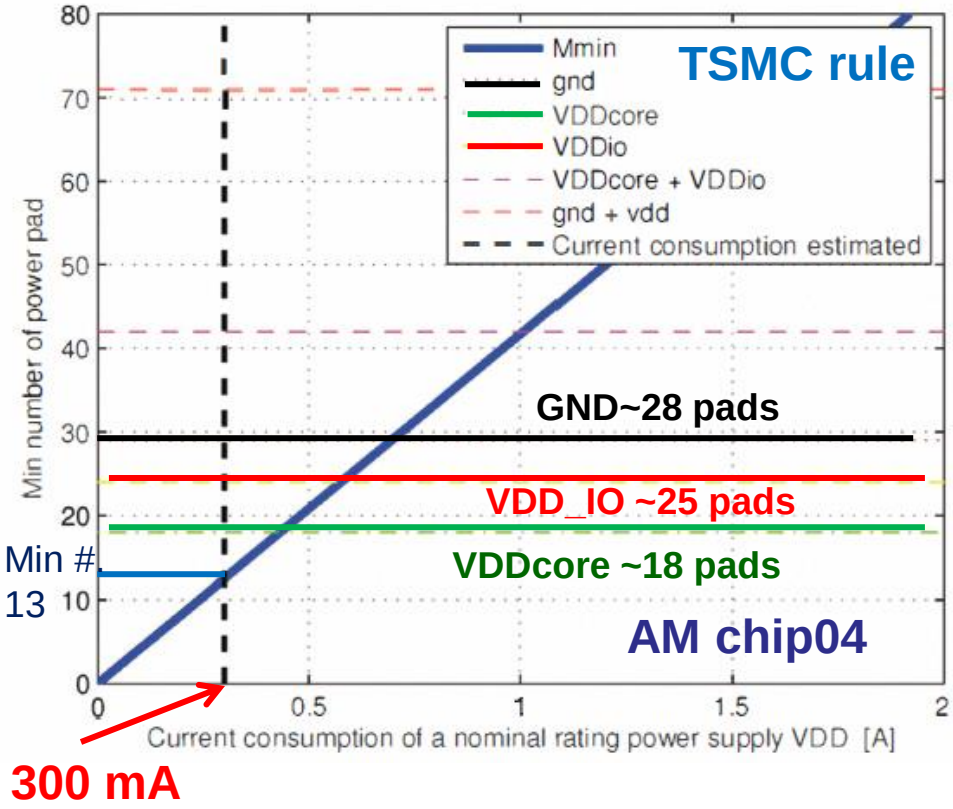


AMchip03 (5 kpatt): 1 A → **1,8 W**
AMchip05 (64 kpatt): 1,45 A→ **1,7 W**
expected **1,6 W**

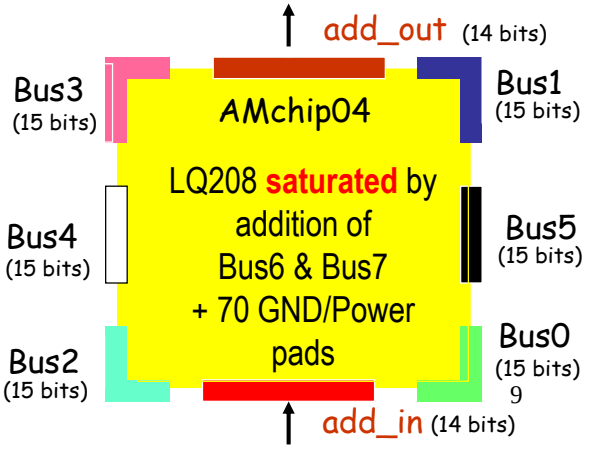
Extremely good result but we would like to have **current/LAMB < 40 A**

AM System (2) AM chip05: # of power/GND pads

MI-LNF-PI-LPNHE



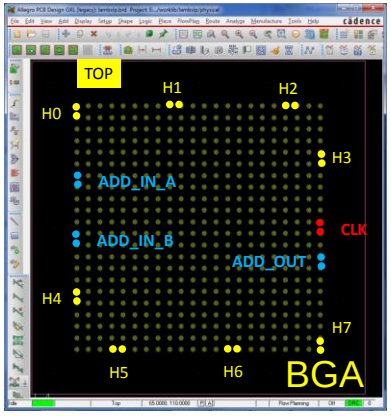
Min #. = 320 pads



Reaction:

AMchip05→ all buses **serialized** → recently **purchased IP**.

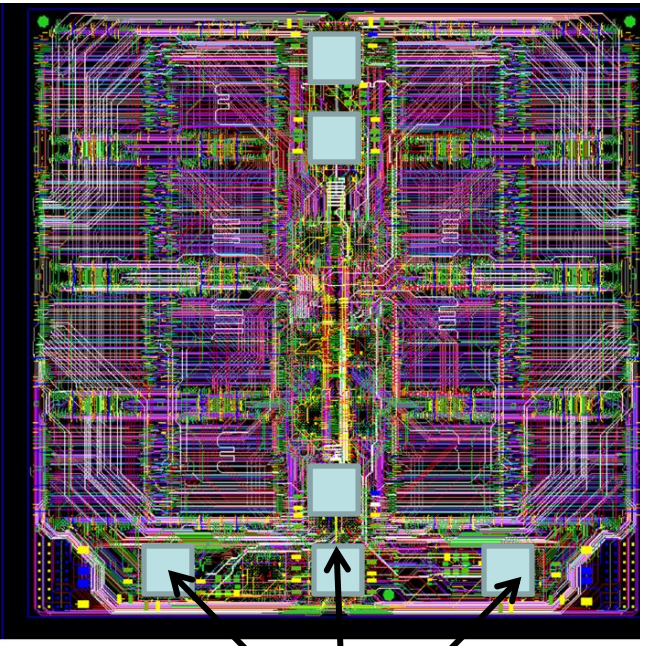
use 23x23 mm^2 **BGA** instead of **LQ208**



mini@sic → **tape out March 2013**.

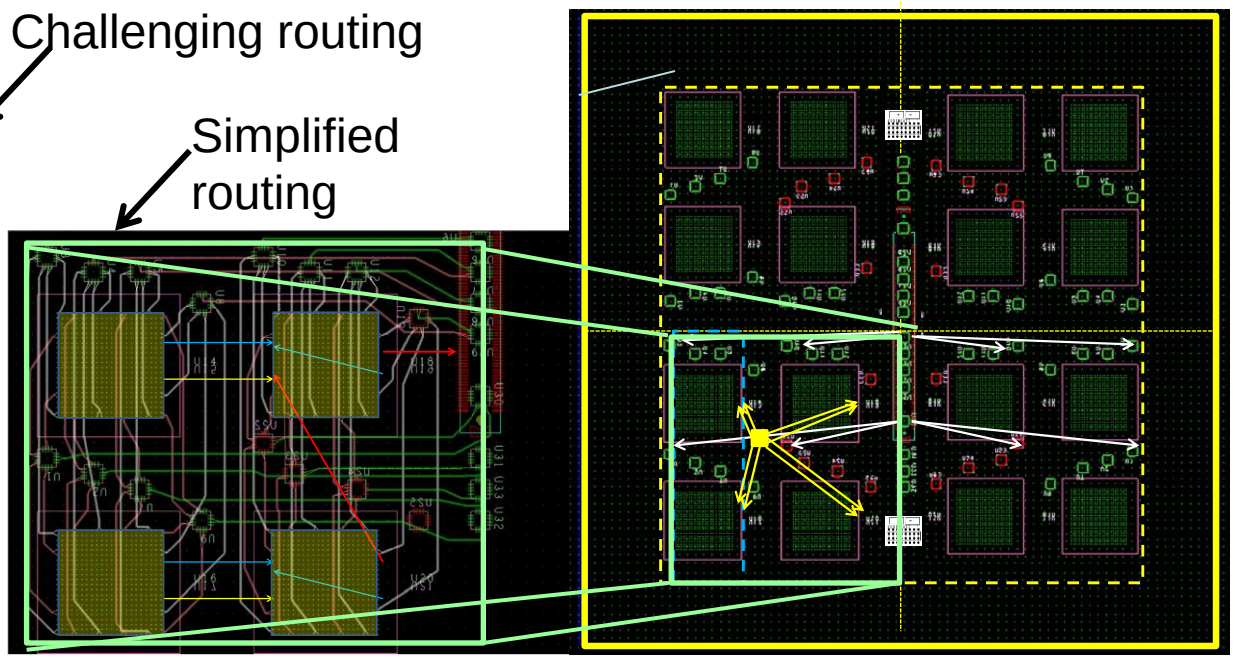
32k or 64k patt chip → **tape out Jan 2014**.

AM System (3) A new LAMB for AM chip05: all buses on serial links



Challenging routing

Simplified routing



FPGAs on LAMBFTK

PG-PI-PAVIA

PG-PI LAMBSLP **reduced size no FPGAs**

BGA with **Flip chip** technique:

(1) high frequency solution for 2.5 Gb/s links

(2) Caps included in the package to be able to solder BGA on both sides **(32 BGA/LAMB)**

(3) Possibility of **multi-packaging**

(4) **AMchip05 more expensive** than expected (IP, flip chip BGA, multipackaging)
INFN budget insufficient → the **AM system** try to become **EUROPEAN**

AM System (4) IAPP and STREP FP7 applications for extra funds

People - Manpower
Funded 1.5 Meuros
Starts Feb 2013
4 years

ICT - funds for Amchip – **requested to EC 3 Meuros**

IAPP – all for Phase 1

UniPisa (Pisa) Dell'Orso - **AM system boards**

LPNHE (Paris) Calderini - **AMchip** (applied also to its funding agency)

AUTH (Tessaloniki) Kordas **board firmware – simulation**

CERN (TE-MPE-EM section) Formenti **board design**

CAEN (Viareggio) Petrucci - **Integration**

Prisma Electronics (Alexandroupolis) Mermigli

board development, assembly, test – firmware

IAPP consortium

Strong technical support

1) WorkPackage 1 Prototype Construction & Production Validation
2) WorkPackage 2 Infrastructure & Integration
3) WorkPackage 3 Commissioning
4) WorkPackage 4 Architecture Simulation
5) WorkPackage 5 Image Processing (UniPisa)
6) WorkPackage 6 Silicon Detectors (CNRS)
7) WorkPackage 7 Outreach (AUTH)
8) WorkPackage 8 Workshops & Trainings (AUTH)

STREP (in Cooperation): ADVANTAGES for FASE I

STREP (coordinator INFN) would add for FTK in fase I:
University of Geneva on **AM system Boards** (applied also to its funding agency)
……..

IMEC for **flip chip multi-packaging** and AMchip submissions to TSMC
MICROTEST - **test setup** for AMchip massive production tests
} **Strong technical support**

Requested money for HW development, setup at the companies:

- AMchip prototype 250 keuros
- Multi-Packaging – small production – tests before packaging 145 keuros + 75 keuros for studies of fesibility
- Tests of large production at the company: 175 + 25 keuros

STREP: Other ADVANTAGES for FASE II: money to study applications

STREP (coordinator INFN) would add for FTK in Phase II:
University of Heidelberg on **3D AM chip** (applied also to its funding agency)
UCL (London) for AMchip use in L1 tracking
CMS: INFN Pisa-University of Florence for use in L1 tracking
AUTH, University of Florence (Del Viva) for applications outside HEP

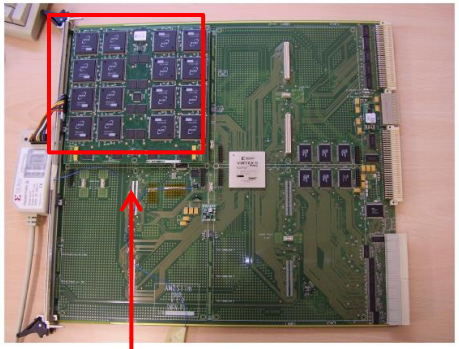
AM System (5) The story of AMB

AMBSLP for AMC05 (Europe)

AMBslim5 64 AMC03 for Vertical slice

AMBslim5++ 128 AMC03 for cooling tests

AMBFTK for AMC04(PI-MI-PV))



(a)

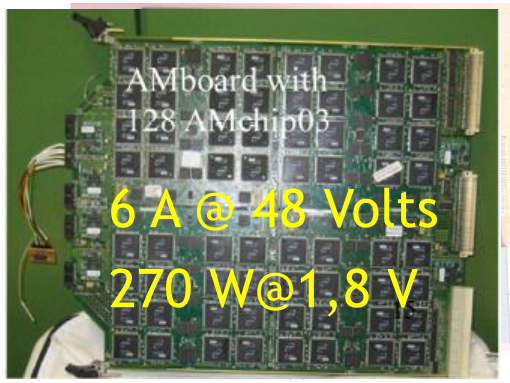
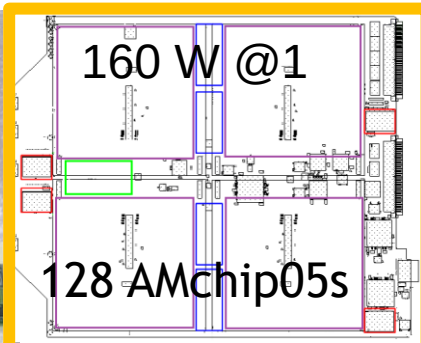


Figure 3: **AM Board** - (a) standard VME VIPA version (b) custom 48V version



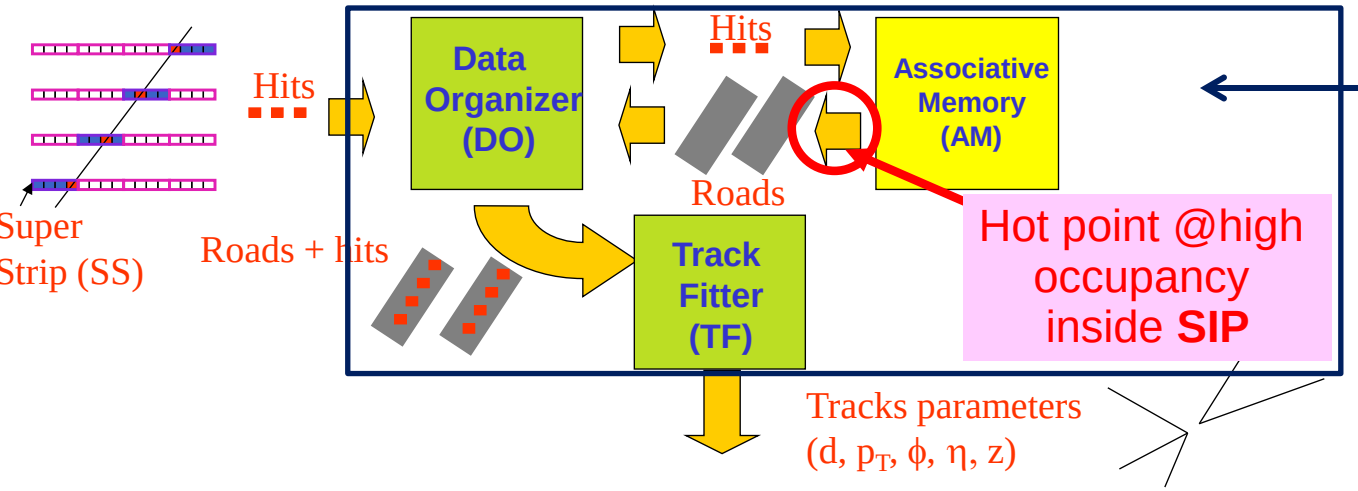
To be tested
In summer
2014

4 mezzanines (LAMB) with 32 AM chips on a AMB (128 Amchips/AMB)

- Older version **used** in the **vertical slice**.
- **AMBFTK** consistent with **AMchip04** - **tested** with the Proto-AUX.
- VME communication and the high speed serial links are OK.
- New Serial Link Processor needed: **AMBSLP** and **LAMBSLP**

New Ideas for PHASE II - FTK could become smaller and smaller

Multi-packaging FPGA & Amchip – mini FTK - Multipackaging

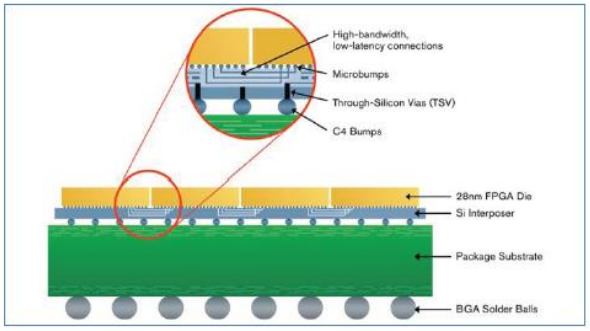


Pattern matching & **track fitting** (TF) **sqweezed in a SIP** (BGA 23x23) **TF highly parallelized**

(1) We have a very interesting **quotation** for FPGA **bare dies** to be packaged with AMchips

(2) IMEC support for feasibility studies

(3) FTK SIP (System In Package) becomes a real possibility – **large impact on AM bank sizes**



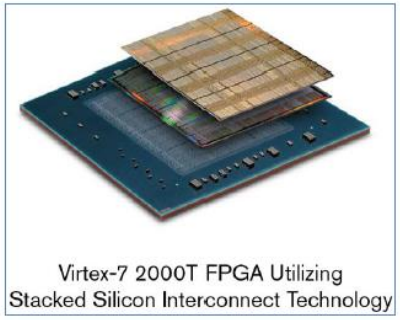
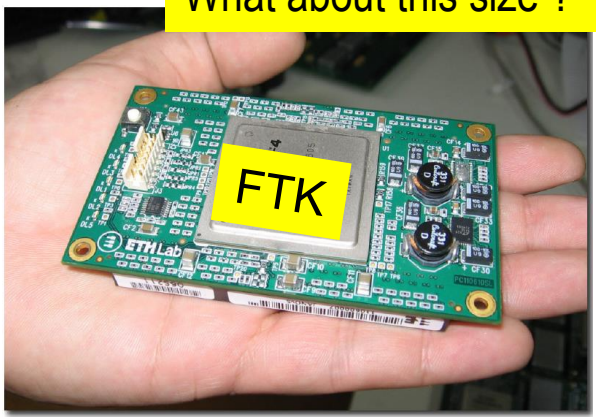


Fig. 1.1.7 Left and right - example of silicon interposer approach for Xilinx Virtex-7 FPGA; This approach will constitute the basis for the innovations that the NEURONS project will develop as described in the text.

FTK miniaturization- FPGA large parallelization
- Phase I - for offline applications: few future LAMBs to cover the whole detector (simulation)

Goal: build a Lamb that can fit in a PC or can be accessed by a PC.

What about this size ?



FP7 IAPP - STREP PROGRAM
Coordinated by University of Pisa
and INFN-Pisa
If STREP is successful it is natural to apply also to IP after STREP

- Phase II - for online applications + larger AMchips, larger banks

FTK vertical slice goals and status

- Goals
  - Use of old FTK prototypes to verify integration with ATLAS TDAQ
  - Verify real data FTK output roads agree with FTK simulation
- Status: ***completed***

Results

  - Data flow and integration tested up to 70kHz

    even with low SCT threshold sending huge "noise" events
  - Cosmics run with FTK included for a few days
  - Real bank loaded and decoding real data format active
  - Simulation applied to real events with real bank ready
  - Stopless removal is working
  - Data taken and compared successfully with simulation

STATO del TDR - IMOU - MOU

- In **April** FTK TDR ready with very simplified physics case
- In **September** TDAQ TDR should include the FTK complete physics case
- ~**April 15** we should know the results of the **STREP** application (FP7) that should cover the AMchip extra- costs
- **In April** we should know also the result of **University of Geneva** application for 400 keuro for FTK
- **June** we should know about **LPNHE** application for FTK (~200 keuro)
- **Heidelberg** should have already ~100 keuro for FTK
- **Waseda (Japan)** is allowed to ask new funds for FTK

Starting from **May** we should be able to prepare the **IMOU**

To be ready for the **MOU** in **Autumn**

Conclusions

- There is good progress on all of the hardware components.
- Progress has been made on the vertical slice.
- FTK collaboration is growing and post TDR ideas are taking shape

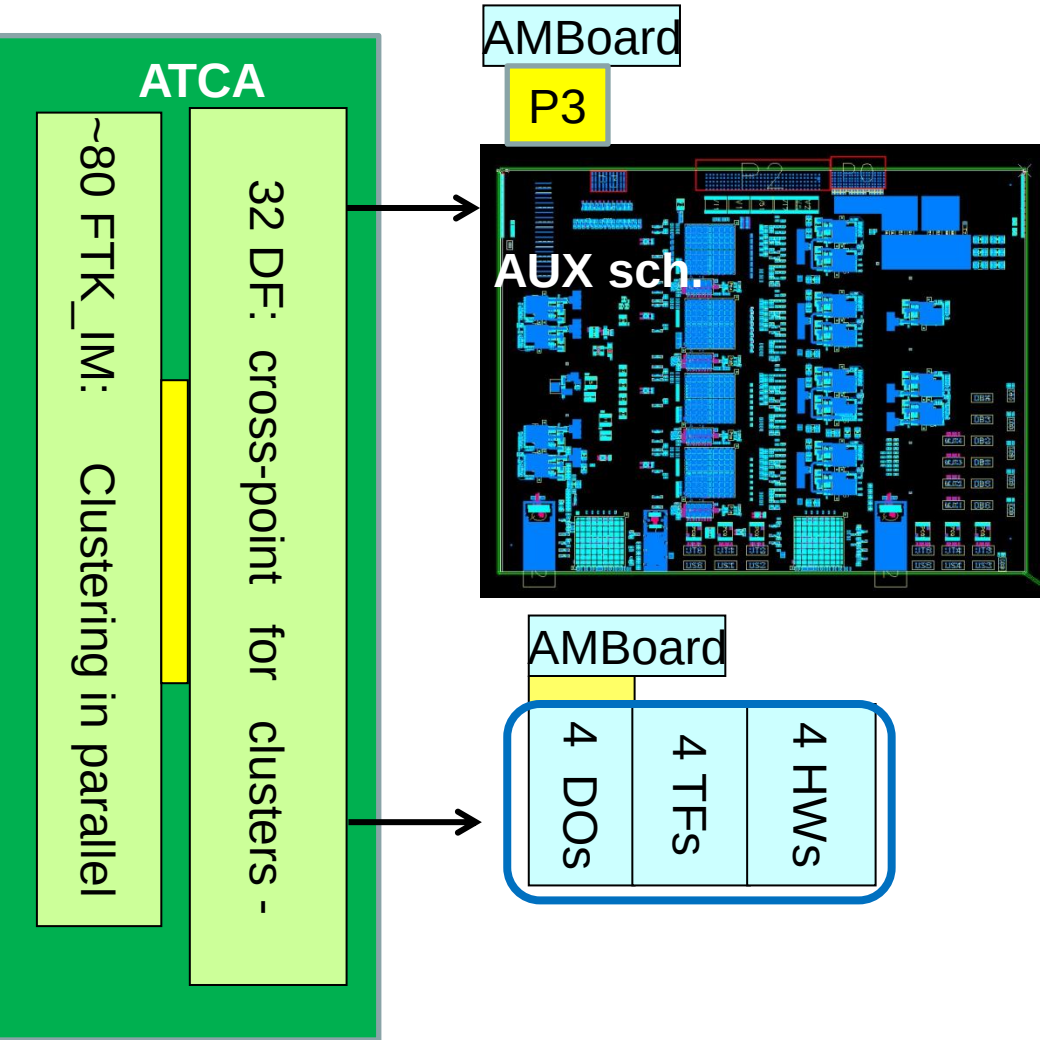
  (***15 FTE + 1,5 FTE*** from IAPP)
- We will know soon which will be the **EUROPEAN & Japanease new support** to the FTK construction
- Phase II: the **same developments** will be used for ***Level 2 and Level 1*** tracking in 2023.

(8) The AM system schedule

	2013						2014												
ASICs Development																			
AMchip05 design & **tape-out**																			
2500 Amchips **tape-out**																			
Test of prototypes										TEST									
2D Multipackaging: 2 AMchips on the same plan							Multipack. chip						MultiPack						
Concept of test and Translation of test vectors																			
Test SW development, Test debug, Test of samples																TEST			
Board Development																			
Firmware and software development	old AMBOARD									1 chip Mezz			first av. LAMB						
LAMB design and development	Design ready									PCB									
LAMB's assembly and first quality test of boards																			
1-AMchip mezzanine for AMchip tests design and test vector design			Pcb design				firm.test												
Firmware for array of AMchip tests and LAMB tests																			
Loadboard Design for Microtest tester																			

Installation of the **first 8 PUs** expected at the beginning of 2015

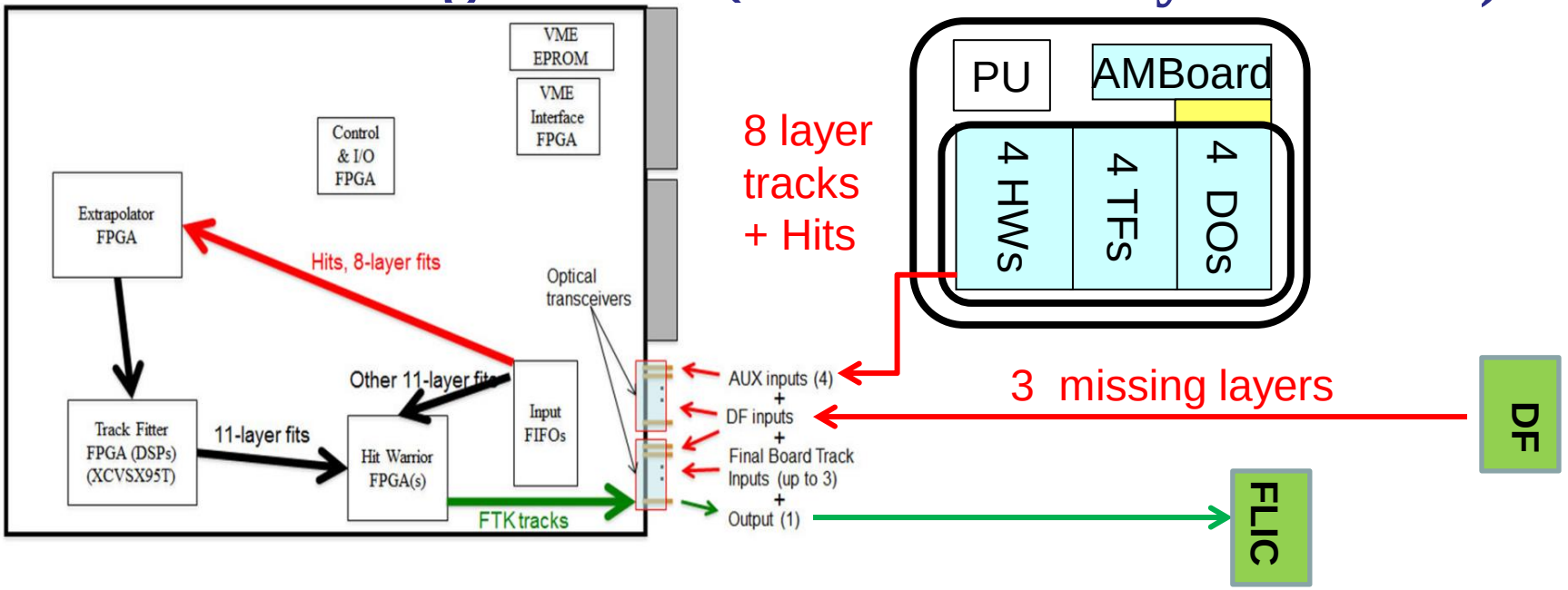
The final AUX (UoC)



- Receives DF data, sends coarse hits to AMB, receives back roads, and does the 1st-stage fitting (8 layers).
- Final board design close to completion.
- Firmware written; testing/integration in progress.
- Engineering review in March.
- Produce prototype in April.

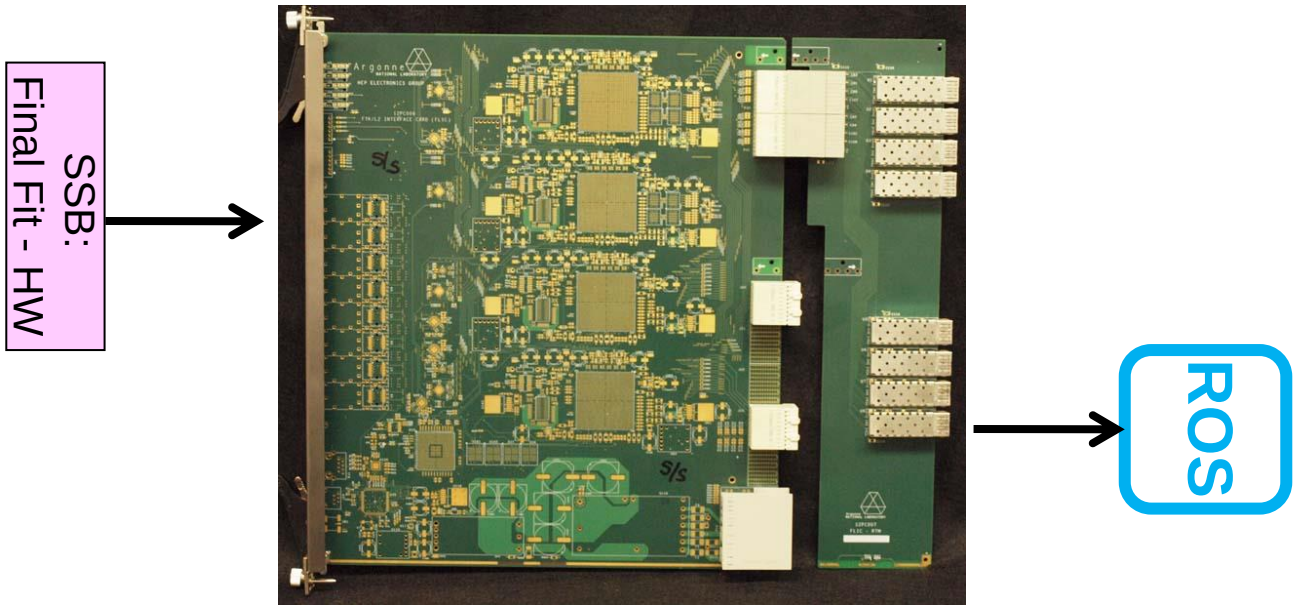
2012	ITALY				USA 01/10/2011	2012		JAPAN 01/04/2012			Germany 2012		
Production					ANL	10							
NO PRODUCTION	Amboard-2 scheda/regior	38	0		Chicago	13							
	DF Mezzanines	80	0		FNAL	11			95				
	LAMB	15	12		Illinois	7							
prototypes	proto-AMBoard		15		TOT	41							
new-FTK_IM			5										
test Amchip			10										
Vertical Slice			3	24									
Services					Services	97		Services	40				
					TOT - M&S	138							
						30							
AM R&D	MPW submission kUSD	115				25	110				MPW submission	55	25
	MPW small production	30				30					MPW small productio	30	
Tech. Personnel						313							
TOT 2012		240	45	24	TOT kusd	223		TOT	135	100	TOT 2012 k€	63	
2013					ott-12	2013					2013		
Production					ANL	28							
					Chic. 1/3 AUX	250							
	DF Mezzanines	55	135		FNAL 1/2 DF	140		DF Mezzanine	55				
prototypes	LAMB	32	12		Illinois 1/2 final	86							
prototypes	Amboard		10		TOT-prod	504							
AM	MPW submission kUSD		115										
Tech. Personnel					AM only	80							
TOT 2013		87	272		TOT kusd	504		TOT	55	50	TOT 2013 k€		
2014					ott-13						2014		
Production					ANL								
	LAMB		32		Chic. 1/3 AUX	250							
	Amboard		38		FNAL 1/2 DF	100							
					Illinois 1/2 final	86		Services	30				
					TOT-prod	436					MLM masks 1/3	168	
	MLM masks 1/3	335				168	244						
AM production	6 wafers-2 AMBs	20	30			20					6 wafers-2 AMBs	17	
Tech. Personnel					AM only	80							
TOT 2014		261	100		TOT kusd	624		TOT	30	30	TOT 2014 k€	136	
TOT PRIMA 2015			681										
2015					ott-14						2015		
Production					ANL								
	Amboard -2 schede	37			Chic. 1/3 AUX	250							
	LAMB for 2 boards	32			FNAL			**=not approved yet					
					Illinois			Services**	15				
					TOT-prod	250							
AM production	6 wafers-2 AMBs -kusd	17				34	44	12 wafers-4 A	34		12 wafers-4 AMBs -kus	34	
Tech. Personnel					AM only	40							
TOT 2015		82			TOT kusd	284			40	20	TOT 2015 k€	25	
2016					ott-15						2016		
	Amboard - 4 schede	74						**=not approved yet					
	LAMB	64						Services**	15				
AM production	12 wafers-4 AMBs -kusd	34				68	89	12 wafers-4 A	34		12 wafers-4 AMBs -kus	34	
Tech. Personnel					AM only								
TOT 2016		163			TOT kusd	68			40	20	TOT 2016 k€	25	
2017					ott-16						2017		
	Amboard - 4 schede	74											
	LAMB	64											
AM R&D	12 wafers-4 AMBs -kusd	34				0		12 wafers-4 A	34		12 wafers-4 AMBs -kus	34	
Tech. Personnel					AM only								
TOT 2017		163	408		TOT kusd	0			25	20	TOT 2017 k€	25	
	SUPER TOT k€	1185			TOT M&S k$	1466							

Second Stage Board (SSB-University of Illinois)



- SSB: **full 11-layer fit**: (a) receives 8-layer good tracks from the PU (b) find hits in the missing 3 silicon layers, (c) fit tracks with 11 lay, (d) removes duplicates.
- basic firmware functions written, testing in progress.
- After that, board design will be finalized.
- An engineering review is planned for late March or early April, with a prototype to be built shortly after.

FTK-to-Level-2 Interface Crate (FLIC-Argonne)



- FLIC sends tracks to ROS's
- ATCA favors communication for global functions like primary vertex finding.
- As with the DF, an early prototype is needed to start exercising the new (to us) ATCA standards.
- first prototype board is now being loaded.

Performance Studies - plan

- **FTK group: update performance for *μ*'s, *τ*'s, and *b*-tagging, and study *e*'s and track-based E_T^{miss}.**
- **The TDAQ and ATLAS communities are interested in seeing how FTK can improve level-2 performance for such things as:**
  - **global quantities such as finding all primary vertices to enable the use of jet vertex fraction and pile-up-corrected jet energies**
  - **track jets**
  - ***μ/e* isolation using the same cone size as offline (to avoid uncorrelated inefficiencies)**
  - **inside-out tracking for the 2nd *μ* in dimuon triggers to reduce the effect of the muon trigger gaps.**
- **All of these studies require Monte Carlo samples.**

TDR needed samples

- **Samples to study trigger at 3E34 (pileup 70)**
  - **W e Z to electrons and muons (10k each)**
  - **bb samples with lepton filter (50k)**
  - **VBF Higgs in taus @125 GeV (40k)**
  - **WH→light jets (100k) and WH→bb (40k)**
  - **Z→bb (10k)**
  - **ttbar (40k)**
  - **Dijet: J0-J5 (20k each)**
  - **No truth sliming: Min-bias, WH→tautau and WH→bb (2k each)**
- **All the samples have to be generated with IBL**

Simulation Status

- **Requested samples for TDR studies (also samples for other upgrades) have not been produced due to the priority of analyzing 2012 data sample. (upgrade management working on the problem.)**
- **We recently decided to start with samples that do exist.**
  - **46 pile-up TDAQ upgrade samples (without IBL)**
  - **perhaps a few 70 pile-up samples that have been made for TDAQ**
- **We have been approved by US ATLAS for some of the US beyond-pledge capacity for our private production of 70 pile-up samples (using standard ATLAS scripts).**

- **We are starting discussions with the simulation and production groups on how best to streamline our simulation for post-LS1 operations.**