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Variable resolution Associative Memory optimization and simulation for the ATLAS FastTracker project

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ATLAS is planning to use a hardware processor, the Fast Tracker (FTK), to perform tracking at the level1 event rate (100 KHz).
The most recent prototype of the Associative Memory (AM) chip developed for the ATLAS Fast Tracker includes ternary logic that can store the "don't care"(DC) value. This feature allows enormous flexibility tuning to the precision of the match for each pattern and each detector layer.
We have studied different methods of building the pattern bank exploiting don't care bits.
We show how merging similar precision patterns into coarser ones achieves the goal of having few enough patterns to fit in the hardware, while maintaining good efficiency and the required rejection against random combinations of hits.
We finally present a detailed preliminary study that shows how with just up to 2 DC bits in each layer in the pixel sensor and 1 DCbit in the strips detector it is possible to build a bank that will allow the system to be fully functional at the luminosities and pileup conditions expected for the LHC after Phase-I upgrades.

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