# Variable resolution Associative Memory optimization and simulation for the ATLAS FastTracker project

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11th International Conference on Large Scale Applications and Radiation Hardness of Semiconductor Detectors
In Florence, Italy 3-5 July

# Outline

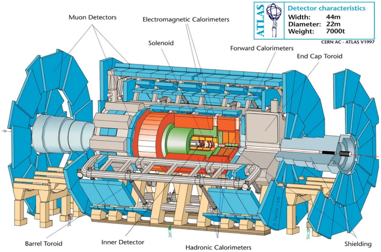
- The FastTracker (FTK)
  - FTK for the ATLAS trigger upgrade
  - FTK algorithm
- Associative Memory (AM)
- Variable Resolution patterns
- Simulation studies
  - Multiple DC-bits study
  - HW constraints per pile-up events
  - Configurations
- Conclusions

# FastTracker for the ATLAS trigger upgrade

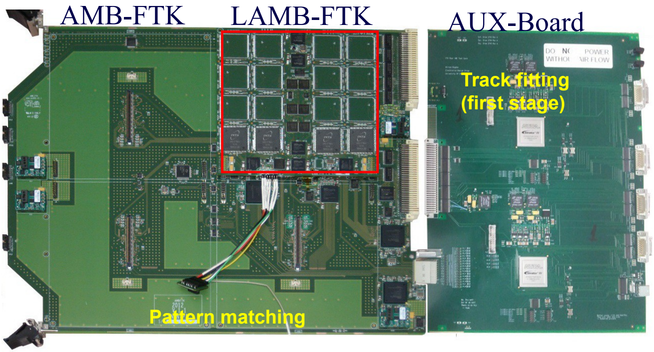
- FTK reconstructs charged particles trajectories in the silicon detectors (Pixel & SCT) at "1.5" trigger level.
- Extremely difficult task

  100 KHz processing rate

  ~70 overlapping events (pile-up) at highest luminosity.



# FTK processing unit



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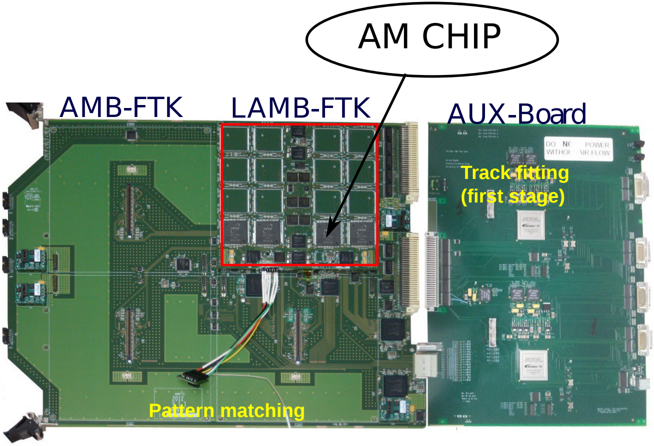
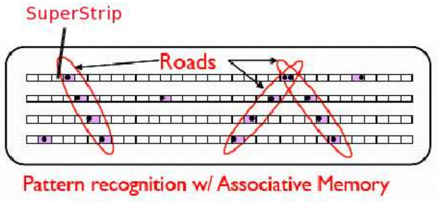


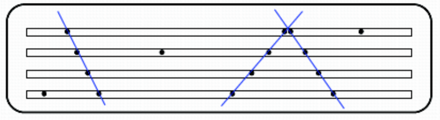
# FTK algorithm

Two sequential steps:

1. Pattern recognition, carried out by a dedicated device called Associative Memory (AM). Find coarse-resolution track candidates called "roads".

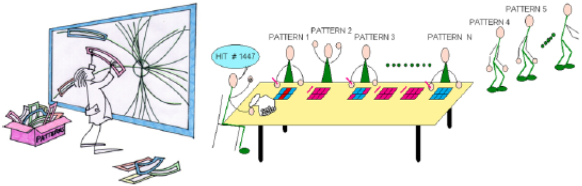



2. Track Fitter fits the full-resolution hits inside the road to determine the track parameters. Only the tracks passing the $\chi^2$ cut are kept.



# AM working principle

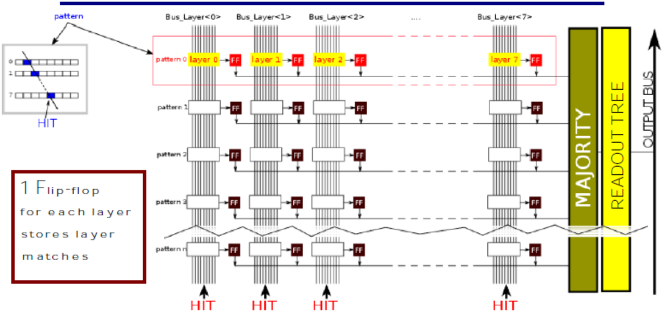
AM = BINGO GAME




- player=pattern
- numbers on the card=bin
- extracted number=hit
- winning players=pattern matching

- Each pattern has its private HW to compare itself with the event
- Bingo game goes on until completion of detector readout
- All the winning patterns go to the output

# AM working principle




All patterns compared in parallel with incoming data. Look for correlation of data received at different times (feature unique to AM chip)

- Fast pattern matching
- Flexible input

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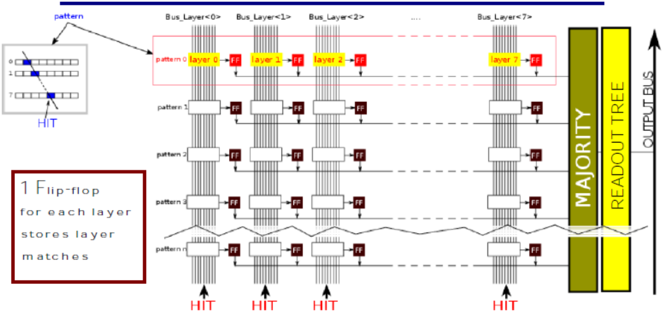


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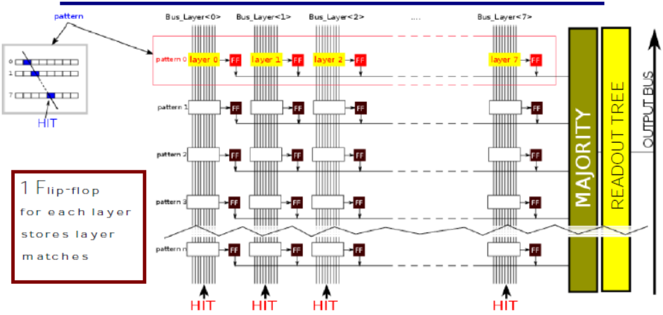


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- Flexible input

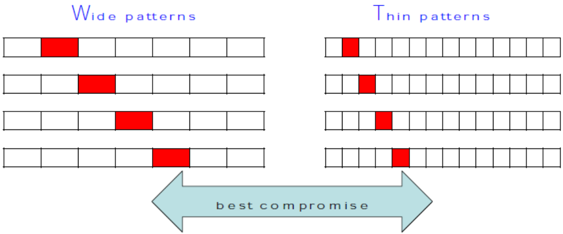
# Parameters to define the pattern-bank performance

## Pattern bank

Each track generates a hit pattern. The collection of all these patterns defines both the space of the tracks we are looking for and how they appear in the detector: this collection is the pattern bank

## Trade-off

Number of roads vs number of fits ⇒ critical parameter: road width




- Too wide ⇒ more fake roads ⇒ excessive work for the Track Fitter
- Too narrow ⇒ more AM patterns ⇒ too large cost

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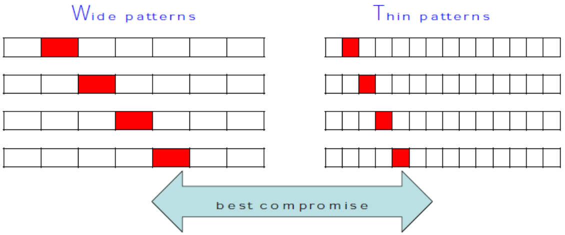


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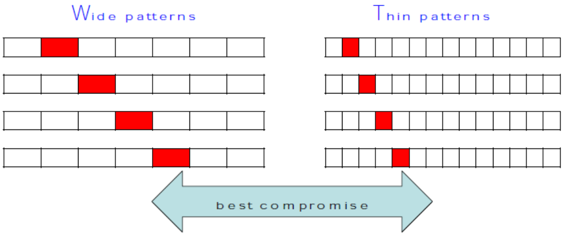


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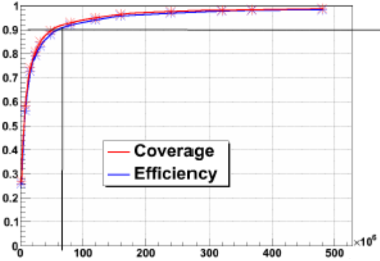
# Bank efficiency and # fakes at 69 pile-up events

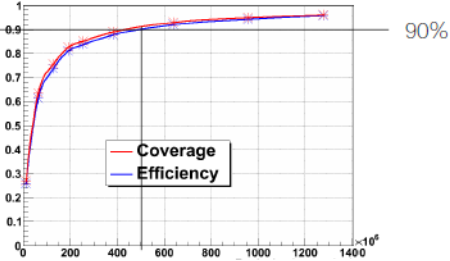
Low resolution
SS=24 pixels in r-ϕ
36 pixels in z
20 strips in SCT




65M Bank size (per region)

**# ROADS/EVENT=342000**

High resolution
SS=12 pixels in r-ϕ
36 pixels in z
10 strips in SCT

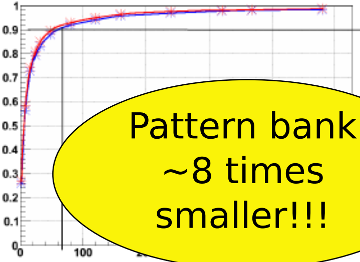



500M Bank size (per region)

**# ROADS/EVENT=40000**

# Bank efficiency and # fakes at 69 pile-up events

Low resolution
SS=24 pixels in r-$\phi$
36 pixels in z
20 strips in SCT




Pattern bank ~8 times smaller!!!

65M Bank size (per region)

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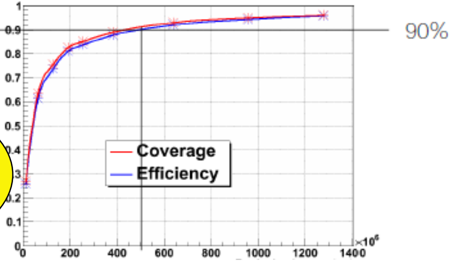
High resolution
SS=12 pixels in r-$\phi$
36 pixels in z
10 strips in SCT




500M Bank size (per region)

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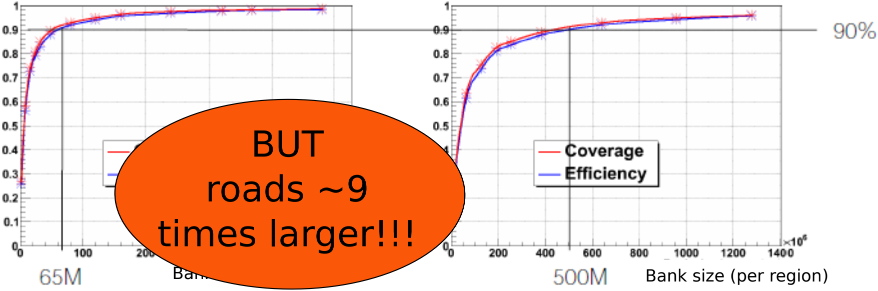


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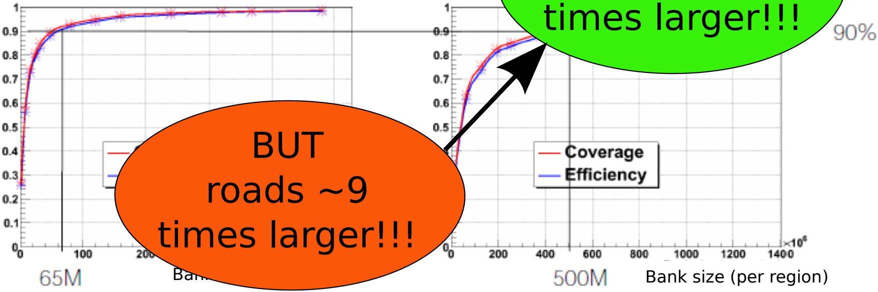


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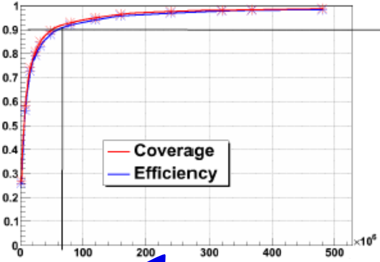
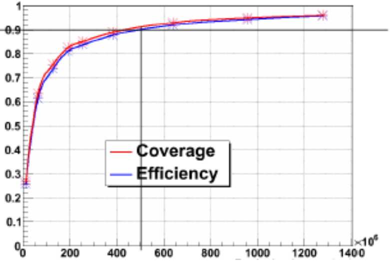



90%

65M Bank size (per region)

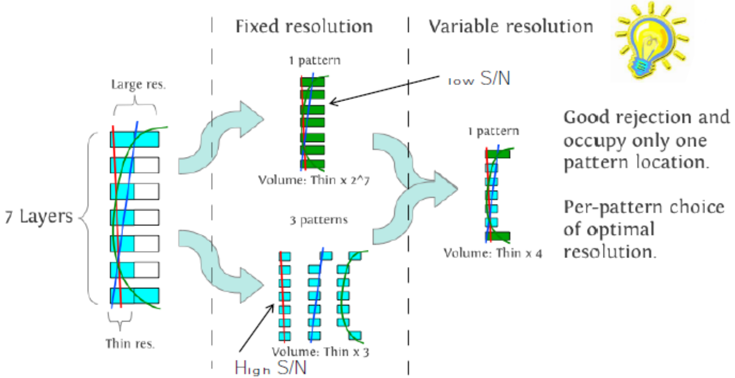
500M Bank size (per region)

Want this

# ROADS/EVENT=342000

# ROADS/EVENT=40000

# Variable resolution patterns




- Don't care (DC) on the least significant bit of hit position

⇒ Number of patterns within the HW limits

⇒ High rejection of fake roads

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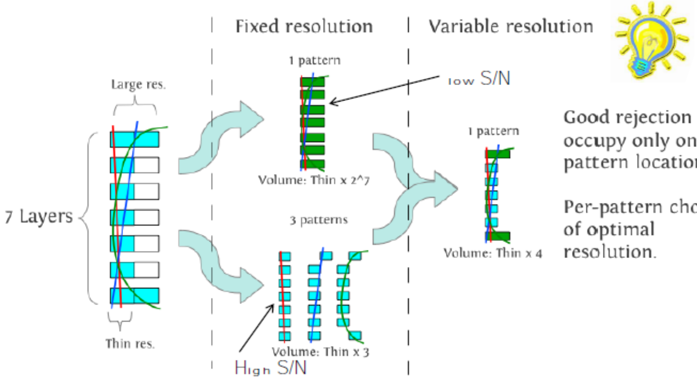


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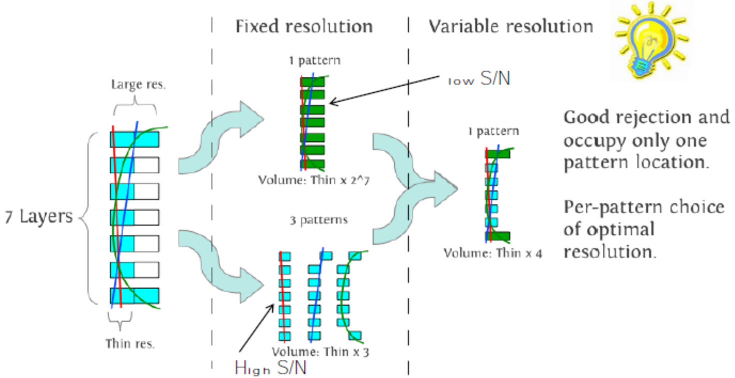


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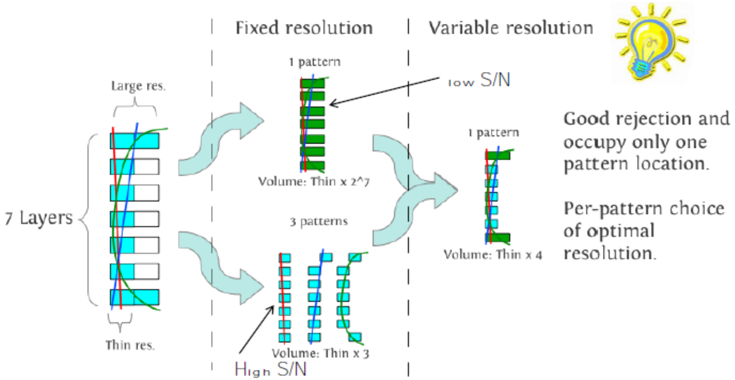


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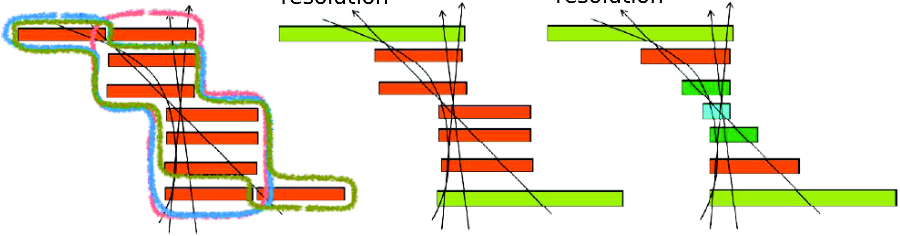
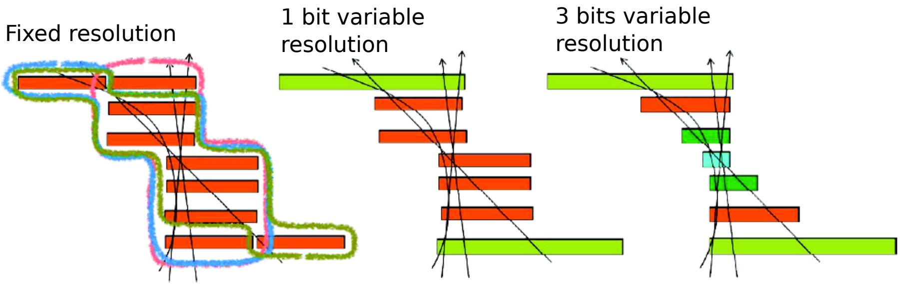
# Many bits variable resolution

Fixed resolution | 1 bit variable resolution | 3 bits variable resolution



- No variable resolution ⇒ 3 patterns needed to accept the tracks
- Simple application ⇒ 1 pattern needed to accept the tracks
- Advanced application ⇒ 1 pattern needed but less volume

# Many bits variable resolution




- fixed resolution
- simple application
- advanced application

Any coincidence based trigger can exploit this technique!

# Multiple DC bits study

## Goals

- Keeping high efficiency with a limited number of patterns
- Limiting Track Fitter workload

⇒ Optimizing use of variable resolution patterns

## Main parameters

- Pattern bank size
- Number of roads
- Roads size
- Number of fits

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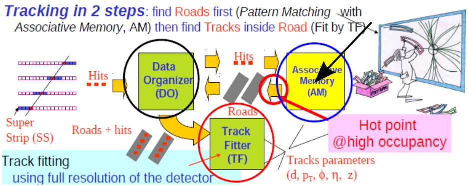

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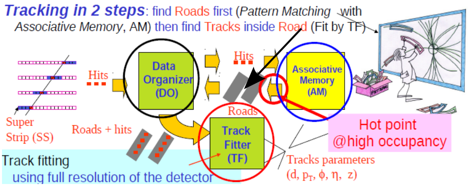

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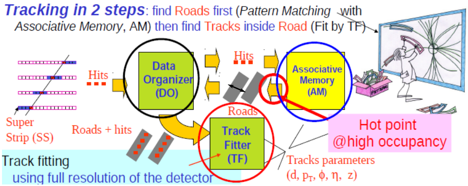

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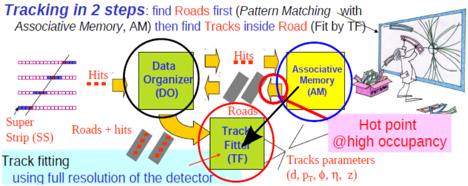

# HW constraints for pile-up events

Maximum limits for each board:

- $8 \times 10^6$ patterns
- $8 \times 10^3$ roads
- $40 \times 10^3$ fits

Simulation results at 25 ns interbunch for 2015 and 2019:

1. 46 pile-up events (2015): 16 boards working on 32 towers
   $\Rightarrow$ constraints for each tower:
   - $\#AMpatterns < 4 \times 10^6$
   - $\#Roads < 4 \times 10^3$
   - $\#Fits < 20 \times 10^3$
2. 69 pile-up events (2019): 128 boards working on 64 towers
   $\Rightarrow$ constraints for each tower:
   - $\#AMpatterns < 16 \times 10^6$
   - $\#Roads < 16 \times 10^3$
   - $\#Fits < 80 \times 10^3$

# Configurations

- High resolution road: 15x36x16
  - $\rightarrow$ 15x36 $=$ number of pixels clustered in the same Super Strip ($\phi \times z$)
  - $\rightarrow$ 16 $=$ number of strips clustered in the same Super Strip ($\phi$)
- Dataset with 69 pile-up events
- Constraints:
  - $\#AM < 16M \times 10^6$
  - $Roads < 16 \times 10^3$
  - $Fits < 80 \times 10^3$
- AM bank configurations:

1. $(30x36)_{pix}x32_{sct}$
2. $(30x72)_{pix}x32_{sct}$
3. $(30x144)_{pix}x32_{sct}$
4. $(30x72)_{pix}x64_{sct}$

$\Rightarrow$ Grouping larger number of the detector channels makes the SS granularity decrease

# Endcap - 69 pile-up events ($\sim$ 2019)

| DC bit | #AM $\cdot 10^6$ | Efficiency(%) R=64 | Roads/evt $\cdot 10^3$ | Fits/evt $\cdot 10^3$ | Tracks/evt |
|---|---|---|---|---|---|
| $(30x72)_{pix}x32_{sct}$ | 18 | 91.2 | 7.1 | 56 | 106 |
| $(30x72)_{pix}x32_{sct}$ | 16.8 | 91.2 | 6.9 | 55 | ... |
| $(30x72)_{pix}x32_{sct}$ | 15 | 91.0 | 6.2 | 50 | ... |
| $(30x144)_{pix}x32_{sct}$ | 8 | 92.0 | 5 | 90 | ... |
| $(30x72)_{pix}x64_{sct}$ | 8 | 93.0 | 9 | 154 | ... |

Table: Results in endcap towers. #AM patterns, #Roads, #Fits and #Tracks are reported for one tower.

- The #Roads provides a measure of the fake roads
- The efficiency is evaluated on a single muon dataset (no pile-up)

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Table: Results in endcap towers. #AM patterns, #Roads, #Fits and #Tracks are reported for one tower.

- For a given DC configuration:
  - Reducing the number of patterns reduces the number of roads and fits
  - Efficiency minimally reduced
  - Number of fake roads proportional to the bank size

# Endcap - 69 pile-up events ($\sim$ 2019)

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Table: Results in endcap towers. #AM patterns, #Roads, #Fits and #Tracks are reported for one tower.

- The power of the variable resolution pattern
  - Increased efficiency and reduced roads number
  - Half size bank!

# Barrel - 69 pile-up events ($\sim$ 2019)

| DC bit | #AM $\cdot 10^6$ | Efficiency(%) R=64 | Roads/evt $\cdot 10^3$ | Fits/evt $\cdot 10^3$ | Tracks/evt |
|---|---|---|---|---|---|
| $(30x72)_{pix}x32_{sct}$ | 21 | 94.8 | 3.9 | 33 | 42 |
| $(30x72)_{pix}x32_{sct}$ | 18 | 94.1 | 3.4 | 28 | 38 |
| $(30x72)_{pix}x32_{sct}$ | 16.8 | 93.3 | 3.2 | 26 | 36 |
| $(30x144)_{pix}x32_{sct}$ | 8 | 95.0 | 4 | 60 | ... |
| $(30x72)_{pix}x64_{sct}$ | 8 | 96.0 | 6 | 98 | ... |

Table: Results in barrel towers. #AM patterns, #Roads, #Fits and #Tracks are reported for one tower.

# Work in progress - 46 pile-up events ($\sim$ 2015)

- Exploring better initial road resolutions and larger number of DC bits
- High resolution road: 11x18x12
  - $\rightarrow$ 11x18 = number of pixels
  - $\rightarrow$ 12 = number of strips
- We are trying some DC-bits bank configurations:
  - $(22x72)_{pix}x24_{sct}$
  - $(44x72)_{pix}x48_{sct}$
  - $(44x144)_{pix}x48_{sct}$
- We will have the efficiency, roads, and tracks numbers soon

# Conclusions

- We have simulated complex configurations of the powerful variable resolution pattern-matching
  - The patterns are able to change in shape and matching volume
  - The "don't care" bit improves the precision only where needed
  - High rejection of fake roads $\Rightarrow$ the number of roads out of the AM chip is reduced greatly by using the variable resolution patterns
  - High compression factor in case of similar patterns $\Rightarrow$ the number of patterns in the AM chip is significantly reduced

Thanks to the variable resolution implementation we are able to set the architecture parameters so that all HW constraints are satisfied.