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SI LAB
Silizium Labor Bonn

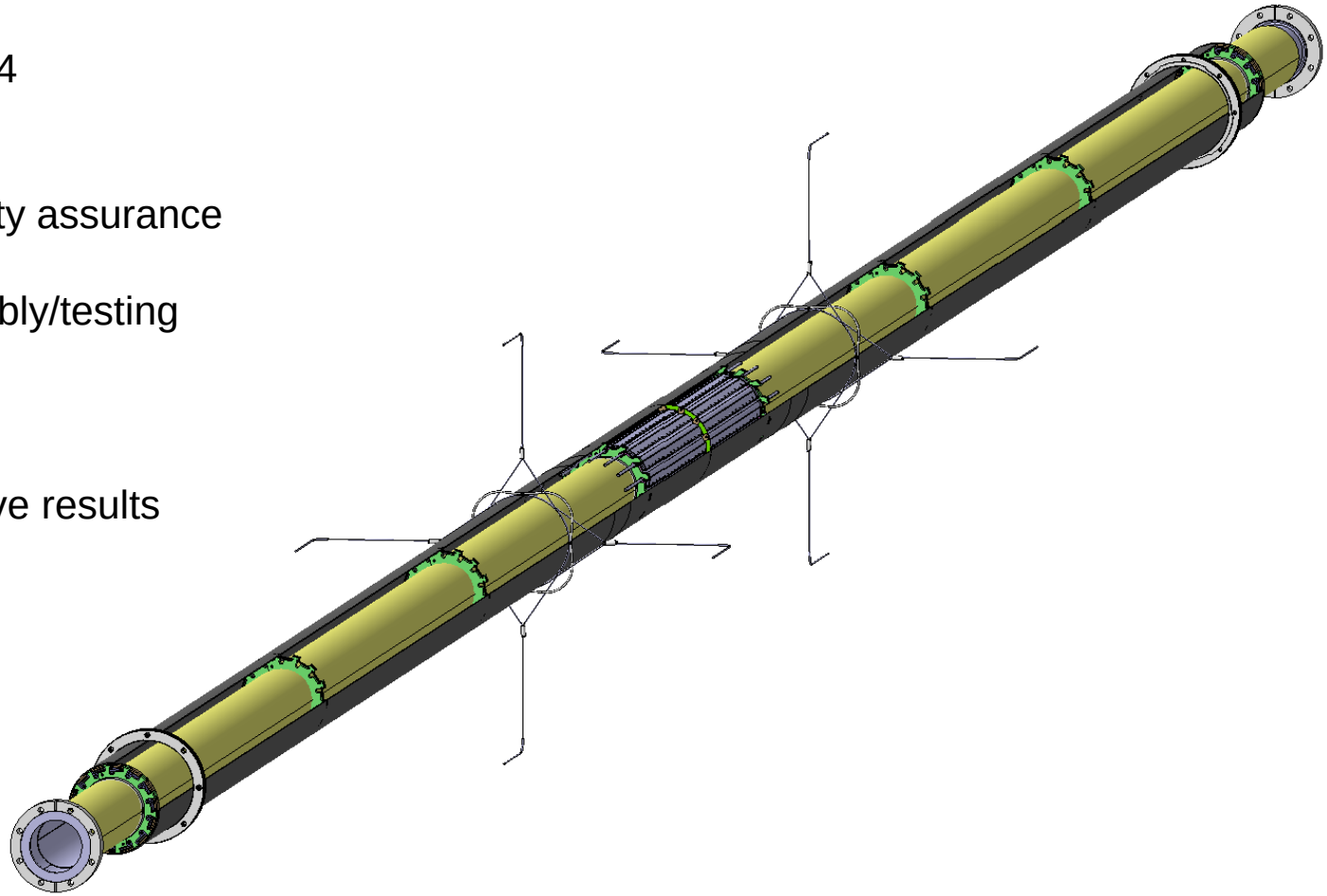
Overview of the ATLAS Insertable B-Layer (IBL) Project

David-Leon Pohl on behalf of the ATLAS collaboration

RD13 – 11th International Conference on Large Scale Applications and Radiation Hardness of Semiconductor Detectors

Overview

- What is IBL?:
  - Motivation
  - Sensor R&D
  - Front end FE-I4
- The production/quality assurance
  - Wafer testing
  - Module assembly/testing
  - Stave loading
- Initial production stave results

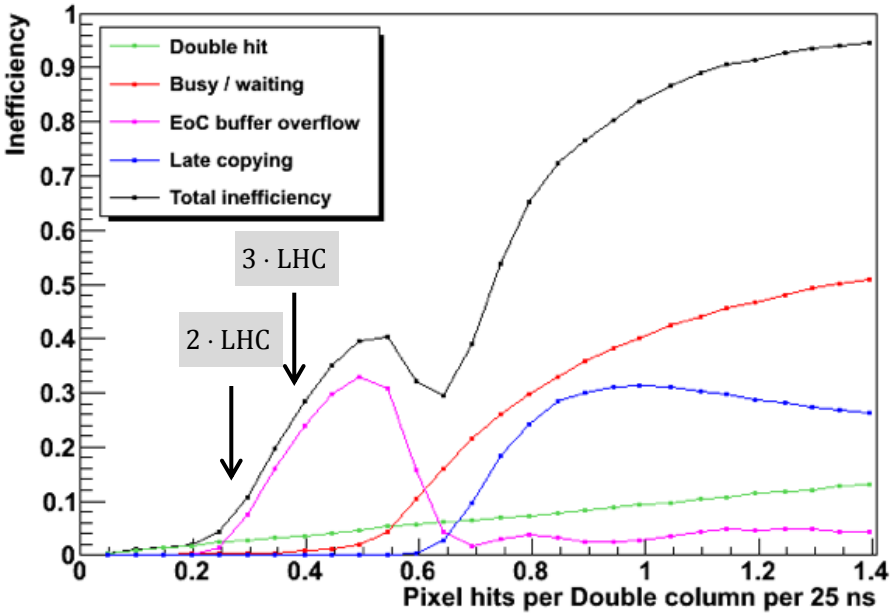


Motivation

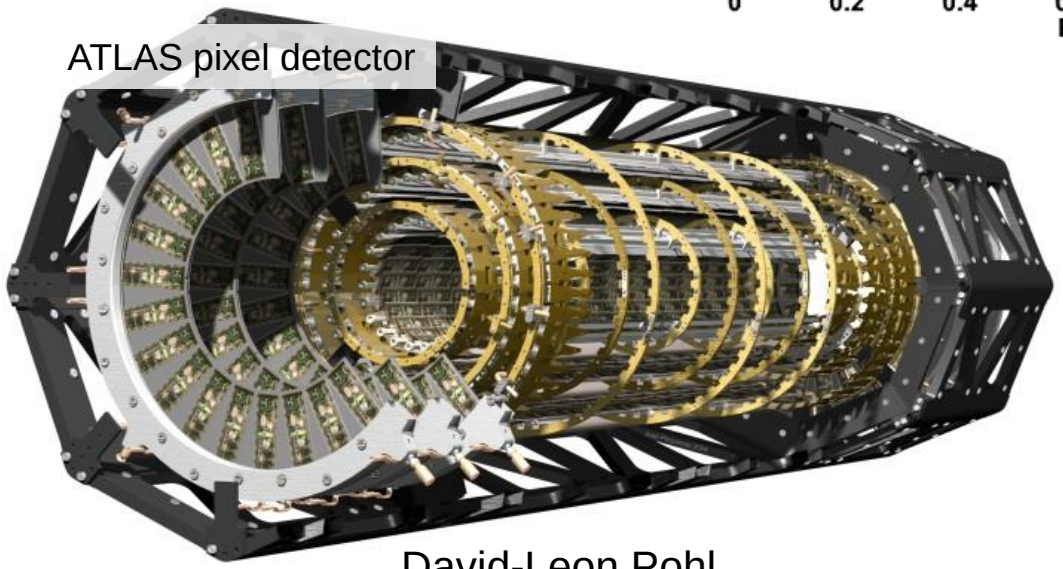
- Actual ATLAS pixel detector:
  - Essential for primary vertex/tracking/b-tagging performance
  - 3 layers of hybrid silicon pixels
  - Showed great performance over the last three years (see talk by Kerstin Lantzsch)

- Upgrades of the Large Hadron Collider (LHC):
  - $\sqrt{s}$: 8 TeV → 14 TeV
  - increase of the nominal LHC luminosity of $\mathrm{L} = 10^{34}\mathrm{cm}^{-2}\mathrm{s}^{-1}$ by a factor of 2-3
  - ~7% inefficiency at $\mathrm{L} = 2{\cdot}10^{34}\mathrm{cm}^{-2}\mathrm{s}^{-1}$ for the B-layer

Simulated inefficiency with FE-I3 B-layer

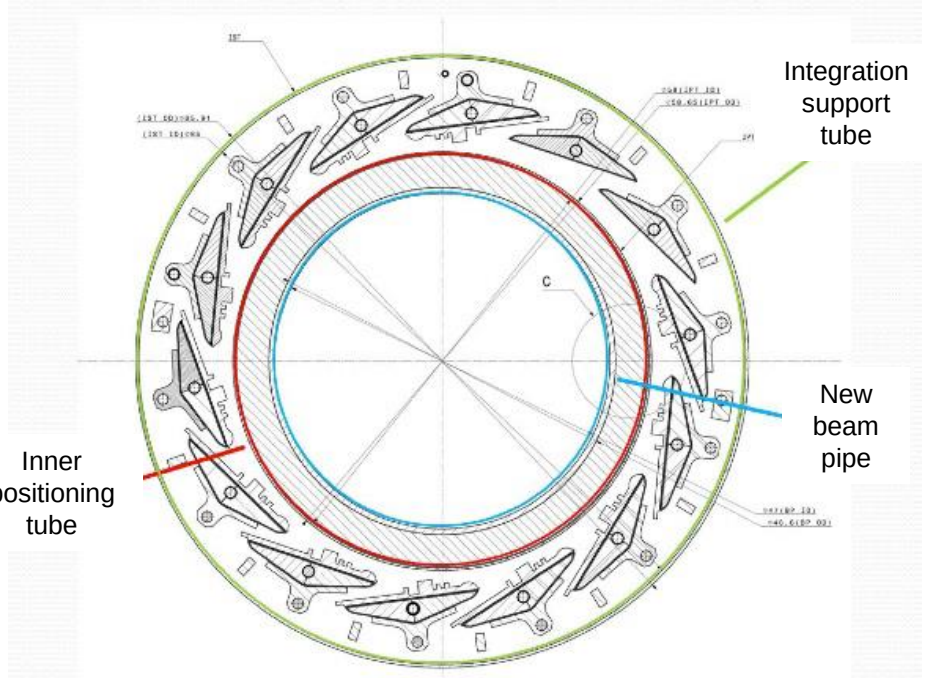


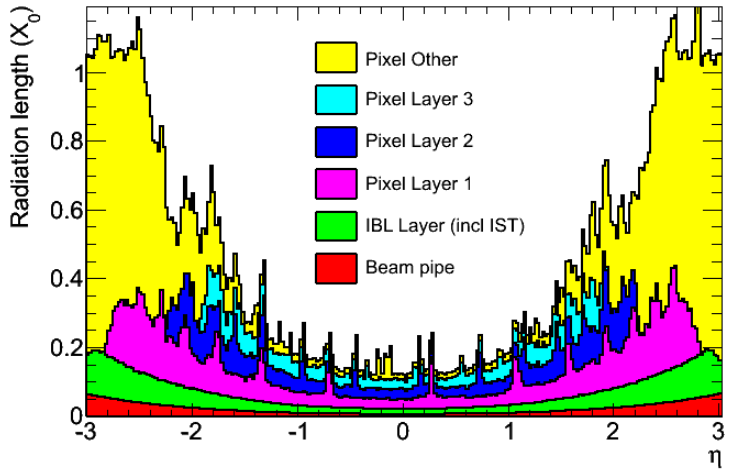
ATLAS pixel detector



Insertable B-Layer: IBL

- A new 4th layer for the ATLAS pixel detector at r = 3.2 cm
- Recover eventual failure of the actual B-layer
- New beam pipe with smaller radius (r = 23.5 mm) gives space for new layer
- 14 staves with tilt angle of Φ = 14° and no overlap in z
- Total radiation length < 1.9% X/X_0:
  - Staves with carbon foam composite material
  - CO_2 cooling
- Higher track density due to smaller radius (50%) and higher luminosity:
  - Radiation hardness: $5 \cdot 10^{15} n_{eq}$ / cm^2 NIEL, 250 MRad total ionizing dose
  - New sensor technologies investigated (3D-silicon, slim edge)
  - New pixel readout chip needed (FE-I4)





Sensors of the IBL

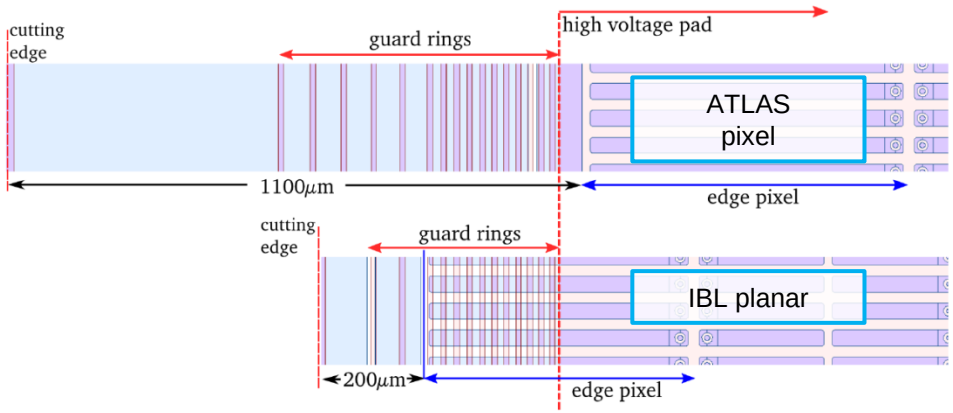
Main Requirements:

- Operational up to $5 \cdot 10^{15}\ n_{eq}/cm^2$ NIEL
- Slim edges

two sensor types chosen

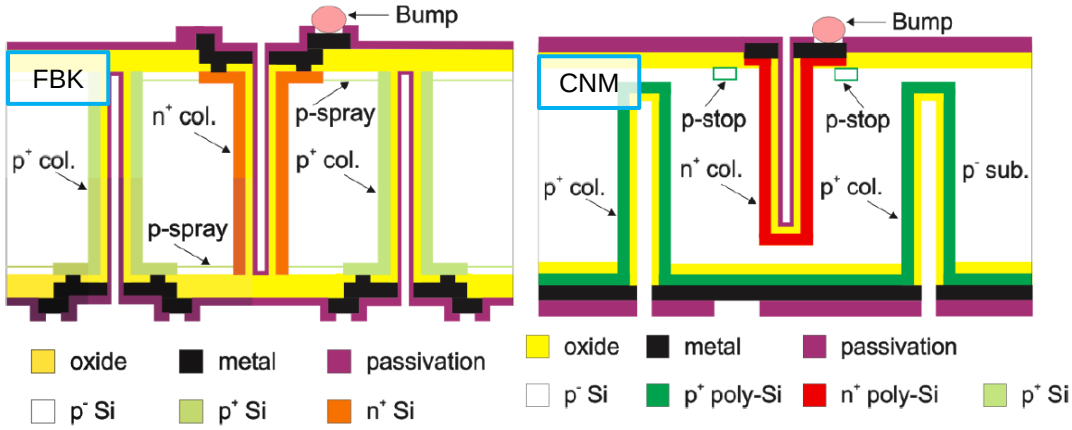
Planar n-in n sensor

- Electrode on top / bottom of the bulk
- Vendor: CiS
- Proven technology with high yield (90% accepted for IBL)
- Depletion voltage 35 V
- 1000 V at $5 \cdot 10^{15} n_{eq}$ / cm^2
- 200 µm thickness
- 75% IBL



3D silicon sensor

- Columns edged into the bulk
- Double sided, 2 E electrode configuration
- 2 Vendors: FBK/CNM
- Yield: 60% accepted for IBL
- Depletion voltage 15 V
- 180 V at $5 \cdot 10^{15} n_{eq}$ / cm^2
- 230 µm thickness
- 25% IBL

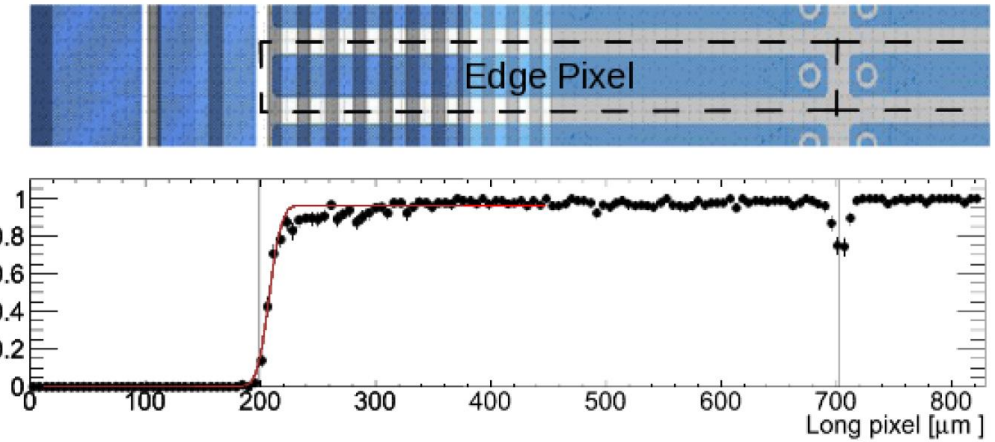


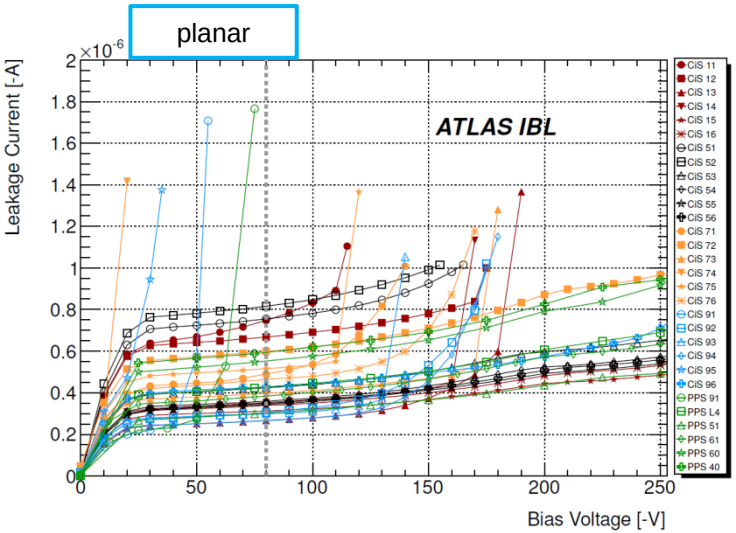
Sensor characteristics (JINST 7 (2012) P11010)

edge efficiencies (test beam, irradiated)

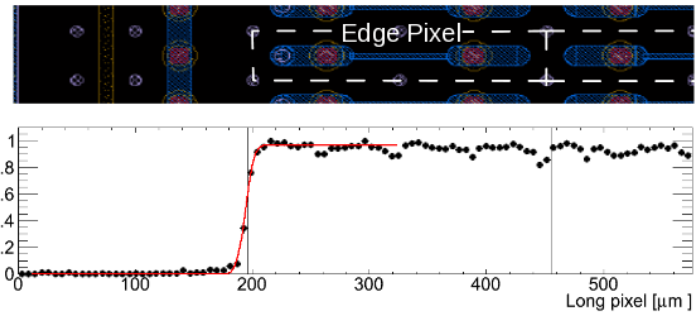
IV curves

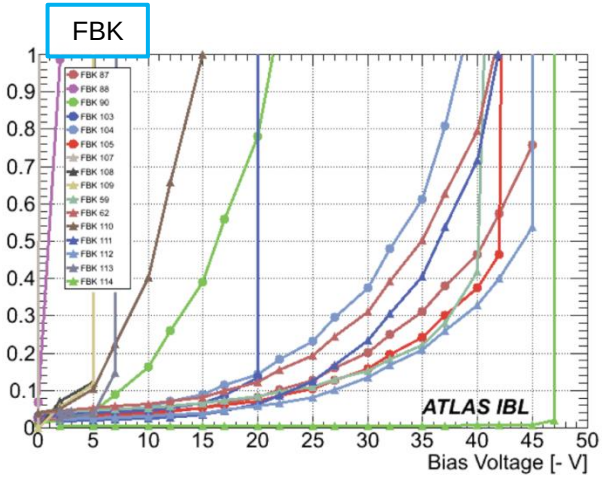
planar

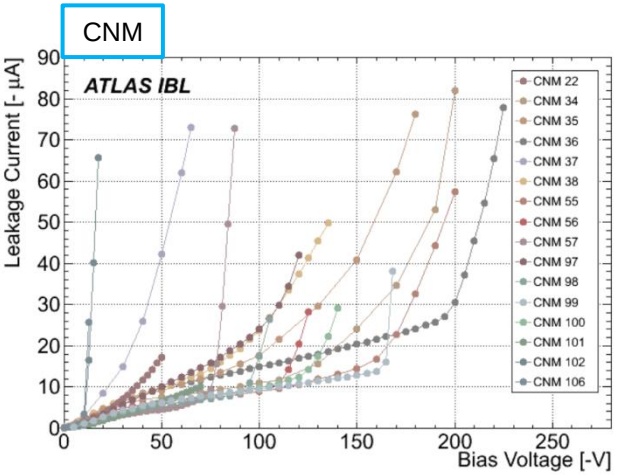




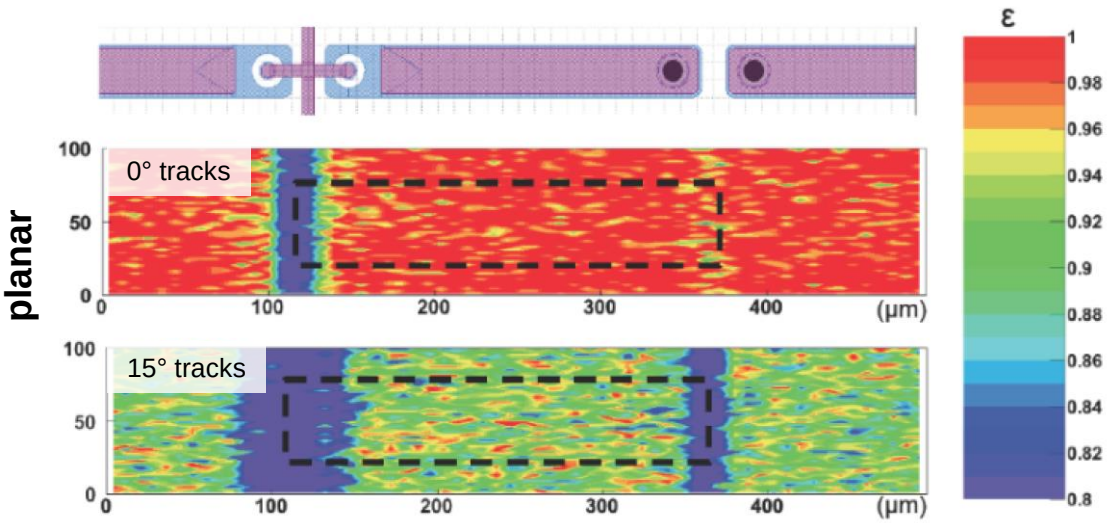
3d



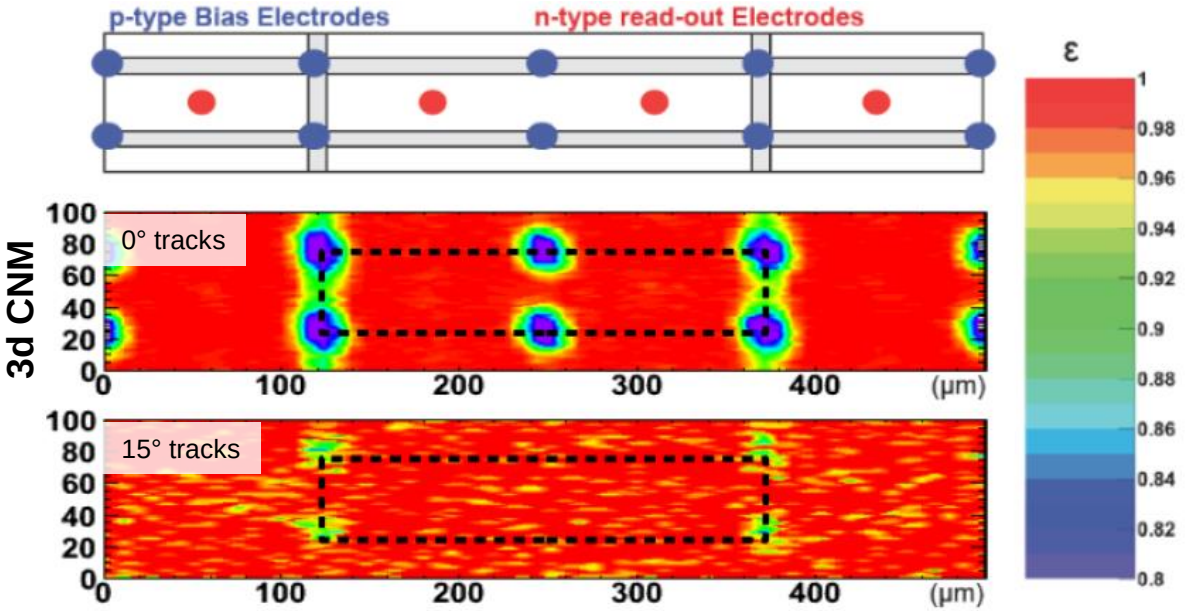




Sensor in-pixel efficiency (JINST 7 (2012) P11010)



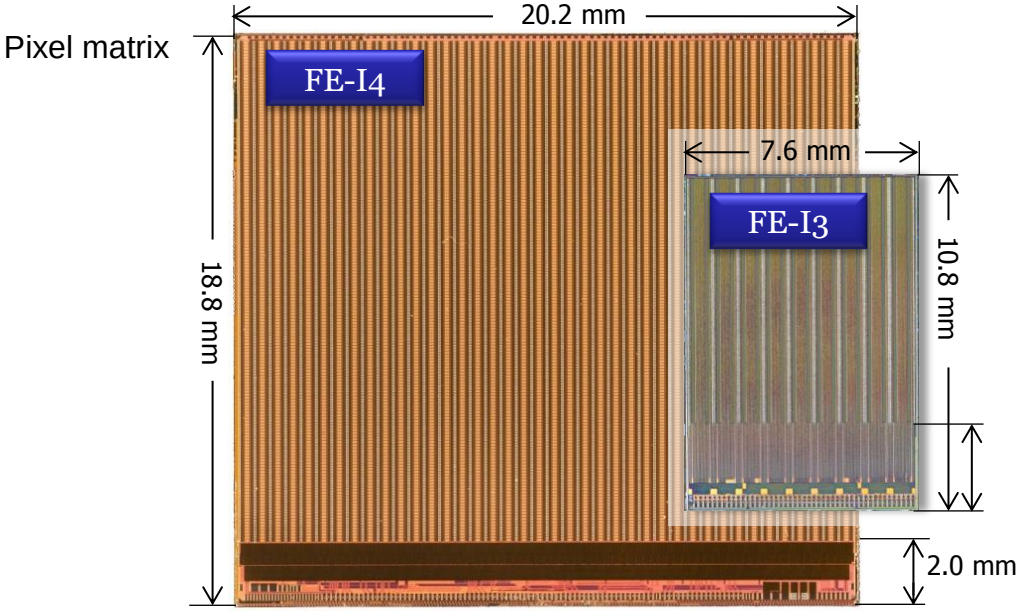
- Irradiated to $6 \cdot 10^{15}$ n_{eq} / cm^2
- Overall efficiency 96.9% (86.4%) at 0°(15 °)

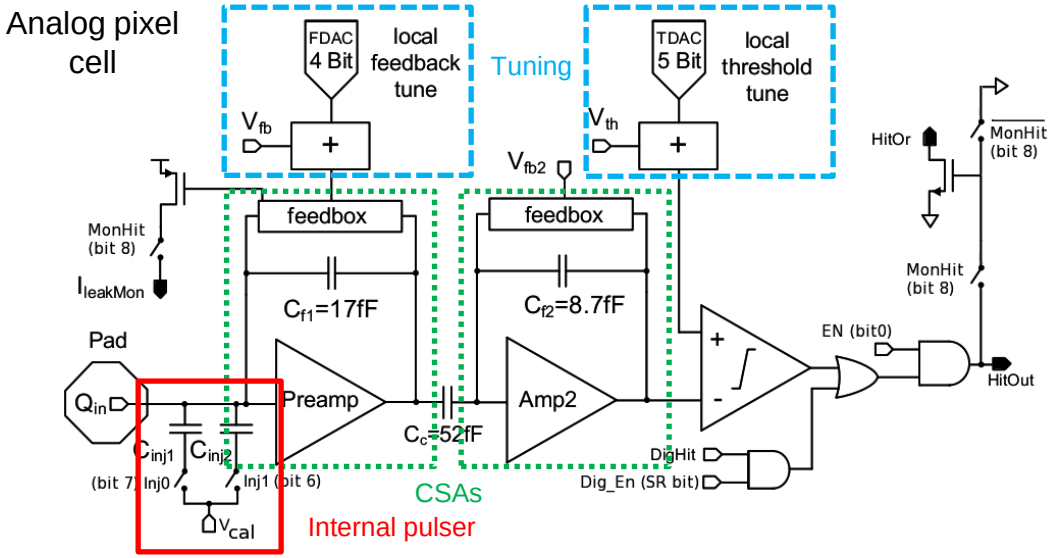


- Irradiated to $5 \cdot 10^{15}$ n_{eq} / cm^2
- Inefficiency at columns (not sensitive areas)
- Overall efficiency 97.5 % (99 %) at 0° (15 °)
- 15° corresponds to the IBL design

FE-I4 pixel read out chip

- ~2 x 2 cm² → ~6 times size of FE-I3
- 26.880 pixels with 50 µm x 250 µm size
- Hits buffering in four pixel regions
- Built in low drop out regulators (LDO) and bandgap voltage references
- > 250 MRad TID (750 MRad working!)
- Charge determination and time stamping with time over threshold technique (4-bit ToT, 40 MHz input clock)
- Tuned threshold dispersion ~ 40 e

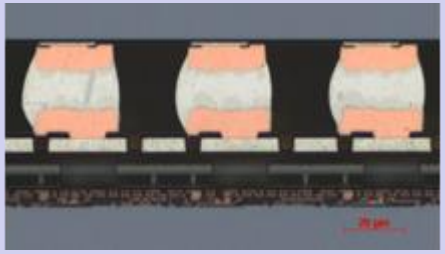




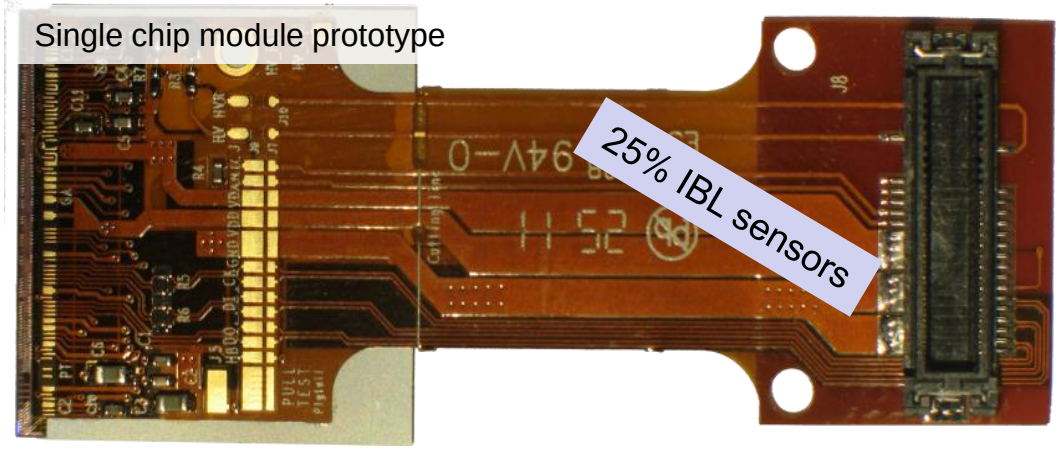
Modules of the IBL

IZM (Berlin):

- bump-bonding of FE and sensor
- thinning of the FE-I4 wafer to 150 µm with glass handling wafer and dicing



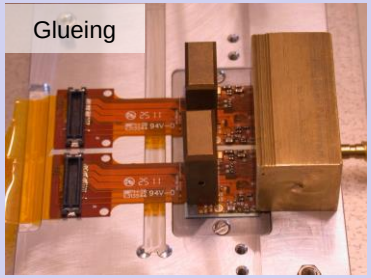
Single chip module prototype



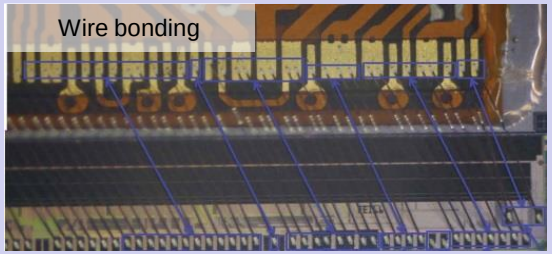
At Bonn/Genova:

- Module assembly and QA

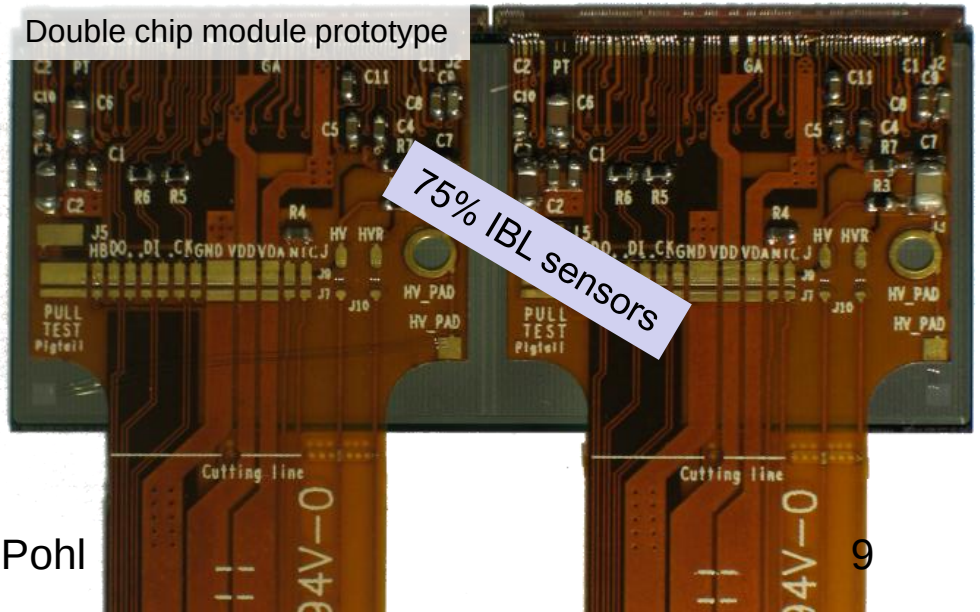
Glueing



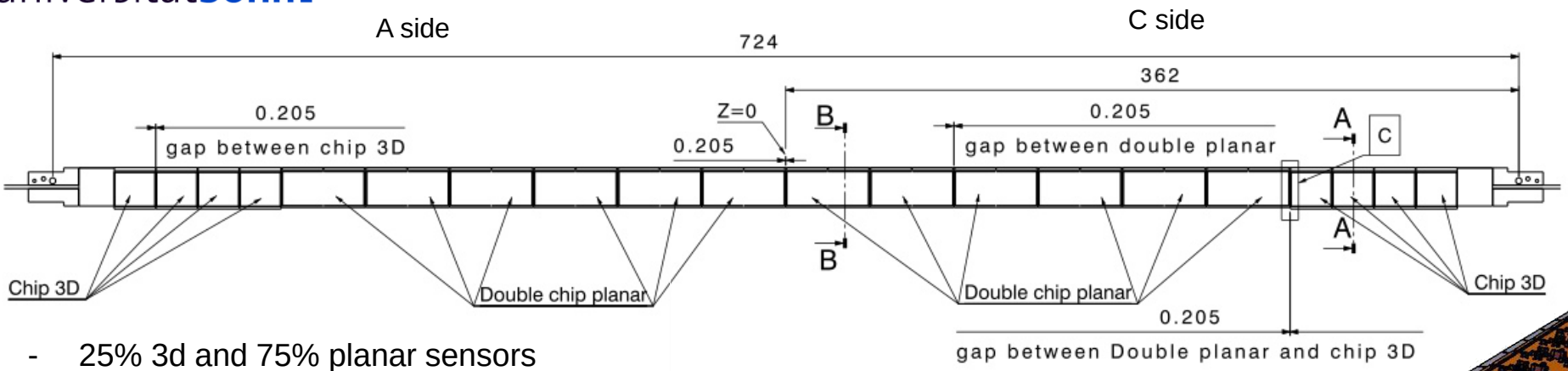
Wire bonding



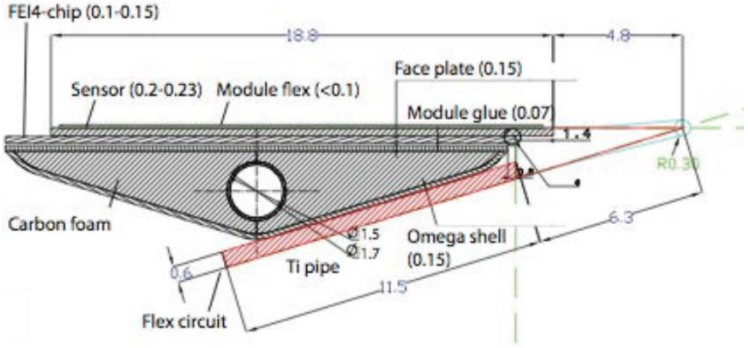
Double chip module prototype

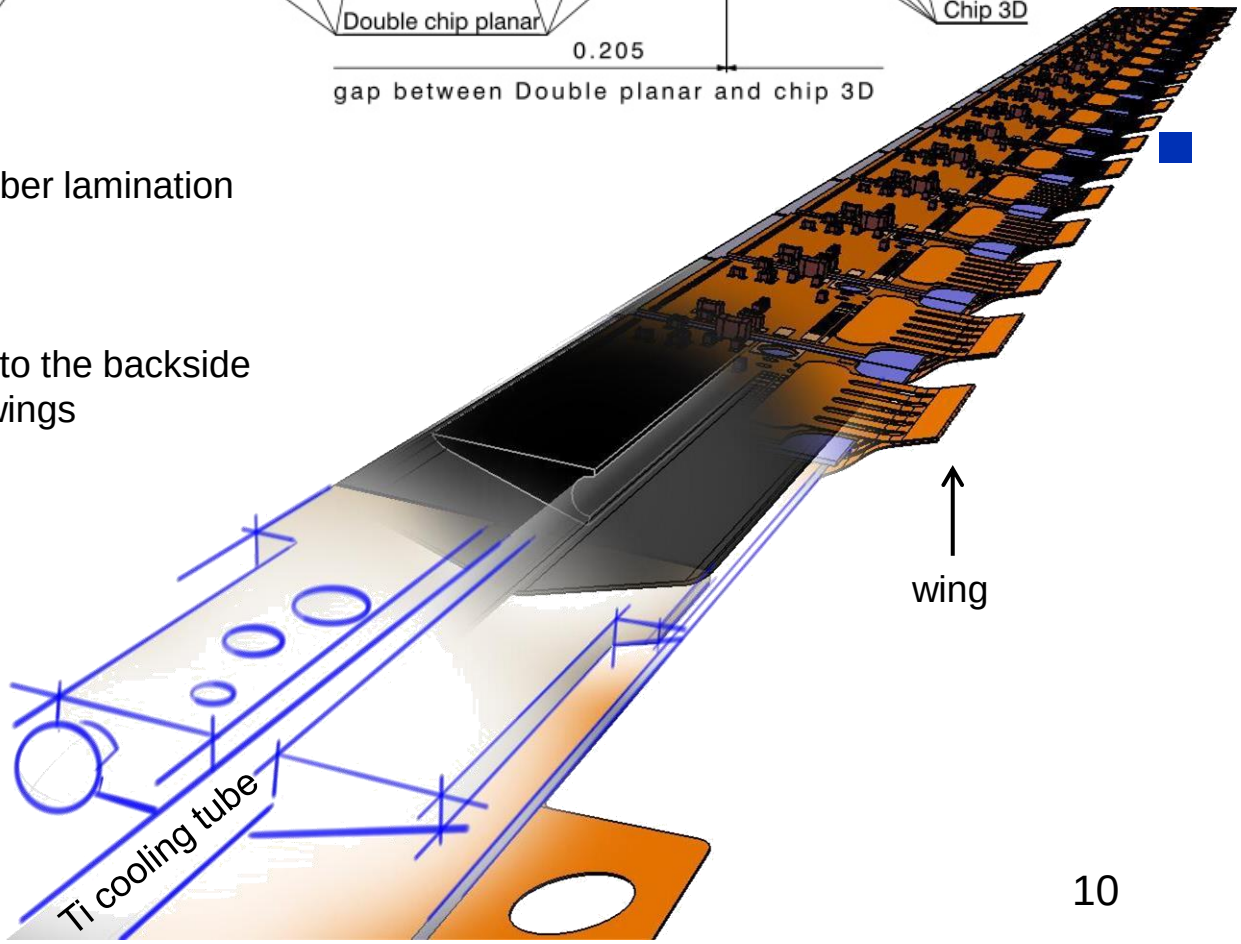


IBL stave



- 25% 3d and 75% planar sensors
- Bare stave:
  - Carbon foam material with carbon fiber lamination
  - Evaporative CO_2 based cooling
  - 1.5 mm Titanium boiling channel
- Stave flex:
  - carries HV (Cu), LV (Al) lines glued to the backside
  - connection to module flex through wings
  - 4 SC / 2 DC form power groups

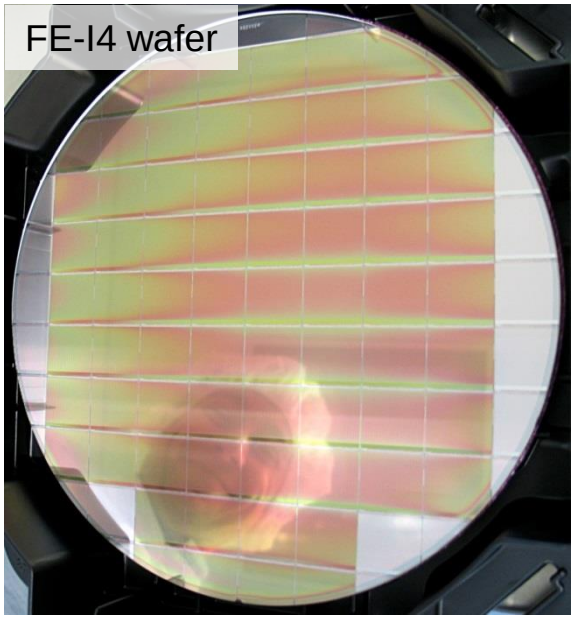




FE-I4B wafer testing

- IBL requires: 14 · 32 · 2 · 125% = 1120 green ICs ≡ 38 wafers

staves · ICs/stave · safety margin · 100% planar 25% 3D · pessimistic yield estimation of 50% green ICs (=30) per wafer



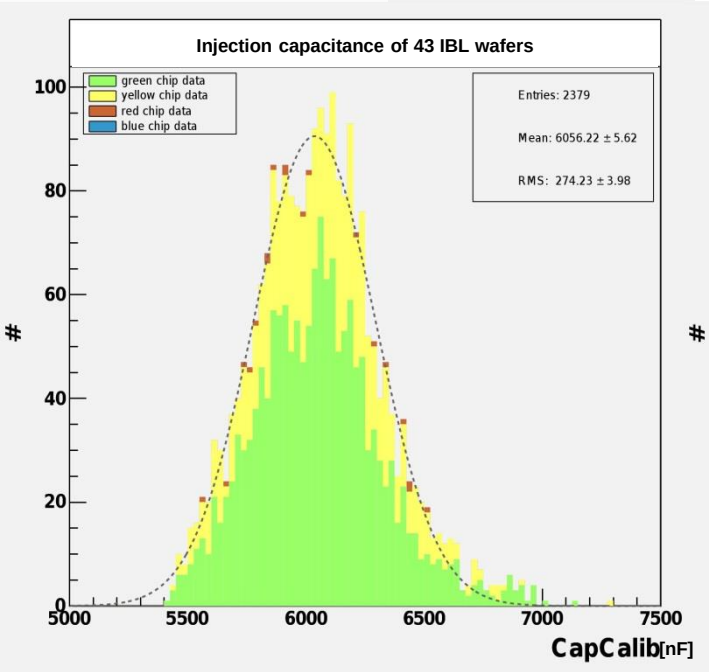
- 60 chips on 8 inch wafer
- All needed wafers were tested in Bonn and are already sent to IZM
- Contacting > 100 pads per FE with needle card
- 2 days measurement time per wafer
- cuts on > 18000 values per wafer with automated software ‚WaferAnalysis'

Chip calibrations (only possible at wafer level)	Global IC tests	Pixel array tests

• Reference current tuning
• Internal pulser calibration:
  • Pulser DAC transfer function
  • Injection capacitance measurement
• 15-bit serial number burning for module identification
	• Current consumption (in different chip states)
	• Global register test
	• Tunable/fixed regulator reference voltages
	• Service records
	• Scan chain tests
	• Injection delay scan of internal pulser
		• Pixel register test
		• Digital test
		• Analog test with different injection caps
		• Threshold scan
		• etc.

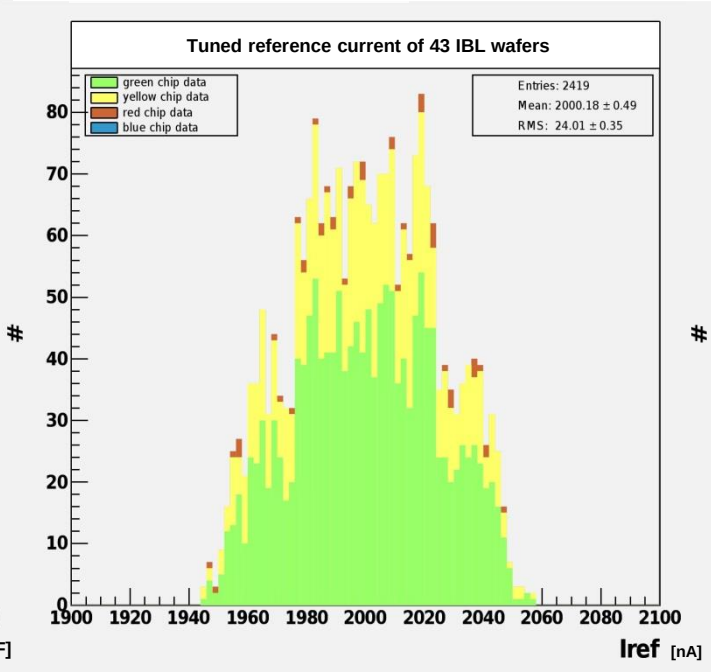
FE-I4B wafer testing results

Injection capacitance



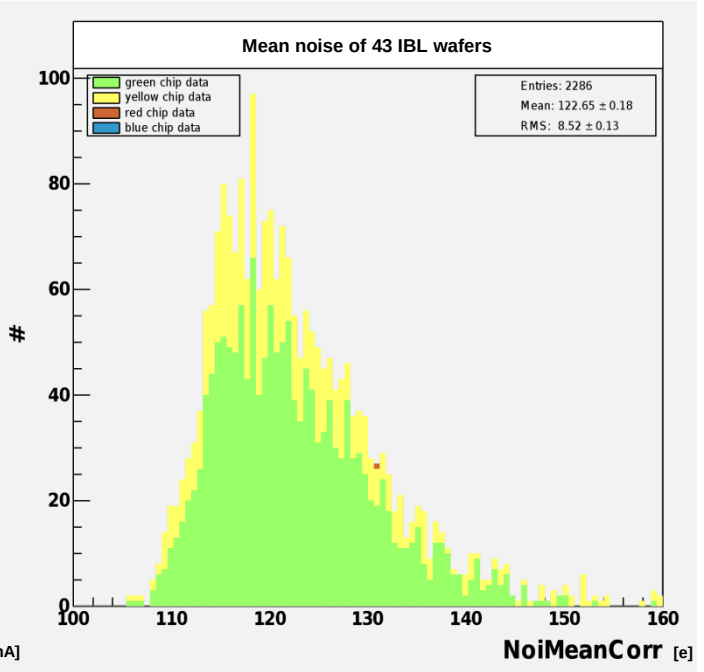
- Injection capacitance: (6.1 ± 0.3) fF
- Simulated value: 5.7 fF
- Value to be used at IBL operation

Reference current



- Used for biasing the analog part
- Design value of 2 µA can be reached with small error (< 25 nA)

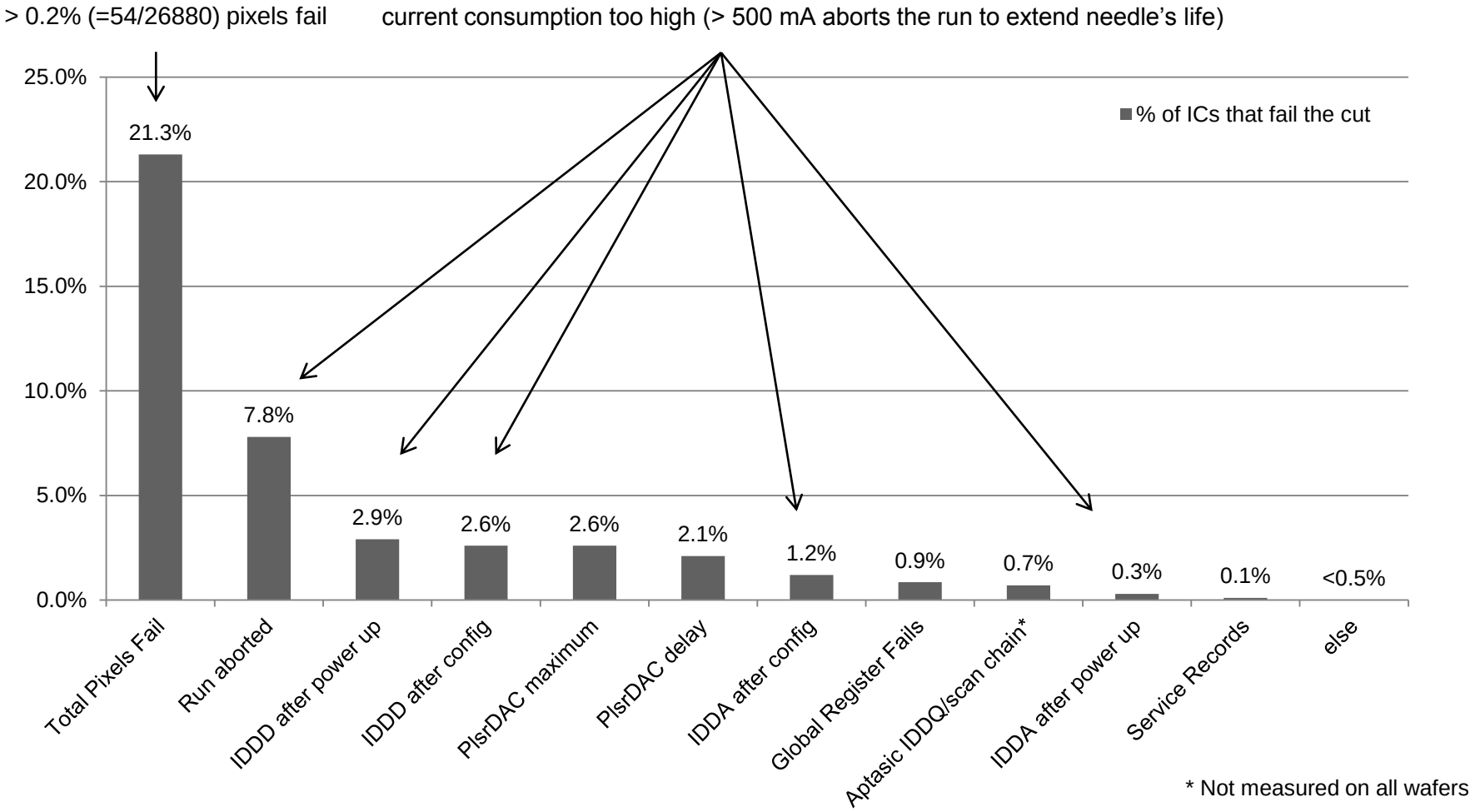
Mean noise



- Expected noise (~ 120 e ENC) of bare chip measured

FE-I4B wafer testing: yield and main failures

- Final yield: 61.0% green (for IBL), 30.5% yellow, 8.5% red
- Main failures:



Module qualification procedure

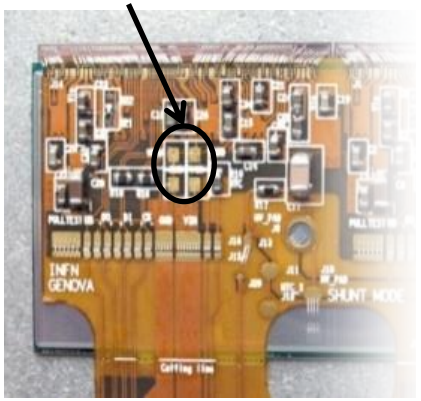
1. Assembly tests at 15 °C:
   - Quickly identify non working modules
   - Set reference current via pulling wire bonds
   - Regulator tuning
   - Identify merged / disconnected bumps:
     - Cross talk test
     - Threshold scan with/without biased sensor

2. Stress test (Burn in):
   - 10 x thermal cycling -40..40° C

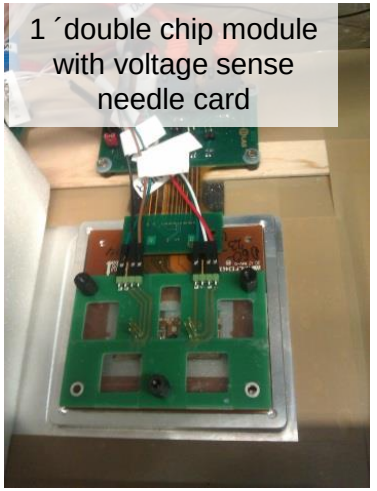
3. Qualification tests at -20 °C:
   - Pixel register test
   - IV curve
   - Analog / digital functionality
   - Low threshold configuration (1500 e)
   - Source scan

4. Module ranking based on # broken channels:
   - < 270 pixels / chip → accepted (<1% of all channels)
   - > 270 pixels / chip → disqualified for IBL

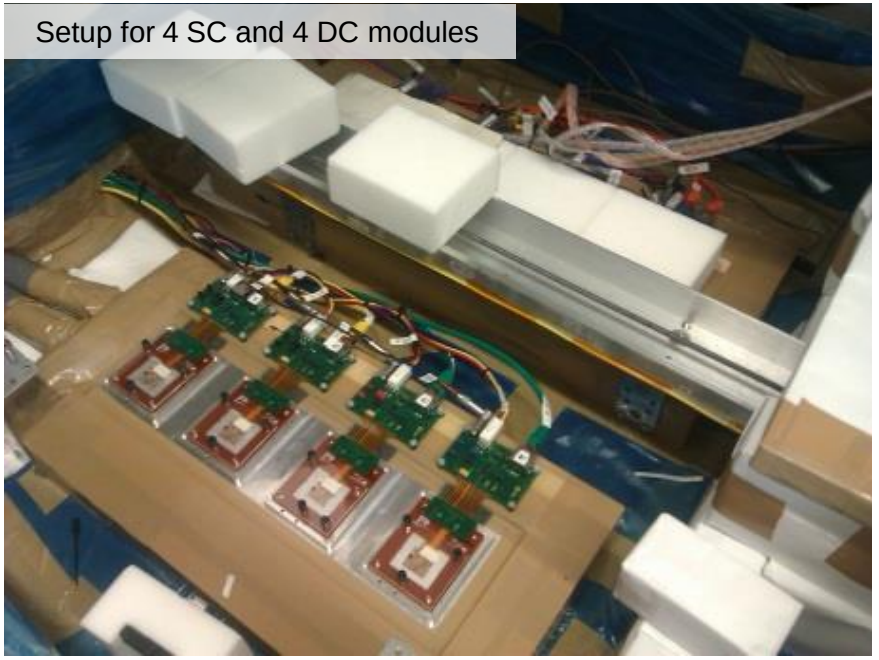
Voltage regulator sense pads



1 ´double chip module with voltage sense needle card



Setup for 4 SC and 4 DC modules

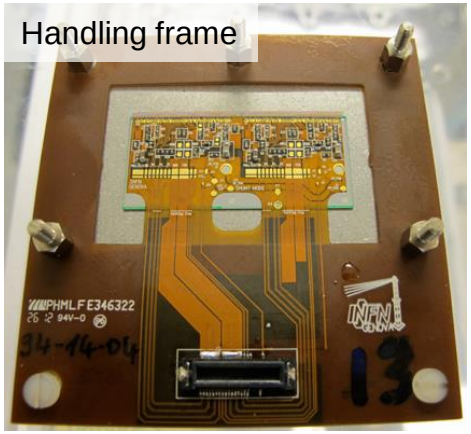


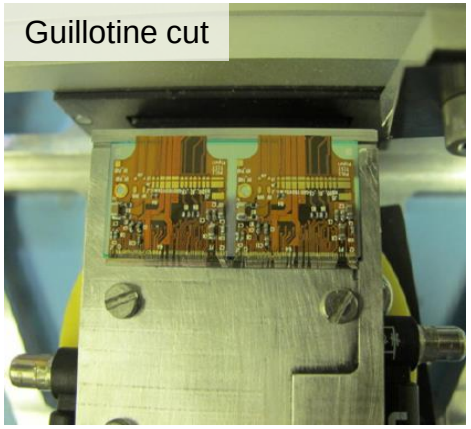
Module yield and status

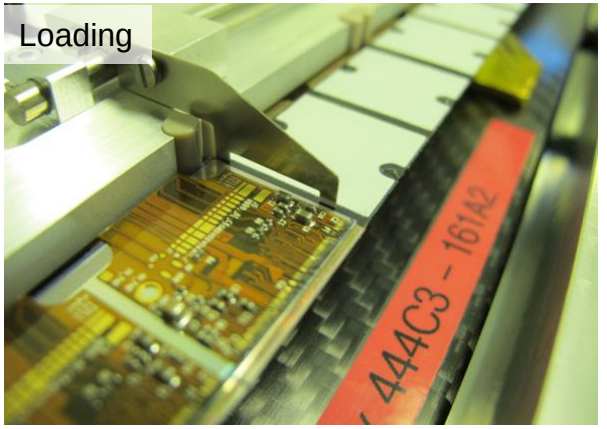
	Single chip modules (SC)						Double chip modules (DC)					
Production Batch	**B1**	**B2**	**B3**	**B4**	**B5**	**total**	**B1**	**B2**	**B3**	**B4**	**B5**	**total**
Built	18	16	37	14	15	100	26	48	50	11	30	165
Accepted for IBL	3 17%	7 44%	18 49%	14 100%	10 67%	**52** **52%**	7 27%	17 35%	41 82%	9 82%	24 80%	**98** **59%**
Handling/ packaging	0	0	1	0	0	1	1	3	1	2	5	12
IV sensor	3	1	8	0	3	15	2	0	1	0	1	4
Low voltage/ data	0	2	0	0	0	2	1	0	0	2	1	4
Regulators	2	0	0	0	0	2	3	1	0	0	0	4
Bump bonding	10	6	9	0	2	27	12	27	6	0	0	45

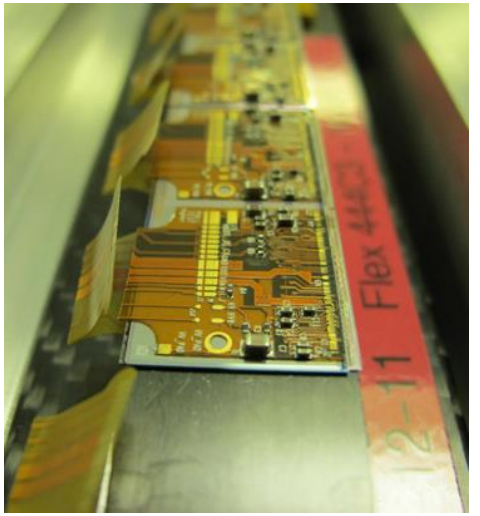
- Bumb bonding failure rate decreased significantly after batch 3
- Batch 4ff: yield > 80% for single/double chip modules
- B1 to B5: almost all modules assembled and tested
- Estimated total number of modules built from batch 5 on: ~200 SC and ~240 DC
- At the actual testing rate the module production is finished by September

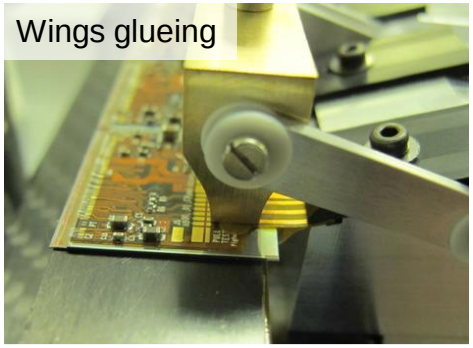
Stave loading procedure

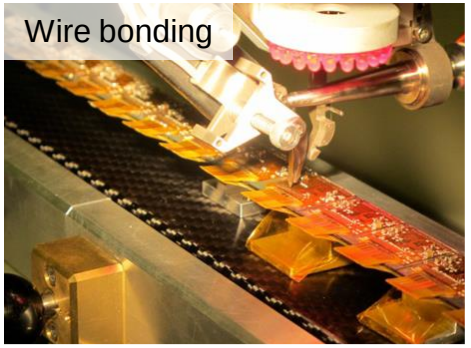


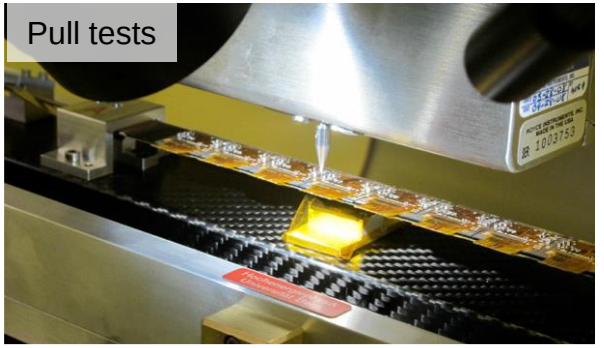












- Stave loading at Geneva university

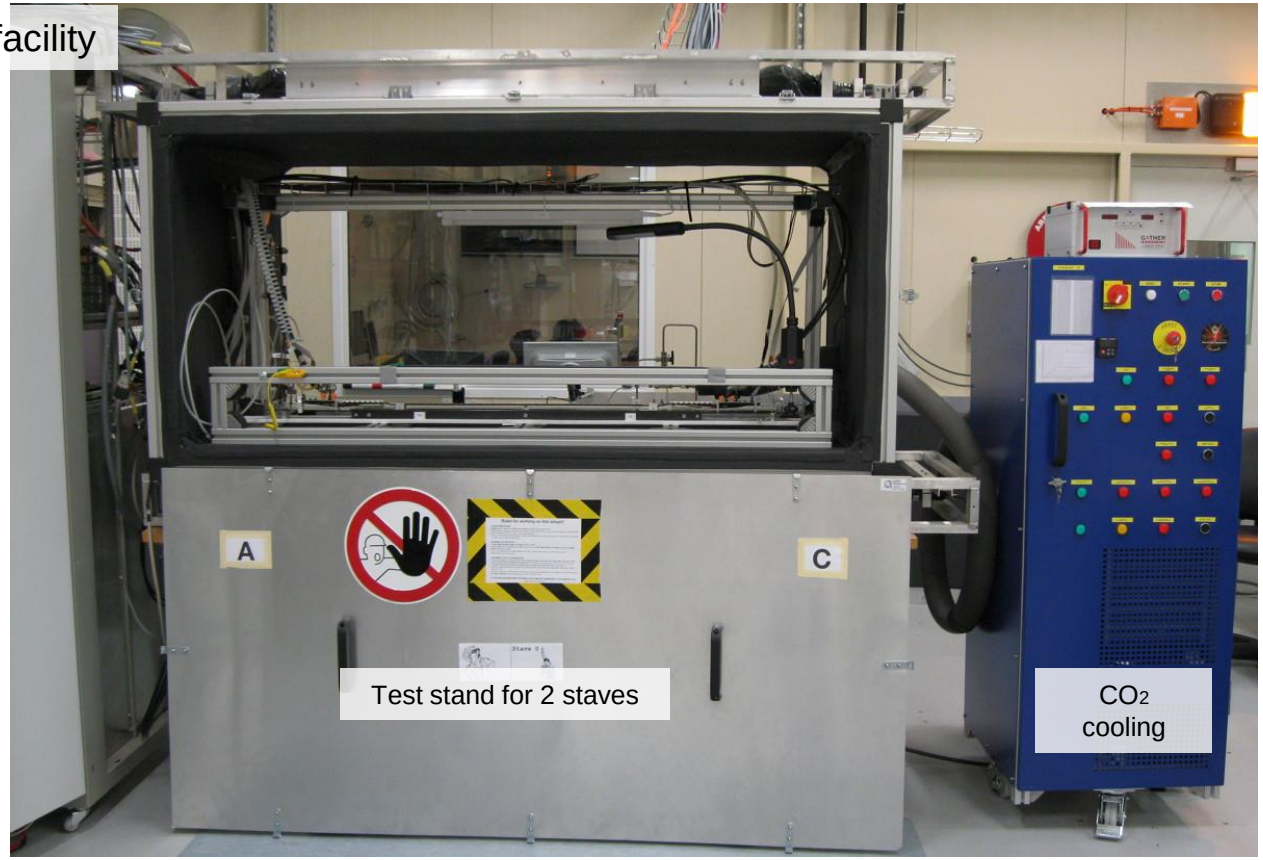
Production Stave QA at CERN

Reception tests at 10° C
- Cross check with Geneva results
- Power up studies
- Communication (register tests, eye diagrams)
- Sensor IV test

Tuning at -15° C
- Different tunings:
  - 1.5/2.0/2.5/3.0 ke threshold
  - 10 ToT @ 16 ke
- Creating noisy pixel masks

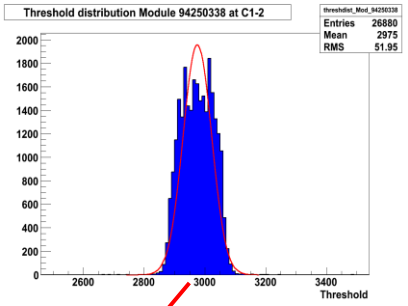
Operational tests at -15° C
- Source scans with Am-241/Sr-90 and self trigger
- Cosmic run with external trigger
- etc.

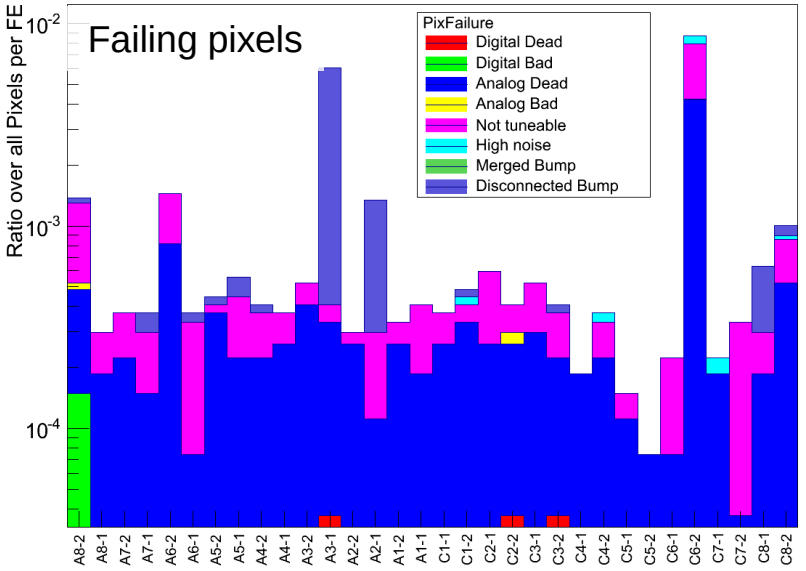
Test stand at CERN SR 1 facility

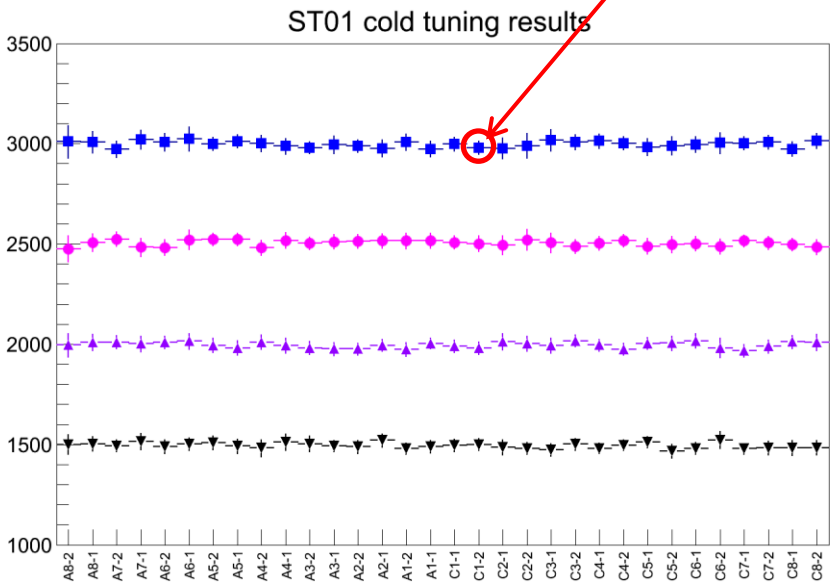


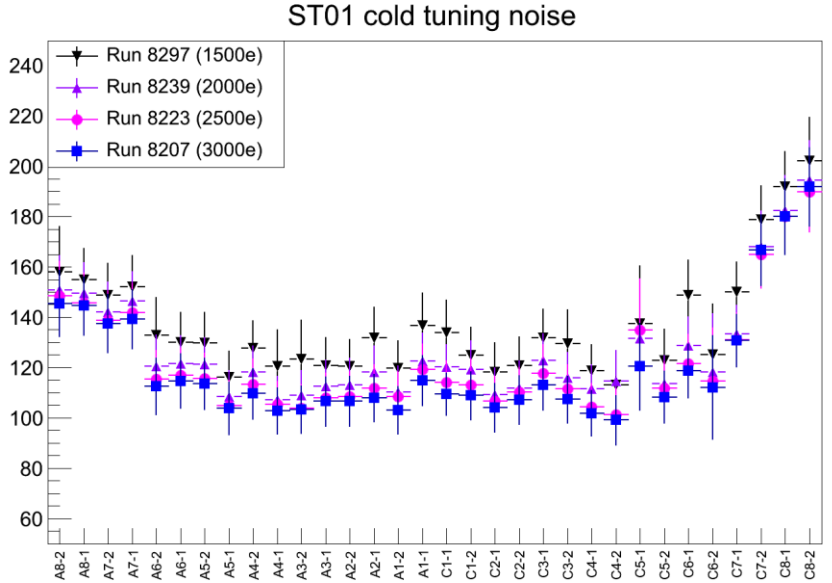
Results from first production stave

- 99.815 % operational pixels
- noise as expected (higher for 3d sensors)
- uniform threshold



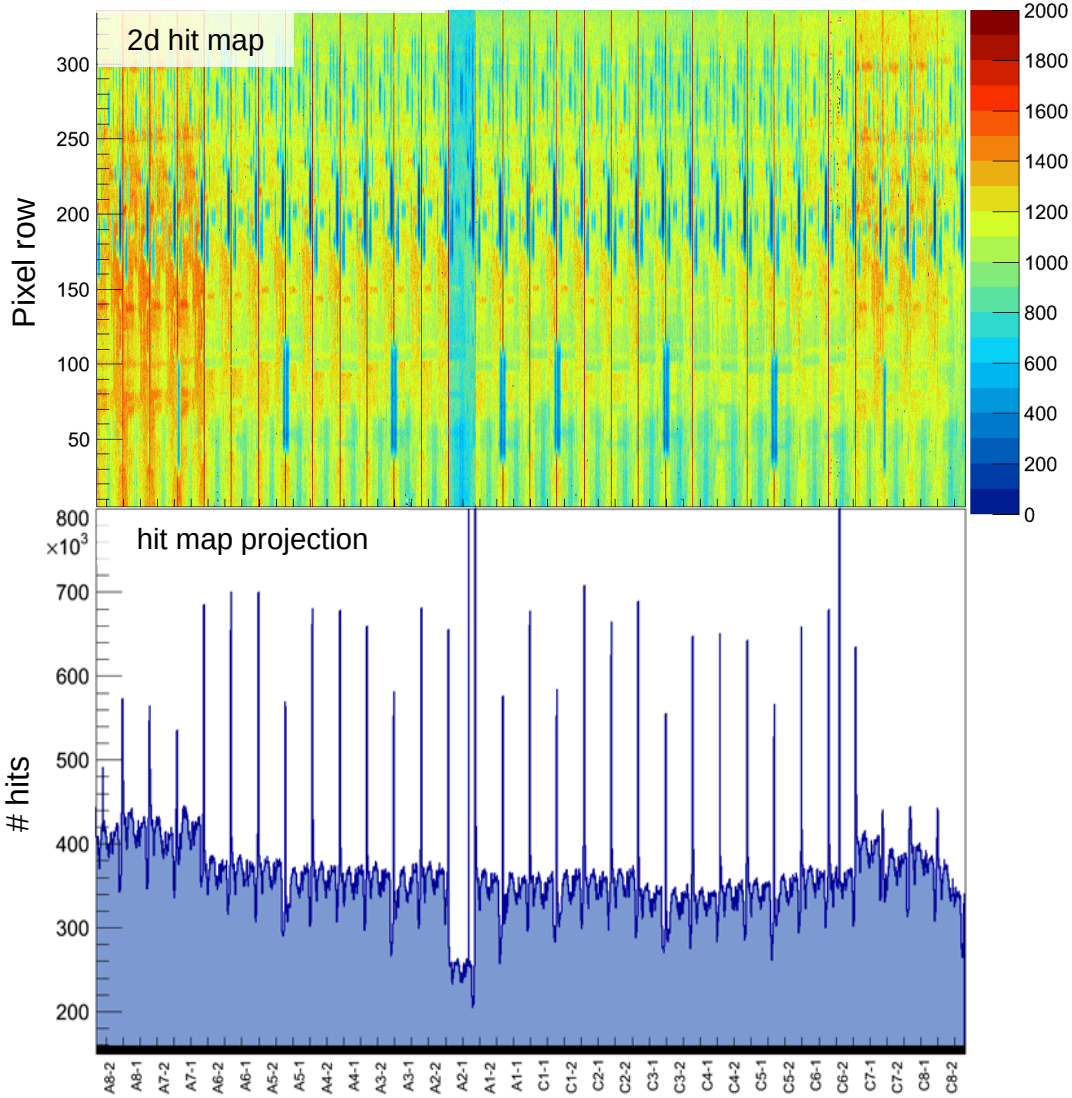






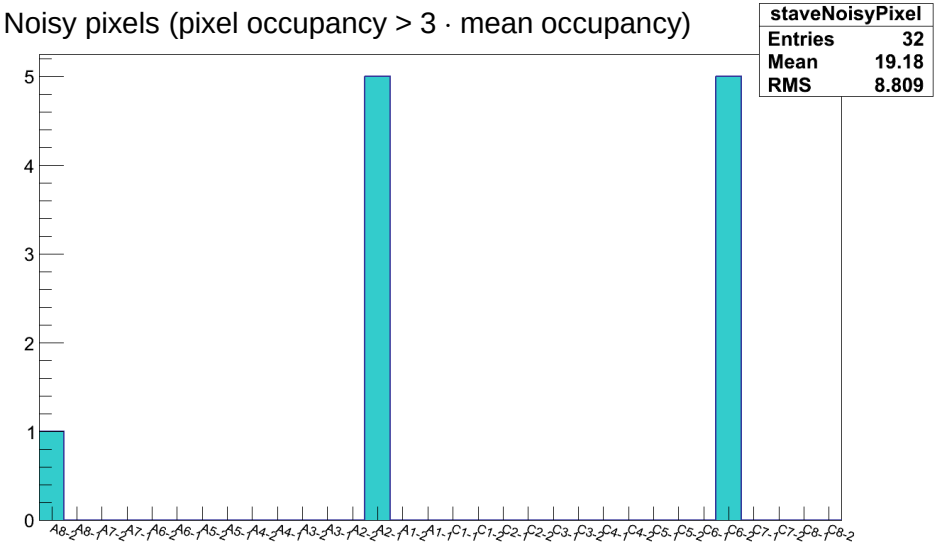
Source scan of first stave

Sr-90 source scan



- 12 h source scan with beta source (Sr-90)
- Less hits in one FE understood: not masked noisy pixels + FE self trigger mode
- Peaks from sensors edges: more sensitive area/pixel

Noisy pixels (pixel occupancy > 3 · mean occupancy)



Summary

- IBL is the new innermost layer of the ATLAS pixel detector
- New readout chip FE-I4 working well and fully tested for IBL with reasonable yield (61%)
- Planar n-in n and first time 3D silicon sensors are used
- Module production and stave tests currently ongoing
- Promising results of the first stave shown, by now already 4 production staves built and tested

Outlook

- Finish module testing in September
- Stave loading and testing until November
- Integration into existing pixel detector in April 2014