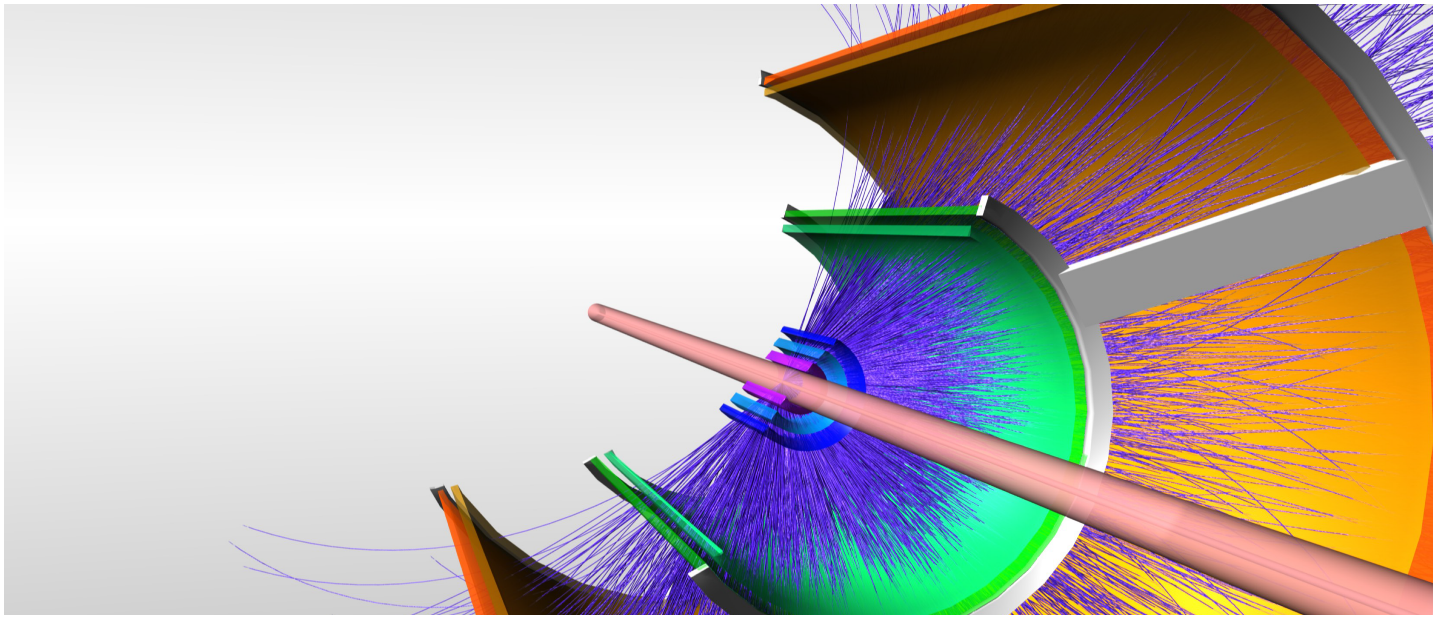
The upgrade of the ALICE Inner Tracking System



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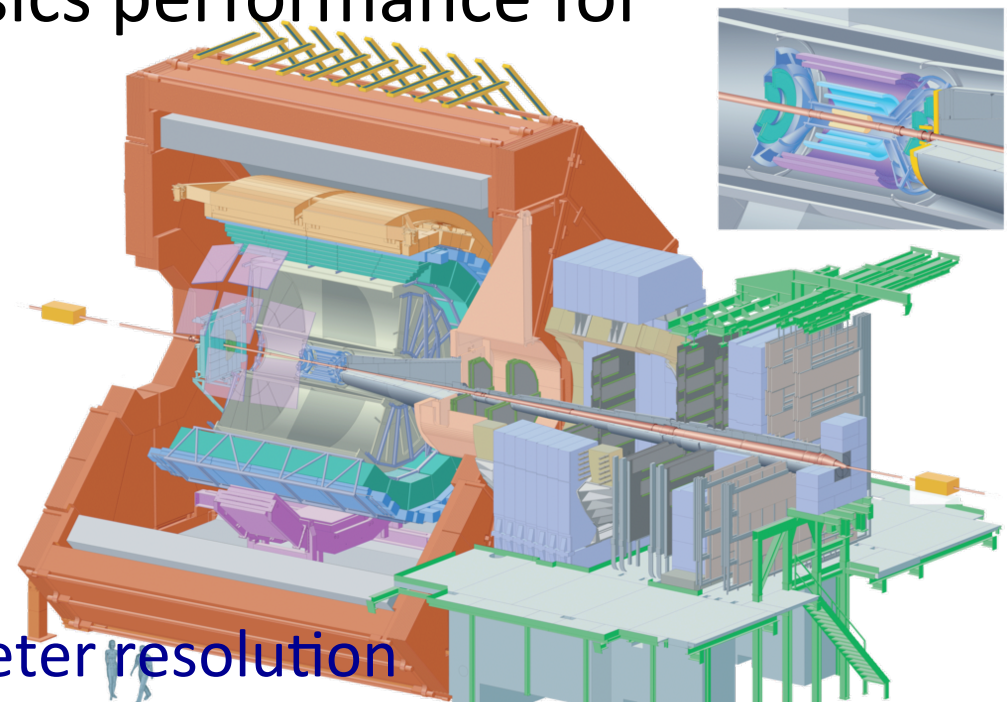
on behalf of the ALICE Collaboration

11th International Conference on Large Scale Applications and Radiation Hardness of Semiconductor Detectors3-5 July, Florence, Italy

Motivations for the ALICE upgrade

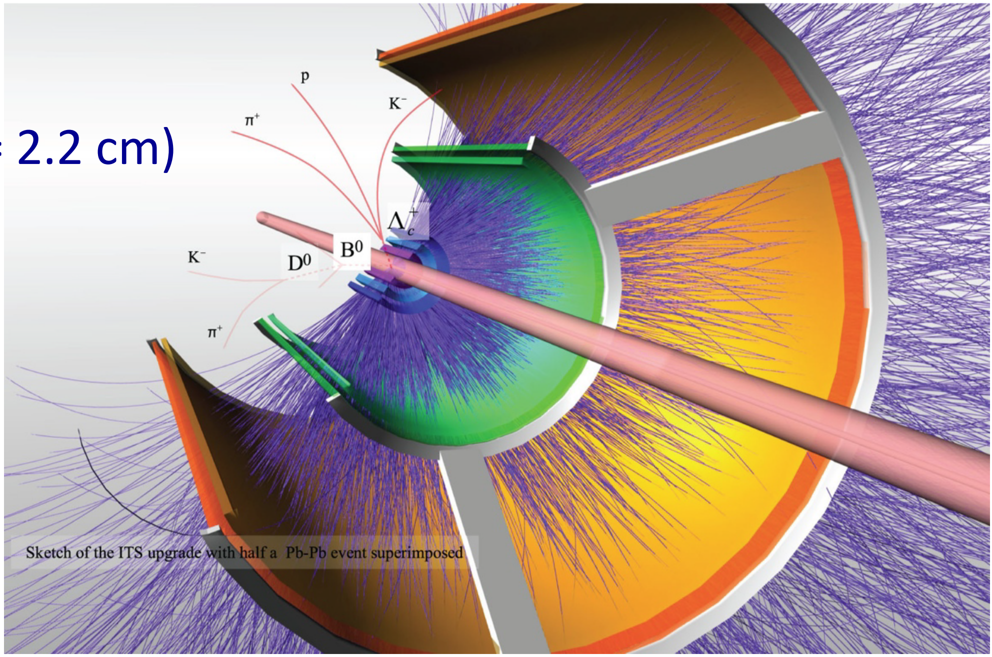


- Why: improve the physics performance for
  - Heavy flavor at low p_T
  - Quarkonia
  - Low-mass di-leptons
  - Heavy nuclear states
- How:
  - Improve impact parameter resolution
  - Higher LHC luminosity: $6x10^{27}$ $cm^{-2}s^{-1}$ -> 50 kHz minimum bias Pb-Pb interactions
- What:
  - New beampipe, TPC and ITS, all readout electronics, etc…

ITS Upgrade features

ALICE

- Good spatial resolution: improve secondary vertex resolution by factor ≈3 (5) in rϕ (z):
  - smaller beam pipe (R = 1.9 cm)
  - inner layer as close as possible (R = 2.2 cm)
  - more layers
  - less material budget
    - thin sensors (goal: 0.3-8 % X_0/layer)
    - thinner beam pipe (ΔR = 800μm)
  - smaller pixel size:
    - monolithic pixels (20μm x 20μm)

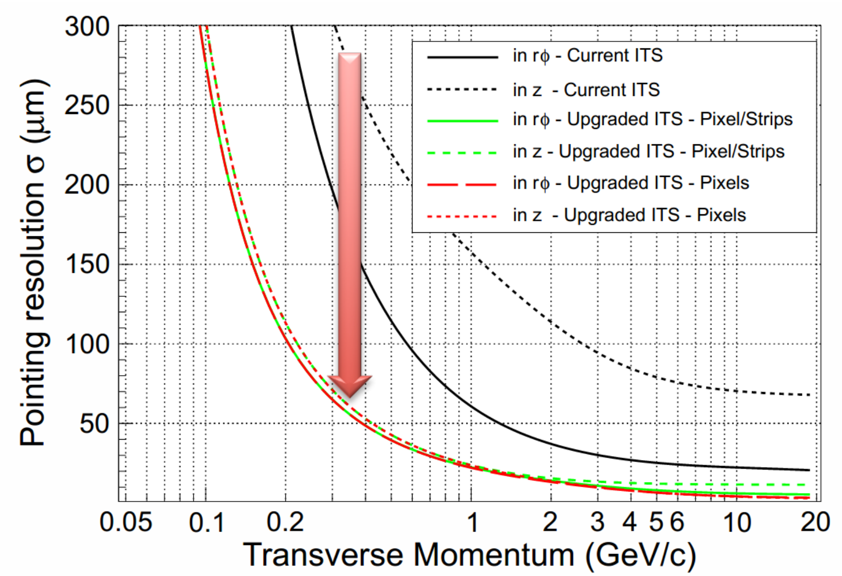


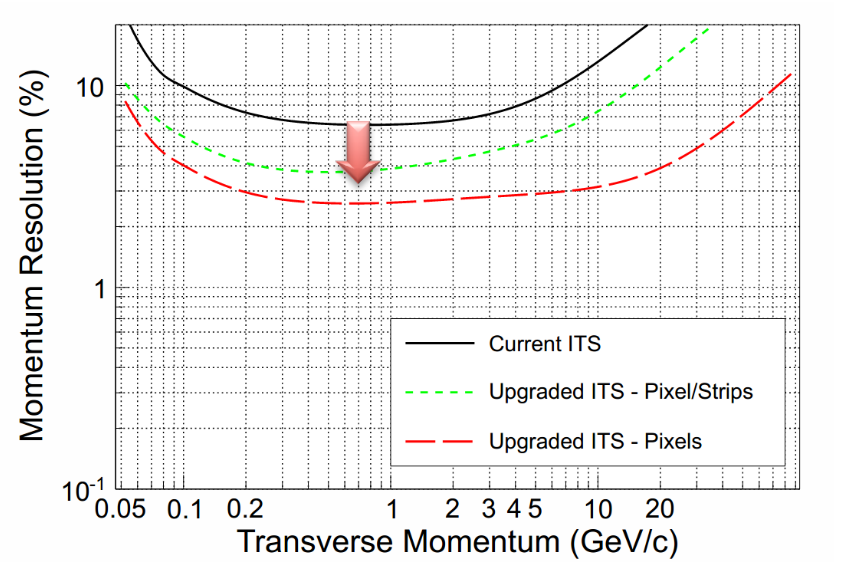
Sketch of the ITS upgrade with half a Pb-Pb event superimposed

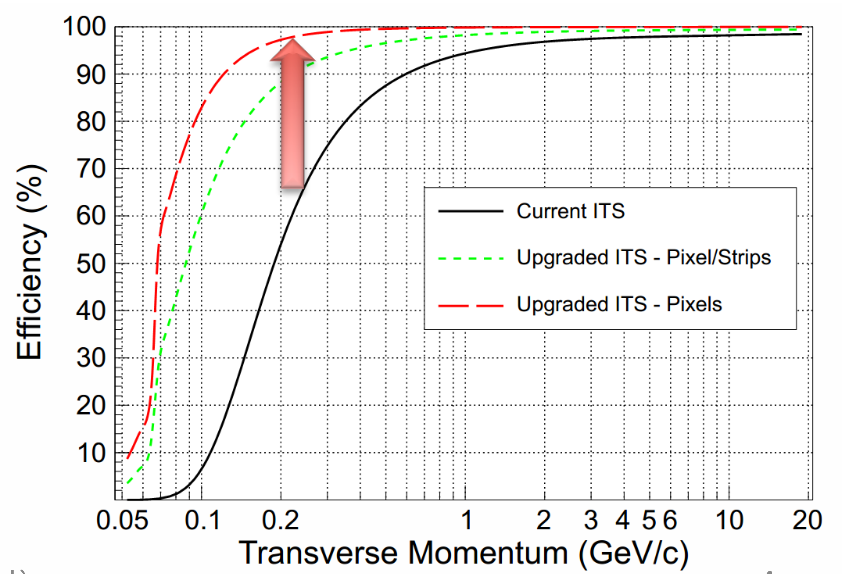
- Radiation level:
  - 700 kRad + 10^{13} n_{eq} /cm^2 for the full integrated luminosity (innermost layer including a safety factor = 4)
- high standalone efficiency and p_T resolution
- fast readout:
  - 500 Hz → 50 kHz in Pb-Pb
  - ~ 200 kHz in pp
- fast removal/insertion to ease possible yearly maintenance

Expected improvements of the detector performance:

- 3 x better pointing resolution
- 2 x better standalone tracking efficiency at low p_T
- 2.5 x better standalone momentum resolution







Conceptual detector layout:

Layer	Type	R [cm]	±z [cm]	Intrinsic resolution [μm] rφ	z	Material budget [% X_0]
	Beam pipe	2.0	-	-	-	0.22
0	Pixel	2.2	11.2	4	4	0.3
1		2.8	12.1	4	4	0.3
2		3.6	13.4	4	4	0.3
3	Pixel	20.0	39.0	4	4	0.8
4		22.0	41.8	4	4	0.8
5		41.0	71.2	4	4	0.8
6		43.0	74.3	4	4	0.8

Inner barrel

Inner Barrel (IB): 3 layers pixels

Radial position (mm): 22,28,36

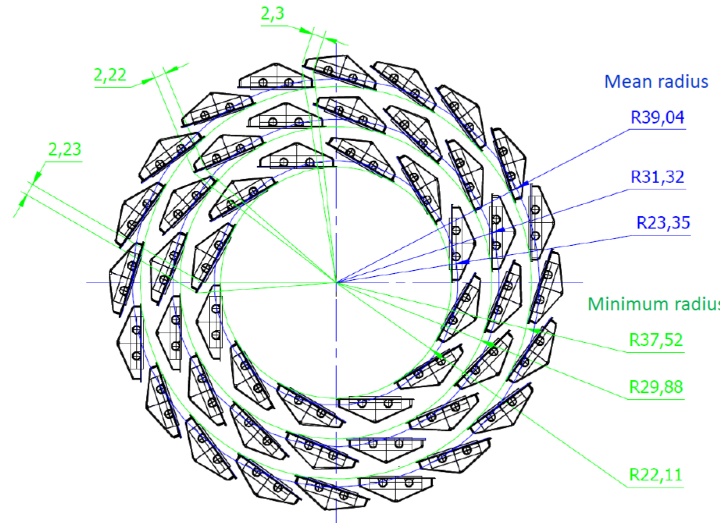
Length in z (mm): 270

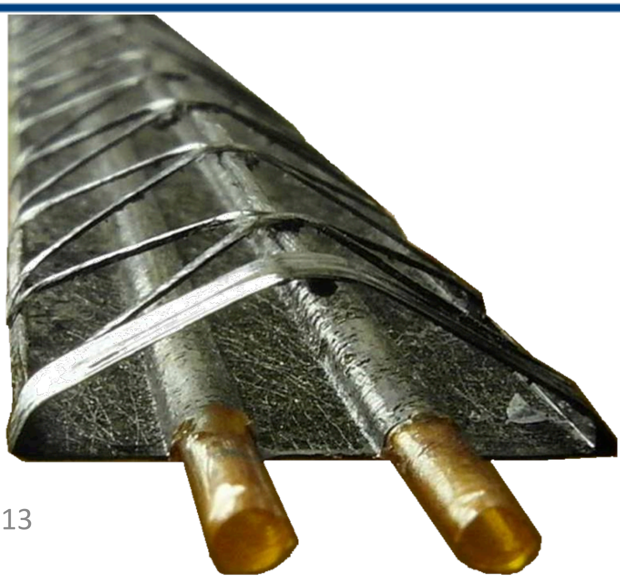
Nr. of staves: 12 + 16 + 20 = 48

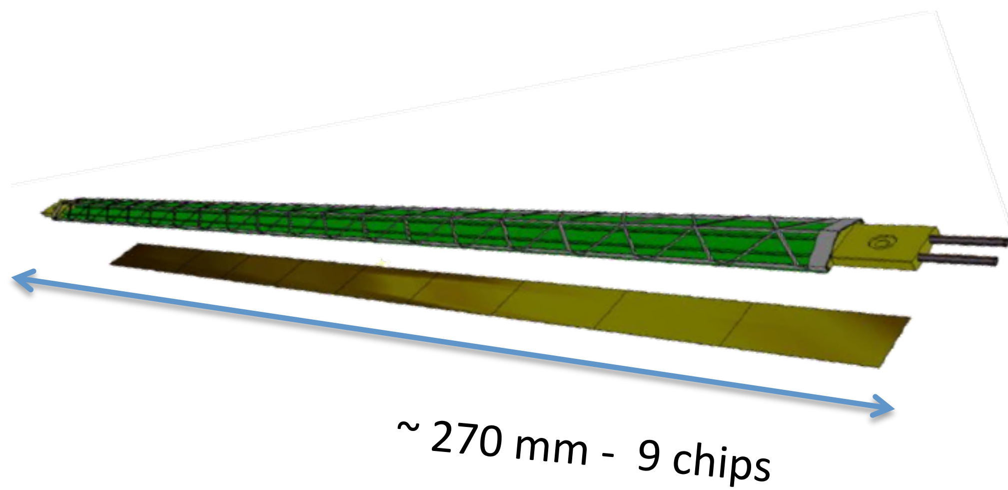
Nr. of chips/stave: 9

Pixel size: ~ 20 µm x 20 (30) µm

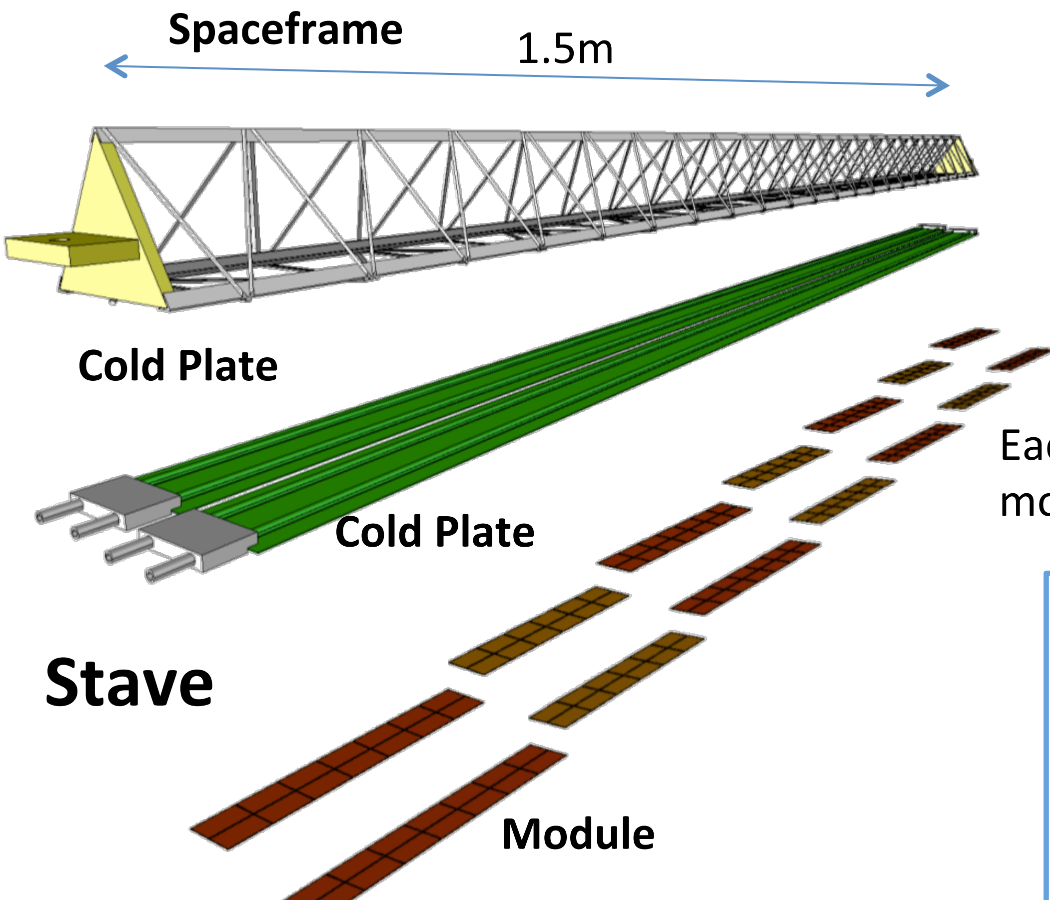
Material thickness: ~ 0.3% X_0

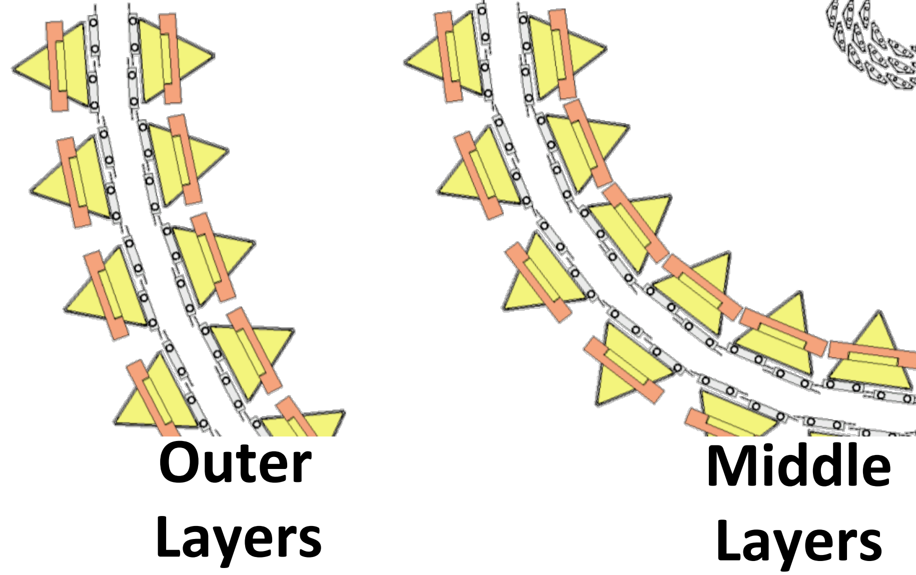






Outer barrel





Half-Stave

Each half-stave will consists of a number of modules glued on a common cold plate

Outer Barrel (OB): 4 layers pixels

Radial position (mm): 200, 220, 410, 430

Length in z (mm): 843, 1475

Nr. of staves: 48, 52, 96, 102

Nr. of chips/stave: 56, 56, 98, 98

Nr. of chips/layer: 2688, 2912, 9408, 9996

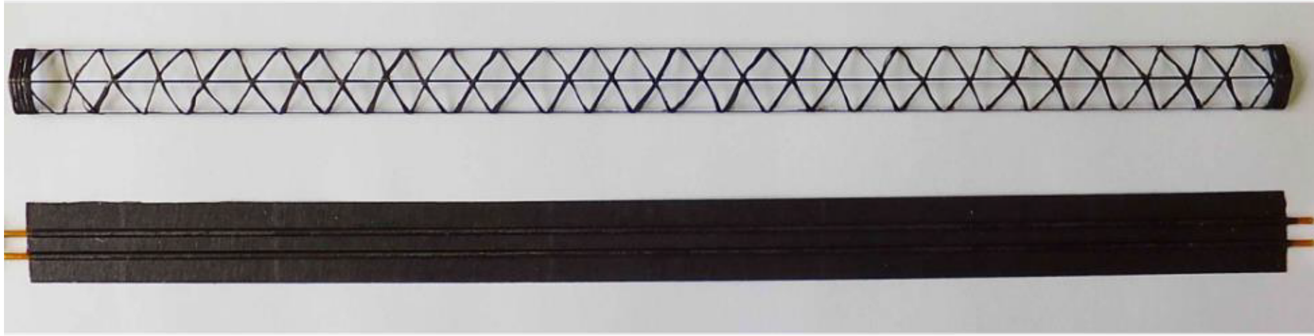
Material thickness: ~ 0.8% X_0

Each module consists of a hybrid integrated circuit, i.e. a number of pixel chips (e.g. 2 x N) bonded on a flexible printed circuit, which might be glued on a carbon ply

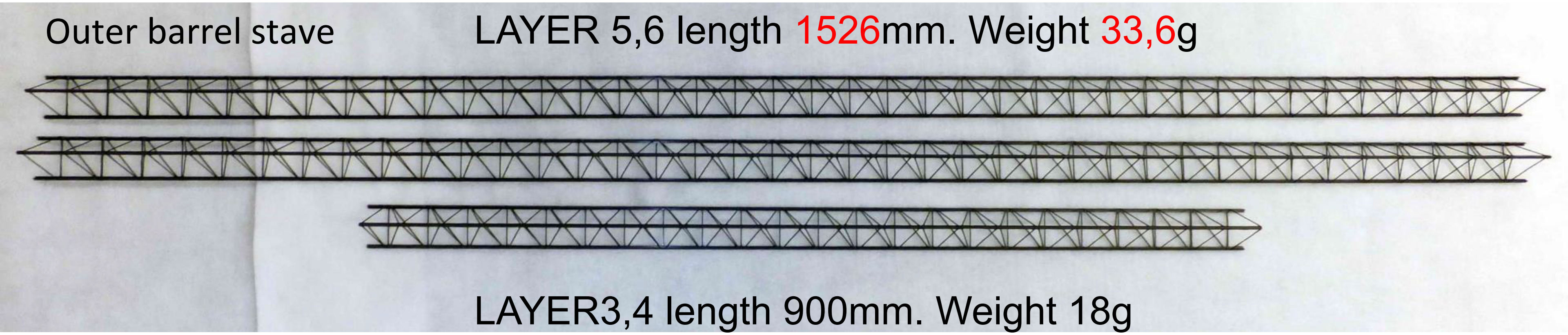
Space frame & cooling

- Inner barrel:
  - Embedded kapton pipes
  - Polymide microchannels
  - Silicon microchannel
- Outer barrel:
  - Embedded kapton pipes

Inner barrel stave

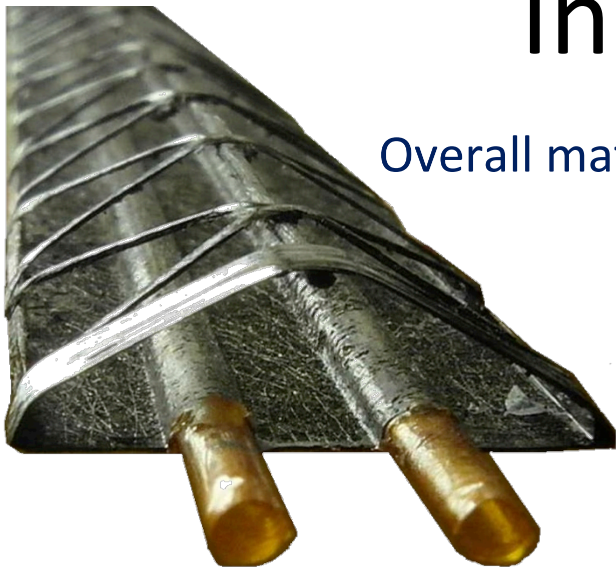


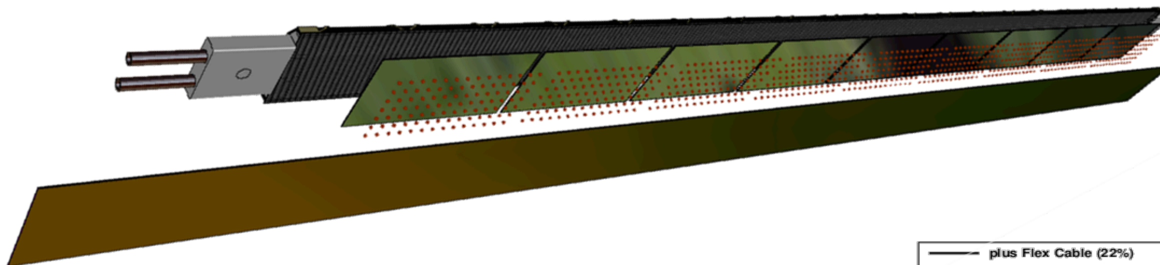
Weight	1.8 grams
X/X0	*0.31%*
Cooling capacity	*<25°C at 0.3W/cm2*
	<30°C at 0.5W/cm2

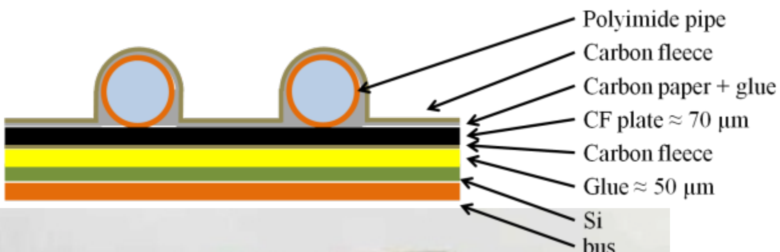


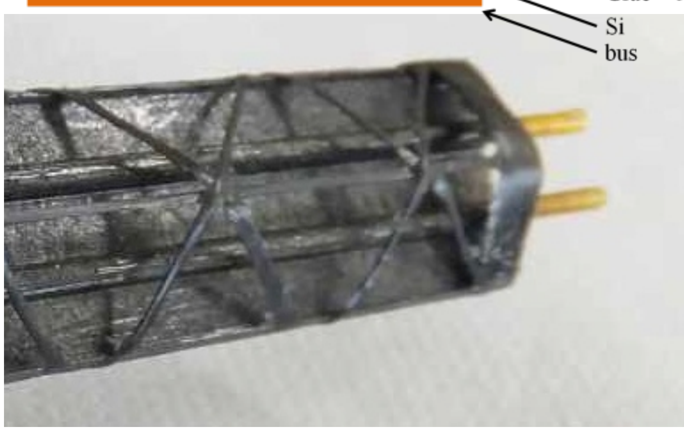
Inner barrel stave

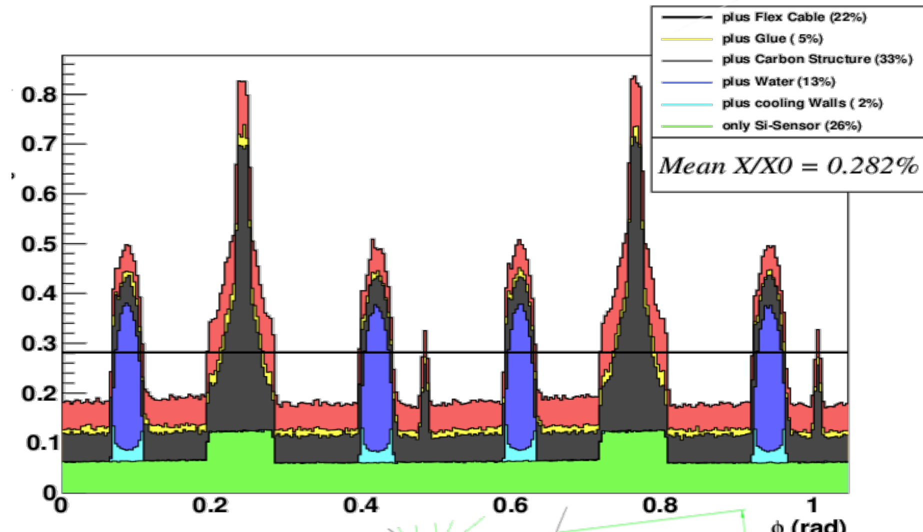
Overall material budget per layer X/X_0: SPD ~1.14% ➡ ~ 0.3%

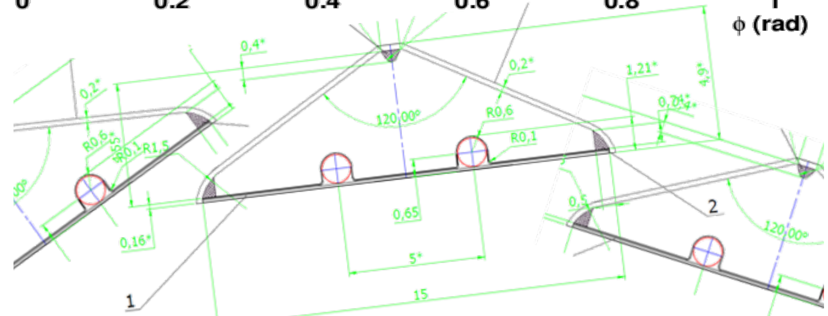






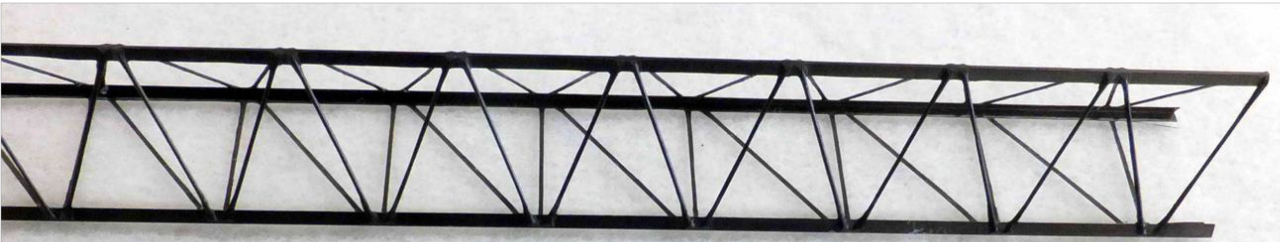






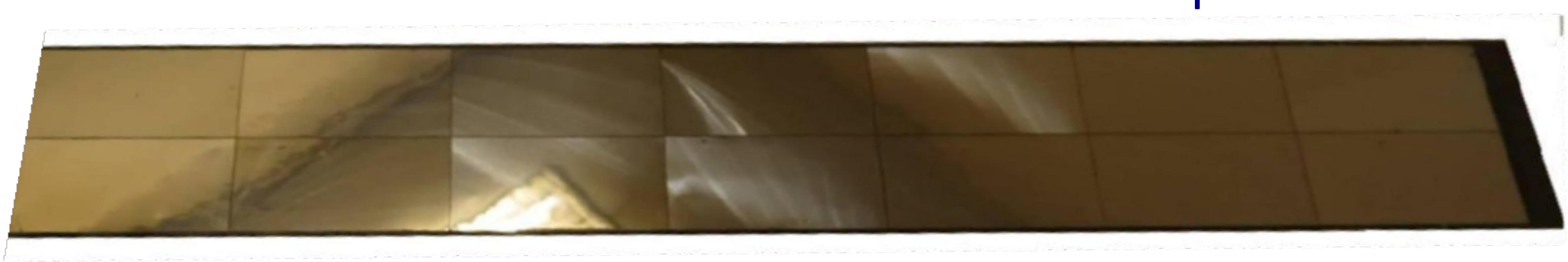
Outer barrel stave and module

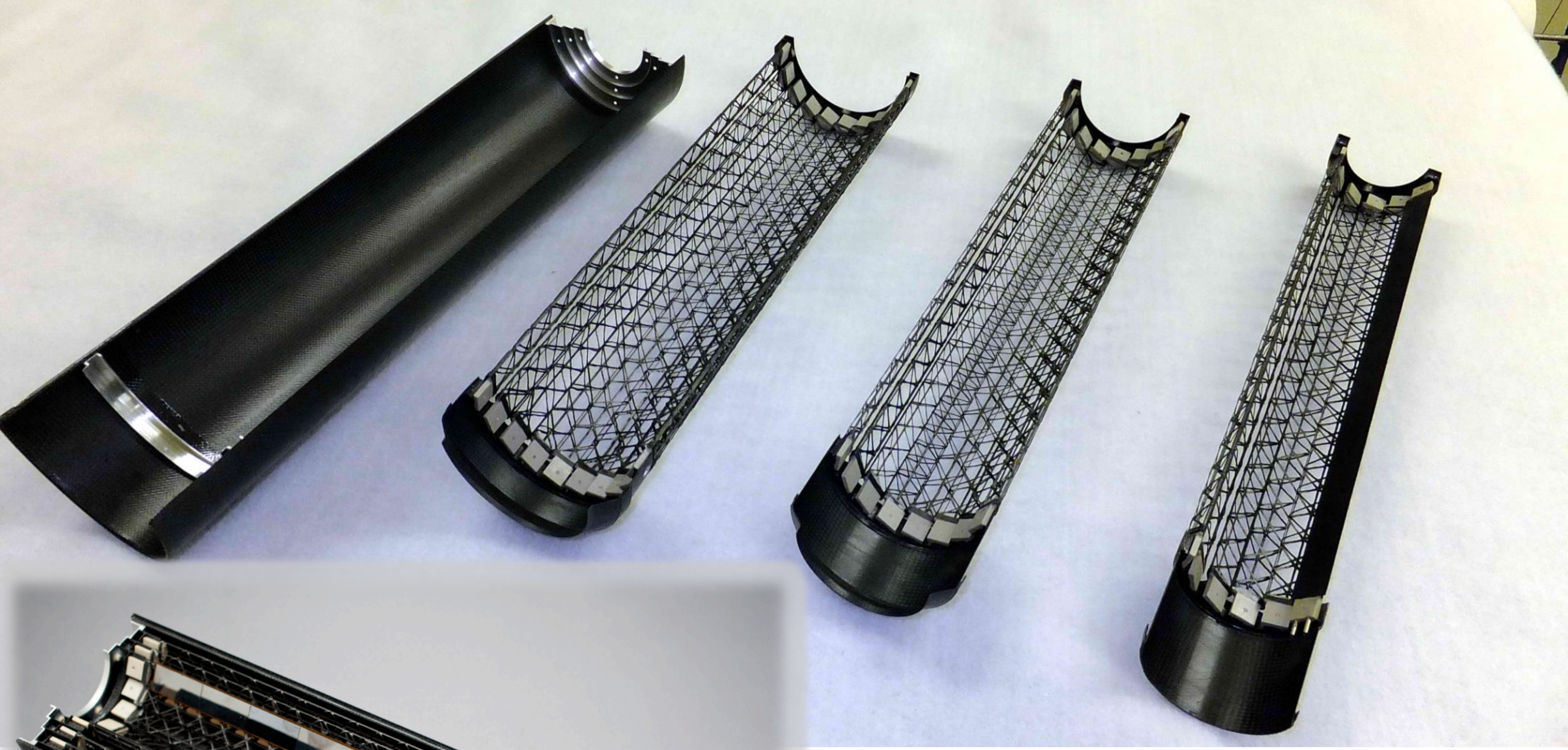
Overall material budget per layer X/X_0: ~ 0.8 %



Design in progress

– Module: 2xN pixel chips
– FPC
– Cooling
– Assembly procedure





Inner barrel prototype

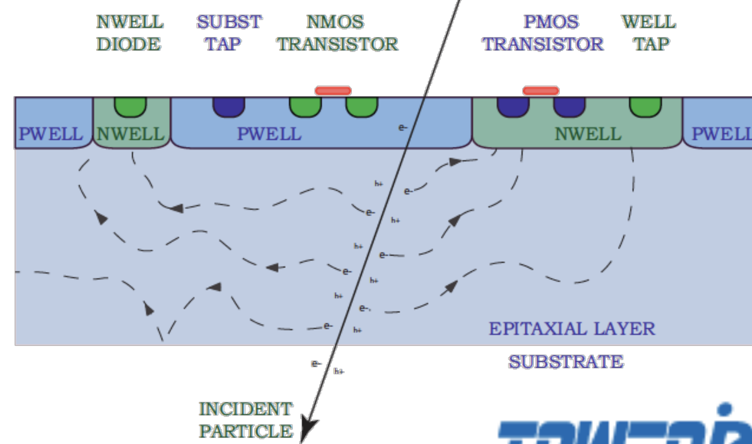
Pixel chip technology R&D

New specialty CMOS technologies available for monolithic pixel detectors.

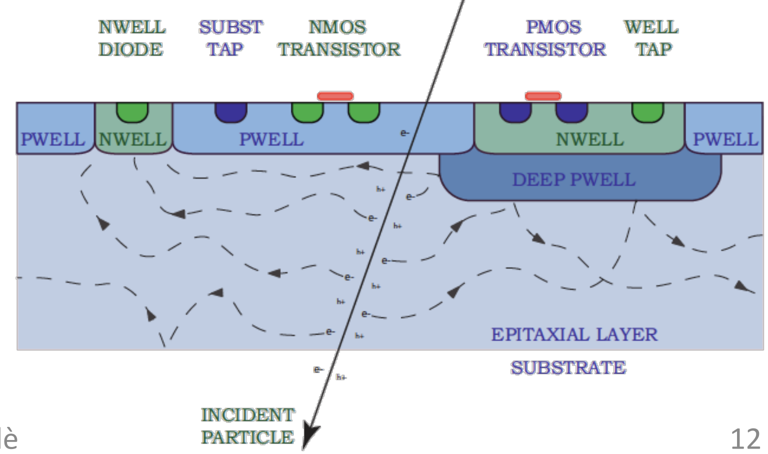
Development of monolithic detectors using

- Tower/Jazz 0.18 µm CMOS technology:
  - Improved TID resistance due to smaller technology node
  - Available with high resistivity (1-5k Ω•cm) epitaxial layer up to 40 µm (substantial depletion at 1-2V)
  - Special quadruple-well available to shield PMOS transistors (allows in-pixel truly CMOS circuitry)

CMOS



CMOS with deep p-well



Pixel chip architecture

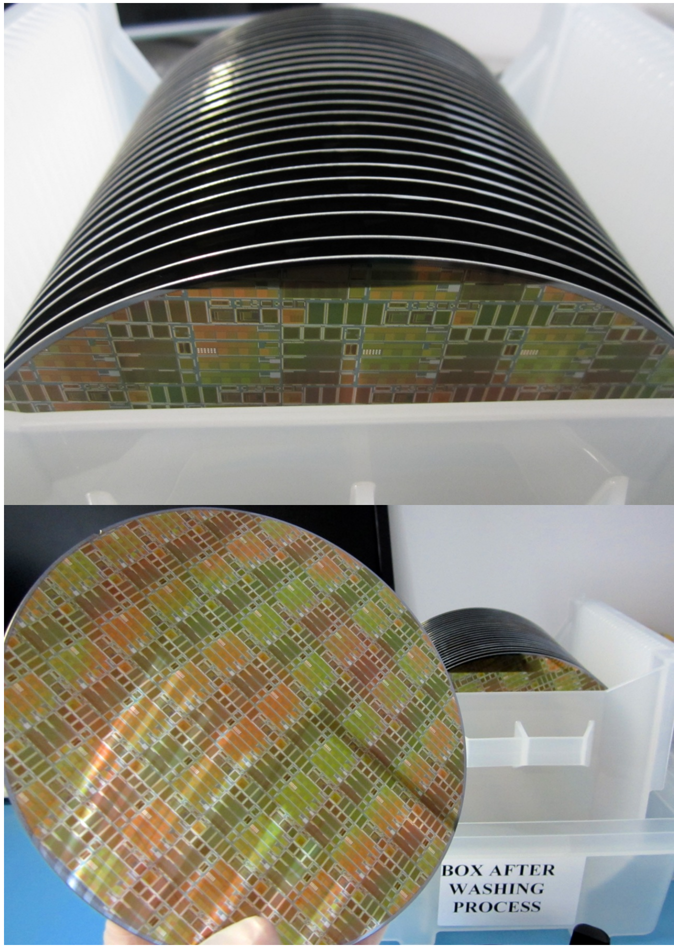
- MIMOSA (IPHC Strasbourg) – baseline (most mature and advanced)
  - Rolling shutter with in-pixel CDS, column-level discriminator, 2 rows parallel RO
  - Integration time: 30 μs
  - Power ≤ 400 mW/cm^2 (ANALOG+DIGITAL)
- CHERWELL: Parallel Rolling Shutter (RAL)
  - Based on previous development.
  - Integration time: ~40 μs
  - Power < 200 mW/cm^2
- EXPLORER: In-pixel discriminator + data driven readout (CERN)
  - shaping time ~2 μs, readout time ~4 μs; <
  - Power ~100 mW / cm^2 (ANALOG ONLY)

- SENSOR OPTIONS
  - collection electrode geometry
  - pixel dimensions/shape etc…

- READ-OUT OPTIONS
  - Priority encoder
  - Orthopix
  - Parallel rolling shutter
  - ….

Engineering run march 2013

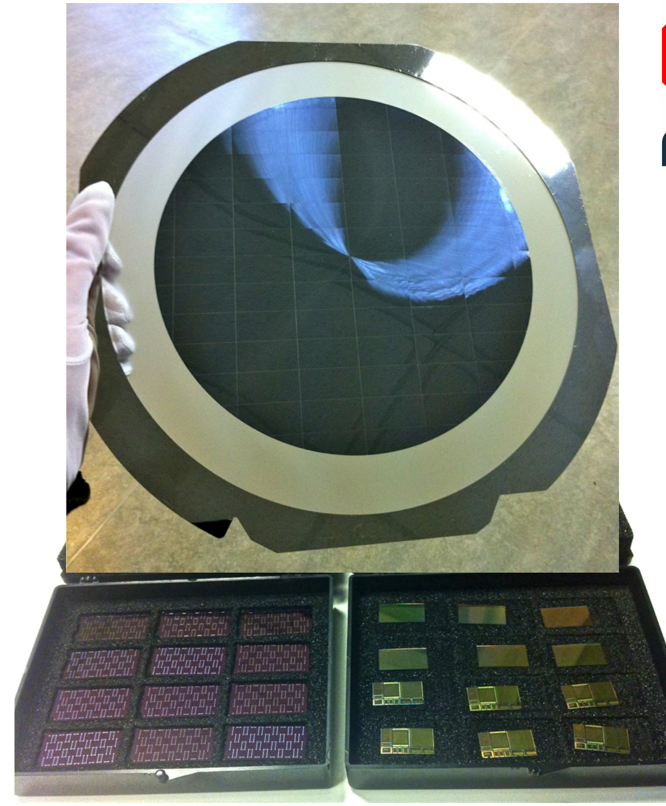
- High resistivity wafers procurement
  - Nominal resistivity (30; >1k; >2k Ωcm)
  - Different epitaxial layer thickness (12-40 μm)
- Complex dicing scheme, 26 dices per reticle:
  - Pixel matrices with:
    - Different architectures (IPHC-CERN-RAL)
    - Different anode shapes and dimensions
    - Different read-out options
  - Resistivity measurements test structures
  - Data transmission logic blocks
- Wafers delivered June 12th
  - Sent to company for thinning and dicing
  - Ready for tests



Thinning @ 50 μm and dicing

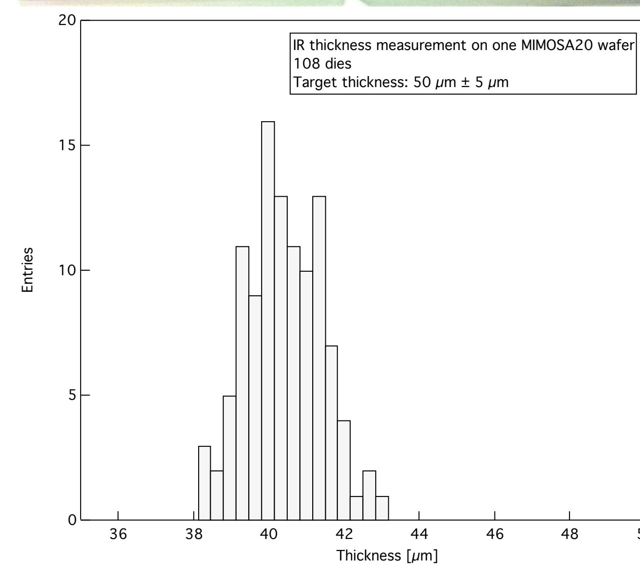
Work with commercial supplier to thin wafers to 50 **μ**m assuming chip size of 15 mm x 30 mm

- Thinning and dicing of blank 200 mm wafers (13) – 2012
- Thinning and dicing of patterned 200 mm wafers (pads for interconnection tests) – 5 wafers – 2012
- Thinning and dicing of one MIMOSA20 wafer (die size 10 mm x 20 mm) – completed



Metrology tests confirm thickness within expectations: 50 ± 5 μm

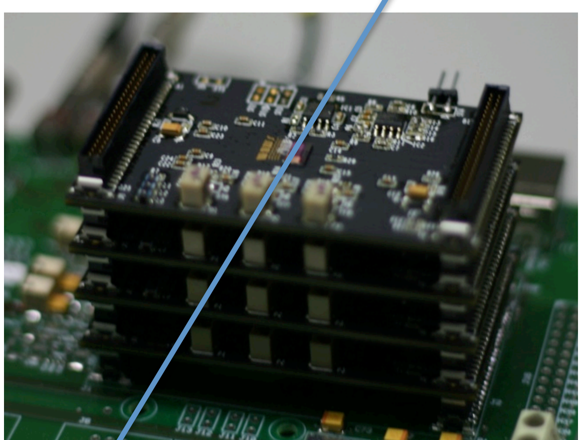
- IR measurement does not take into account metal and inter-metal layers; there are 6 metal-layers corresponding to ~10μm offset

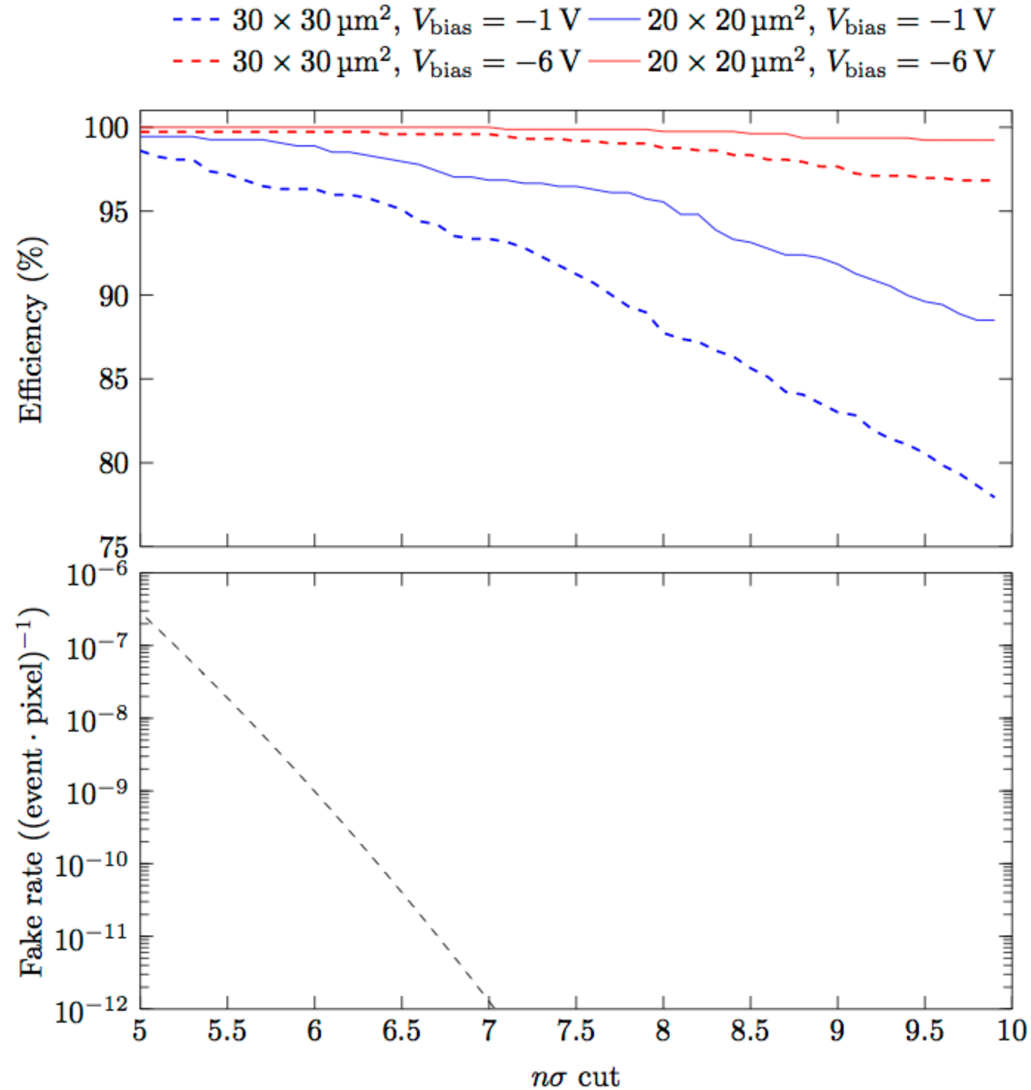


Test beams (1)

- Test Beams:
  - CERN PS - December 2012

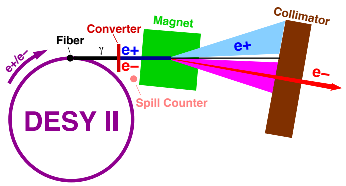
    Explorer chip: 4 chips forming a self-contained telescope at PS





High efficiency (>99%) at low fake hit rates

Reverse substrate bias gives extra margin



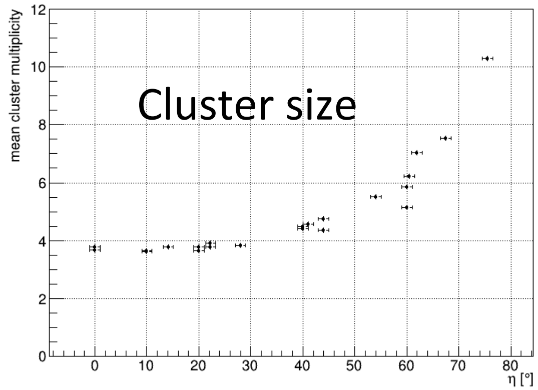
Test beams (2)

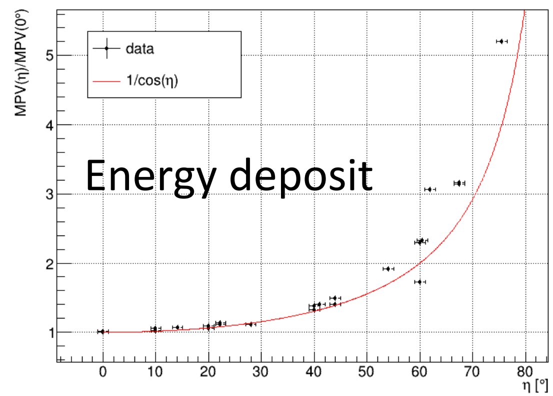
- Test Beams:
  - [DESY - March 2013]
  - DESY - June 2013
  - DESY – July 2013

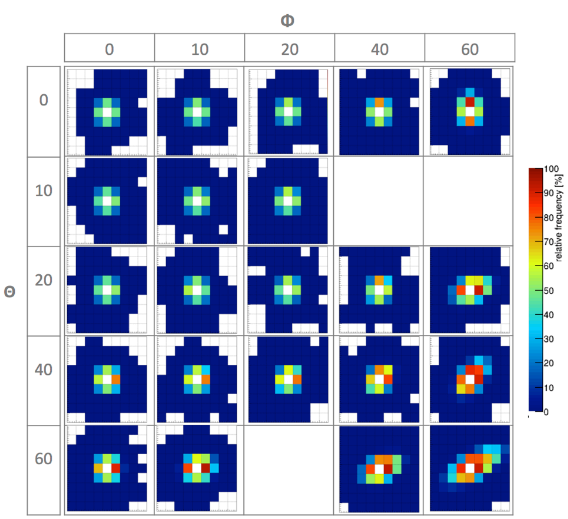
Goals:

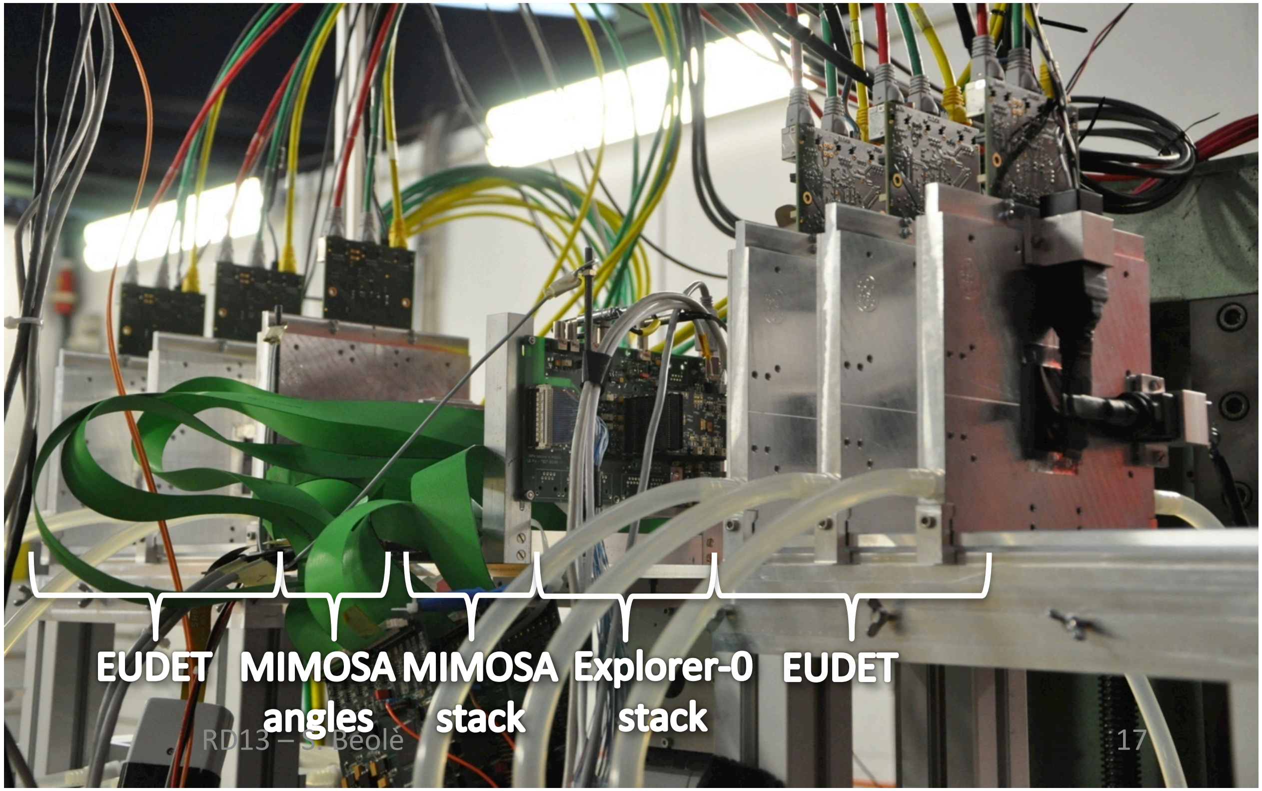
- Verification of MC model for inclined tracks
- Characterization of irradiated samples

MIMOSA 32









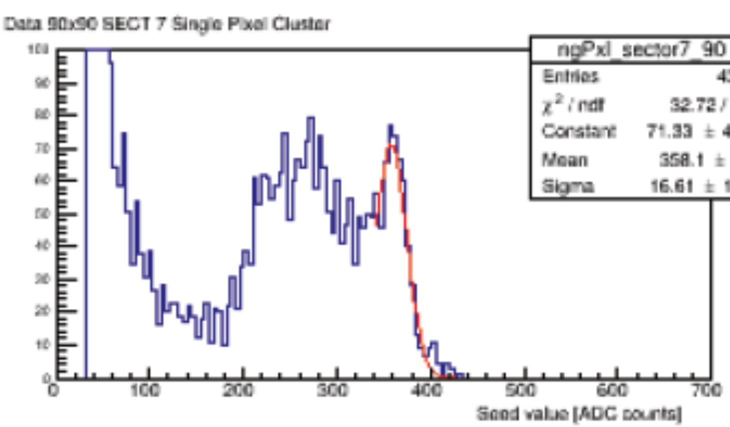
Preliminary results on Explorer-0

Charge collection efficiency measured with Fe^{55} source

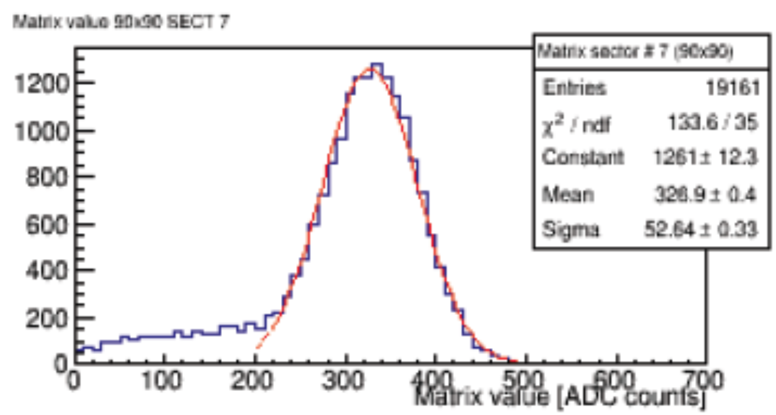
- CCE is calculated as the ratio between the MPV of the charge collected in a cluster divided by the single pixel collection peak peak value
- CCE measured for
  - different pixel size
  - different V_{bias} values (-1; -6 V)
  - with and without threshold on the seed surrounding pixels

Very good (>98%) charge collection (-> detection) efficiency for pixel size ~ 20µmx20µm

A) Seed spectrum
(single-pixel clusters)



B) Cluster spectrum
(sum of 5 × 5-matrix around peak)



Radiation Damage tests

Chip	Period	Facility	Radiation type	Results
TJ180_TID	August 2012/ February 2013	CERN	10 KeV X-Ray (TID < 10 Mrad)	Study of the CMOS Threshold shift and leakage current => adequate tolerance for ALICE ITS
TJ180_SEU	April 2013/ May 2013	NPI Prague	Proton beam (28 MeV, 35 MeV)	SEU Cross section (per bit): 10^{-13} cm^2 (Very preliminary results) => adequate tolerance for ALICE ITS
Explorer0	December 2012	CERN	PS, Line T10	No radiation damage studies. Tracking efficiency with 5 GeV/c pions: ~ 100% tracking efficiency at 5σ threshold.
Explorer0	March 2013	DESY	Electron beam	(First result on non ionizing radiation damage 10^{13} n_{eq}) Evaluation of the Noise (+8%) and Signal to Noise (-13%)
Explorer0	17 June 2013 -> 25 June 2013	DESY		
Explorer0	22 July 2013 -> 04 August 2013	DESY		

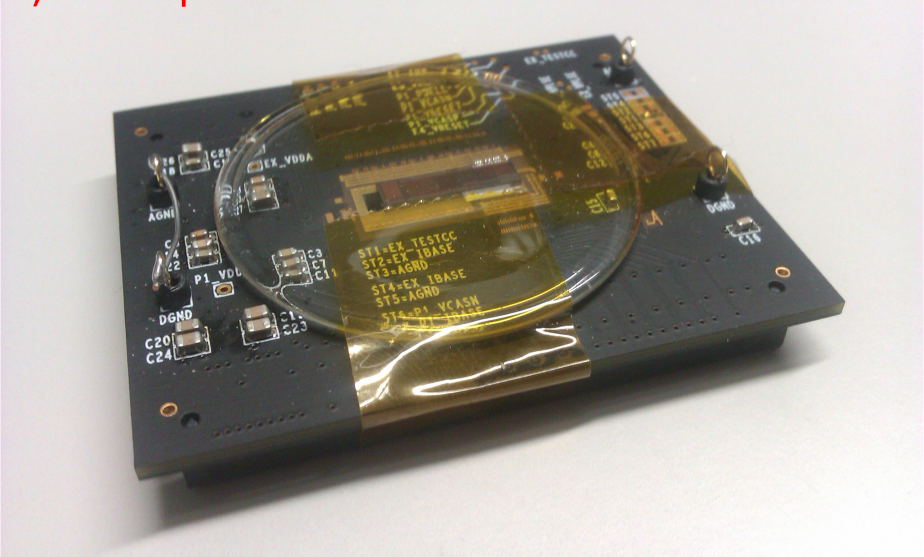
Very preliminary results on Explorer-0 and test structures

Beam test data analysis ongoing

Architecture qualification

- Dedicated test system developed in the framework of the chip design
  - Hybrid board to allocate DUT, custom for each chip.
    - Developed by UK (Cherwell) and CERN (Explorer-1 & Priority encoder)
    - Ready to bond first dices from engineering run
  - Proximity board, common to all chips.
    - Designed by Padua, production and assembly to be done at CERN. First version equipped with components
    - Under test NOW
  - DAQ system, common to all chips.
    - Use of “Scalable read-out system” (SRS) developed at CERN.
- Test campaign
  - Fe55
  - Laser tests
  - Beam tests @ Desy (July-August)

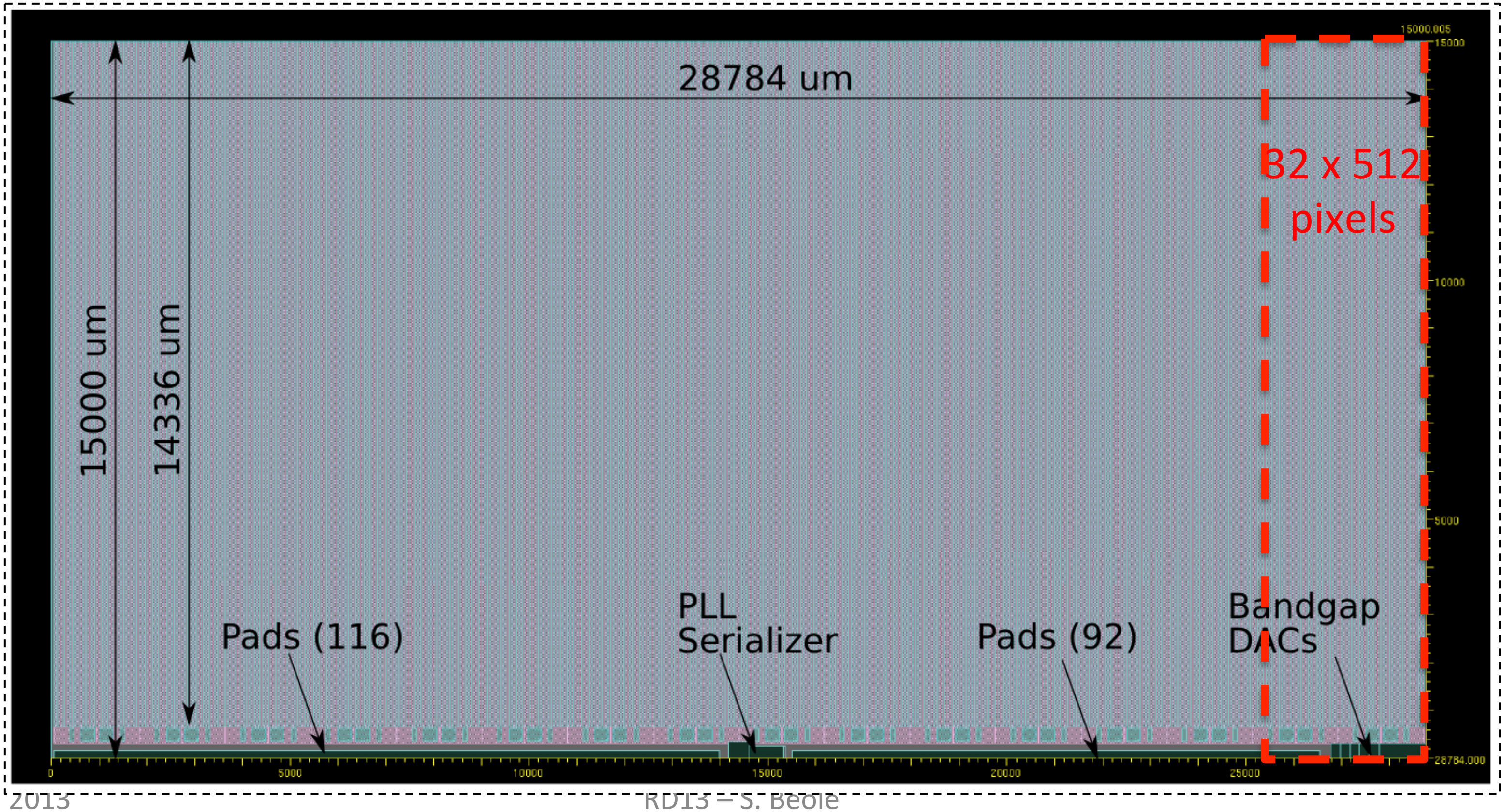
first results expected within the end of July



Engineering run end of 2013: large scale demonstrator

- Based on the priority encoder & front end circuit already submitted in the previous engineering run
  - 32 regions of 32 columns each, 512 pixels per column (28 μm x 28 μm) ≈ 29 mm x 15 mm

Pixel sub-matrix: 0 → 31

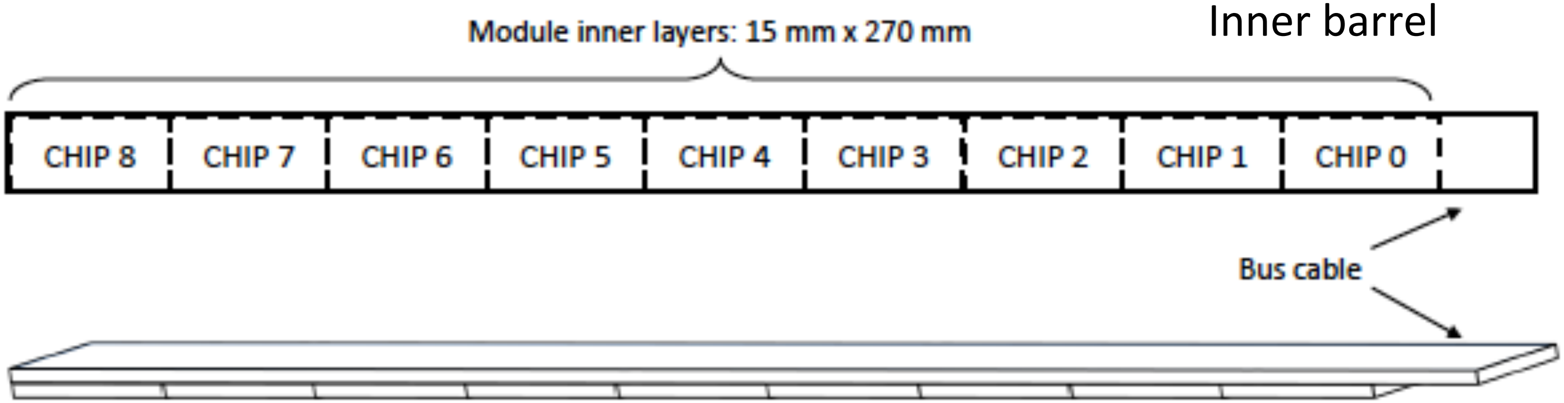


System aspects

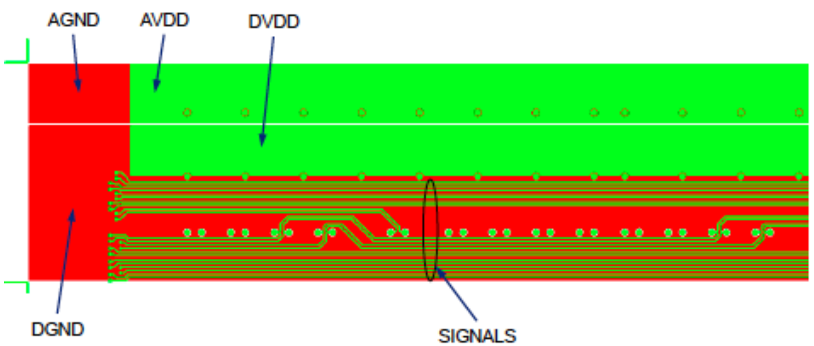
- Very large chip: optimization of architectural aspects in pixel matrix and digital circuitry/data transmission
  - constraints on digital circuitry due to timing/area
  - power consumption (0.3-0.5 W/cm^2 power budget is upper limit)
  - Operation with realistic trigger rate and detector occupancy: data compression, multi-event buffer
  - Serializer
  - Effects of the connection pads
- Production Yield
- Chips used to produce working modules for inner and outer barrel

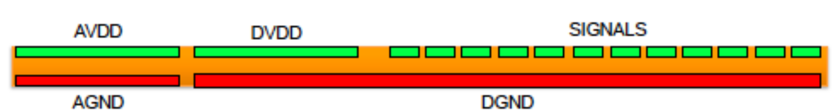
Flex Printed Circuit

Inner barrel



- Bus cable:
  - Al + polyimide + Al
- Chip-On-Flex connections:
  - Au-stud
  - Laser soldering

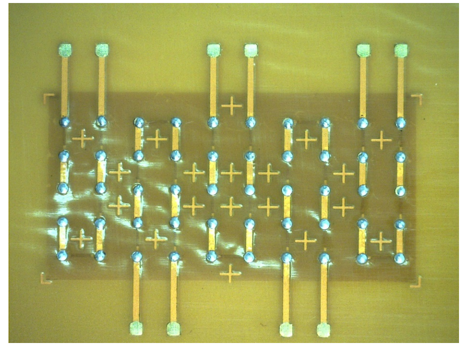


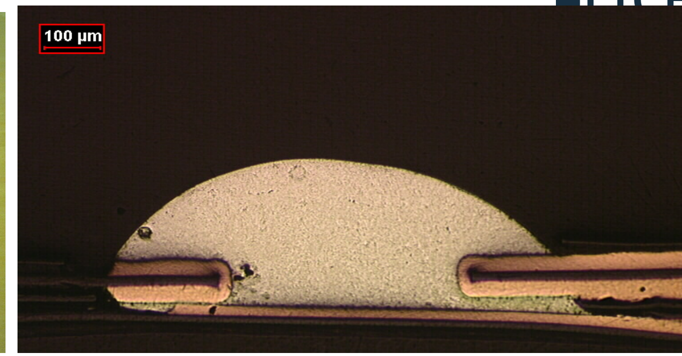


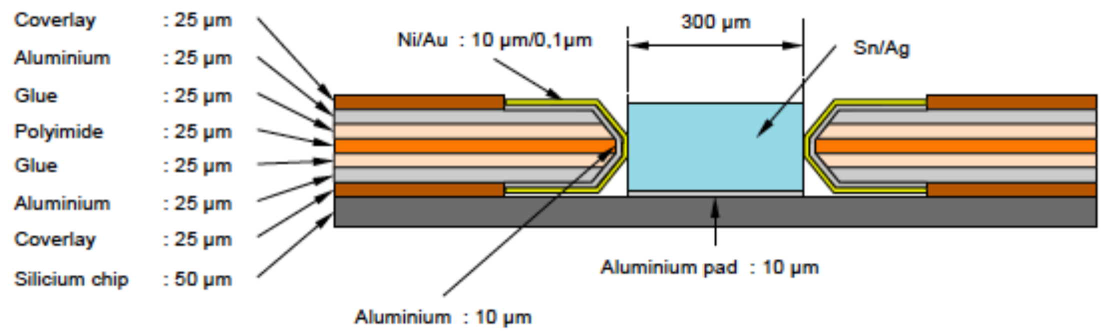
Soldering techniques

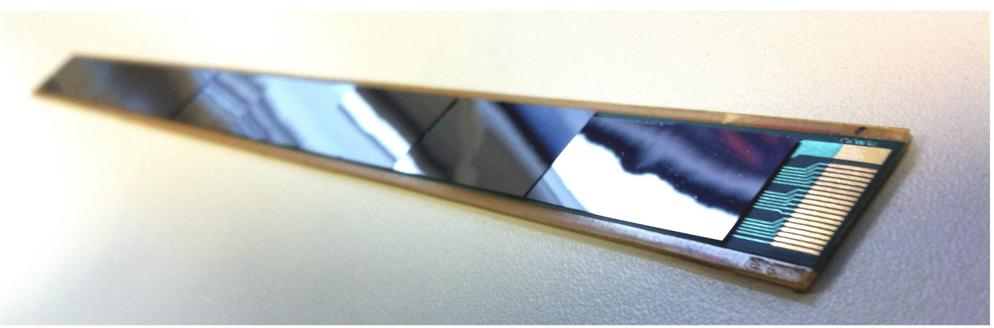
Laser soldering:

- First validation of the technique by soldering kapton-kapton assemblies
- Solder 50 μm silicon die to polyimide foil representing the module PCB
- Tests ongoing with different solder ball sizes









Au-stud:

First dummy module produced using silicon chips (50 um) and a polyimide PCB (27 cm long, 9 chips)

- Au stud bonding using 80 um diameter stud on chip (100 contacts per chip, 400 um diameter pads)
- Bus connected using conductive glue drop (glue polymerized at 80°C)
- Further optimization of the bus layout and study of the polymerization temperature needed

Timeline

- 2012–2014 R&D
  - 2012 evaluation of technologies & prototypes
  - 2013 selection of technologies, eng. Design, TDR
  - 2014 final design and validation
- 2015-18 Construction and Installation
  - 2015-16 production, construction and test of detector modules
  - 2017 assembly and pre-commissioning
  - 2018 installation in the cavern

Summary

The ALICE Inner Tracking System Upgrade will allow to address new physics topics like:

- Quark mass dependence of in-medium energy loss
- Thermalization of heavy quarks in the medium
- Heavy nuclear states production

New Tracker composed of 7 silicon layers characterized by:

- Impact parameter resolution improved by factor 3x
- First detecting layer @22 mm from the beam line
- Material budget x/X_0 ~ 0.3 % in the first layers
- High tracking efficiency down to low p_T (> 95% for pt > 200 MeV/c)
- Fast access for maintenance

Detector technology evaluation ongoing - to be installed during LS2