Status of the tests on the 8x32 *3DTC* chips and preliminary results of the 2012 beam test on *INMAPS*

beam test on INMAPS

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and the 2012 testbeam team

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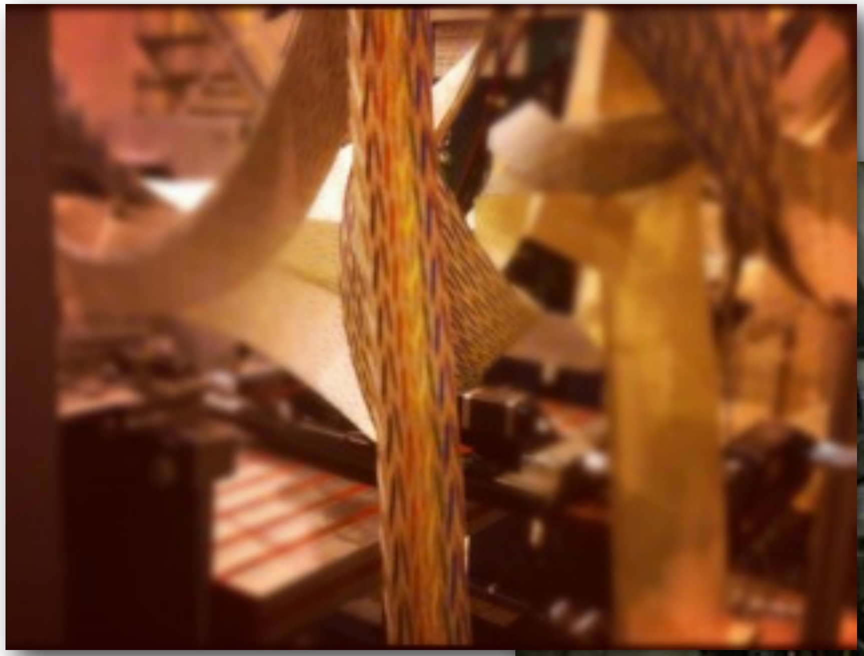
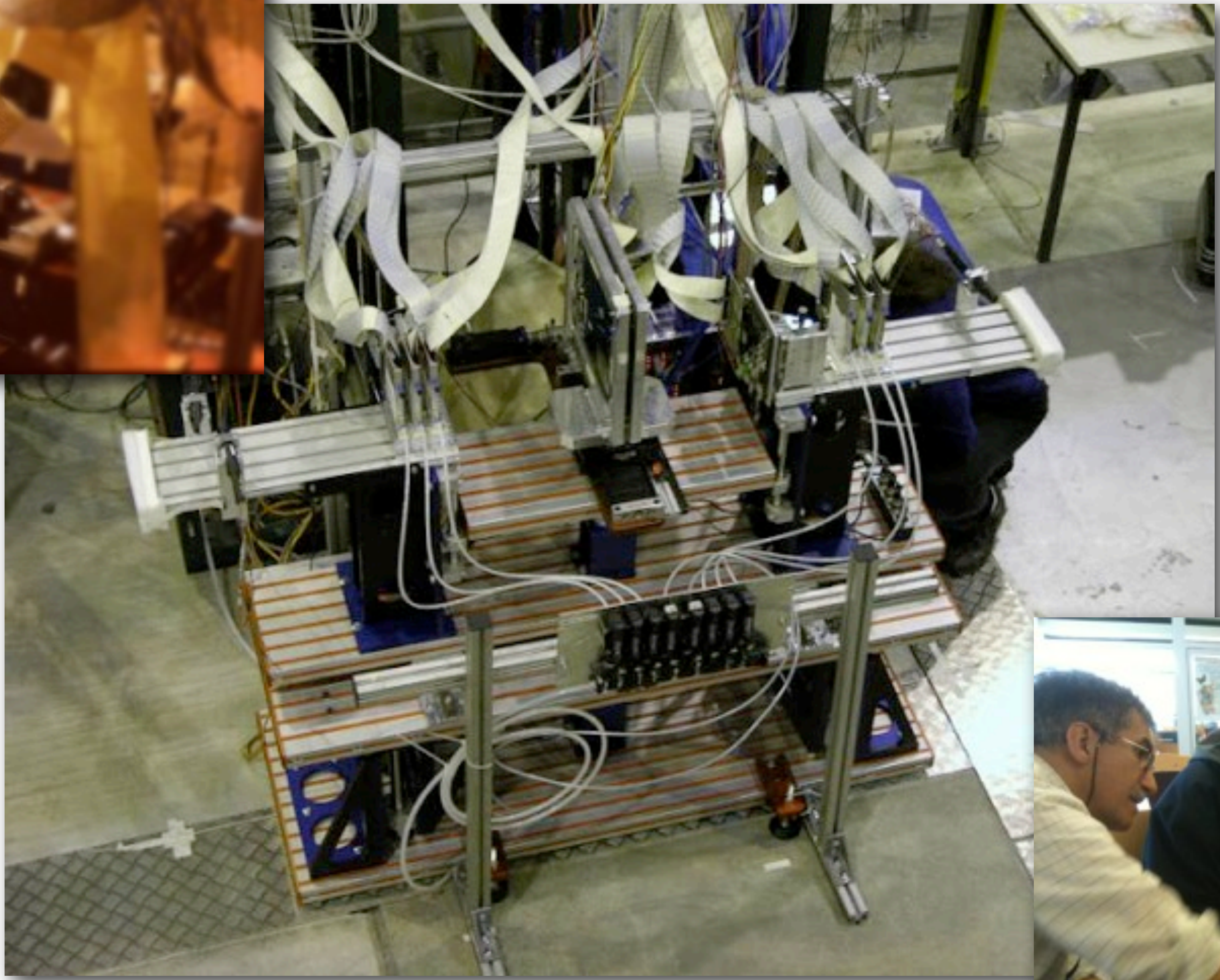
outline

- ➡ CMOS MAPS in 180 nm INMAPS technology: ***Apsel4Well***
  - testbeam results, efficiency vs threshold
  - results of the lab tests on inductions
- ➡ Vertically Integrated DNW MAPS: ***Apsel3D_TC***
  - lab characterizations
  - interconnection of the two layers
  - tests on inductions

NOTE: signal amplitudes in mV are *not corrected* for the buffer scaling factor (0.9)





Apsel4Well

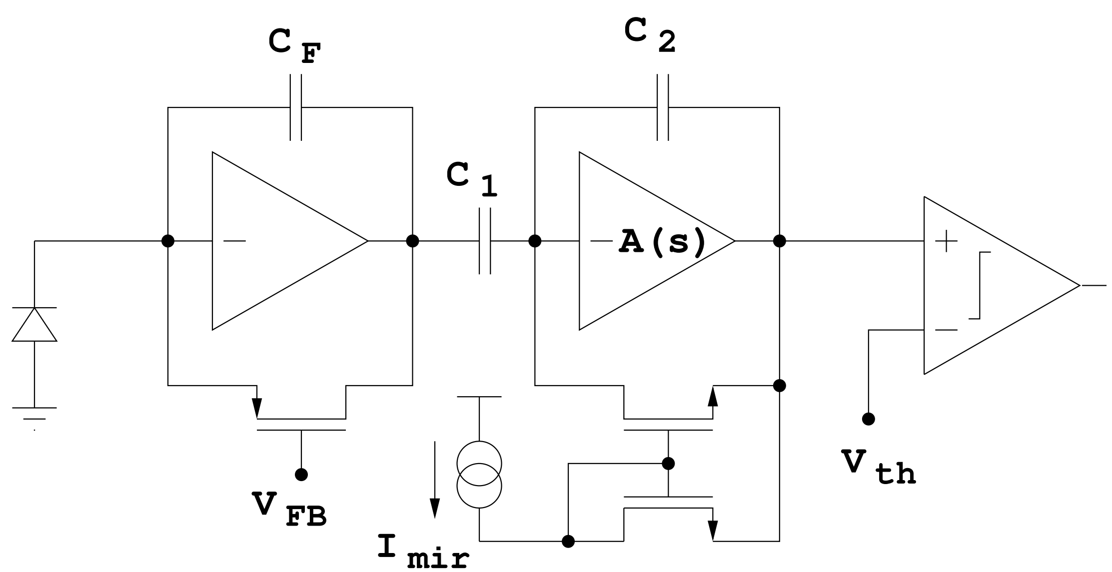
Apsel4Well reminder

- ➡ 32x32 matrix organized in 2x8 macropixels (MP)
  - can mask selected MPs
  - data-push & triggered readout architecture
- ➡ 3x3 analog-only chips
- ➡ thickness: 5 and 12 μm
- ➡ resistivity: standard (10 Ωcm) and high (1 kΩcm)

12μm - highΩ	DAC	mV(*)	e^-
thr. disp.	34	10	80
noise	17	5.1	42
gain (mV/fC)	860(*,c) (diff. spectr. ^{55}Fe)		
gain disp.	5%		
MIP	-	115.5	930
^{55}Fe peak	-	203(c)	1640
S/N	22		

(*)*corrected* for buffer scaling factor (0.9)
(c)central pixel (chip42)

- ➡ block diagram of the pixel analog front-end:



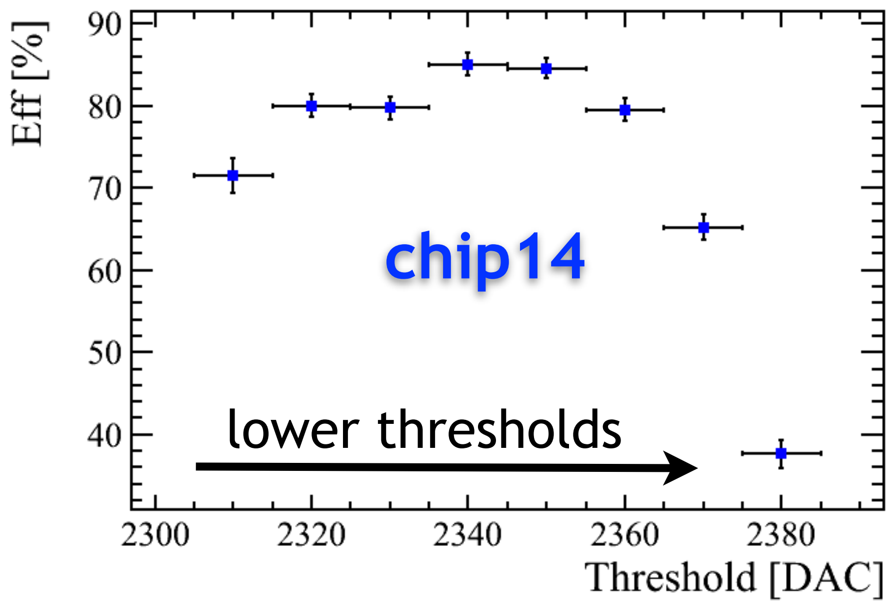
- shaping with a current mirror in the feedback network (V_{rifmir} adjusts discharge time and gain)
- analog output available for pixel (31,31)
- can inject a charge only in pixel 31,31
- the signal is *negative*

Apsel4Well on beam

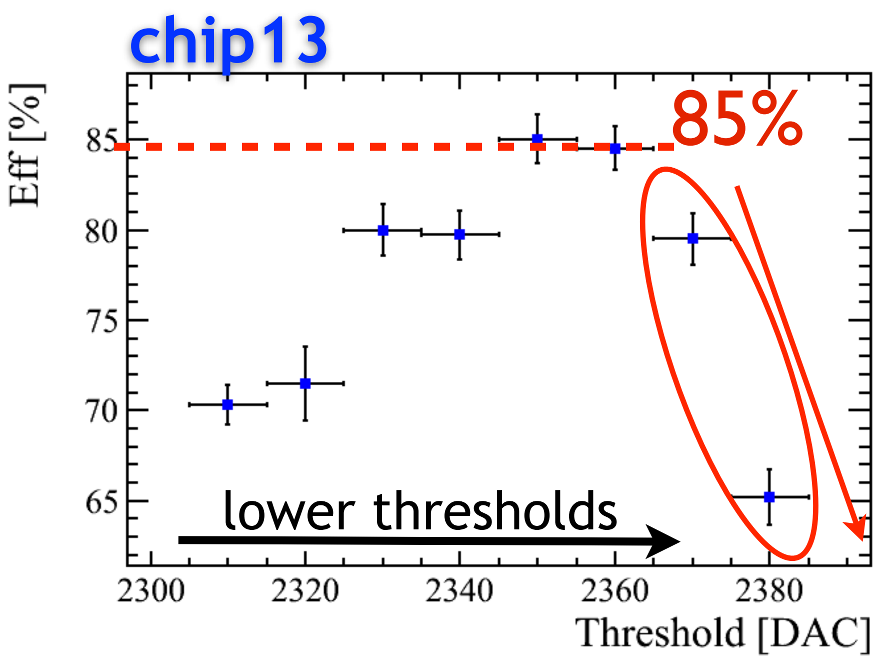
- analog INMAPS and 3 chips 32x32, (hiΩ,12 μm) have been tested with a 120 GeV/c pion beam
  - analog INMPAS results not available yet
  - preliminary results available for digital chips:
    - efficiency vs threshold (DAC)
    - efficiency vs angle
    - resolution
    - resolution vs angle
    - lattice & pixel isotropy (still convolved with telescope resolution)

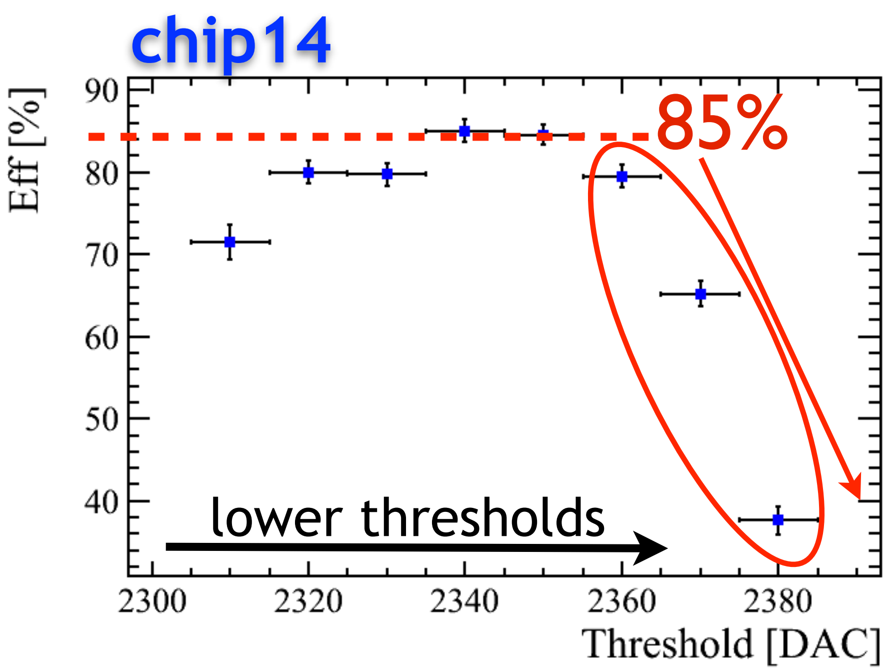
presented at the SuperB General Meeting in December

- The main issue with this chips is related to the low maximum efficiency reached and its deterioration at low thresholds:
  - current explanation: inductions effects



Efficiency vs Threshold



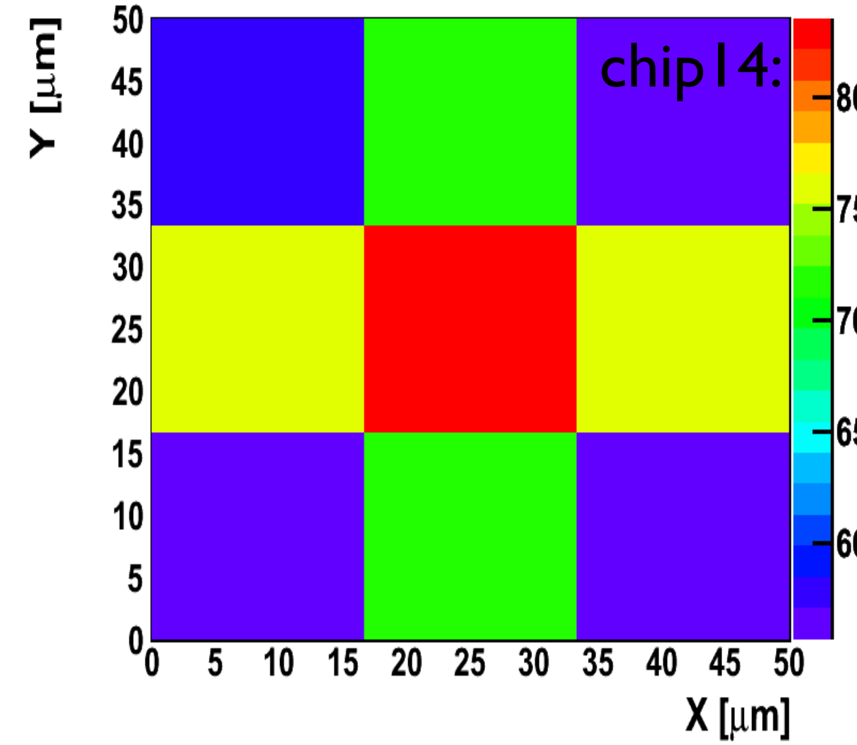


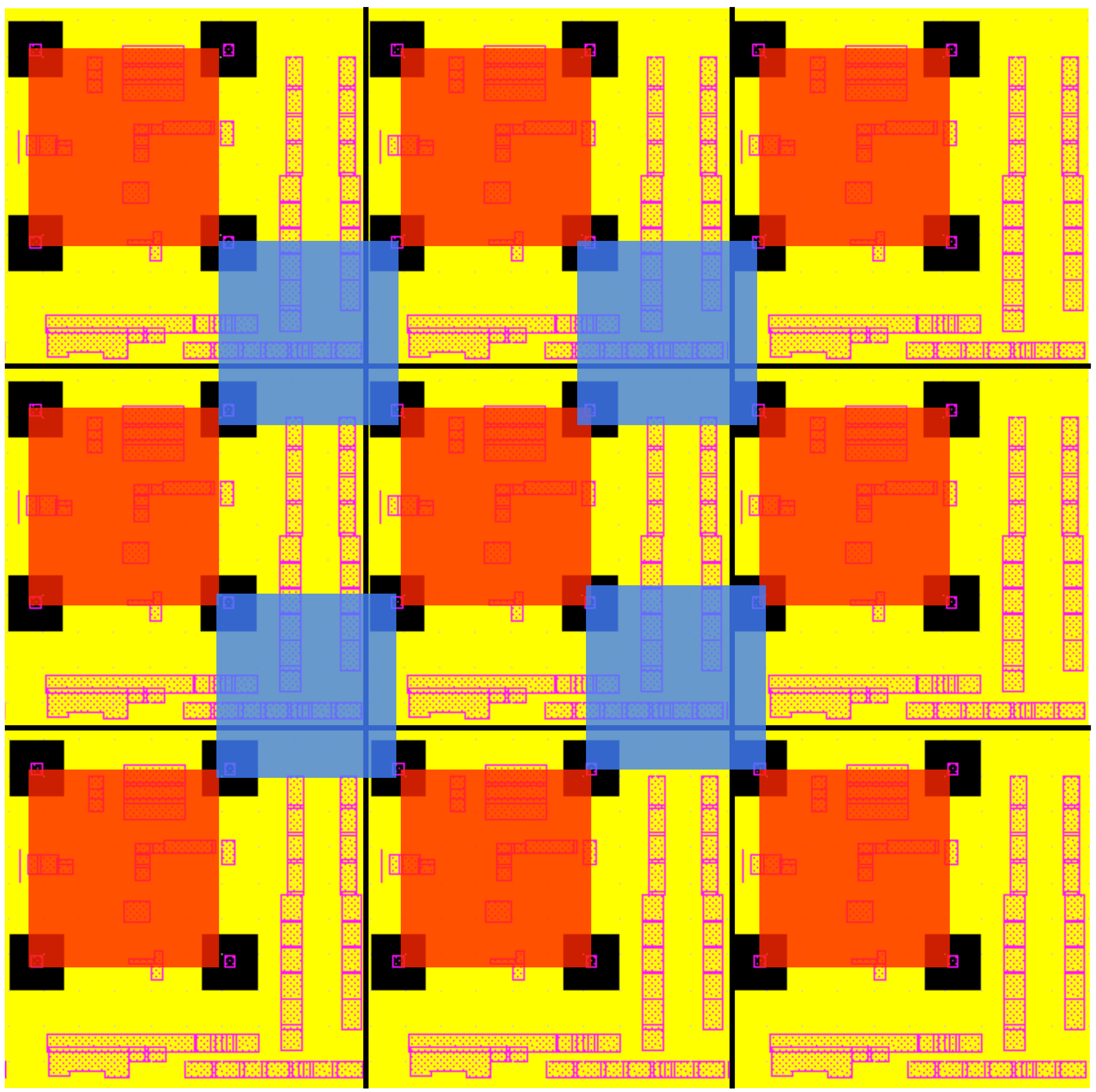
- ε_{max} ~ 85% (@ 2360 DAC ~ 300e$^-$), deterioration at lower thresholds.
- possible answers:
  - inefficiency due to the fact that the pixel is already fired (on noise, or other...): excluded (v. bkp slide 20)
  - inefficiency due to **induction effects** (positive induction related to digital activity masks negative signal from particles)
  - *other effects* that may be related to the low maximum efficiency: charge sharing (v. next slide and 27) and too high threshold (v. bkp slide 28)

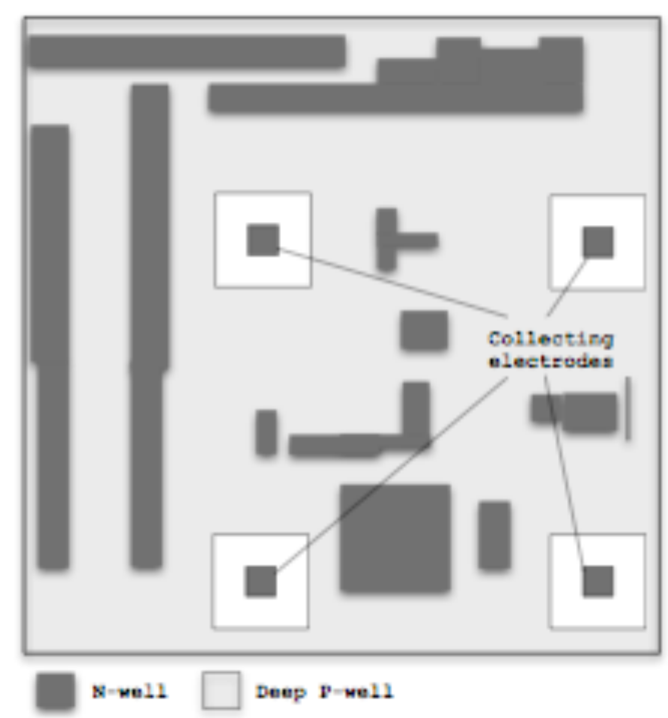
Efficiency Within Pixel

➡ Low efficiency regions: the released charge is shared among more than 1 pixel and not enough to go below threshold.

in-pixel efficiency (still convolved with telescope efficiency):

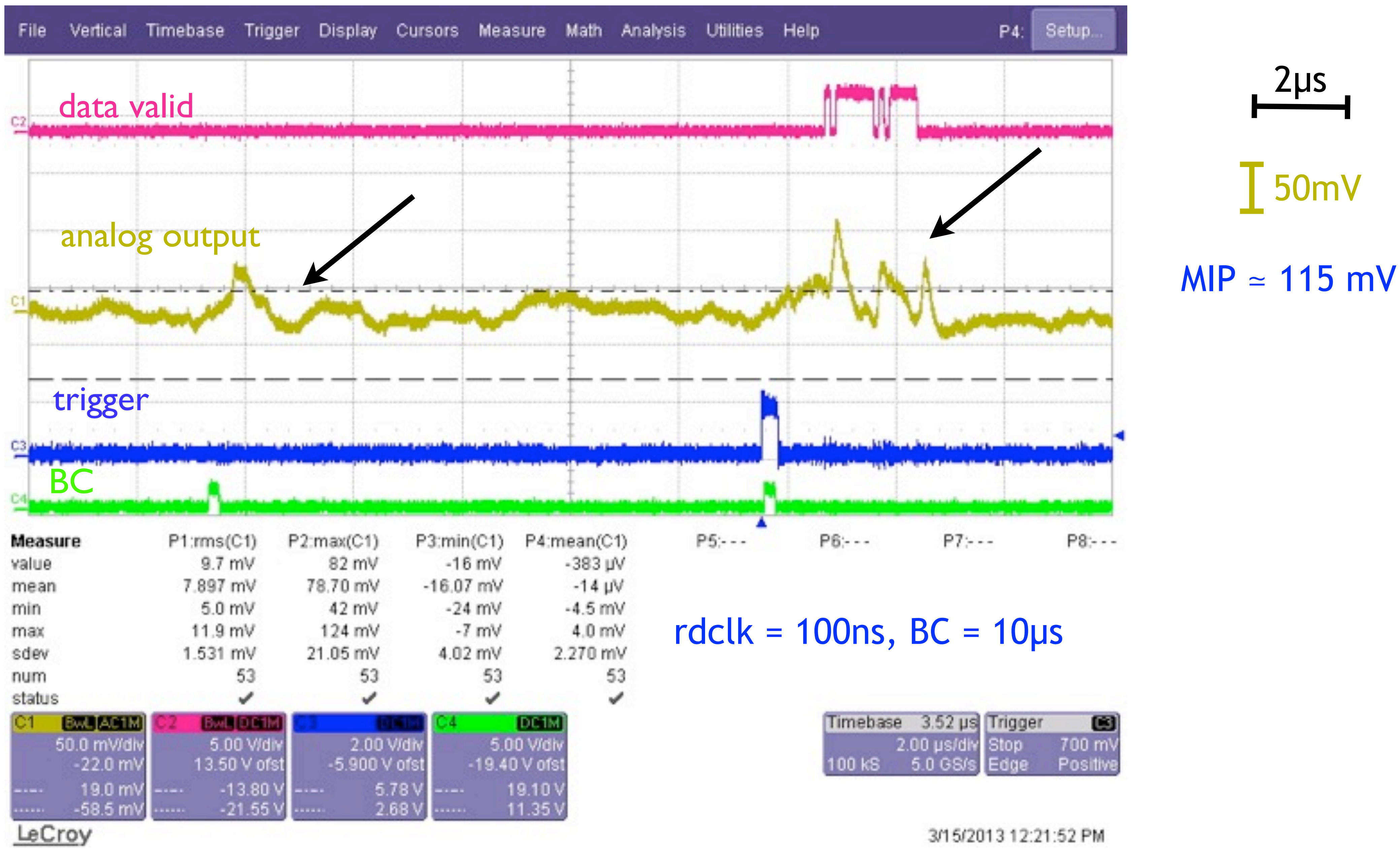






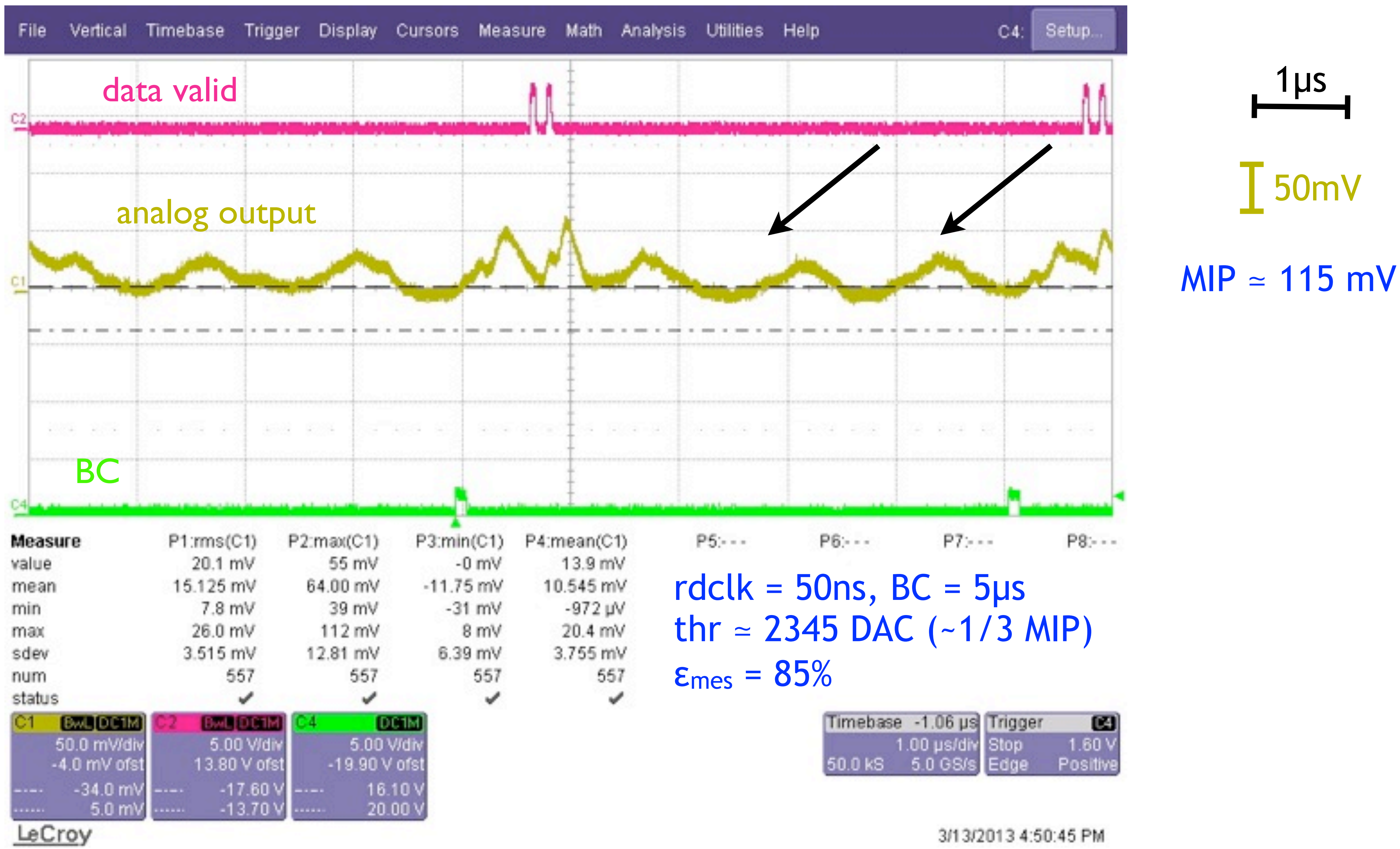
Induction Effect #1

1. When a timestamp or a hit is readout we observe **big positive spikes** on the analog output (50 - 100mV). Also in correspondence of some BCs, signals going towards the matrix (TS update) induce **positive and negative spikes**



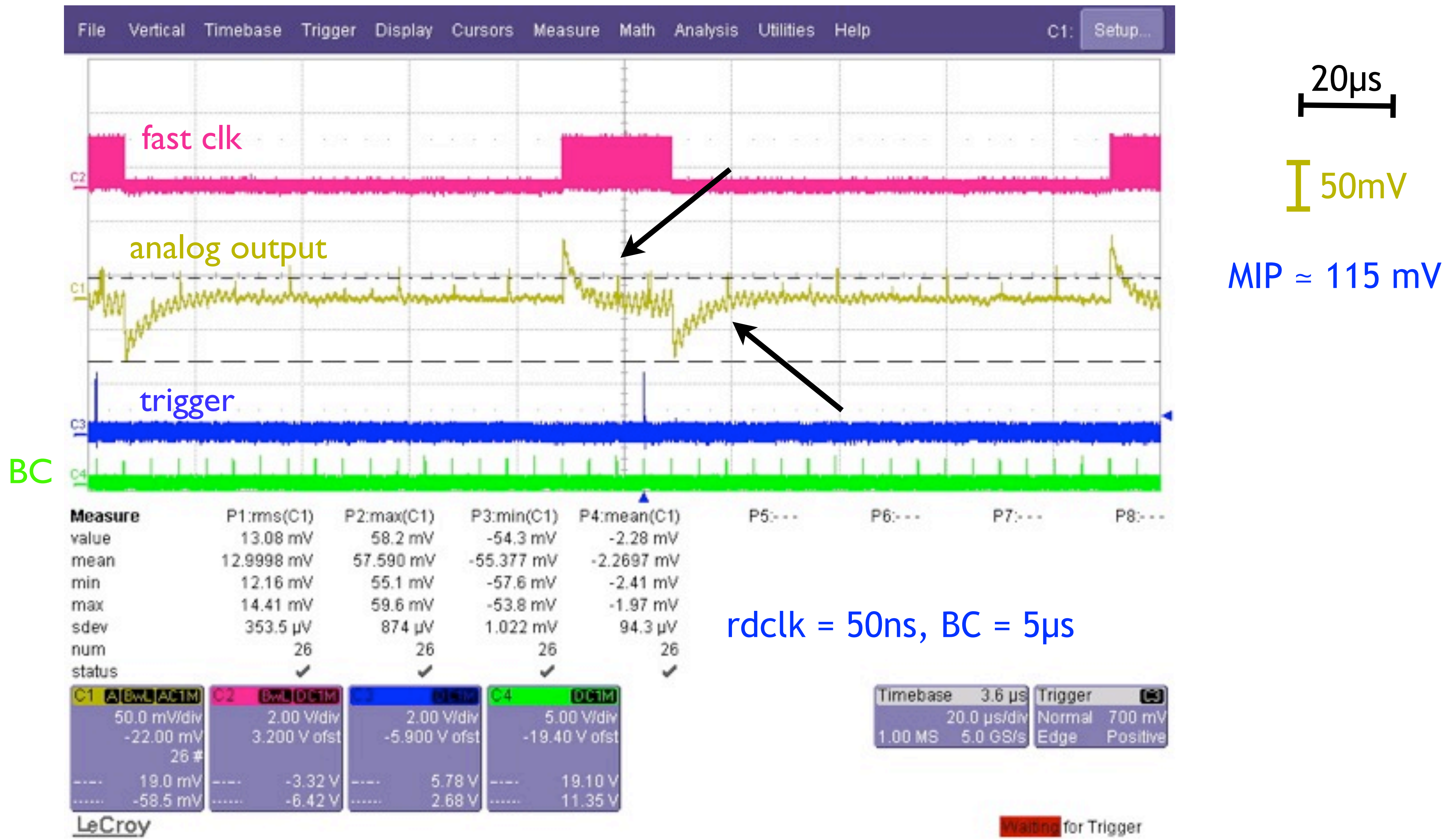
Inductions Effect #2

2. When rdclk/fastclk > 20MHz (50ns) we observe an **oscillation** independent of the BC period present only if fastclk is active (due to activity in the periphery).



Induction Effect #3

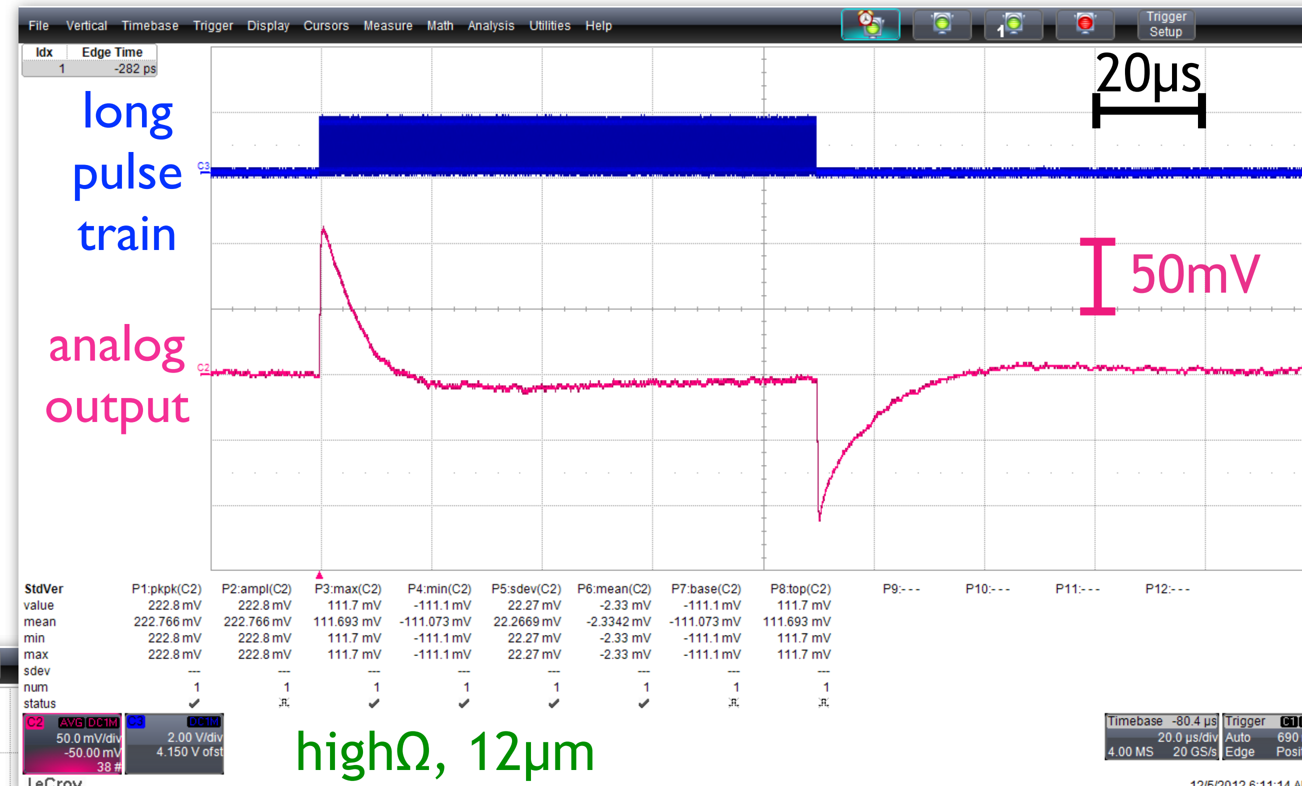
3. We observe **big** (50 - 100 mV) **positive (negative) spikes** when fastclk starts (ends) in the periphery. The superimposed **oscillation** is present only if fastclk > 20MHz and is attenuated in ~ 30 μs.

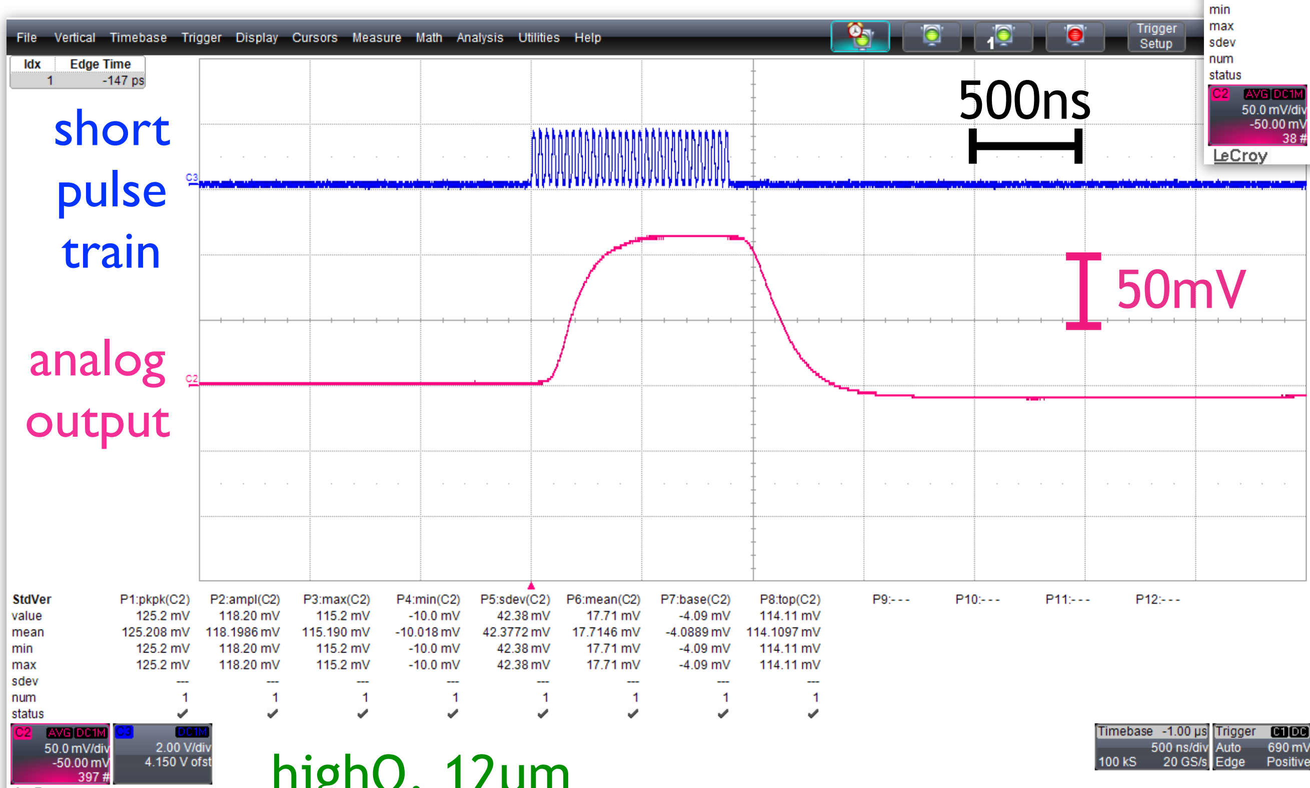


Tests on Analog 3x3 Matrices

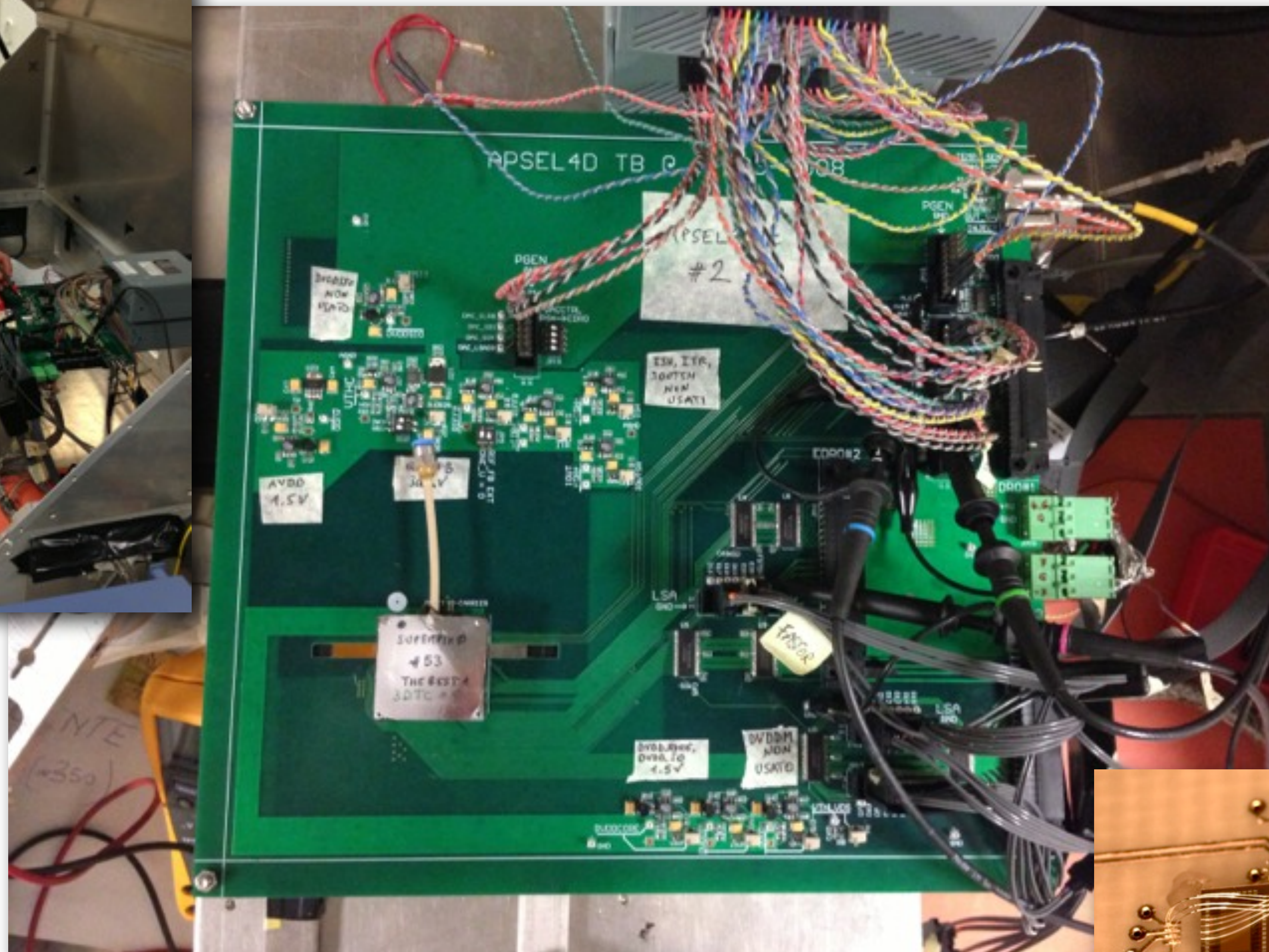
➡ Tests on a 3x3 analog matrix show similar effects when digital signals run on the chip.

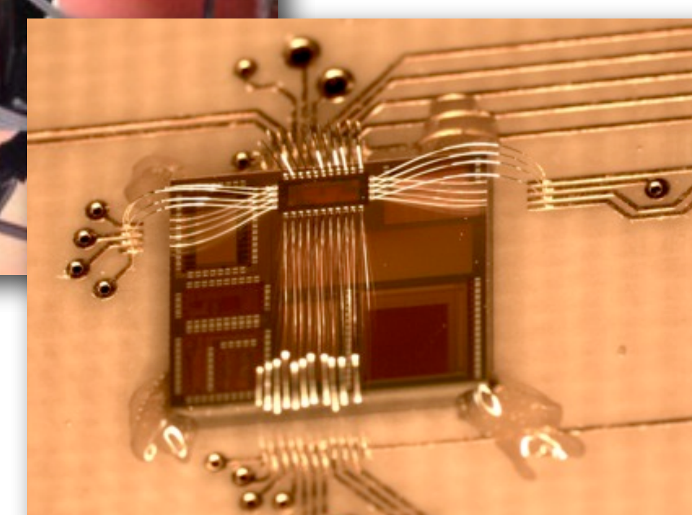
- positive pulse triggered by the start of the train and sensitive to the frequency of pulses
- negative pulse, same amplitude as the positive one, triggered by the interruption of the pulses
- when train is shorter, the two pulses merge





1. maximum effect obtained with pulse train period of 25 - 30 ns
2. level of induction is ~proportional to the amplitude of the pulse train
3. the effect is independent of the stimulated track
4. the effect in some lowΩ chips seems smaller





Apsel3D_TC

Apsel3D_TC reminder

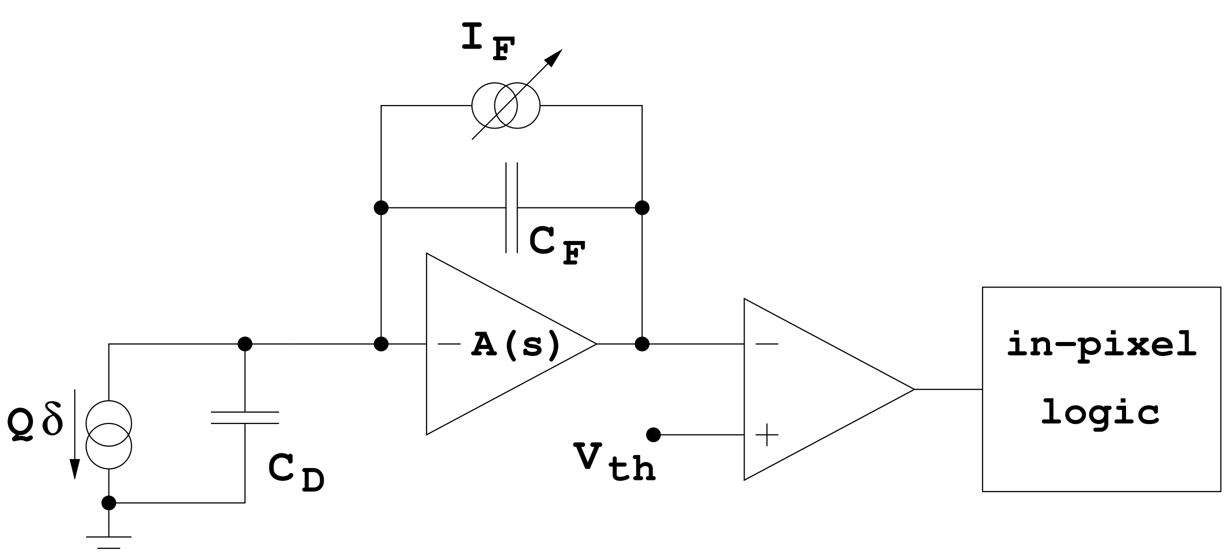
➡ 8x32 matrix organized in 4x4 macropixels (MP)

- can mask selected MPs
- data-push readout architecture

➡ 3x3 analog-tier only chips

	DAC	mV	e-
thr disp	11-14	3.4 - 4.3	80 - 90
noise	5.4 - 6.2	1.7 - 1.9	40
gain (mV/fC)	290 (digital)		320 (analog)
gain disp.	**20%**		
MIP	-	40	1000
^{55}Fe peak	-	80	
S/N	23		

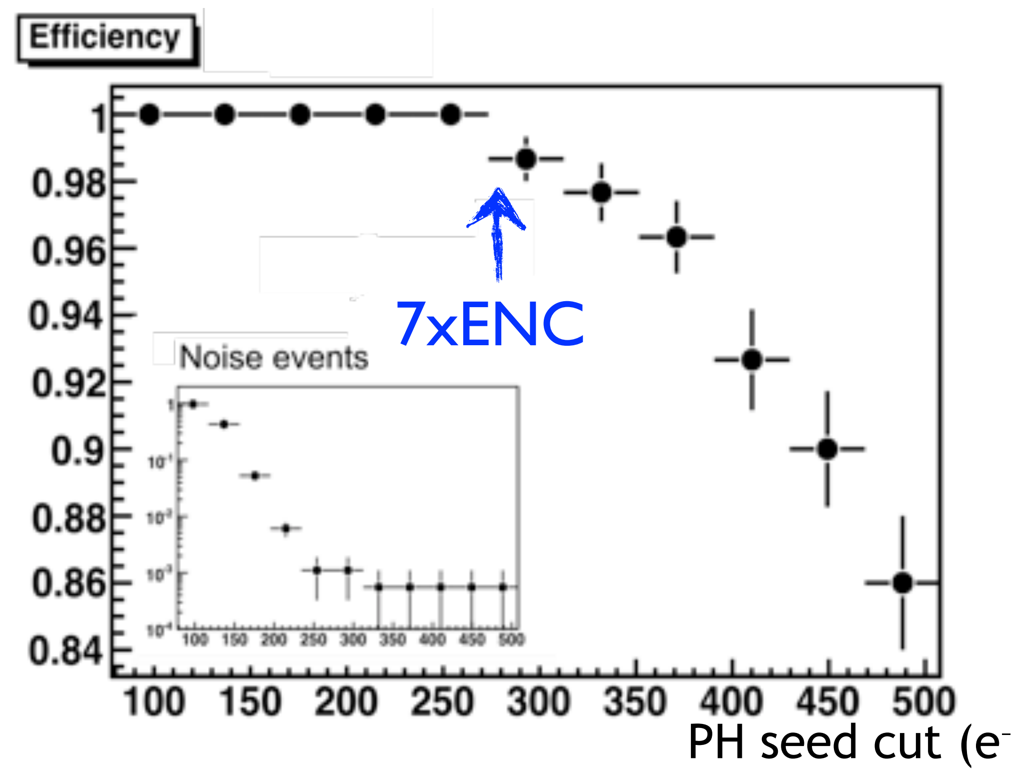
➡ block diagram of the pixel analog front-end:



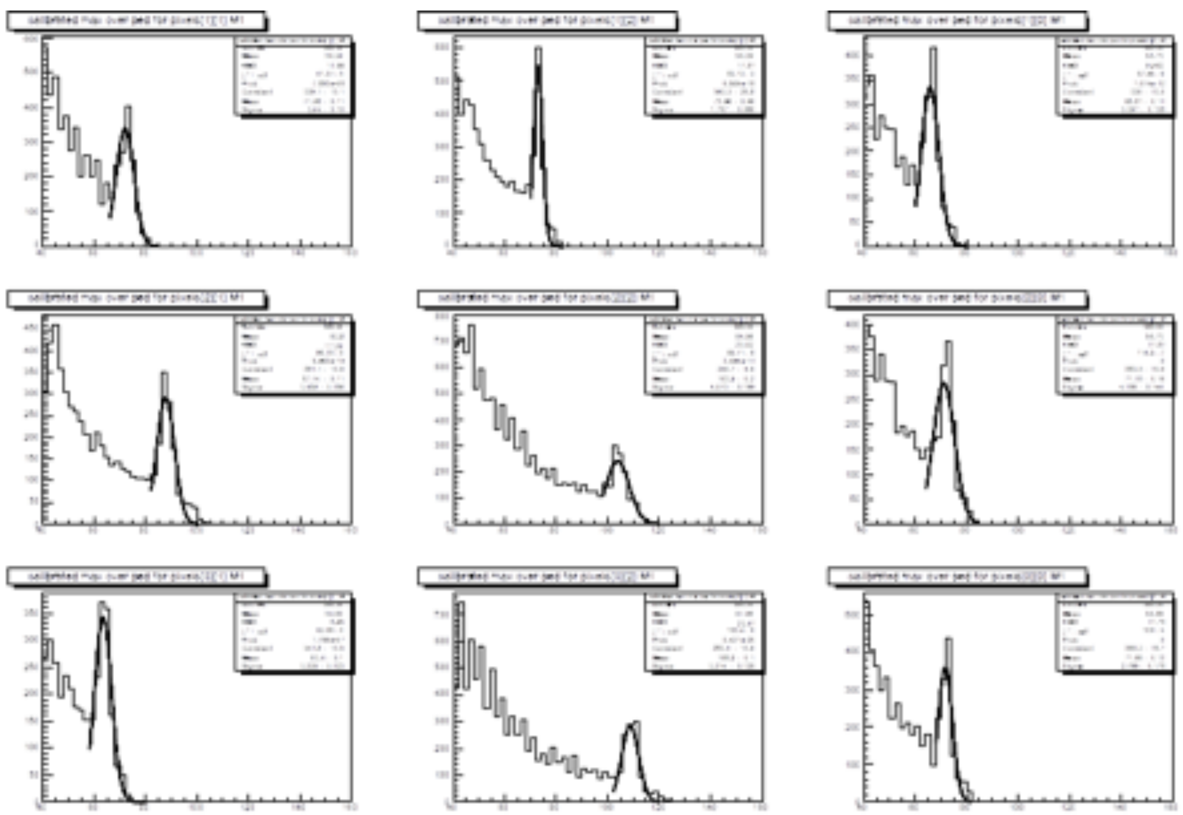
- bandwidth-limited preamplifier to improve signal-to-noise
- analog output available for pixel (31,7)
- can not inject a charge
- the signal is *positive*

Apsel3D_TC – analog-tier only

- tested on beam (2011):
  - 3x3 cluster signal MPV ≃ 1000 e-
  - S/N ≃ 23
  - efficiency ≃ 98% at thresholds up to 7xENC



differential spectrum of the 3x3 pixels (^{55}Fe):



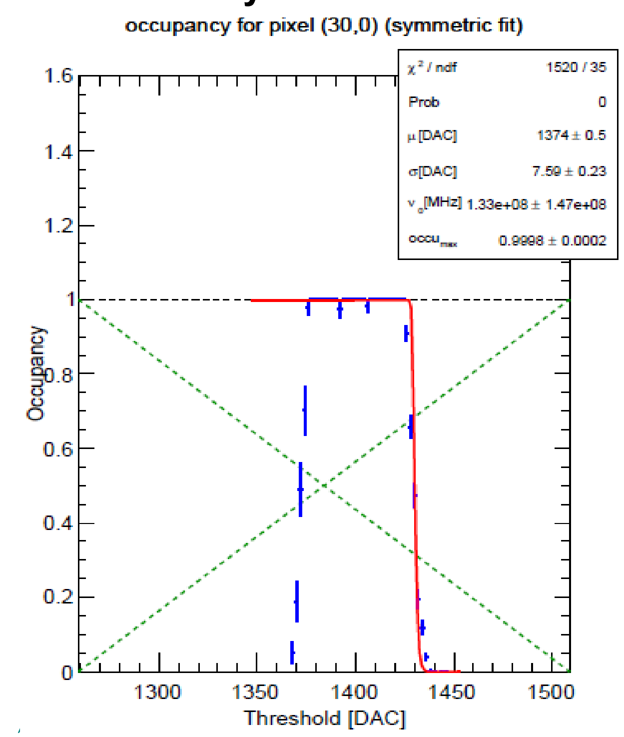
- tested with a ^{55}Fe source:
  - 5.9 keV γ, 1640 e- ≃ 2xMIP
  - measured gain ≃ 320 mV/fC (half the expected value) and quite dispersed
    - feedback capacitance of the preamplifier realized exploiting parasitic capacitance of two tracks
    - value estimated from post-layout simulations: not reliable (→ low gain) and quite dispersed (→ dispersed gain)

Apsel3D_TC calibrations

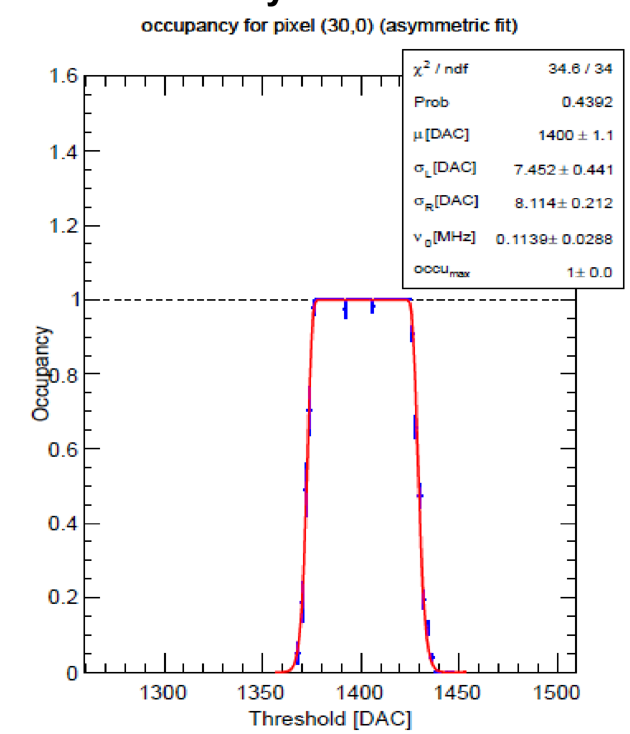
- Noise Scans:
  - need to fit with *asymmetric* function
    - $\sigma_L \simeq 85\% \sigma_R$, $\sigma_R \simeq 1.7 - 1.9$ mV
    - $\sigma_R \sim$ in agreement with what seen on the analog output of pixel (31,7)
  - limited threshold dispersion
    - 3.4 - 4.2 mV (~2.5xσ_R)

something asymmetric in the circuit? comparator?

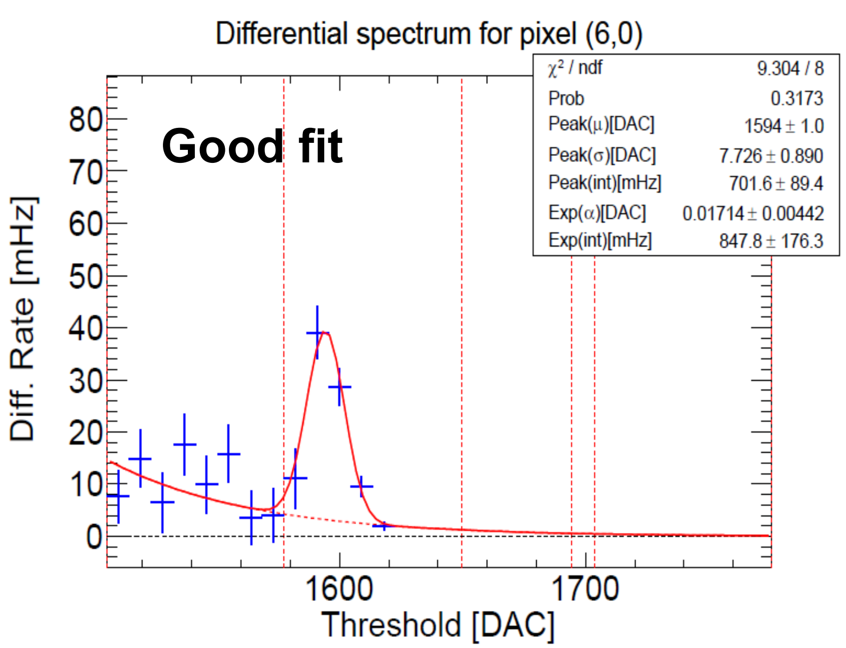
Symmetric fit

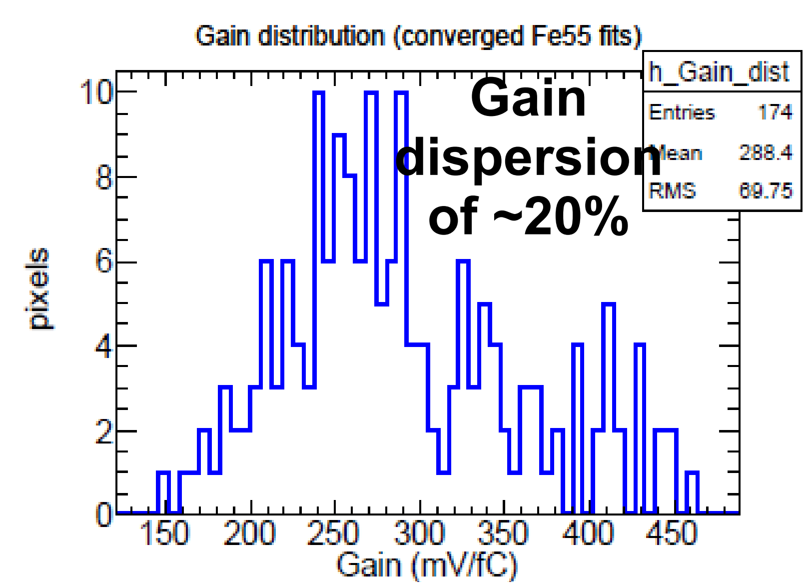


Asymmetric fit



- Gain Calibrations with ^{55}Fe (1640 e- ≃ 2xMIP), differentiated digital scan:
  - central value ≃ 285 mV/fC, very large dispersion, o(20%) (even within a MP)





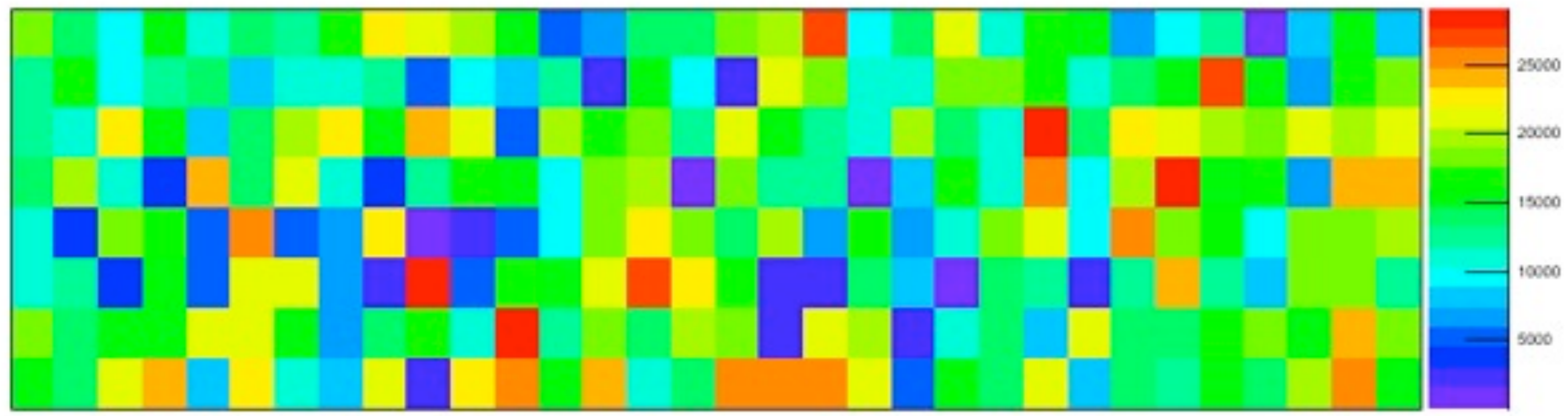
- difficult to pilot with a single threshold → 8x32 digital matrices *not* tested on beams

Interconnected Chips

➡ response of the digital 8x32 devices to a ^{55}Fe source:

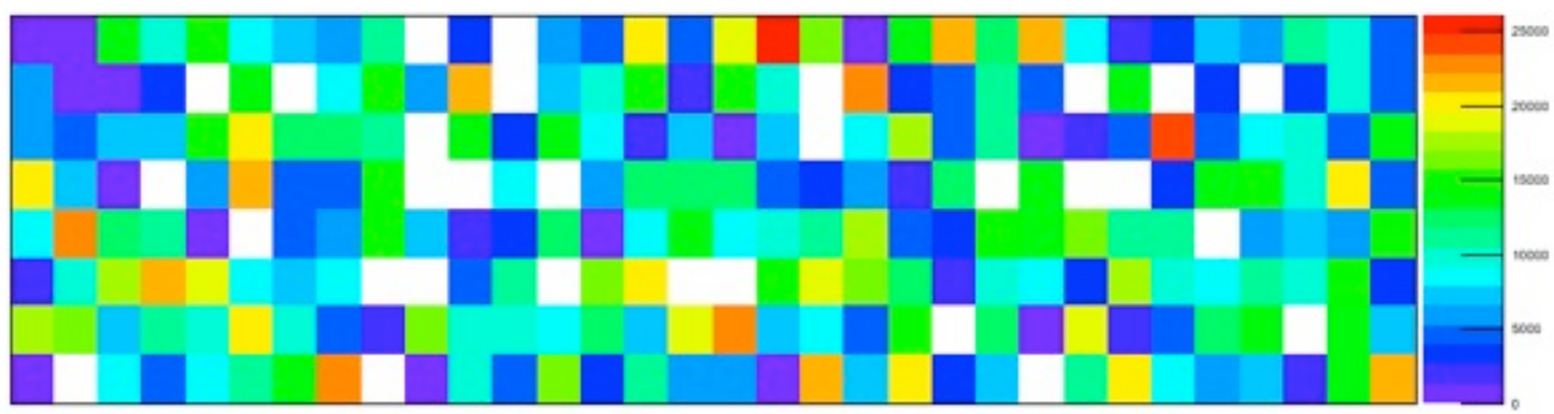
chip5:

all pixels are interconnected!



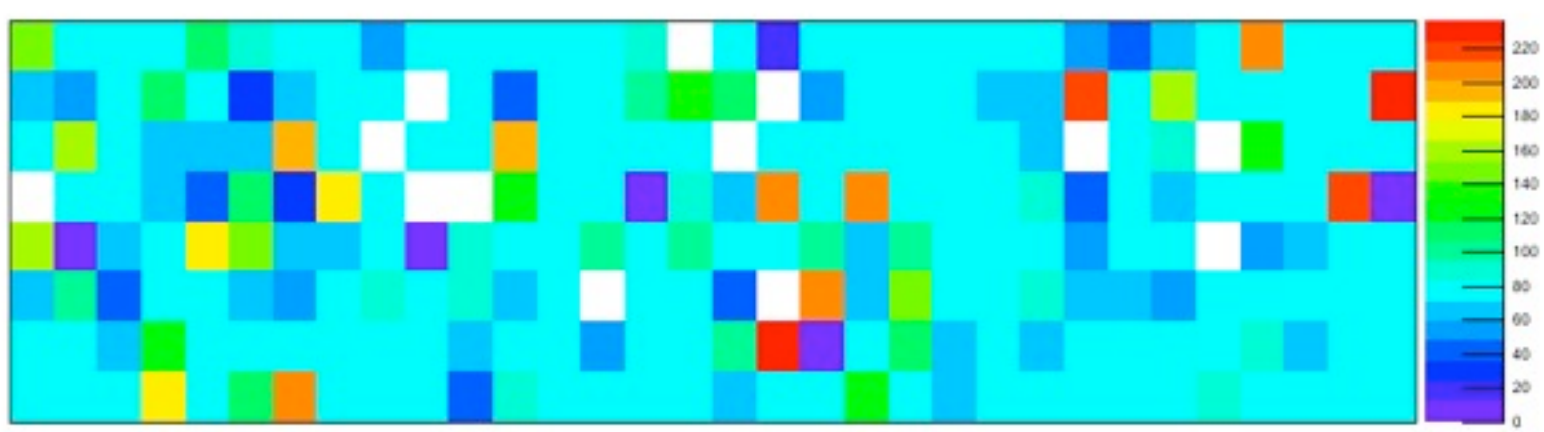
chip6:

30 failures (12%)



chip7:

13 failures (5%)



Tests on Inductions

➡ No significant inductions visible at the analog output of pixel (31,7):

tested at very high clk rates:

- rdclk = 50 MHz (20ns)
- BC ≃ 2.5 μs
- checked that pixels beloning to the same MP as pixel 31,7 are fired

readout running:

data valid

MLE

analog output

BC

- small induction, order of the noise (2 mV) due to the clk, on chip? testboard?
- 1/4 MIP (10mV) ≃ 5 x noise
- safe operations

2μs

5mV

MIP ≃ 40 mV

Tests on Inductions

➡ No significant inductions visible at the analog output of pixel (31,7):

tested at very high clk rates:

- rdclk = 50 MHz (20ns)
- BC ≃ 2.5 μs
- checked that pixels belonging to the same MP as pixel 31,7 are fired

no readout:

- small induction, order of the noise (2 mV) due to the clk, on chip? testboard?
- 1/4 MIP (10mV) ≃ 5 x noise
- safe operations

MIP ≃ 40 mV

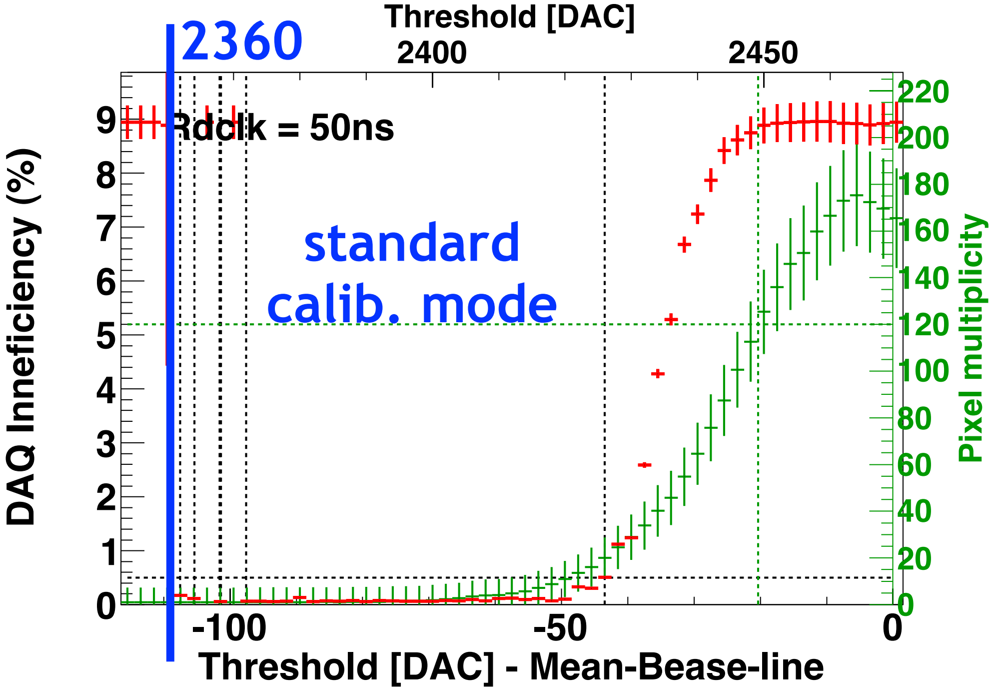
Conclusions

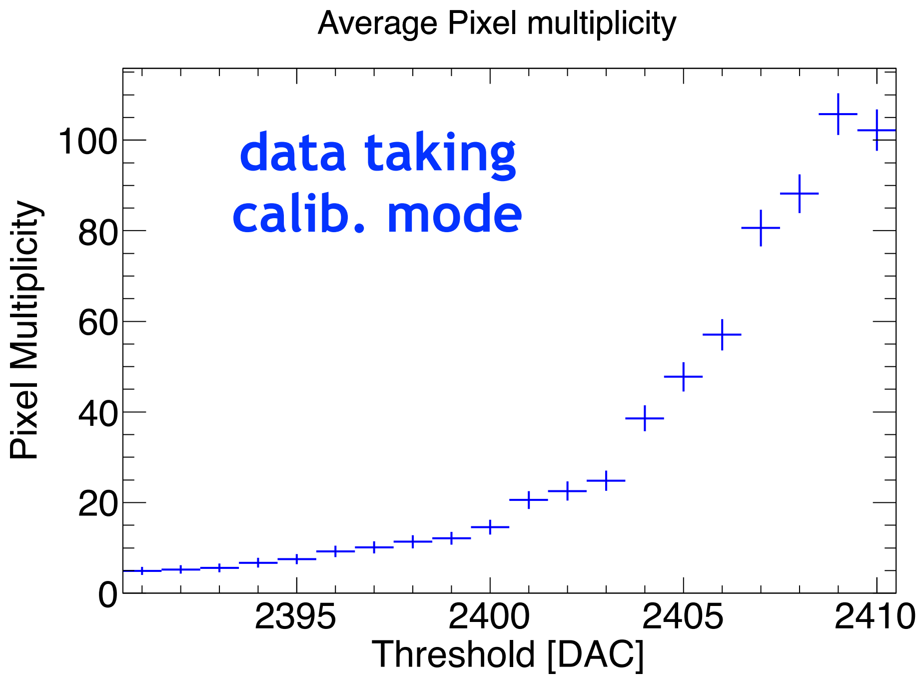
- Apsel4Well:
  - serious induction effects deteriorate the performance of high resistivity devices, less pronounced on low res ones
  - need to understand the cause of the observed induction
  - other effects (as charge sharing) may also play a role to explain the low maximum efficiency
- Apsel3D_TC:
  - promising results from analog devices: 98% efficiency
  - 3 working interconnected chips
  - large gain dispersion prevented the test with beams
  - no significant induction

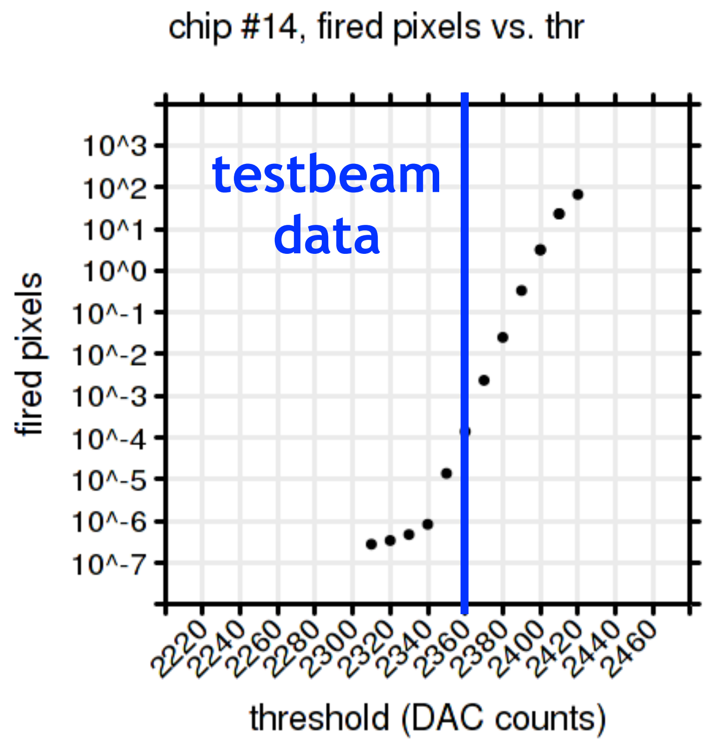
Additional Slides

Apsel4Well: Pixel Multiplicity

- pixel multiplicity in standard calibration is smaller than 1:
  - too low to cause inefficiency
  - test also in data-taking mode (pixels are enabled all the time, no observation windows)
- pixel multiplicity in data-taking mode:
  - confirm testbeam observations
  - still too low to cause observed inefficiency

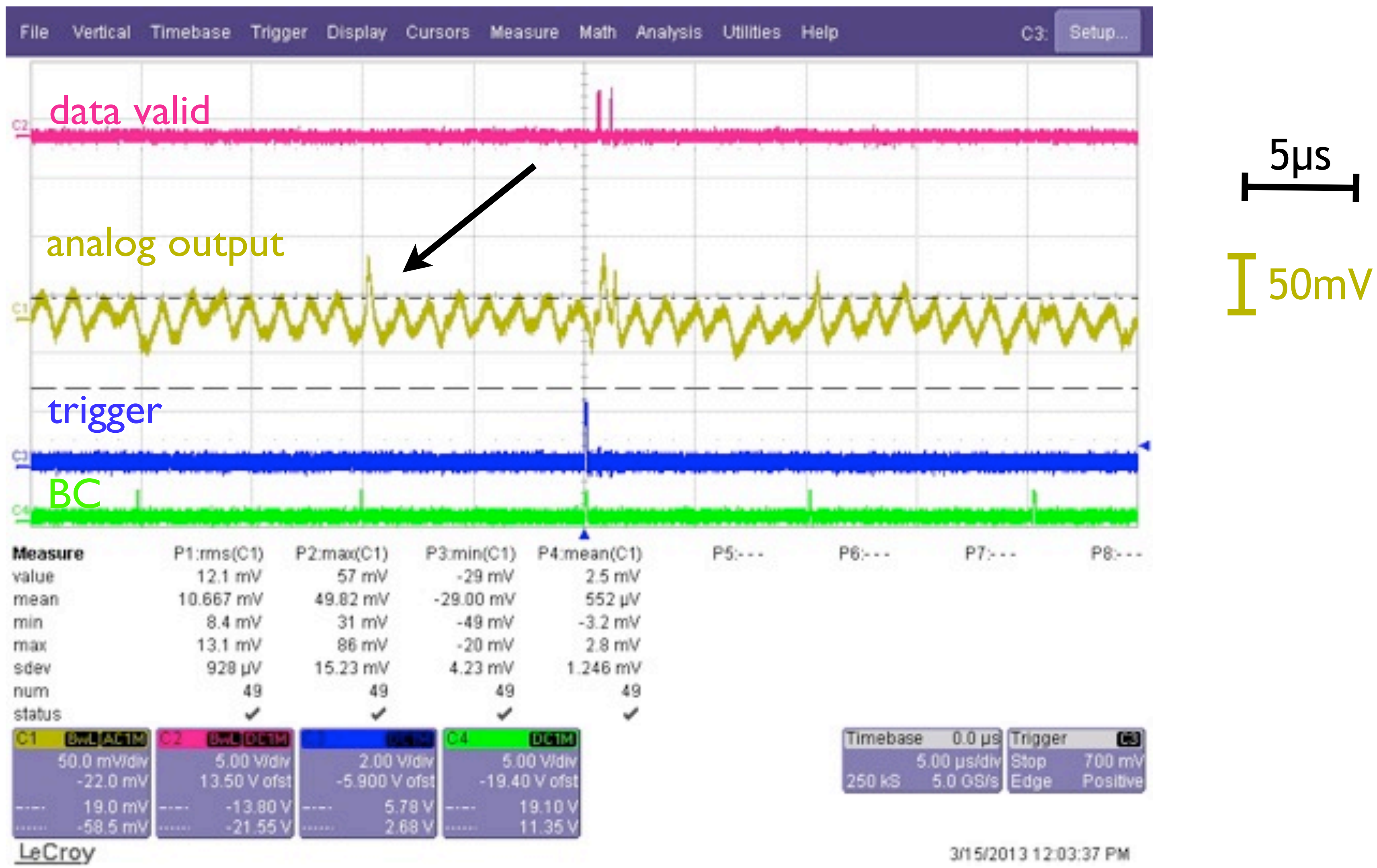






Apsel4Well Inductions: oscillation

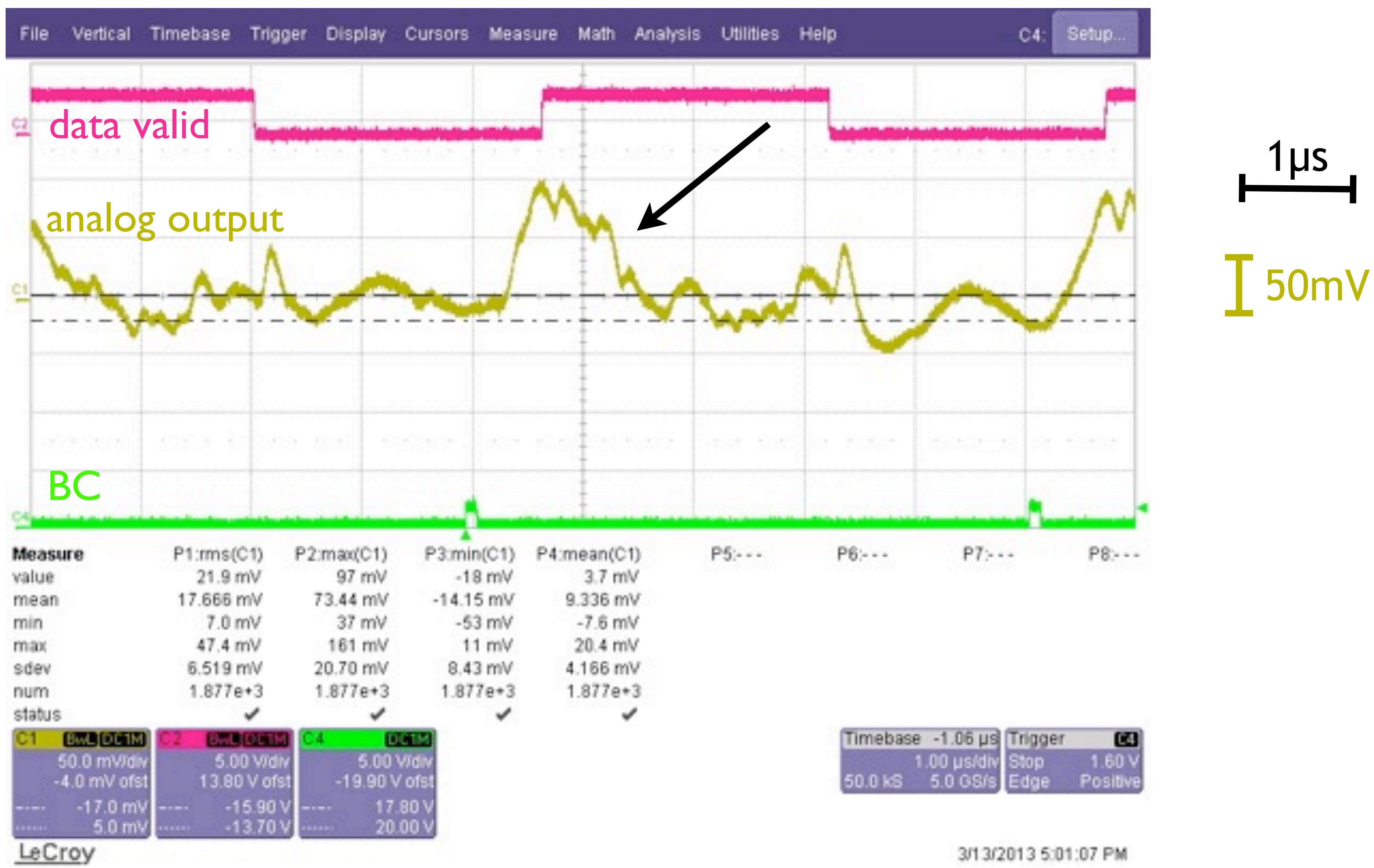
- ➡ when rdclk is fasten to 50ns, an oscillation appears
  - period ~1.5μs, ampl ~ 20 mV



note: MIP ≃ 115 mV

data-push mode, thr ≃ 2400 DAC

- ➡ positive induction (~ 100mV) covers a non-negligible fraction of the time between two BCs: if a MIP hits the pixel in this time, the signal doesn't cross the threshold → inefficiency!

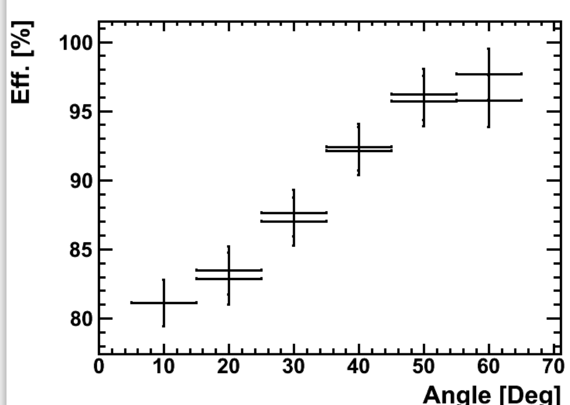


note: MIP ≃ 115 mV

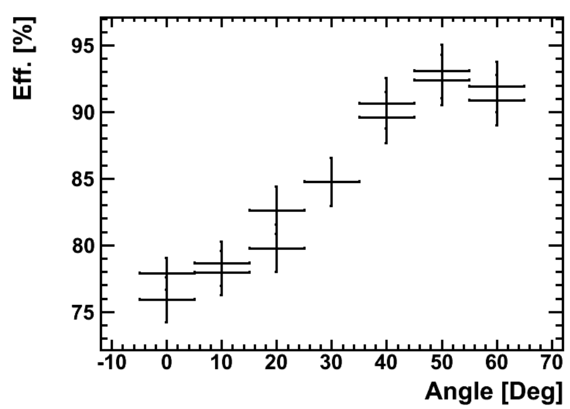
Apsel4Well: angle dependence

Eff vs. angle

CHIP 13



CHIP 14



THRESHOLD: 2360 $\rightarrow$ $280e \pm 5\%$

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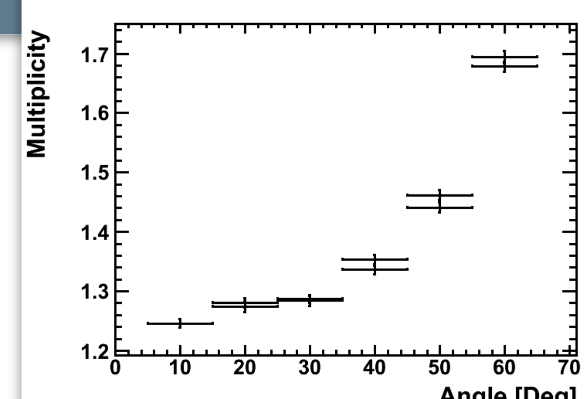
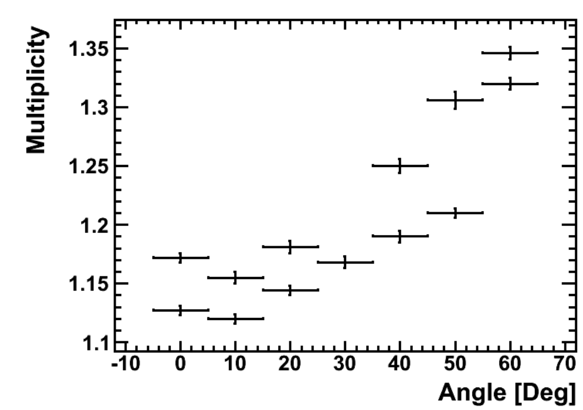
presented at the SuperB General Meeting in December

Multiplicity vs angle

CHIP 13



CHIP 14



THRESHOLD: 2360

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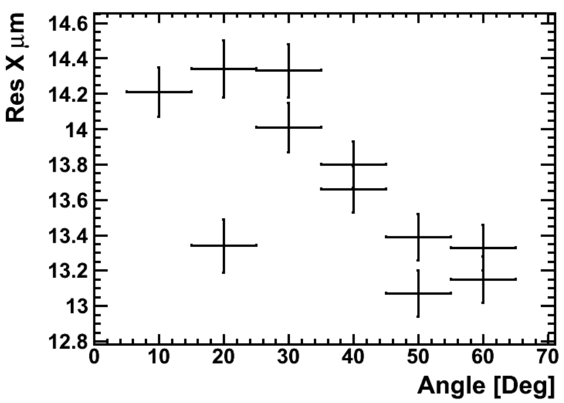
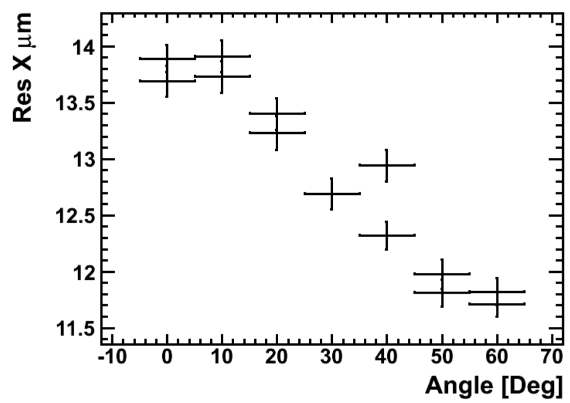
Apsel4Well: resolution

Resolution X vs angle

CHIP 13



CHIP 14



THRESHOLD: 2360

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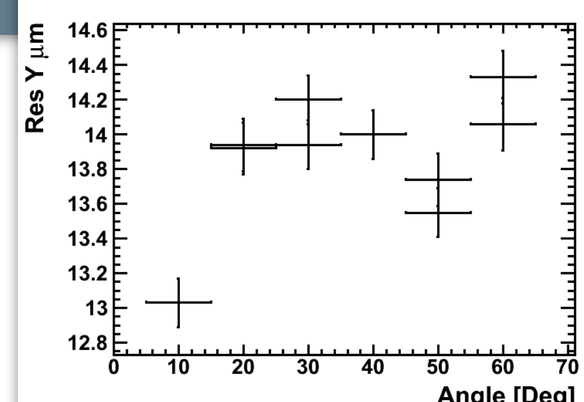
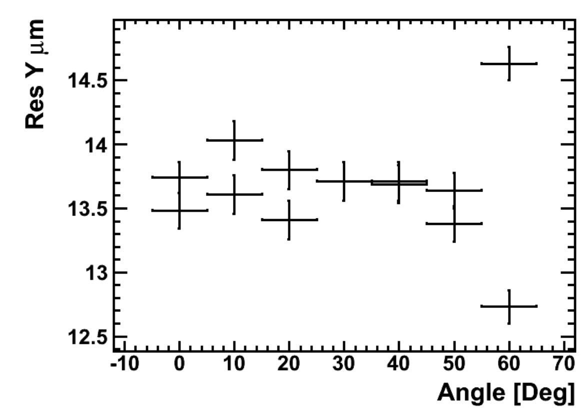
presented at the SuperB General Meeting in December

Resolution Y vs angle

CHIP 13



CHIP 14



THRESHOLD: 2360

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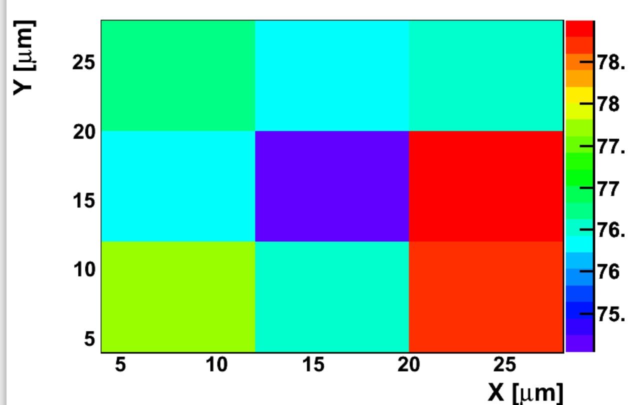
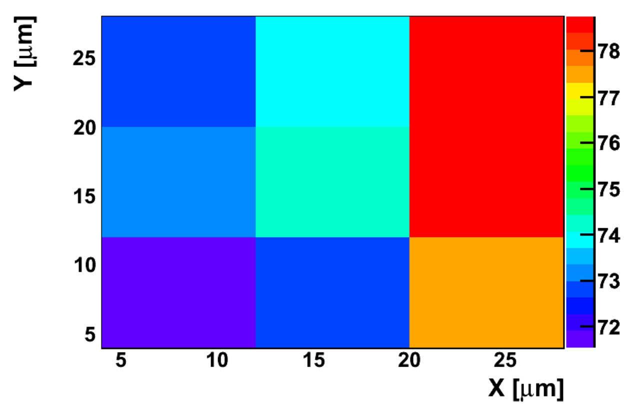
Apsel4Well: lattice & pixel isotropy

Lattice isotropy

CHIP 13



CHIP 14



THRESHOLD: 2360

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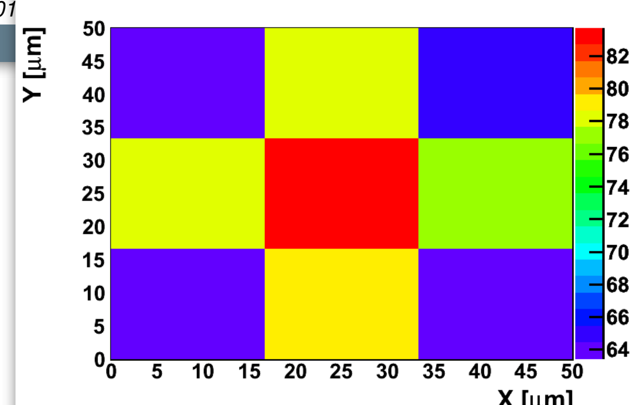
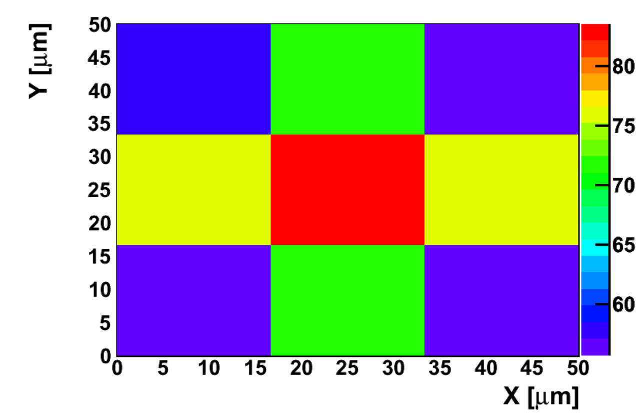
Pixel isotropy

CHIP 13



CHIP 14



Before deconvolution the telescope resolution!
THRESHOLD: 2360

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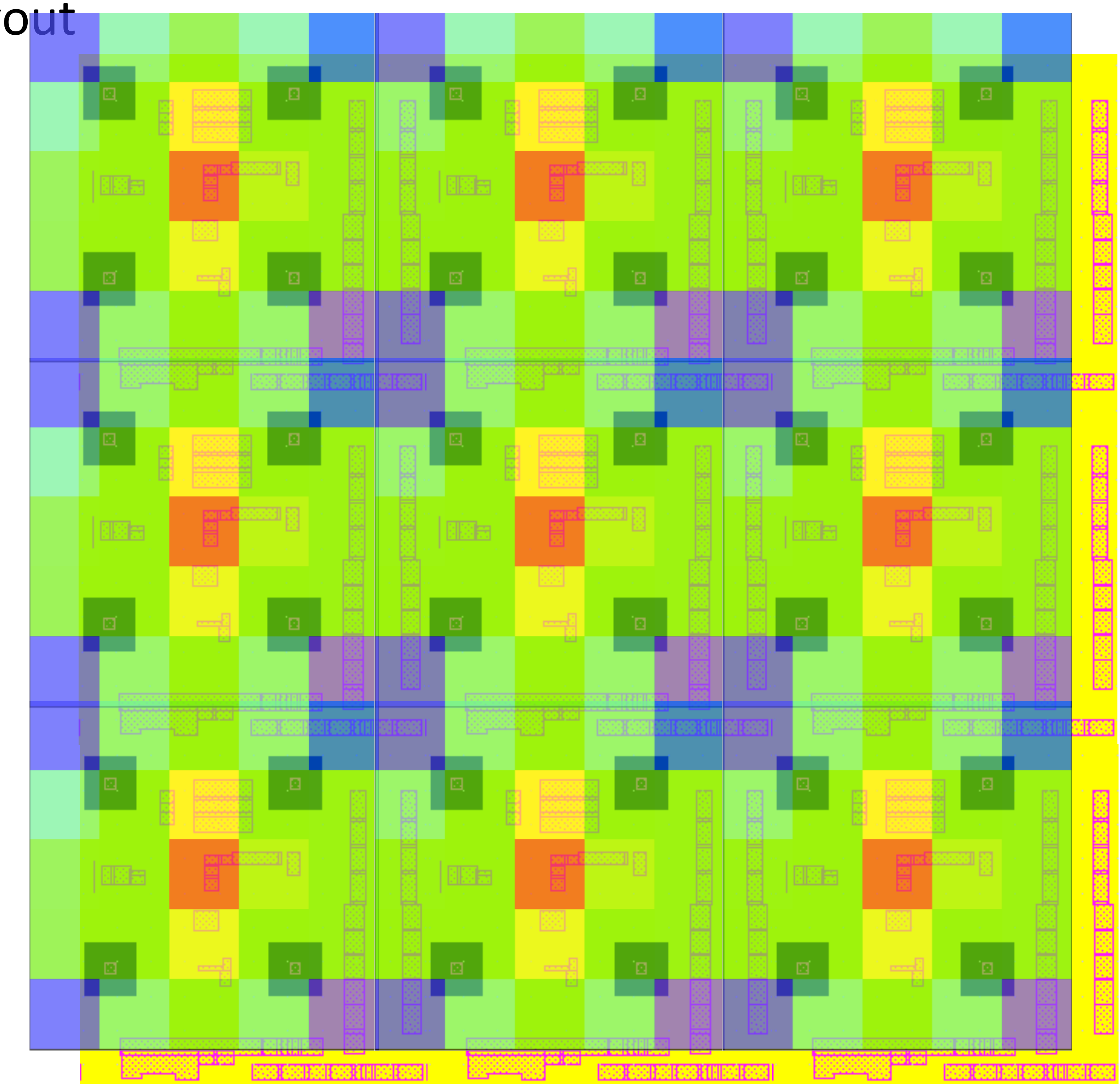
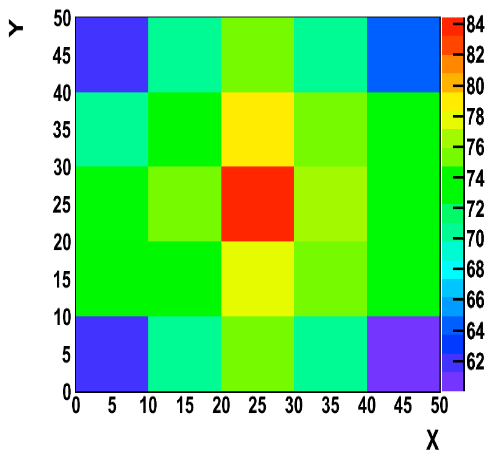
Efficiency Within Pixel, 5x5

Apsel4well pixel layout

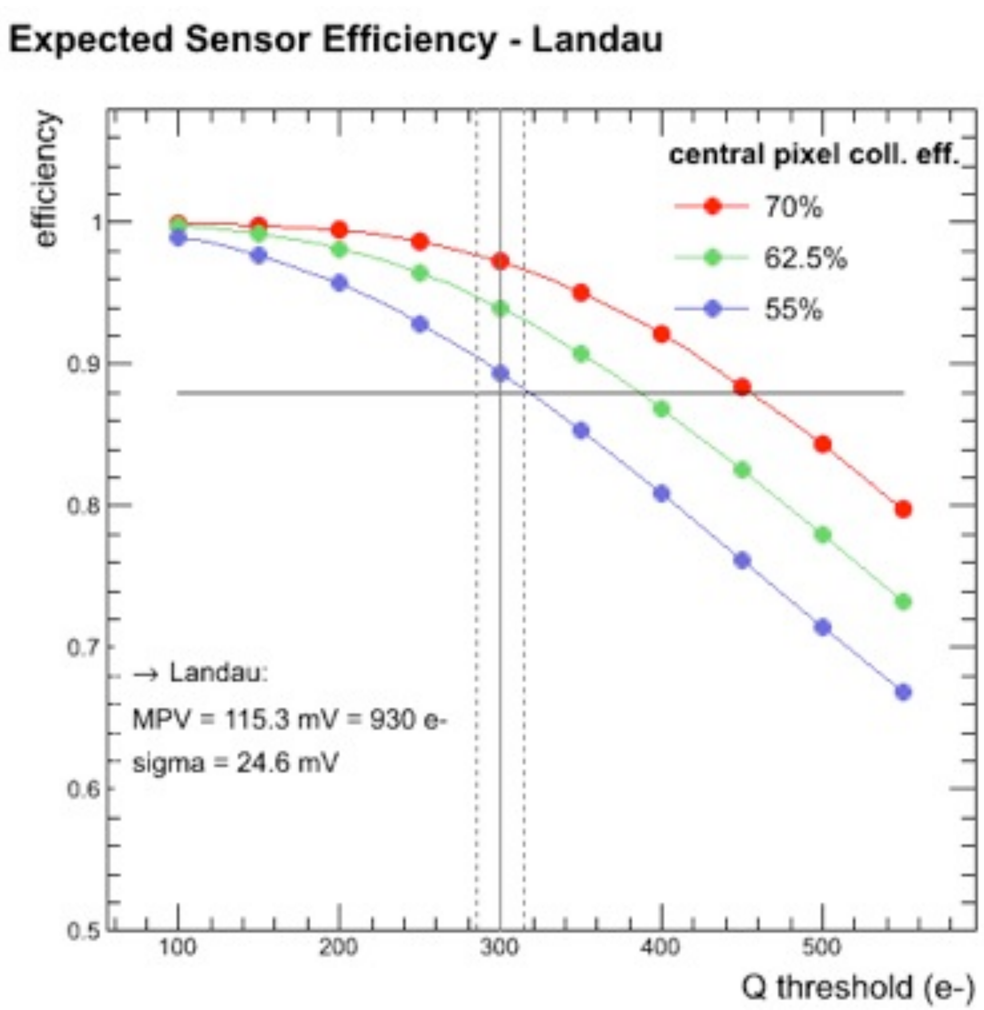


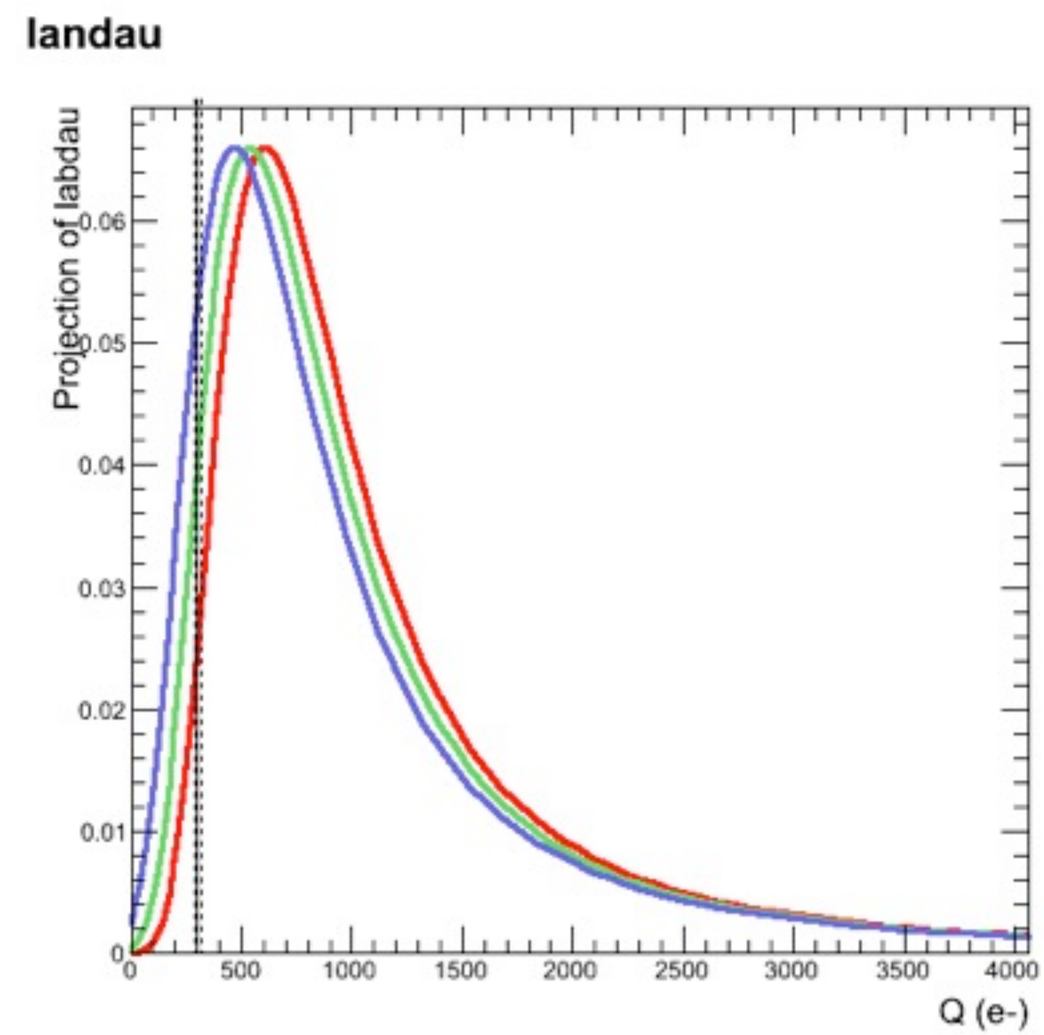


In-pixel efficiency map

Landau from ^{90}Sr Measurements

- ➡ Landau measured with ^{90}Sr on analog devices
  - MPV = 115mV, sigma = 24.6 mV
- ➡ use gain to translate mV into e^-
- ➡ Vary the central pixel collection efficiency

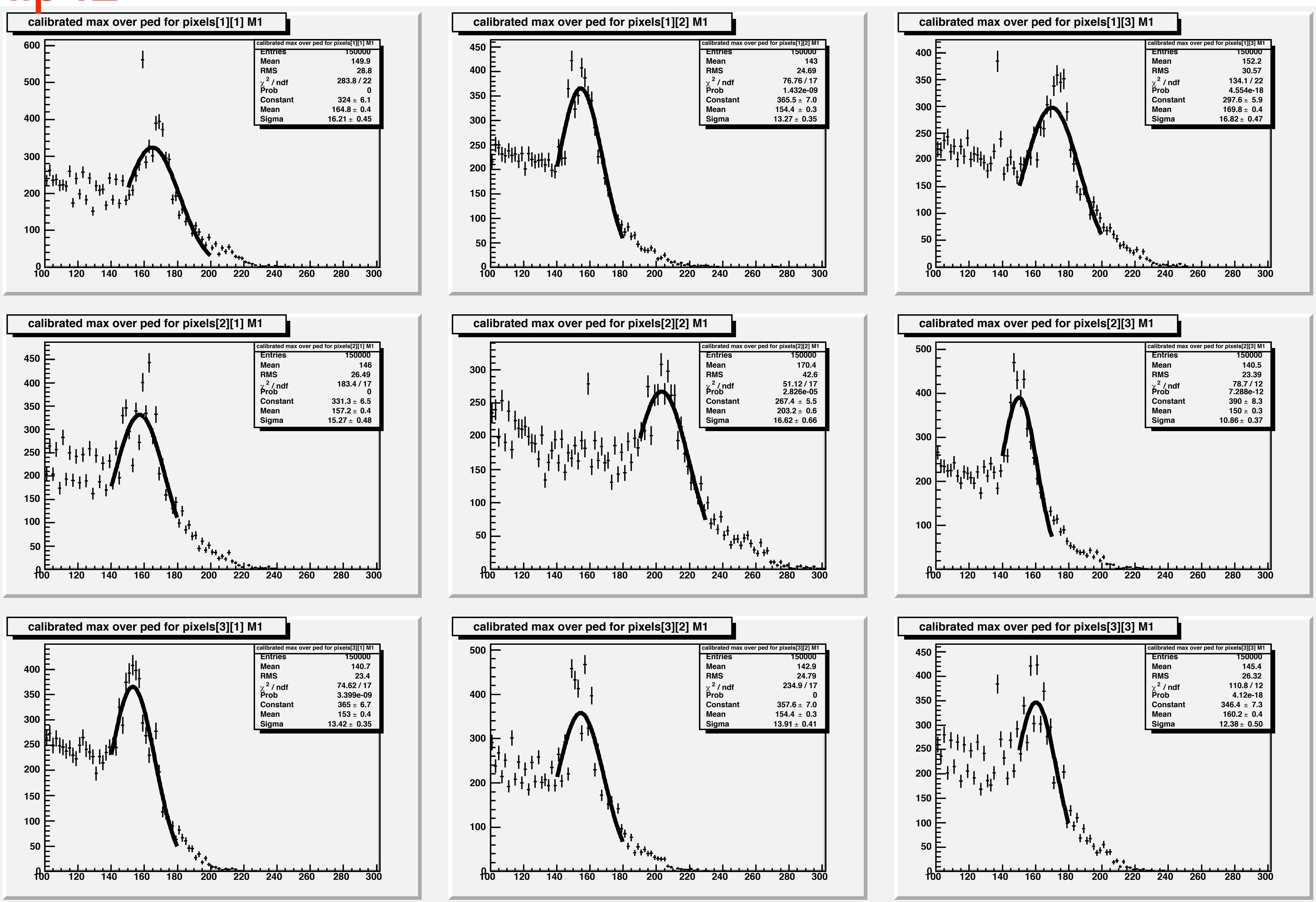




- ➡ central pixel collection efficiency:
  - 70%
  - 62.5%
  - 55%

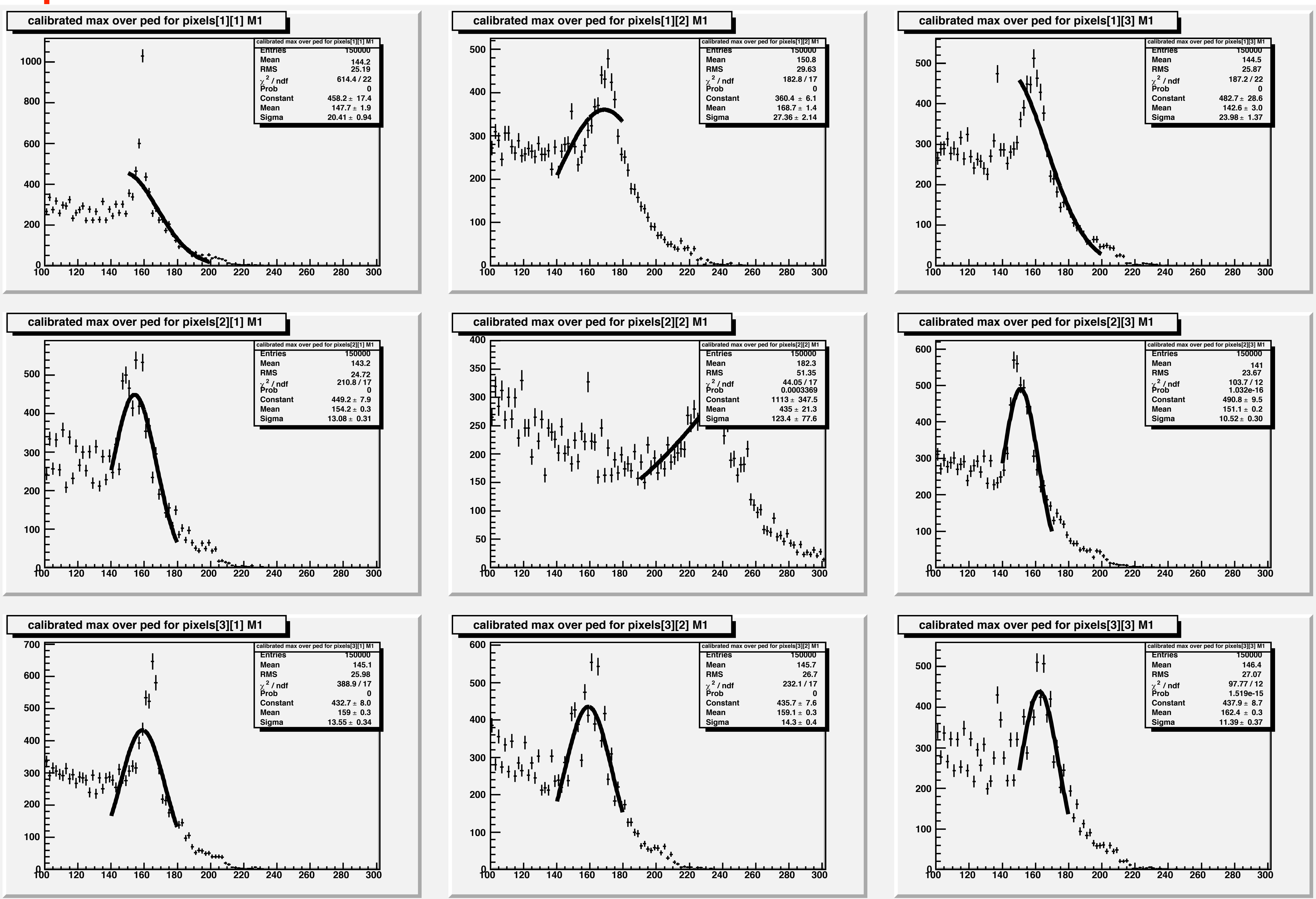
Apsel4Well: ^{55}Fe calibrations

chip42



chip41

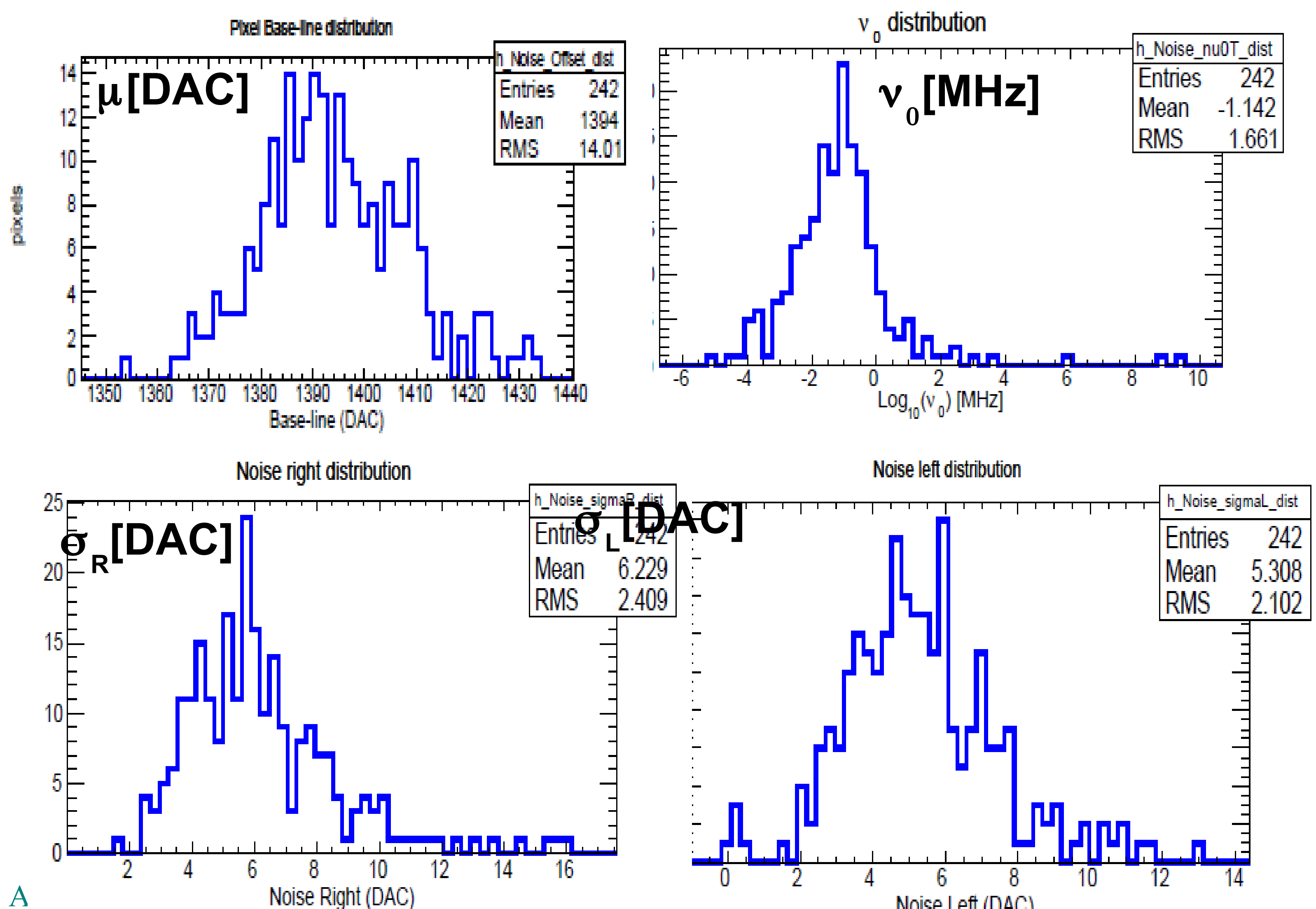
Apsel4Well: ^{55}Fe calibrations



Apsel3D_TC characterization

Noise scans: Chip5

- In some cases the fit doesn't converge properly. Those pixels are not used for the plots below. 221 fits converged (there is 1 dead pixel).

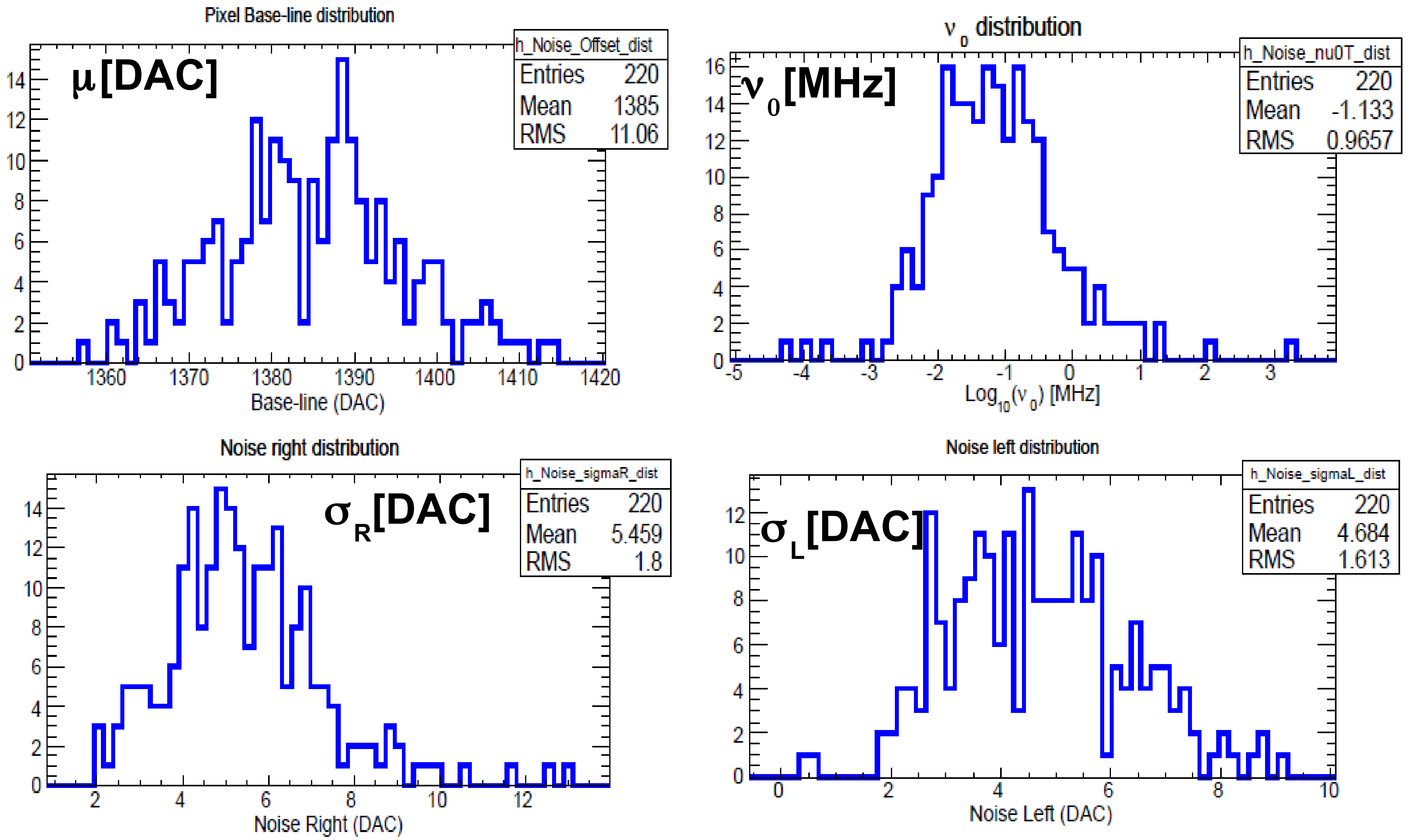


A 8

Apsel3D_TC characterization

Noise scans: Chip6

- In some cases the fit doesn't converge properly. Those pixels are not used for the plots below. 204 fits converged (there is 28 dead pixel).



Alejandro Pérez, LNF SuperB meeting, Dec. 12th 2012 9