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Thin Multilayer Bus

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- 3-Chip Bus Status
  - Production: lesson learned
    - BUS construction phases
    - Some consideration
  - Test set-up for BUS characterization status
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  - Multilayer flex processes used for “interposer” or special components
- Conclusions

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3-CHIP BUS

Pixel Bus second generation:

- → Layout details agreed with CERN
  - → Various iterations ..... about 2 years
    - → Signal layers modified
    - → Opening between layers were optimized
- → Production completed on November 2012
  - → Layer by layer stack-up did not work out ...
    - → Thin layers and registration problems
    - → Layers separated into 3 groups ... Few pictures
  - → Evaluation of the «few samples» received ... How we plan to procede

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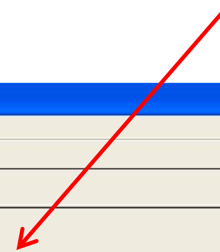
3-Chip BUS Stackup

No real layers !! inserted only for simulation



Stackup Editor

File Edit View Help

Basic | Dielectric | Metal | Z0 Planning | Custom View

	Layer Name	Type	Usage	Metal	Thickness um	Er	Bulk R ohm-m	T coef 1/°C	Test Width um	Z0 ohm	Loss Curve
1	TOP	Metal	Signal	Copper	1	<Auto>	1.724e-008	0.00393	5000	<Error>	View...
2	SOLDER_MASK	Dielectric	Substrate		1	4.5					
3	AVDD	Metal	Plane	Aluminum	25	<Auto>	2.688e-008	0.0038	5000	0.9	View...
4	Glue	Dielectric	Substrate		5	4.5					
5	Kapton	Dielectric	Substrate		12	3.5					
6	Glue	Dielectric	Substrate		5	4.5					
7	AGND	Metal	Plane	Aluminum	25	<Auto>	2.688e-008	0.0038	5000	1	View...
8	Glue	Dielectric	Substrate		50	4.5					
9	Kapton	Dielectric	Substrate		12	3.5					
10	Glue	Dielectric	Substrate		50	4.5					
11	INNER1	Metal	Signal	Copper	3	<Auto>	1.724e-008	0.00393	50	66.9	View...
12	Glue	Dielectric	Substrate		50	4.5					
13	Kapton	Dielectric	Substrate		12	3.5					
14	Glue	Dielectric	Substrate		50	4.5					
15	DVDD_CORE	Metal	Plane	Aluminum	25	<Auto>	2.688e-008	0.0038	5000	1	View...
16	Glue	Dielectric	Substrate		5	4.5					
17	Kapton	Dielectric	Substrate		12	3.5					
18	Glue	Dielectric	Substrate		5	4.5					
19	DGND_CORE	Metal	Plane	Aluminum	25	<Auto>	2.688e-008	0.0038	5000	1	View...
20	Glue	Dielectric	Substrate		50	4.5					
21	Kapton	Dielectric	Substrate		12	3.5					
22	Glue	Dielectric	Substrate		50	4.5					
23	INNER3	Metal	Signal	Copper	3	<Auto>	1.724e-008	0.00393	50	66.9	View...
24	Glue	Dielectric	Substrate		50	4.5					
25	Kapton	Dielectric	Substrate		12	3.5					
26	Glue	Dielectric	Substrate		50	4.5					
27	DVDD_MAT	Metal	Plane	Aluminum	25	<Auto>	2.688e-008	0.0038	5000	1	View...
28	Glue	Dielectric	Substrate		5	4.5					
29	Kapton	Dielectric	Substrate		12	3.5					
30	Glue	Dielectric	Substrate		5	4.5					
31	DGND_MAT	Metal	Plane	Aluminum	25	<Auto>	2.688e-008	0.0038	5000	0.5	View...
32	Glue	Dielectric	Substrate		5	4.5					
33	Kapton	Dielectric	Substrate		12	3.5					
34	BOTTOM	Metal	Plane	Copper	1	<Auto>	1.724e-008	0.00393	5000	0.7	View...

Z ~ 70 Ohm

☑ Calculate Er for metal layers from surrounding dielectrics

TOP
SOLDER_MASK
AVDD
Glue
Kapton
Glue
AGND
Glue
Kapton
Glue
INNER1
Glue
Kapton
Glue
DVDD_CORE
Glue
Kapton
Glue
DGND_CORE
Glue
Kapton
Glue
INNER3
Glue
Kapton
Glue
DVDD_MAT
Glue
Kapton
Glue
DGND_MAT
Glue
Kapton
BOTTOM

Z0 = <Error>
Z0 = 0.903 ohm
Z0 = 0.963 ohm
Z0 = 66.9 ohm
Z0 = 0.963 ohm
Z0 = 0.963 ohm
Z0 = 66.9 ohm
Z0 = 0.963 ohm
Z0 = 0.458 ohm
Z0 = 0.692 ohm

☑ Draw proportionally   Total thickness: 690 um
☑ Use layer colors
No errors in stackup.

OK | Cancel | Help

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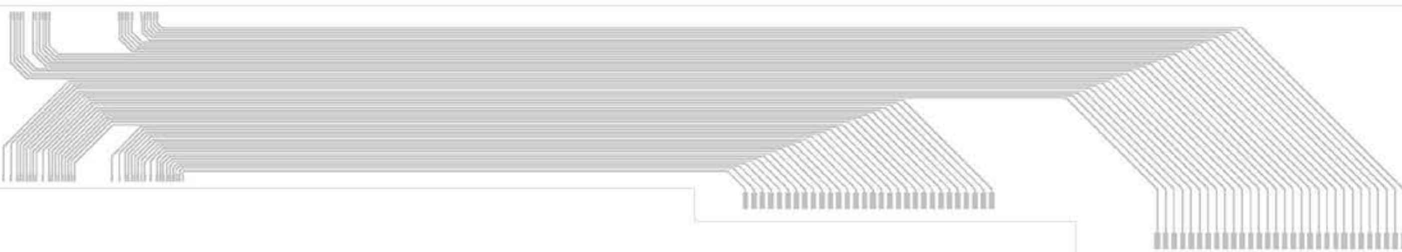
Signal/Power layers

Two IC signals will share the same plane

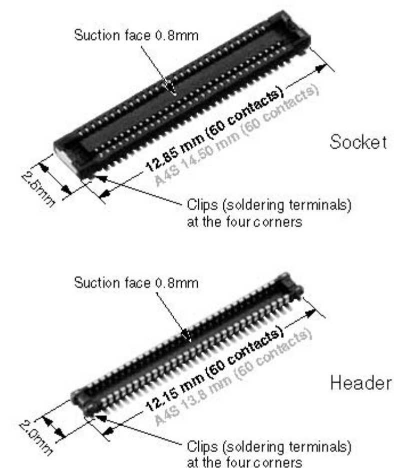


Simplified plane-cuts

Panasonics high density connectors

Overall view (using transparent layers)

1. The world's smallest size* (width: 2.5 mm, Terminal pitch: 0.35 mm and Mated height: 0.8 mm)
The footprint when mated is down approx. 10% from our existing A4S model (60 contacts), contributing to the functionality enhancement and size reduction of target equipment.

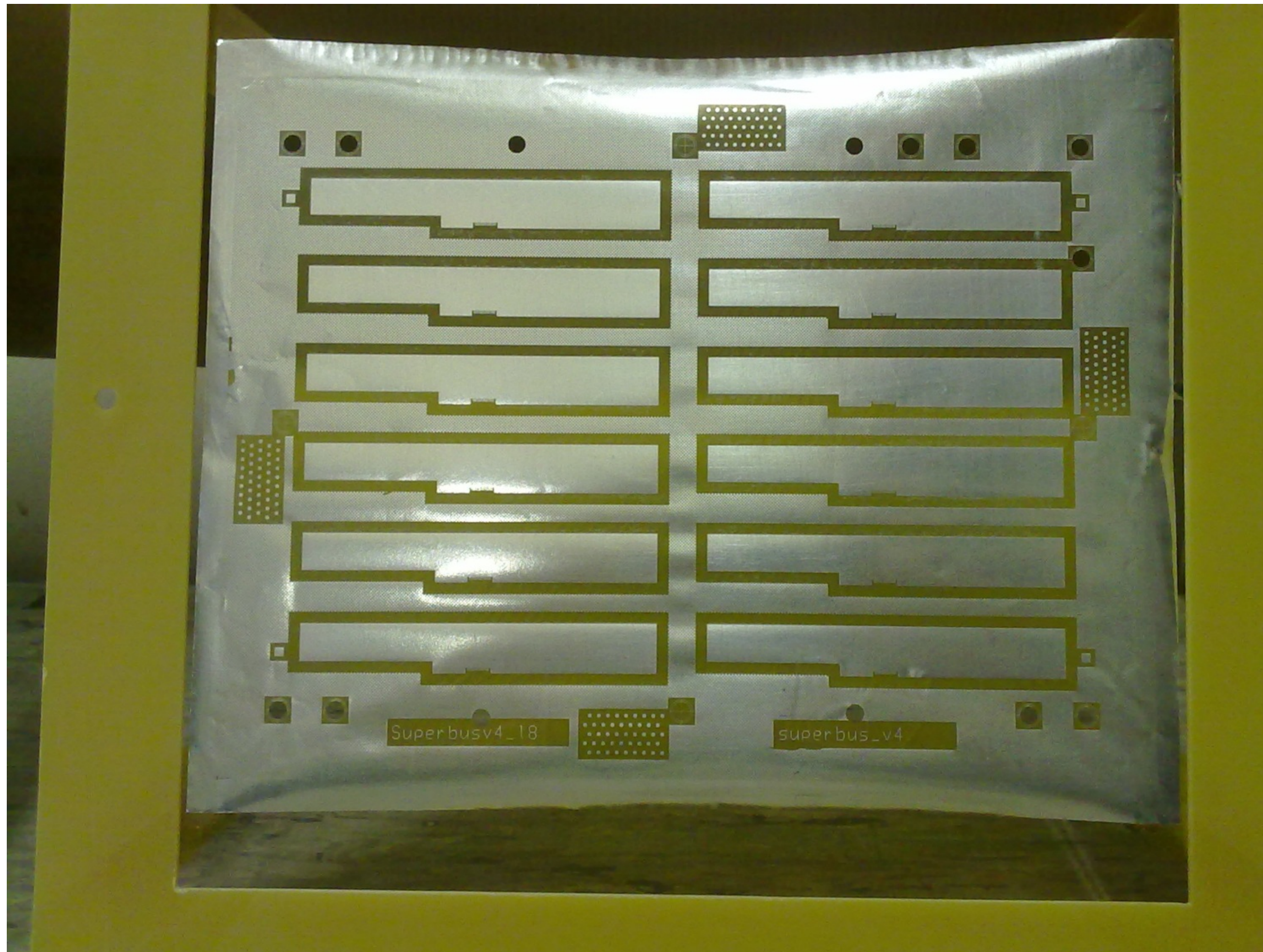


Layers were properly stacked … cut-outs per each layer were optimized to preserve "bonding topology"

Bus produced using a Frame that contains 16 structures

→ **In the picture "dgnd_core.bottom" is shown (1 layer)**

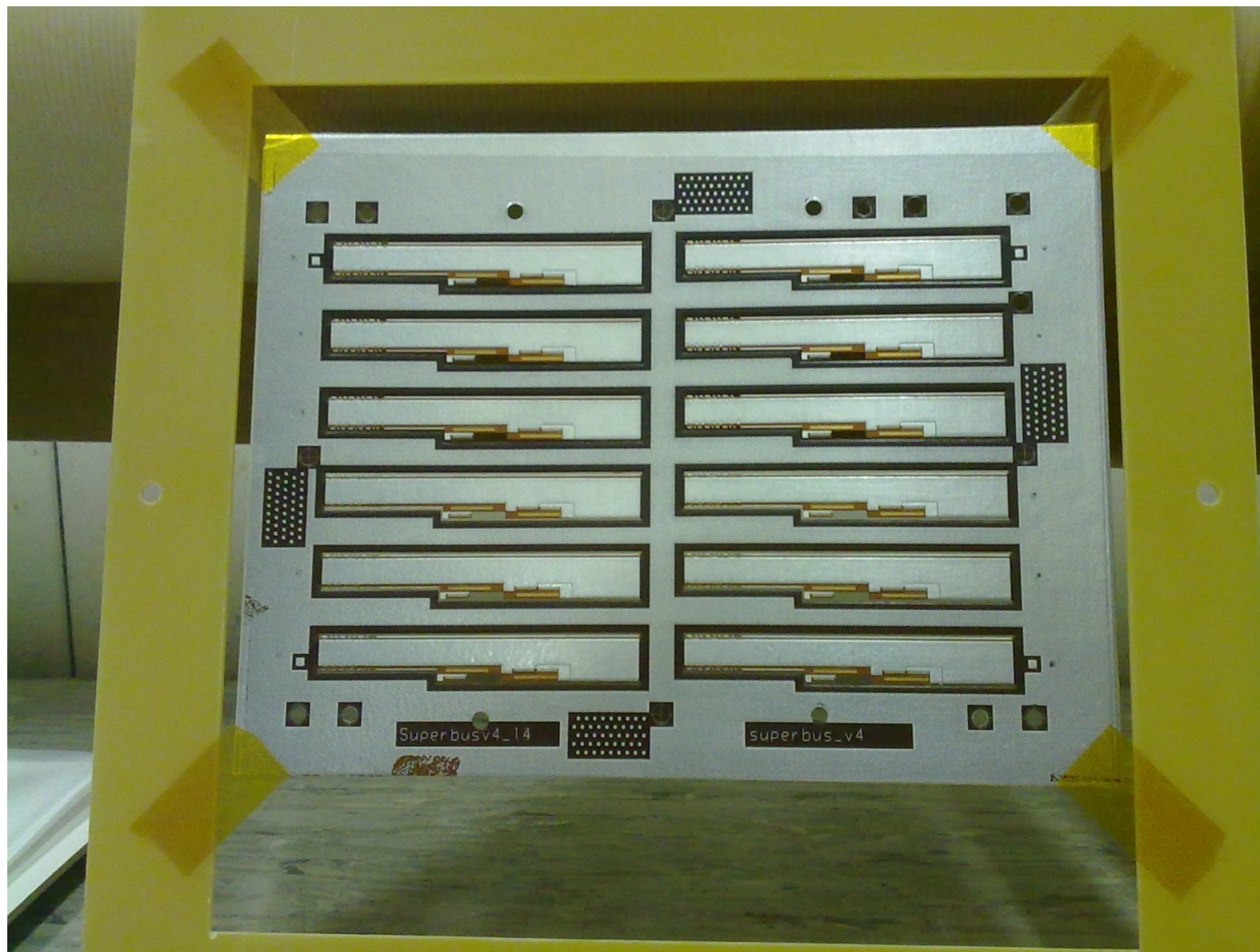
→ **Extremely flexible layer but difficult to align properly**



2nd sandwich made of 4 layers: 3 planes, 1 signal layer

→ **In the picture are shown: "dvdd_core.inner6", "signal2.inner5", "dvdd_mat.inner3" and "dgnd_mat.inner4"**

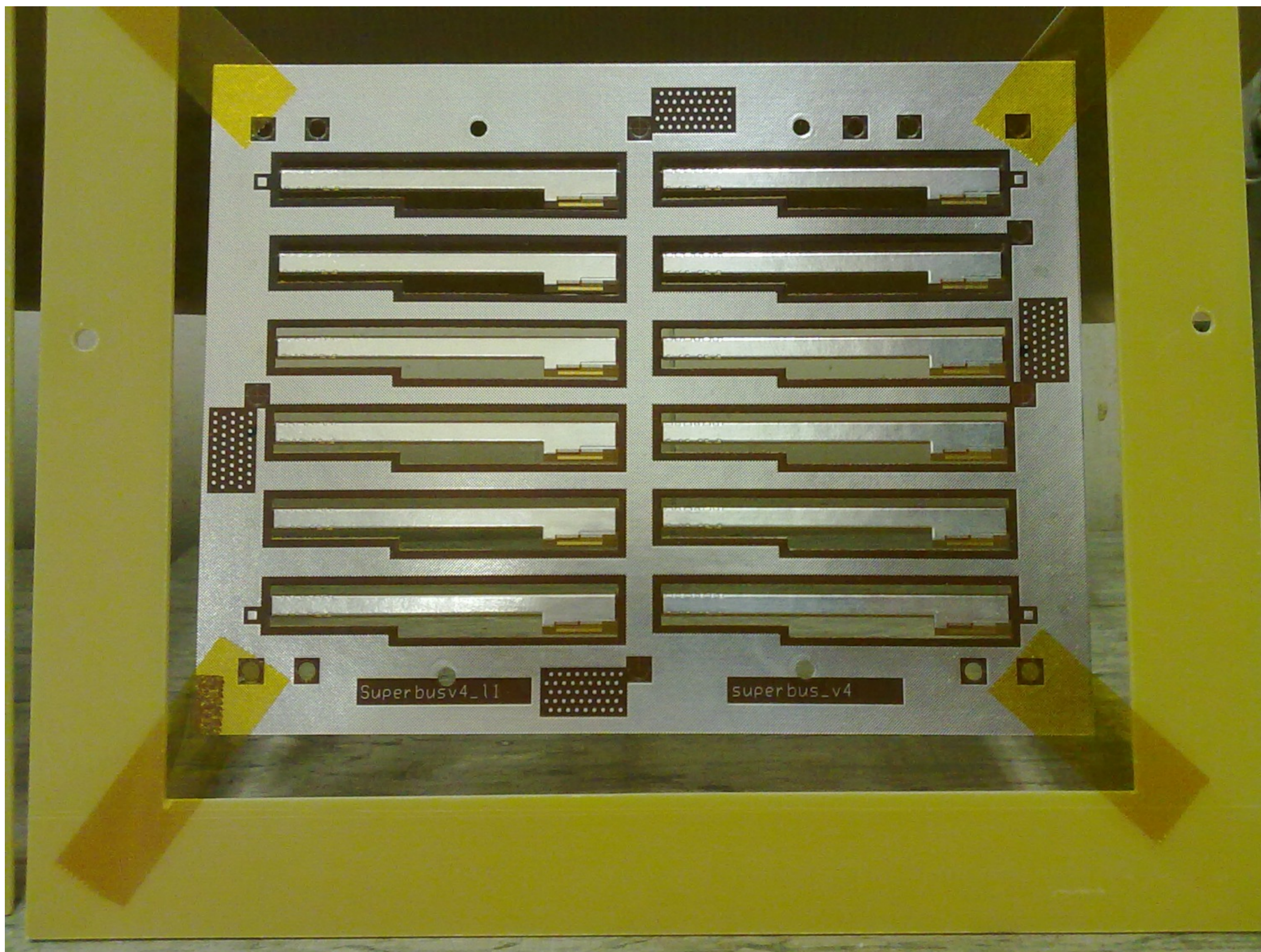
→ **Yield ~ 100 %**



2nd sandwich made of 3 layers: 2 planes, 1 signal layer

→ **In the picture are shown: "avdd.top", "agnd.inner1" and "signal1.inner2"**

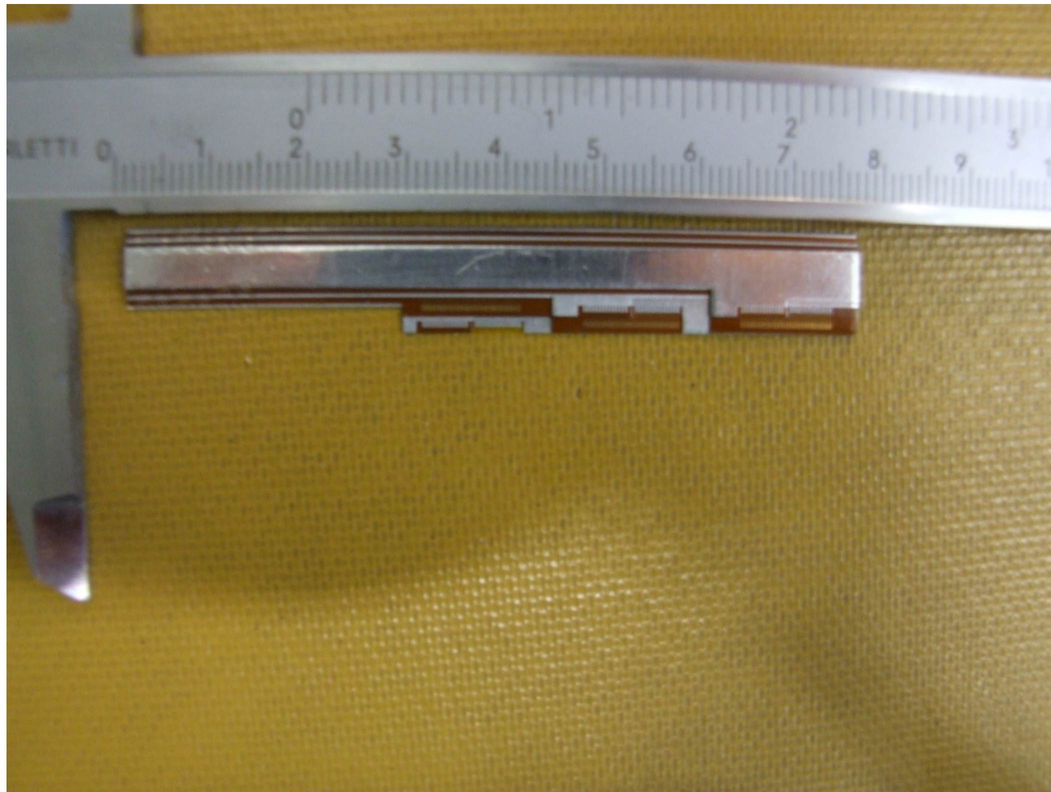
→ **Yield ~ 100 %**



Final Object

→ **To obtain the final bus the 3 sandwiches are "glued" together after alignment and preparation**

→ **Yield is low, < 50 % : 2 pieces in Milan, 2 at CERN plus 3-4 pieces to be evaluated carefully**

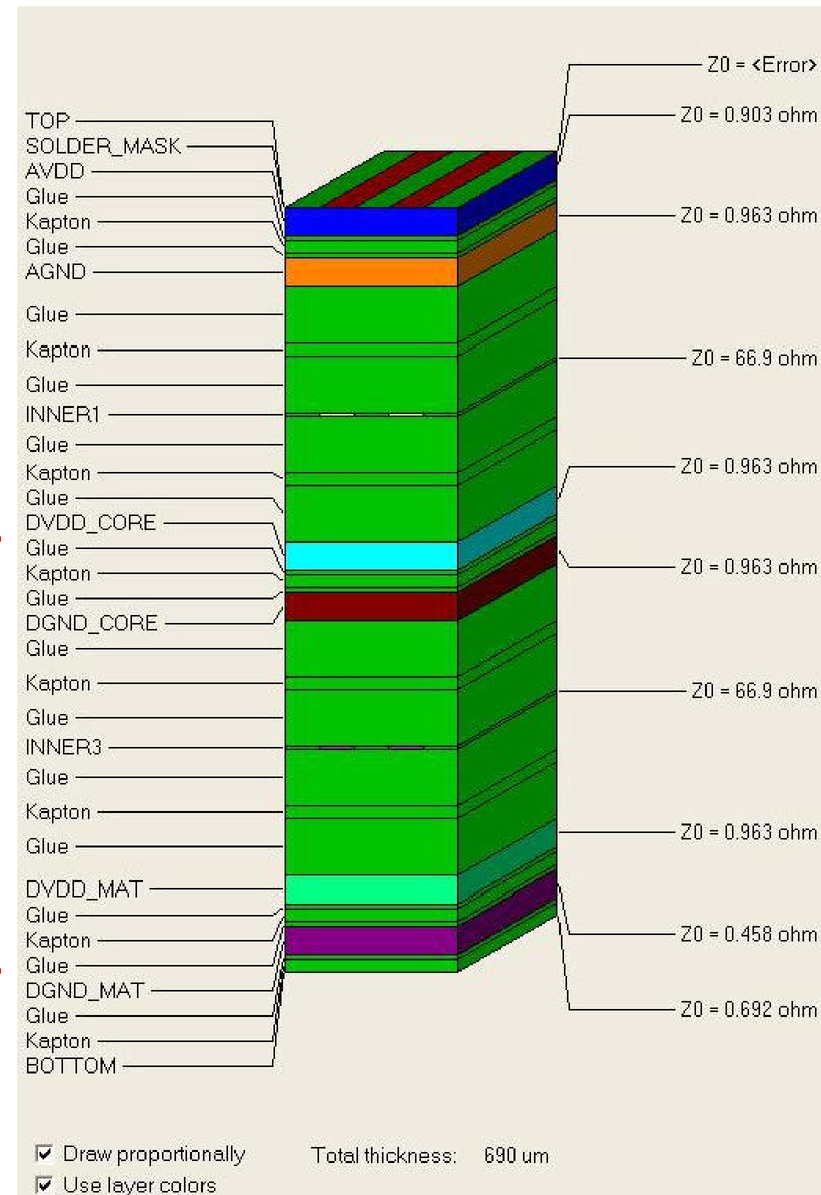


Consideration and X0 reduction

What could be probably done:

- No. of power planes: 2 …. max 3
  - *One plane subdivided in Analogue and Digital sub-planes? Not clear. No “sophisticated” pattern capability if treated as planes*
- However two planes allow strip-lines design (better for crosstalk)
- Signal trace pitch could be reduced to ~ 50 micron to have only one signal layer for the signal.
  - *Aluminum lines possible !*

Thickness, after optimization, could be ~ 350 um



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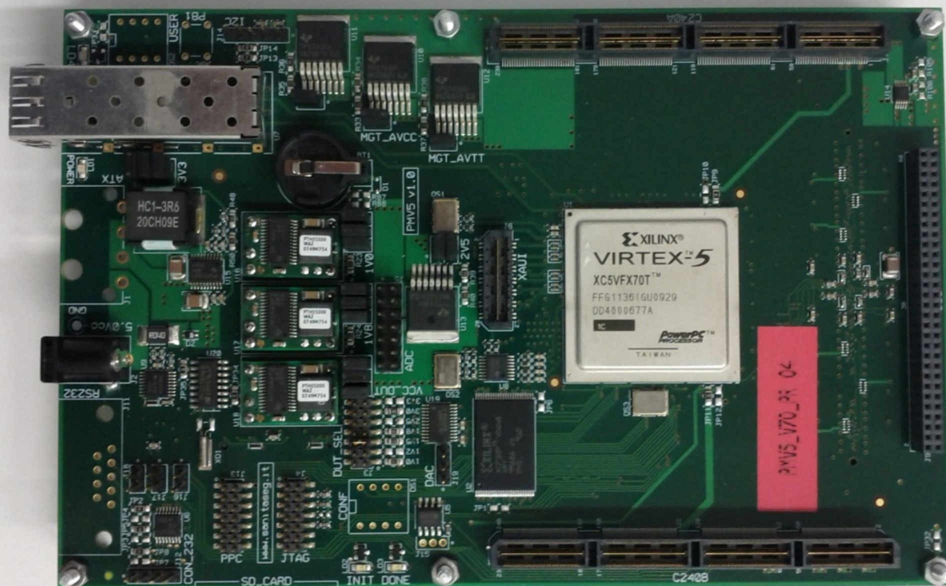
BUS Characterization Setup

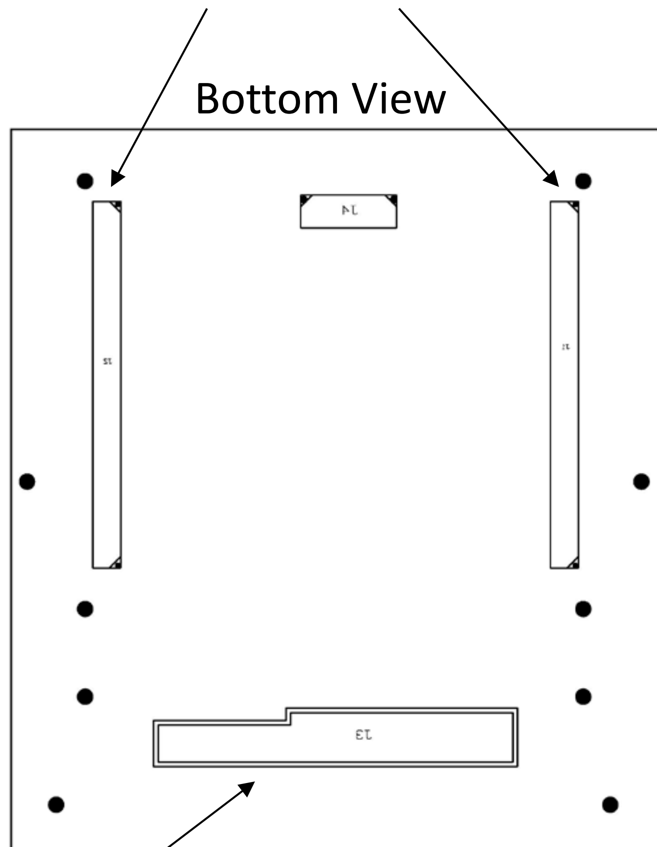


Multipurpose mother/daughter combination of boards developed together with SANITAS S.r.l (Milano):

- Based on a Virtex 5 “controller board” (showed in picture)
- Multiple daughter boards can be plugged in to customize testing (using connectors on the right side of board)
- Daughter board for BUS testing is in production at TVR
- Firmware is almost complete
    - To inject signals/patterns (via Pattern generator or via FPGA)
    - To measure Bit Error Rate (at various frequency, w/wo jitter, w/wo skew)
    - The system can grow to emulate full data link (stacking up more daughter boards)

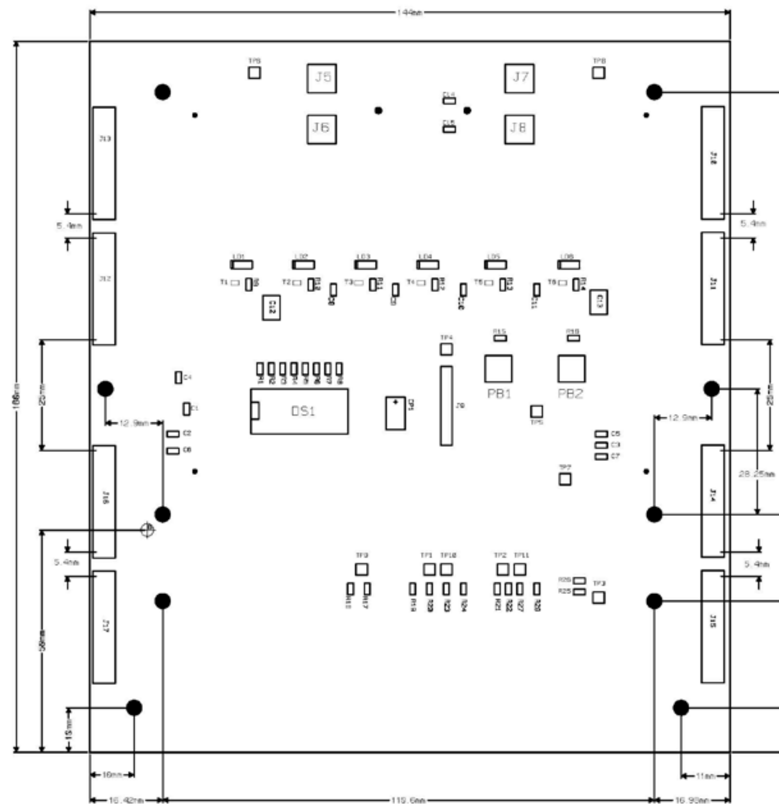
Daughter board for the BUS

High density connectors matching motherboard



3-Chip Fanout

Top View



IN/OUT lines matched for impedance and “paired” in length for each chip (ΔL ~ cm)

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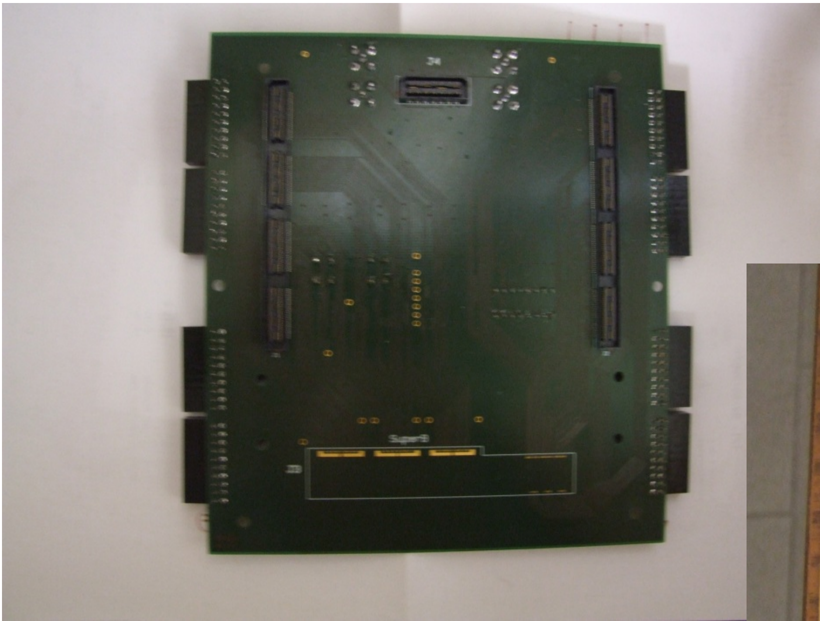
Daughter Card



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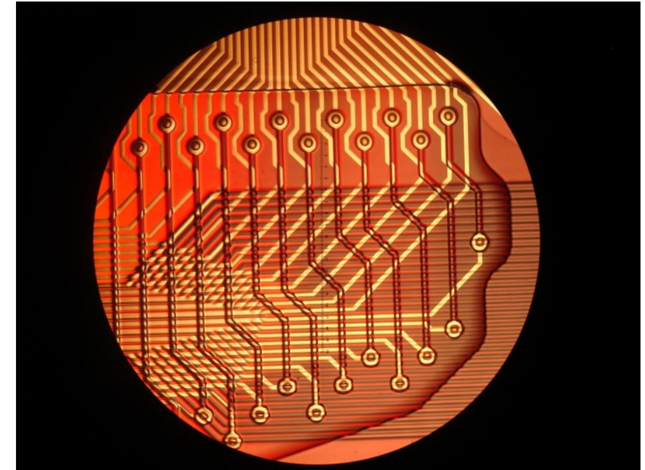
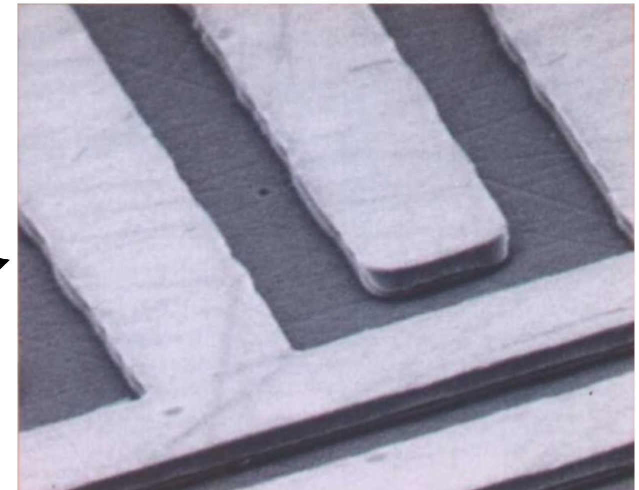
Future Solution

What is needed:

- Ultra high resolution single and multilayer circuitry on flexible materials → YES
- Aluminum instead of copper → MAYBE
- Using high resolution photolithography, precision electroforming, and thin film deposition, high resolution flex circuits and electrode array plates can be made … up to ~ 2x2 cm
- Conductor widths and spaces of 5 microns can be achieved …. But on what maximum dimensions? ~ 2cm
- Specialized companies ….. Are they interested in prototyping? YES, initial cost to be understood





MAGNIFICATION: 1.21 KX
5 Micron Conductors
5 Micron Spaces

Conclusions

- → CERN has undoubtedly a proven capability in producing low mass, multilayer, flexible circuits
  - → However 3-4 layers it's the limit
    - → 2-3 planes (~50 um), 1 signal (10 um)
    - → 50/50 um pitch in Al possible
  - → We still need to verify how close the BUS matches our design specs
    - → We should have asked for the individual sandwiches
- → Special commercial applications are requesting ultra-thin flexible circuits
  - → At least one company is willingly to talk to us and it is also interested in producing prototype
  - → Power planes: "strange beasts" for these technologies, again low power is welcome

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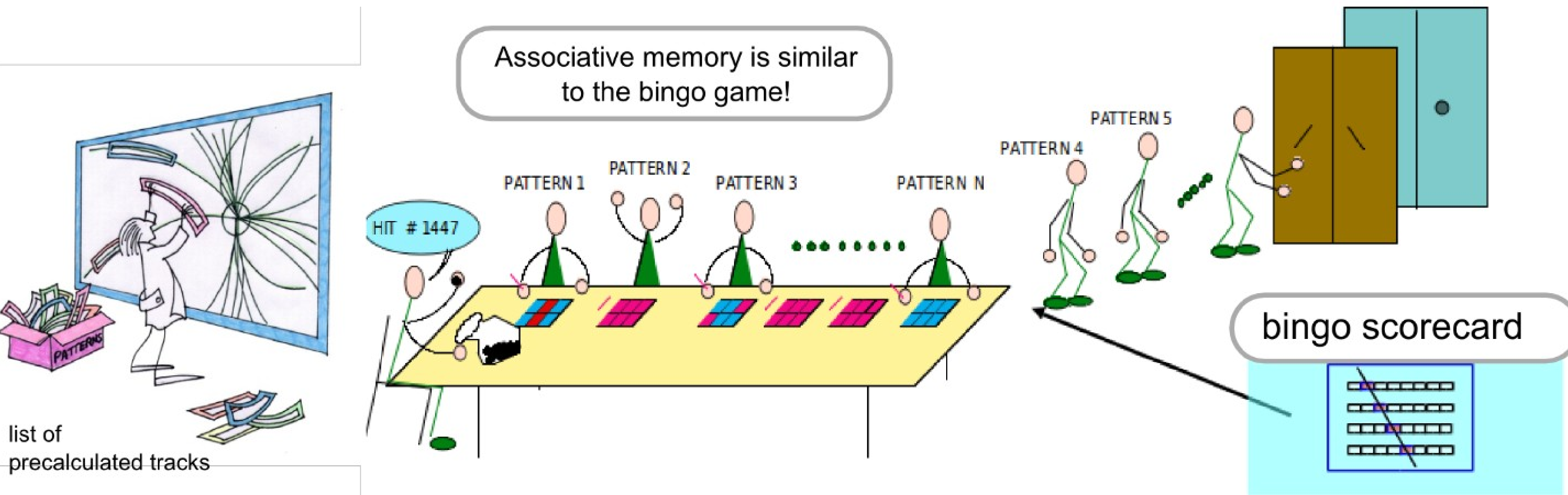
FTK on going effort

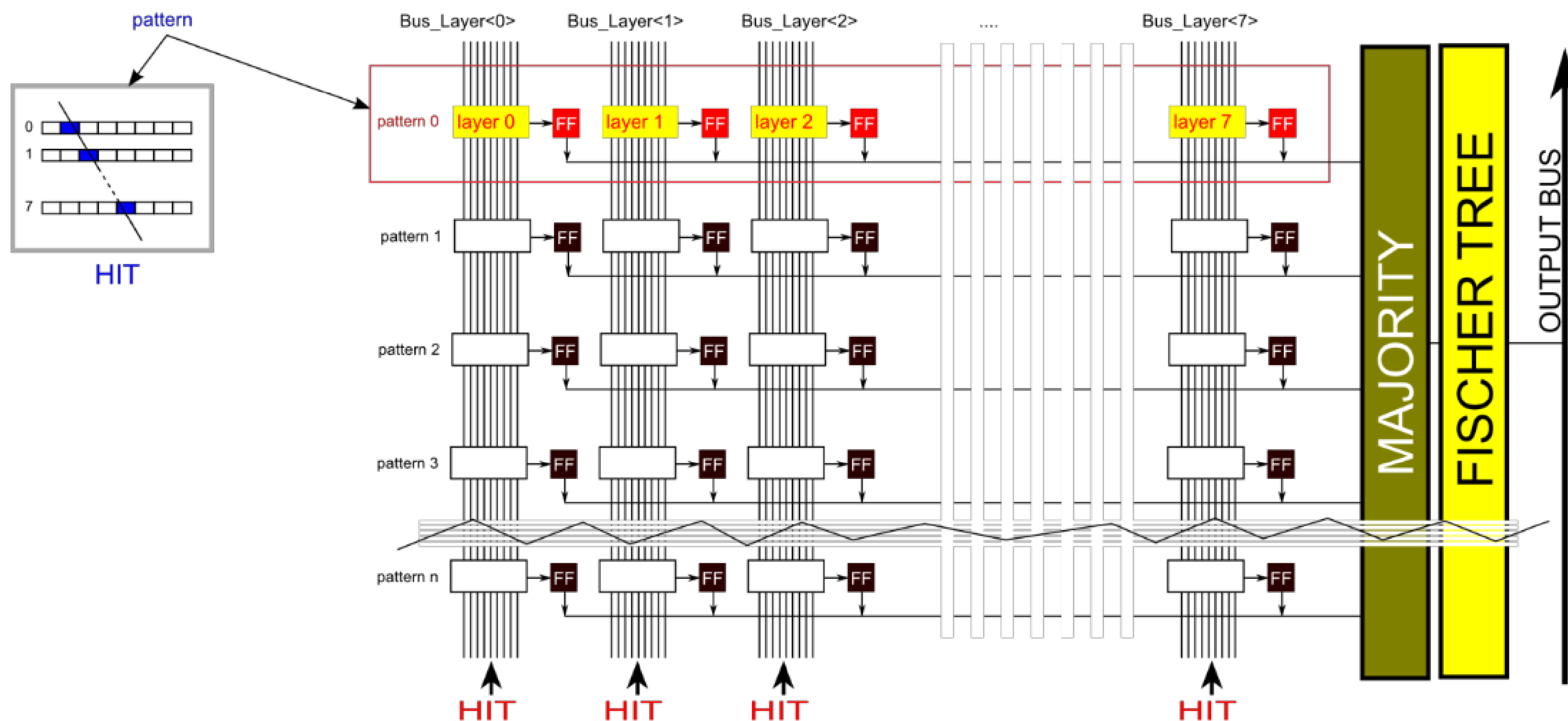
AMchip theoretical principle

- Associative Memory chip: AMchip
  - Dedicated VLSI device - maximum parallelism
  - Each pattern with private comparator
  - Track search during detector readout



Amchip

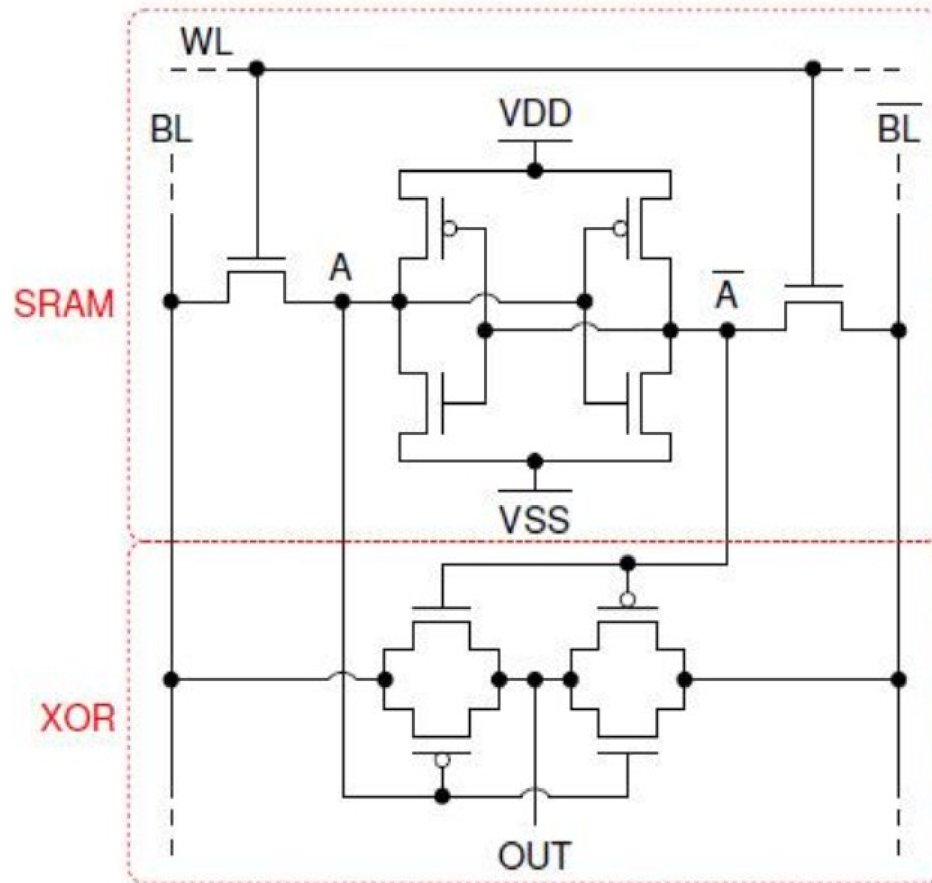
- Main aim: **pattern recognition of Super Strips!**
  - Count the number of matching layers (from 6 to 8 layers)
  - **Bit map** of matching patterns
  - **Variable resolution “pattern-by-pattern” and “layer-by-layer”**

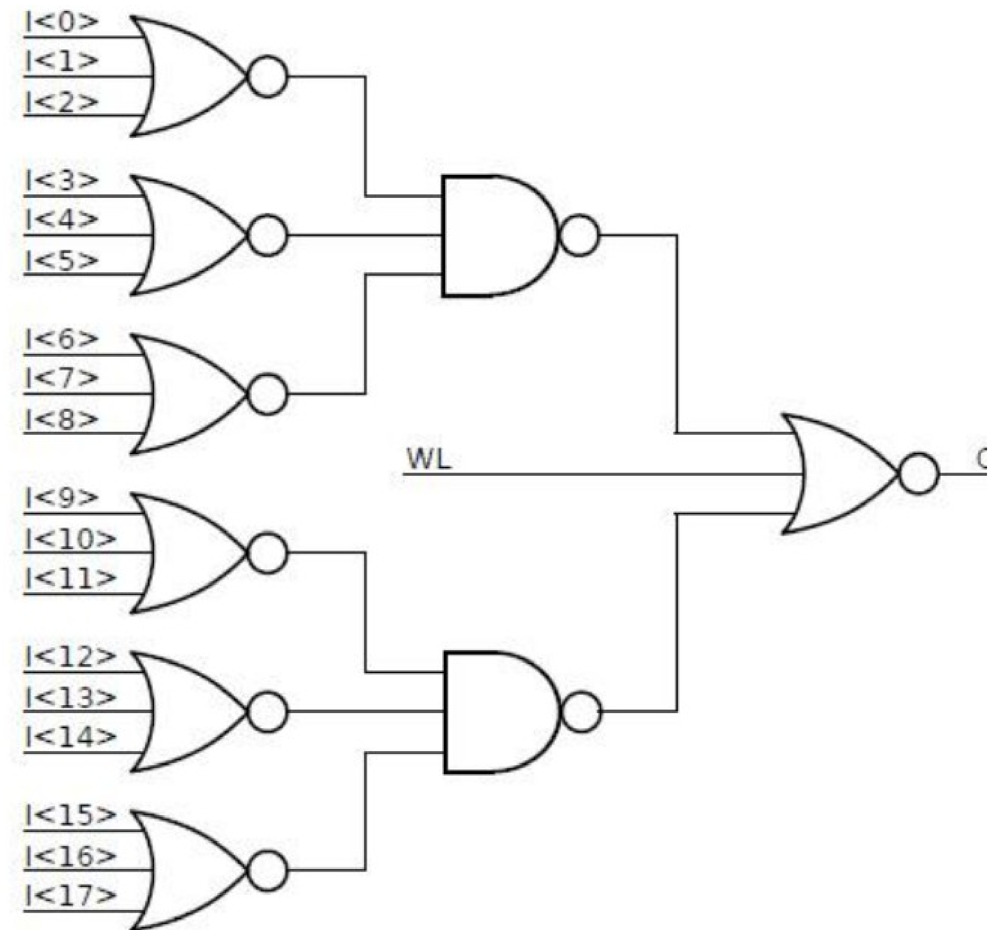


Mini@sic goals & description

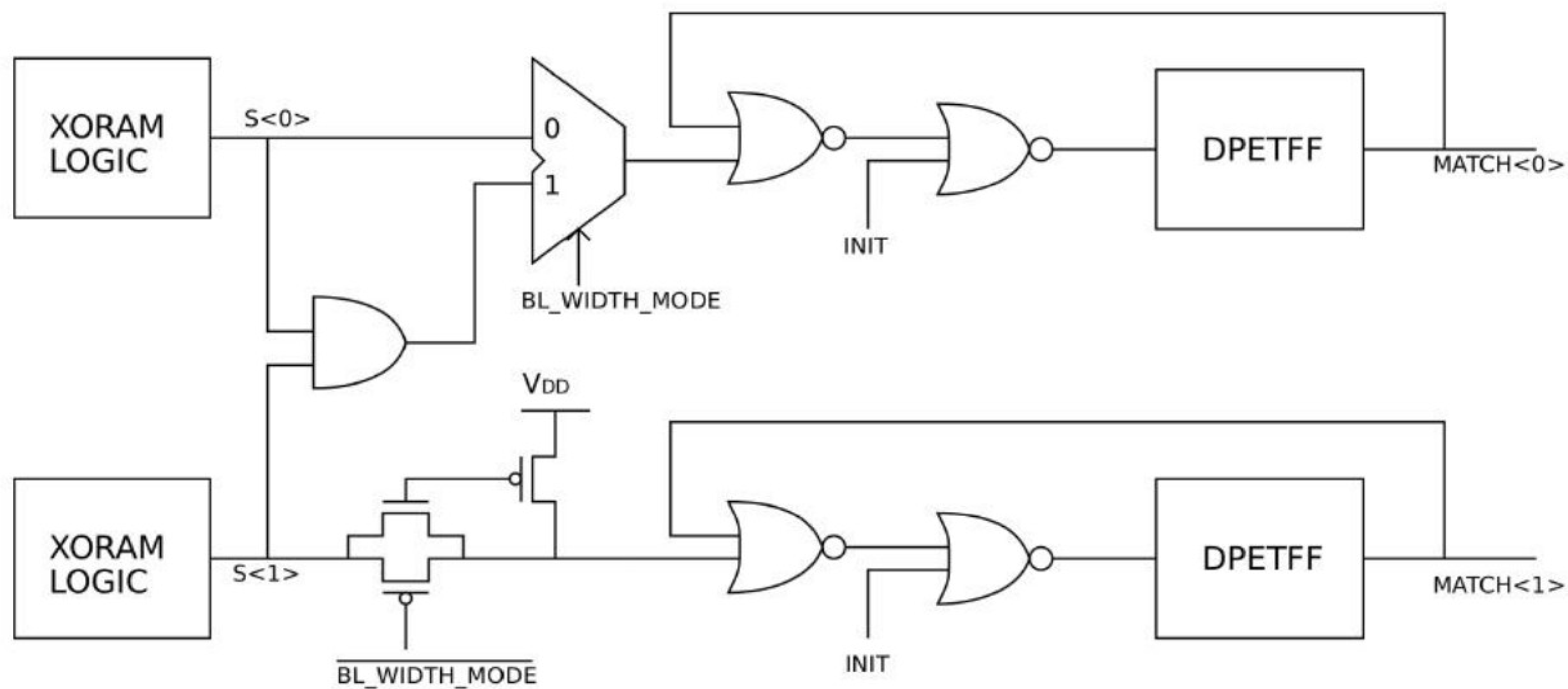
- Test chip between the AMchip04 and AMchip05
  - New features
    - Hits and roads are **serialized and de-serialized** inside the chip core
      - **Silicon Creation® SerDes** IP blocks have been used for this purpose
      - Silicon Creation® LVDS pad has been used to bring inside the chip an external LVDS clock
        - The LVDS pad needs of a Band Gap Voltage Reference (always by Silicon Creation ®)
    - Two different type of Associative Memory (AM) cells have been used
      - **A new XOR+RAM cell** has been used with the aim to reduce silicon area and power consumption
    - A **more programmable Bit Line (BL) width mode**
      - With the XOR+RAM is possible to select how much is large the hit buses: 30 bit or 15 bit
    - **Built-In Self Test (BIST)** used to stimulate the AM banks at maximum working frequency through JTAG commands
      - PRBS generator to stimulate the banks

The new “XOR+RAM = XORAM”





XORAM architecture



Submission