Activity on the design and characterization of front-end electronics in the frame of the PRIN09 project

Luigi Gaioni[a], Alessia Manazza[a], Massimo Manghisoni[b,a], Emanuele Quartieri[c,a], Lodovico Ratti[c,a], Valerio Re[b,a], Gianluca Traversi[b,a], Stefano Zucca[a]

[a] INFN sezione di Pavia

[b] Università di Bergamo

[c] Università di Pavia

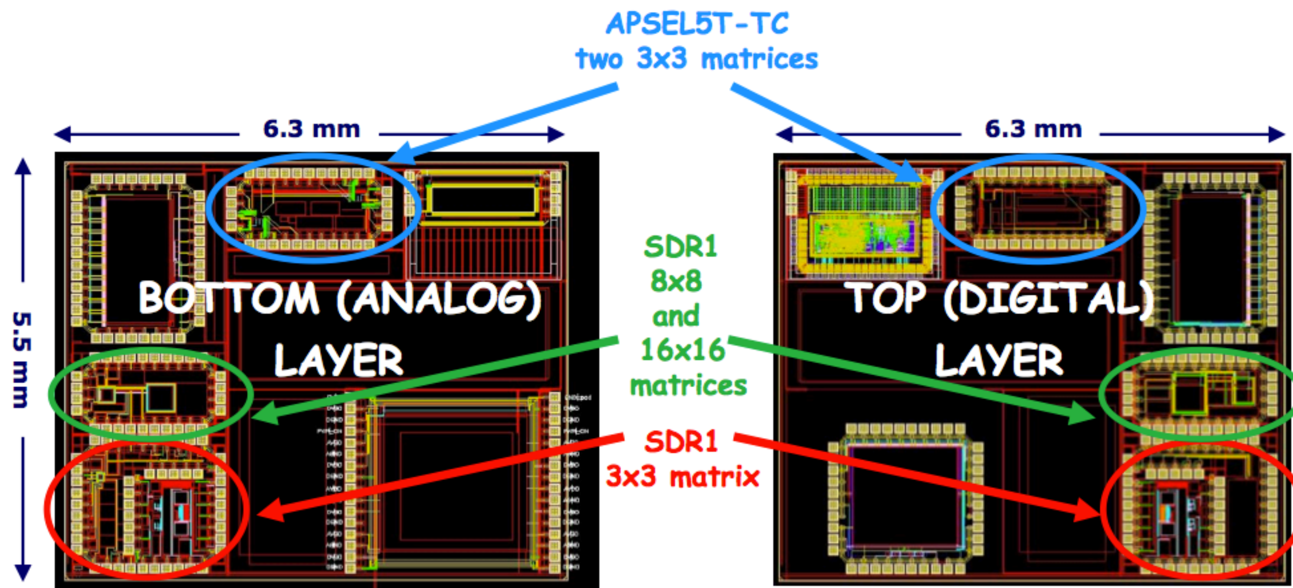
PRIN09 Collaboration Meeting, Milan, March 27th 2013

What is in the PRIN09 proposal (FE electronics-wise)

- Optimization of high granularity detection systems for charged particle tracking according to the SuperB SVT requirements – granularity (40-50 um), detection efficiency, power distribution, threshold dispersion, radiation hardness, material budget
  - 40 um pitch MAPS with DNW collecting electrode in a vertically integrated, two-tier, 130 nm CMOS technology
  - 50 um pitch mixed-signal front-end circuits in a vertically integrated, two-tier, 130 nm CMOS technology for hybrid pixel detectors
  - also DNW MAPS (Apsel family) and front-end chips for hybrid pixels in 130 nm planar CMOS technology and MAPS in the INMAPS, 180 nm process were mentioned
- Feasibility study of particle detectors for high precision event timing, using diamond or 3D detectors
  - planar 65 nm and vertically integrated 130 nm CMOS technologies proposed for front-end electronics design
  - jitter and time walk minimization, implementation of timing methods (fractional triggering, time to digital conversion, time to analog conversion, TAC-based TDC, time vernier)

Vertically integrated MAPS (Tezzaron/Chartered)

- Fully functional samples available since last summer, more available in the coming weeks
  - Apsel3DTC samples tested on the SPS beam at CERN
  - Radiation tolerance tests on SDR1 chips are in progress

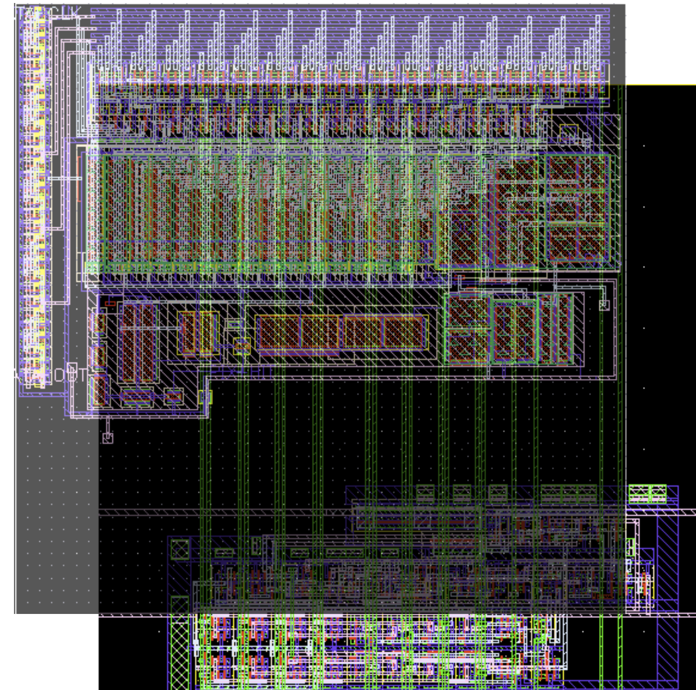


- Characterization of the SDR1 and Apsel test structures already covered by Giulia and Alessia this morning

APSELVI and Superpix1 (Tezzaron/Globalfoundries)

- Design of the APSELVI 3D MAPS and of the Superpix1 chip for hybrid pixels is in progress - to be submitted hopefully at the beginning of next Summer

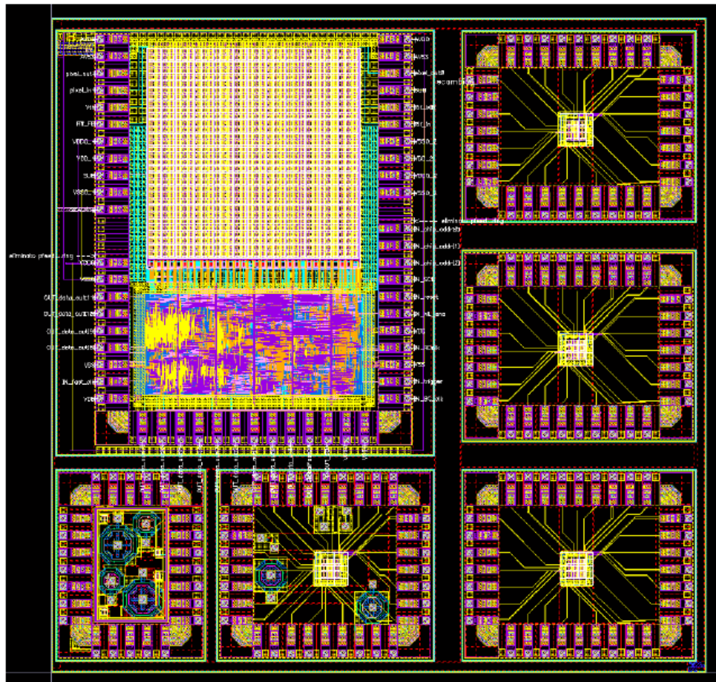
  - some solutions implemented to improve power distribution (voltage drop minimization circuit) and threshold dispersion (threshold correction circuit)
  - on chip pulser for charge sensitivity calibration and general functional tests
  - polarity selection available for signal readout from different kinds of detectors
  - device simulation for best trade-off between noise and charge collection efficiency



- Design of the APSELVI and Superpix1 chips already covered by Luigi and Alessia this morning

Apsel4well – MAPS in INMAPS technology

- Monolithic sensors in a 180 nm CMOS technology with deep P-well implant

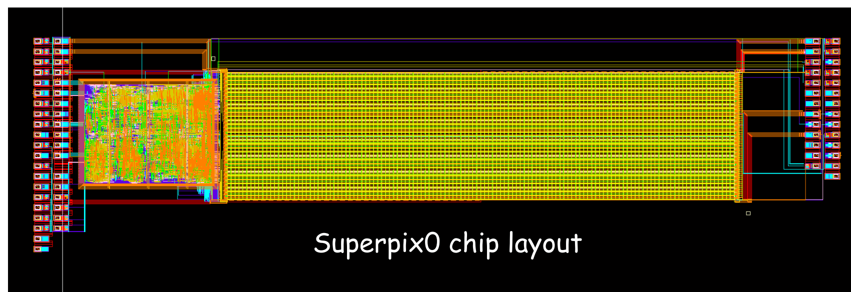


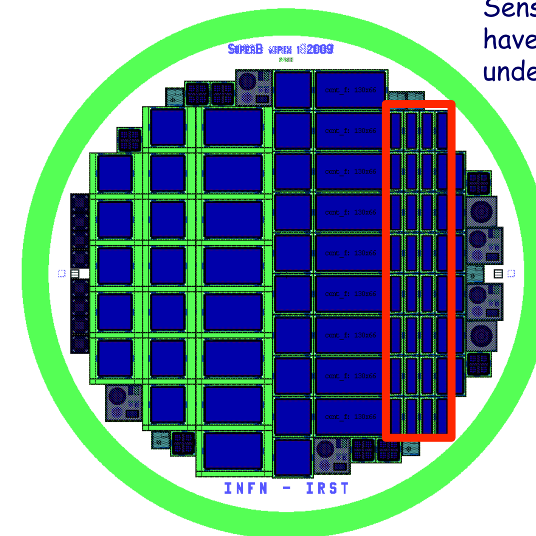
- different technology solutions tested – 5 and 12 um epi-layer thickness, standard and high resistivity epi-layer (10^{13} and 10^{15} cm^{-3})
- extensive radiation tolerance characterization (bulk damage tests up to 10^{14} cm^{-2}, TID characterization is in progress, planned to reach 10 Mrad total dose)
- quite bad substrate noise problems under investigation

- Characterization of the Apsel4well test structures already covered by Stefano Zucca this morning

Integration of heterogeneous layers with T-Micro

- Very high interconnect density, with small bond pads (squares with a side of 5 or 10 μm, depending on the bump size, 2x2 μm^2 or 8x8 μm^2) both on the sensor and the readout sides ➔ more room for top metal routing, in particular for power and ground lines, smaller capacitive coupling, less material
- Preliminary test of the T-Micro integration process performed on pre-existing readout chips (Superpix0) and high resistivity n-on-n pixel sensors (VPix1)





Sensors in the red box have no metal layers under the markers

- Front-end chips and a pixel sensor wafer shipped to T-Micro in Dec. 2012
- 5 vertically integrated chips now waiting for customs expenses to be paid

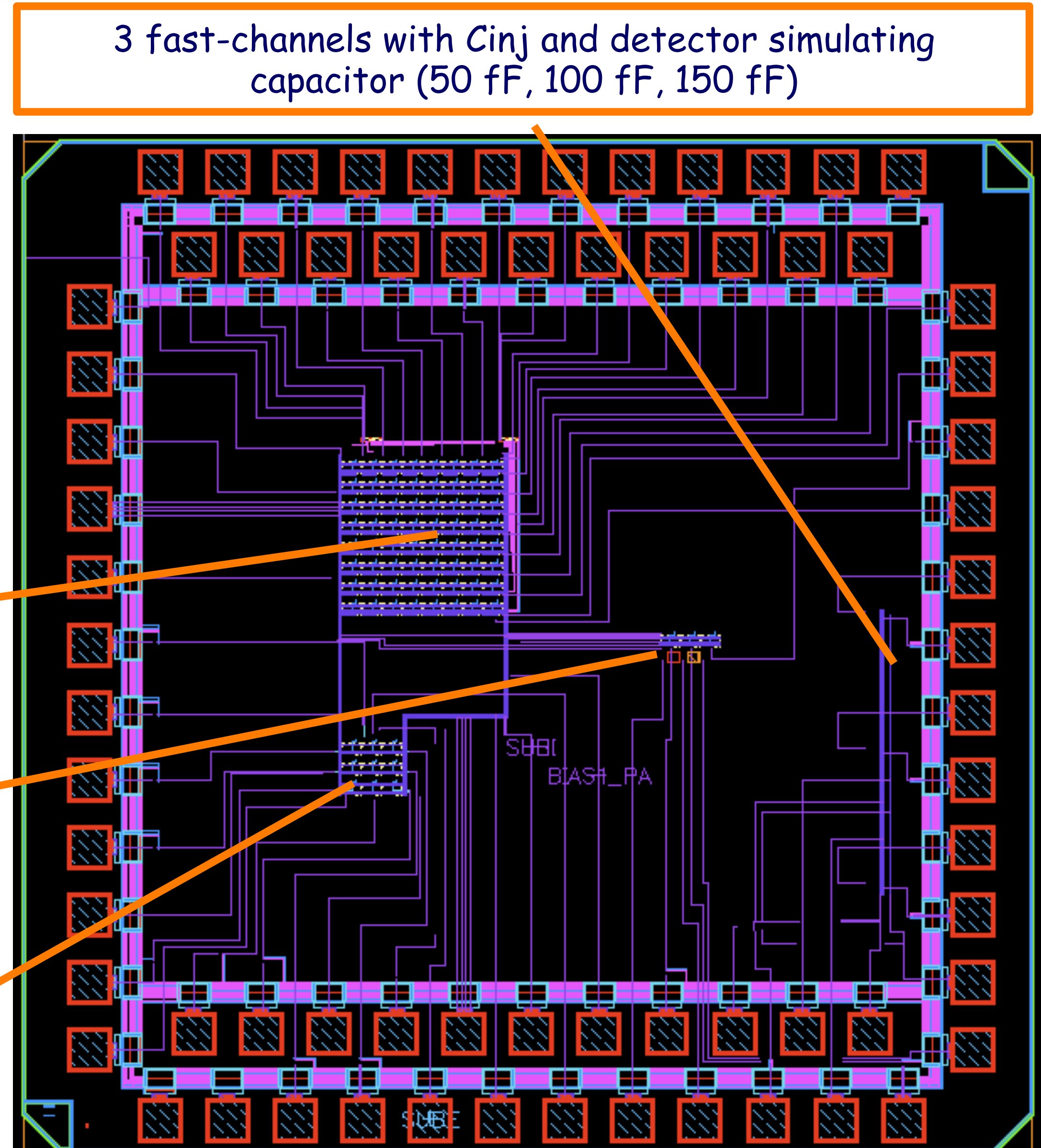
Apsel65 Fast Front-End (FFE) chip

- Developed in a CMOS 65 nm technology (IBM) for the readout of pixel sensors (C_D of the order of 100 fF)
- Relatively fast operation (25 ns peaking time)

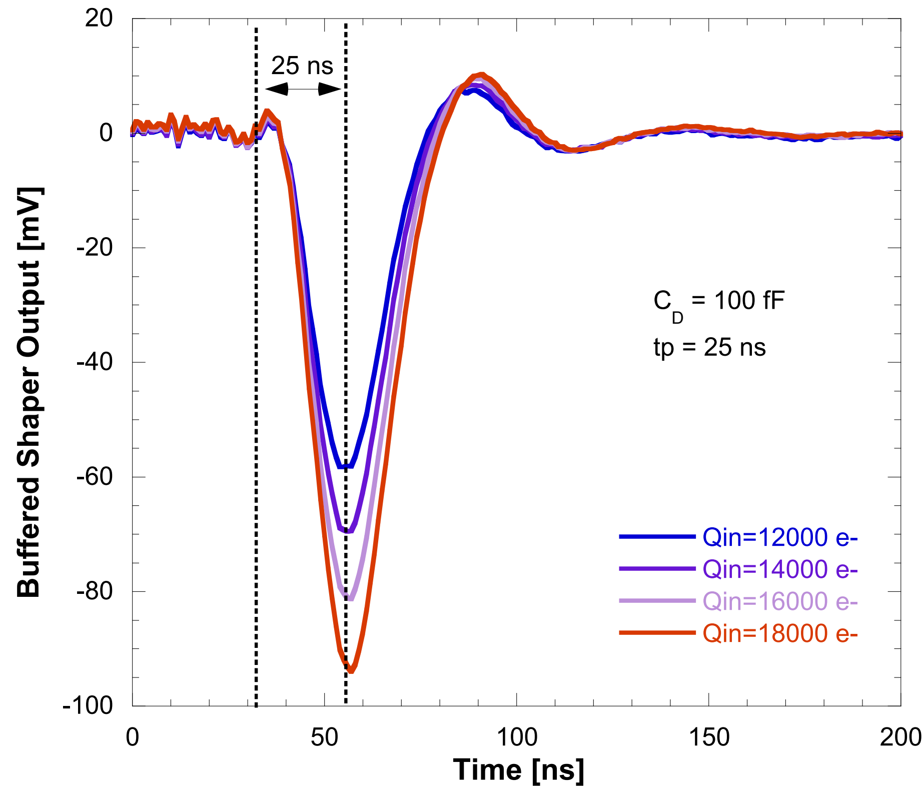
8x8 DNW MAPS matrix
- digital outputs
- outputs of the shapers can be accessed through row and column decoders and read out one at time

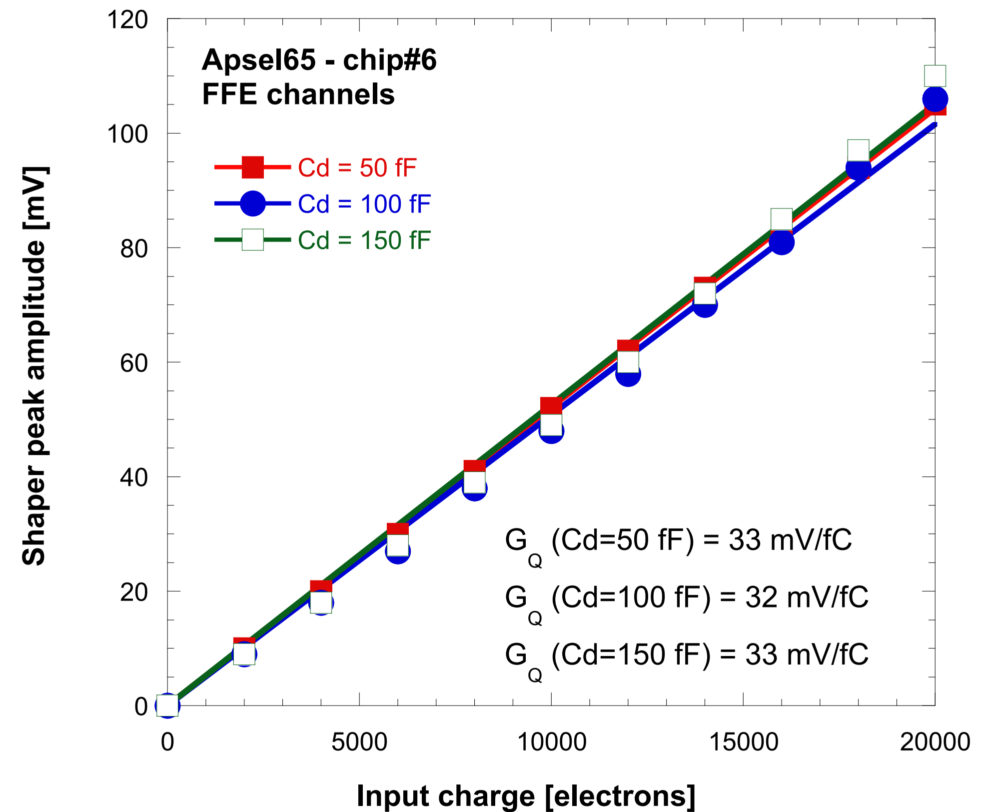
3 standalone channel with Cinj and detector simulating capacitor (250 fF, 350 fF, 450 fF)

3x3 DNW MAPS matrix
- 9 analog outputs
- Digital output of the central pixel
- Cinj on central pixel



Fast Front-End standalone channels





- **Peaking time** (at analog buffer out) is close to 25 ns
- **Charge sensitivity** has an average value of 33 mV/fC. Since output buffer gain ≈ 0.89 → G_Q @ shaper output is close to 37 mV/fC (42 mV/fC simulated)
- **Noise:** ENC=214 e^- rms (204 e^- rms simulated)

Apsel65 DNW MAPS

Main design features

-W/L PA input device: 28/0.25

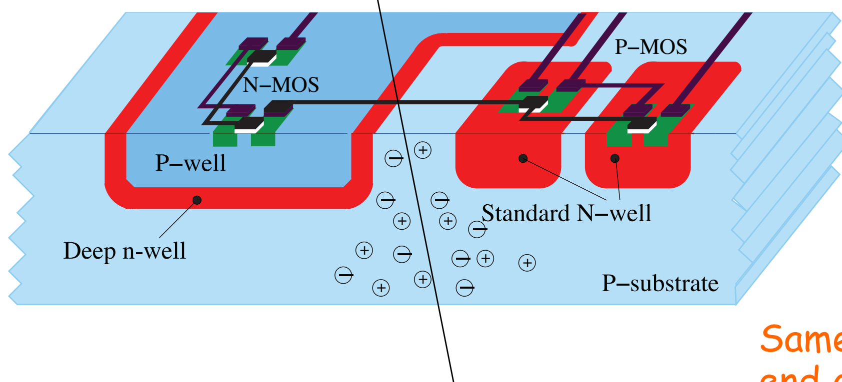
- Power consumption: 20 μW/cell

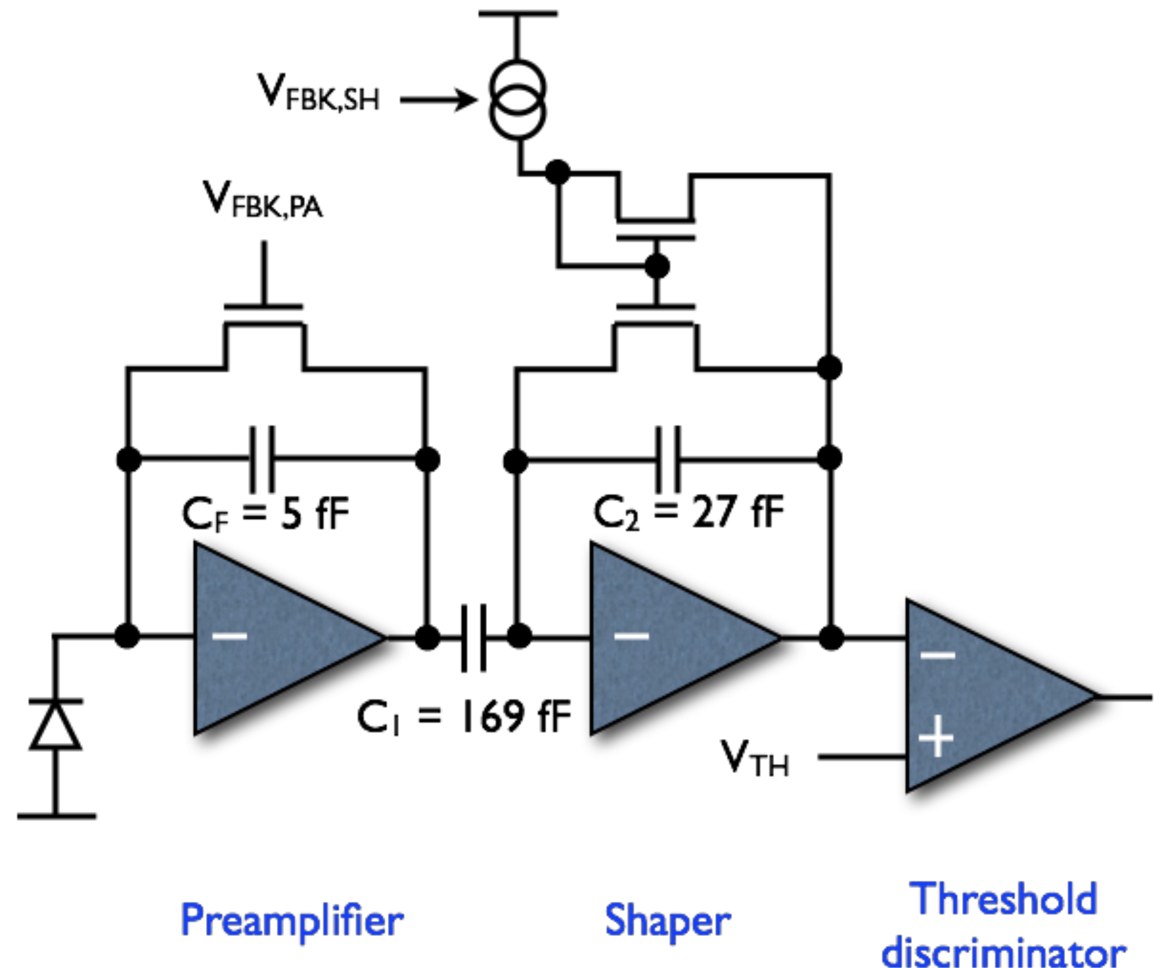
- Equivalent noise charge: 38 e^-

- Threshold dispersion: 38 e^- (main contributions from shaper input device and NMOS and PMOS pair in the discriminator)

- Charge sensitivity: 725 mV/fC

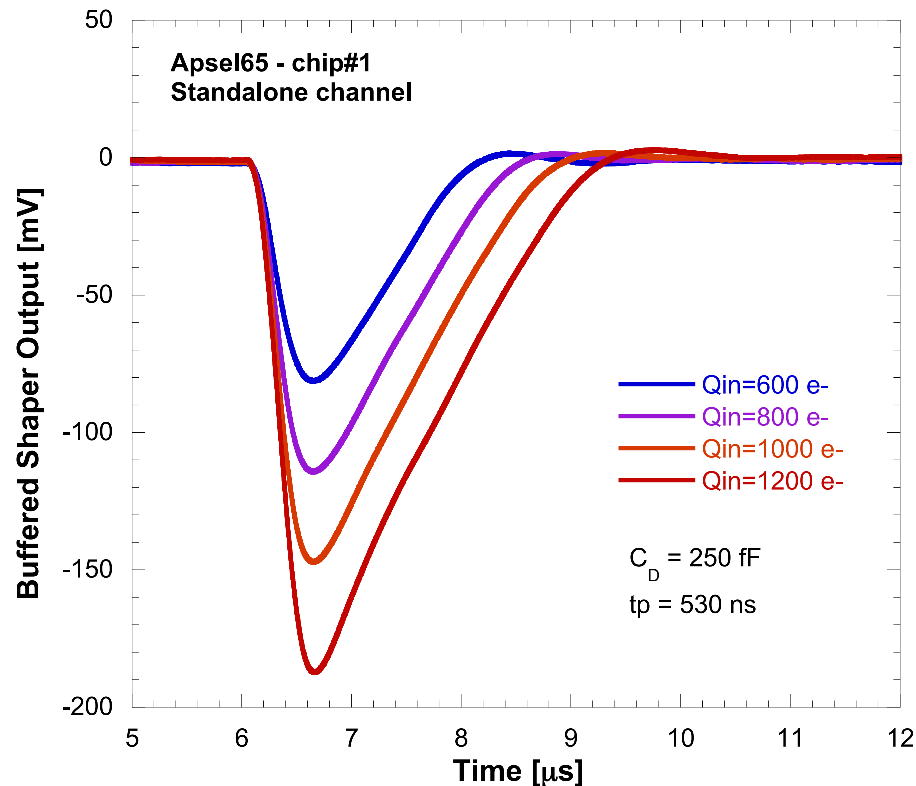
- Peaking time: 300 ns

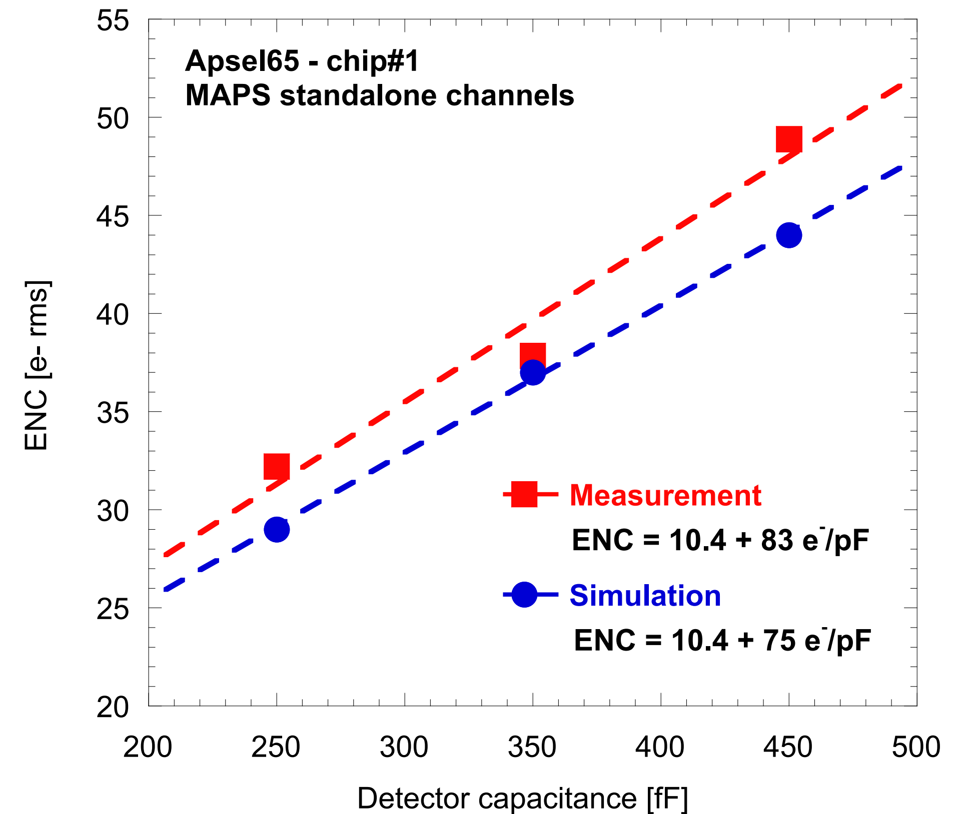




Same readout scheme (except for components value) for the fast front-end channels which were designed according to the typical specifications associated with the readout of fully-depleted pixel sensors (tp = 25 ns)

Standalone DNW MAPS

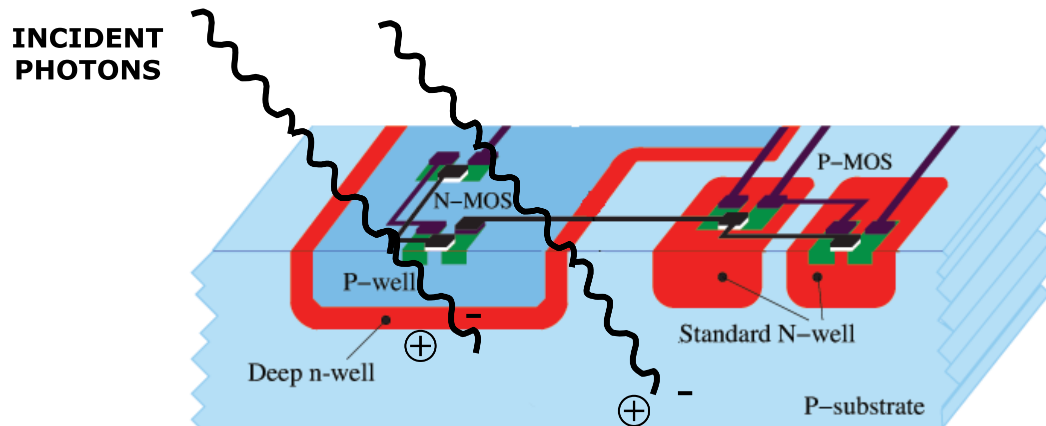


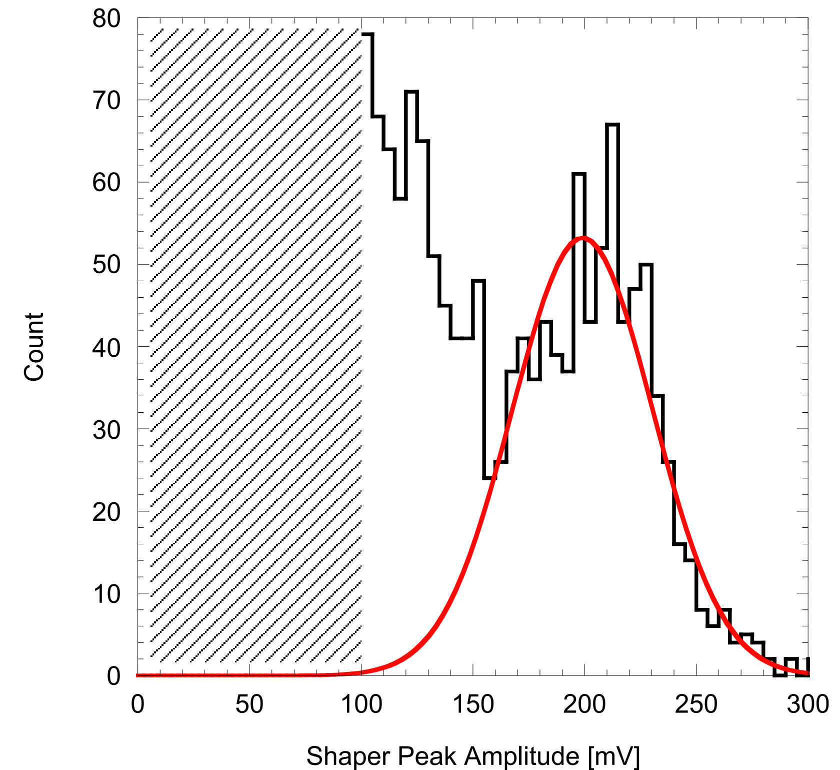


- **Peaking time** (at analog buffer out) is close to 530 ns (for Qin=800 e^-) - Simulation data: tp=300 ns at shaper out, tp=400 ns at buffer out
- **Recovery time** increases linearly with the signal amplitude (C2 discharged by a constant current source)
- **Charge sensitivity** has an average value of 760 mV/fC (725 mv/fC simulated)
- **Measured ENC** is about 10% higher with respect to simulated values

^{55}Fe measurements

- **Soft X-ray from ^{55}Fe source** (5.9 keV) used to calibrate pixel gain in channels with no injection capacitance



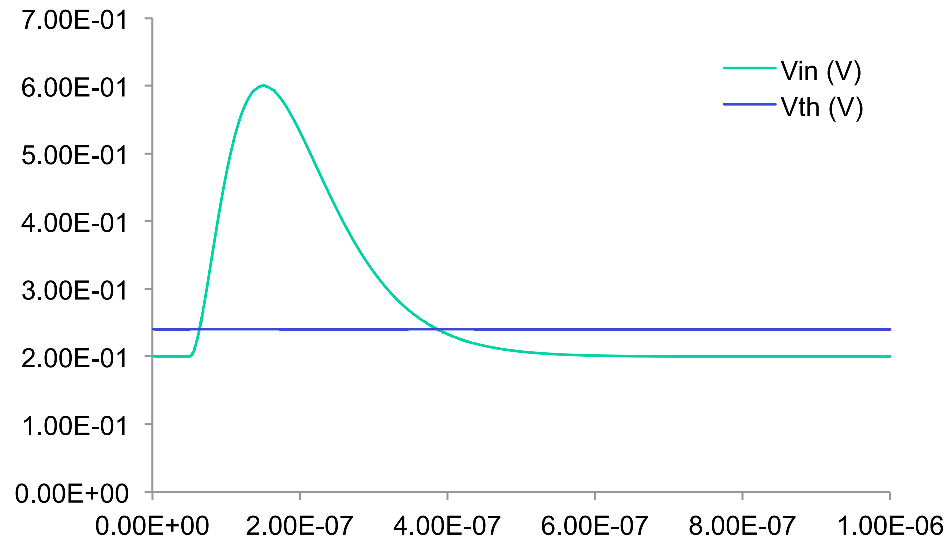


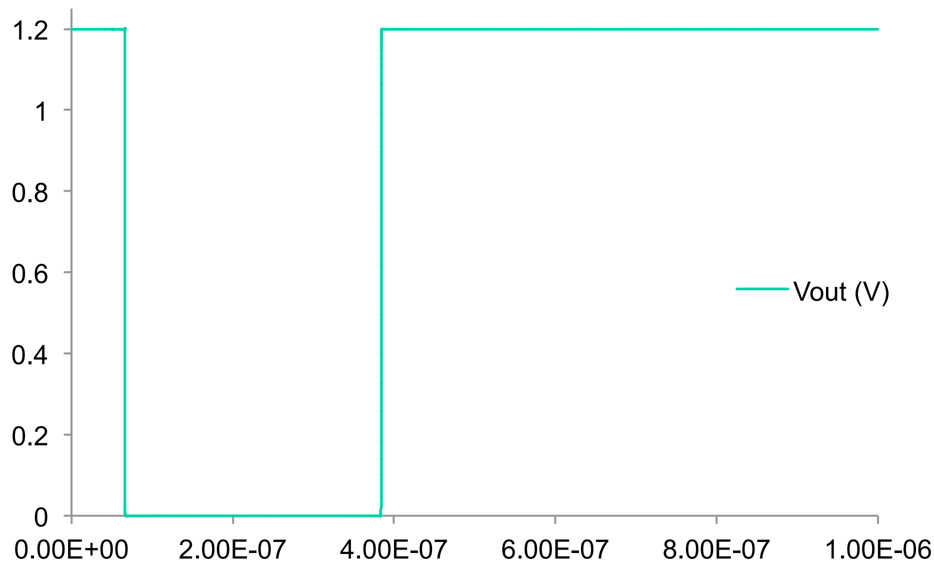
- 5.9 keV line ≈ 1640 e/h pairs
- With charge **entirely collected** clear peak @ 200 mV → G_Q = 760 mV/fC
- Using ^{55}Fe gain calibration: pixel noise 4.6 mV → ENC=38e$^-$ rms

Low power, high speed threshold discriminators

- Discriminators compatible with applications in high granularity pixel detectors
  - CMOS 65 nm TSMC technology
  - low power (< 10 uW), high speed (no more than a few ns delay), small area (fitting in a 50 um pitch pixel, of course together with the other analog and digital blocks), low threshold dispersion (not larger than the noise)
- Twofold purpose
  - minimize the impact of the discriminator delay on hit time resolution in tracking detectors
  - avoid non-linearity at small input charge values in the channel response as seen by the digital section
- Two architectures have been evaluated (classical preampli+shaper analog front-end is assumed)
  - differential stage with mirror load (directly driven by the shaper output)
  - transimpedance amplifier (driven by the shaper output through a transconductor)
- Best trade-off among the above mentioned specifications can be reached by including a 5-bit threshold correction circuit

Low power, high speed threshold discriminators





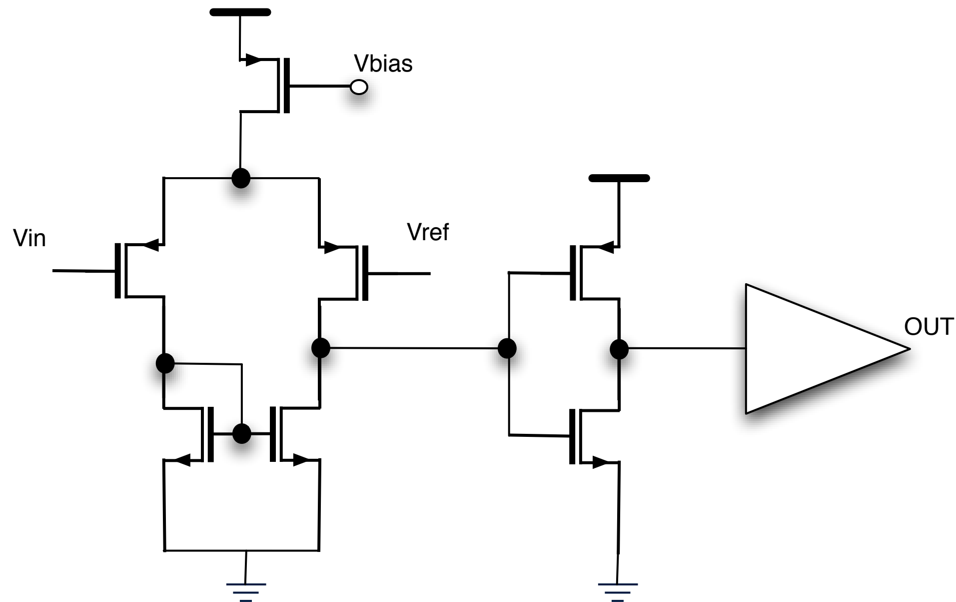
- Analog front-end specifications:

  DC voltage at the shaper output: 200mV
  Output dynamic range: 800 mV
  Threshold voltage: 240 mV
  ENC: 150 electrons

- Parameters of interest: delay (Δt, defined as **t(***Vout exceeds 600 mV***)-t(***Vin exceeds Vth***)**, threshold dispersion (σ_{th}), power dissipation (P)

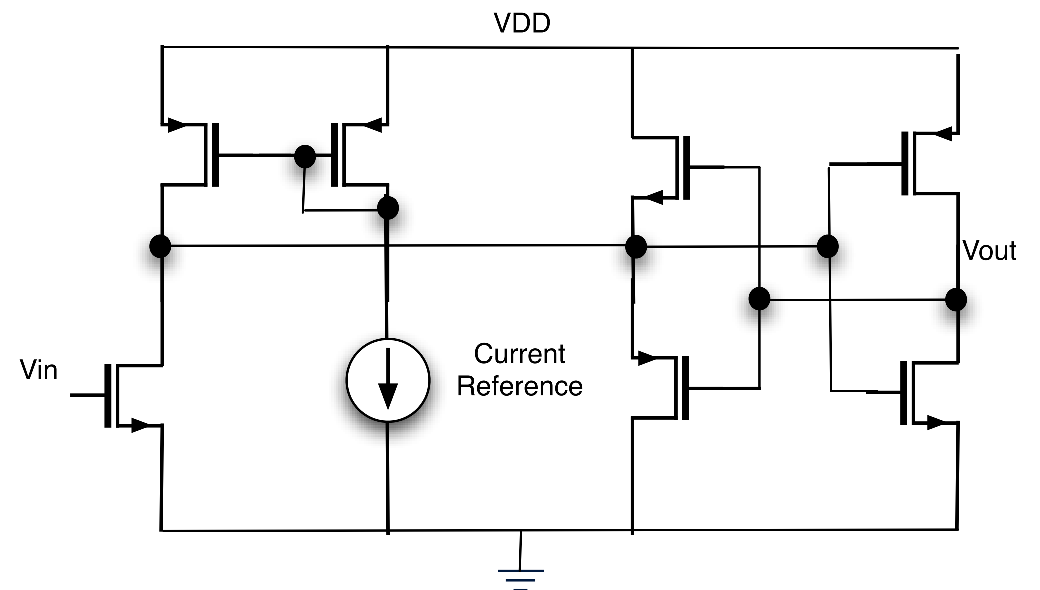
- A figure of merit M is defined as $\Delta t \times \sigma_{th} \times P$

Discriminator architectures



Voltage discriminator

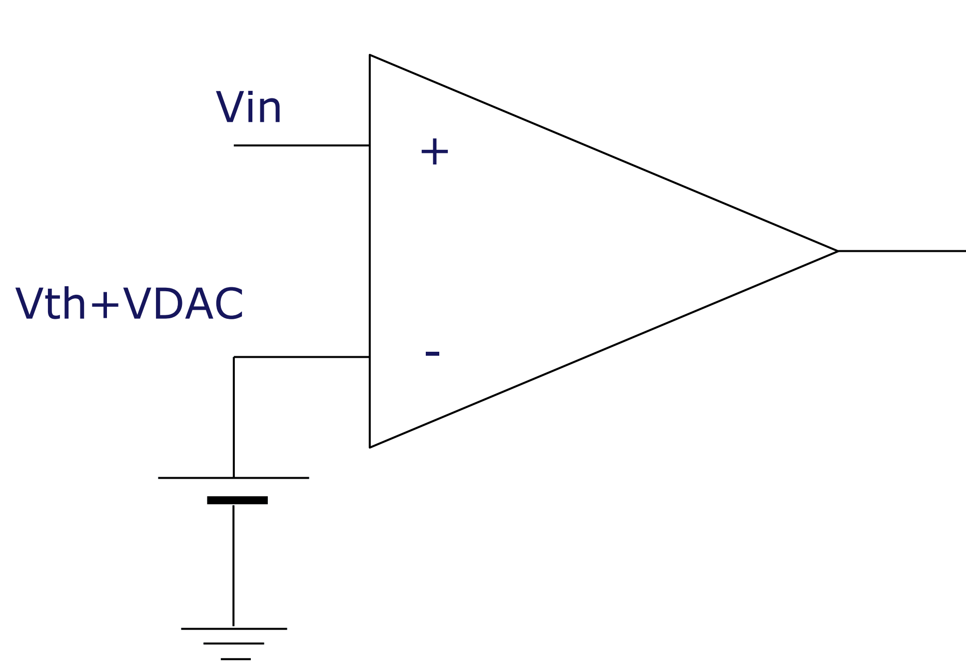
Current discriminator

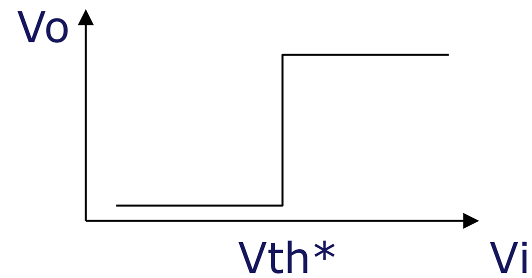


Some results for the voltage discriminator

Version		Delay [ns]	Dispersion [mV]	Current [uA]	FOM
1 uA	HS	5.04	10.09	1.00	50.87
	MD	12.94	2.87	1.00	37.11
	LD	18.32	1.71	1.00	31.35
2 uA	HS	1.26	15.27	2.00	38.41
	MD	4.67	5.58	2.00	52.09
	LD	13.83	1.45	2.00	40.07
5 uA	HS	1.53	8.97	5.00	68.54
	MD	5.37	2.96	5.00	79.43
	LD	11.42	1.37	5.00	78.00
10 uA	HS	0.69	8.21	10.00	56.54
	MD	2.09	3.10	10.00	64.61
	LD	7.15	1.98	10.00	141.17

Threshold correction circuit





- 5 bit DAC
- Correction Factor≈0.057@DAC Range≈6σ