Vertical integration of heterogeneous layers with T-Micro and INMAPS sensor substrate thinning with Aptek

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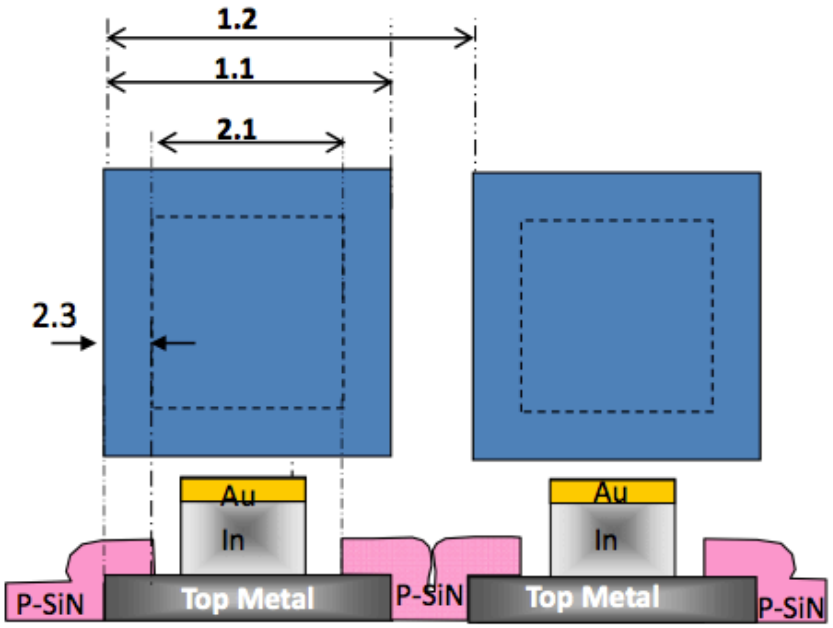
Vertical integration with T-Micro

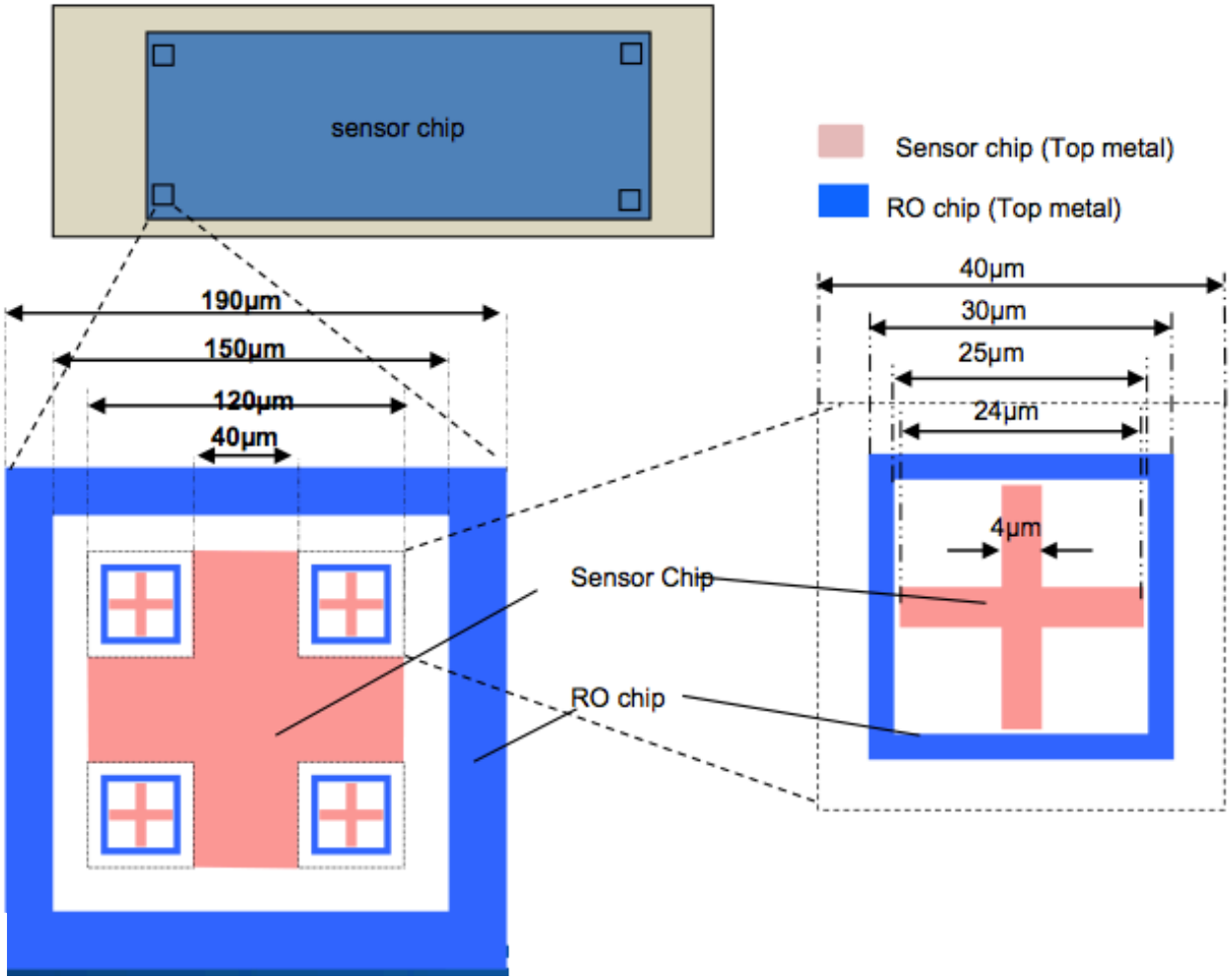


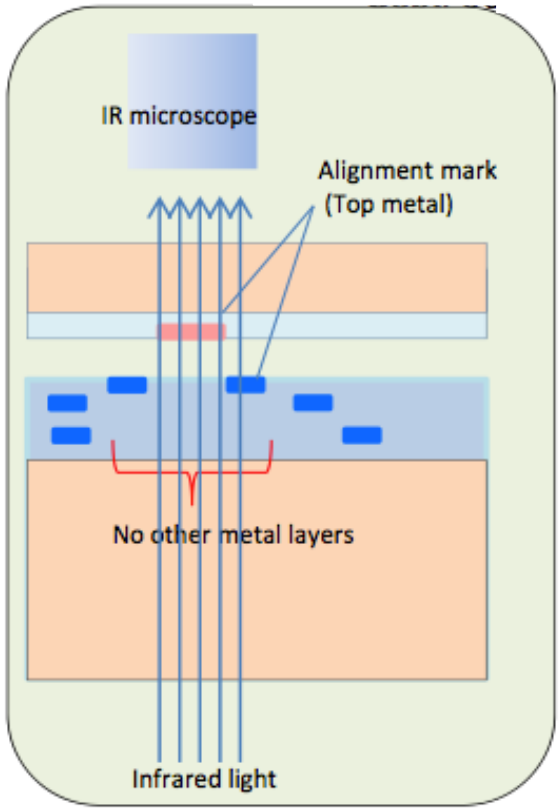
- Very high interconnect density, with small bond pads (squares with a side of 5 or 10 μm, depending on the bump size, 2x2 μm^2 or 8x8 μm^2) both on the sensor and the readout sides ➔ more room for top metal routing, in particular for power and ground lines, smaller capacitive coupling, less material

Minimum size	DR1 8x8um bump	DR2 2x2um bump
1. Top metal (Landing pad of bump)		
1.1 size	12 um	4um
1.2 pitch	15um	5um
1.2' Pitch (dummy pad)	15um	5um
1.3 minimum space to scribe edge	10um	10um
2. Pad opening		
2.1 size	10um	3um
2.2 pitch	15um	5um
2.3 minimum pad overlap of pad opening	1um	0.5um

Alignment rules

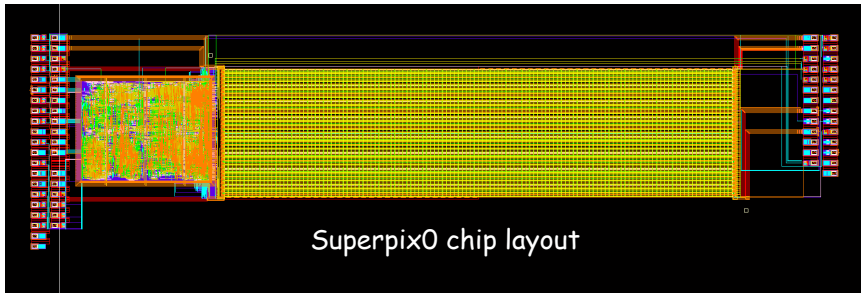
- Markers for rough and fine alignment (through IR imaging), apparently not mandatory

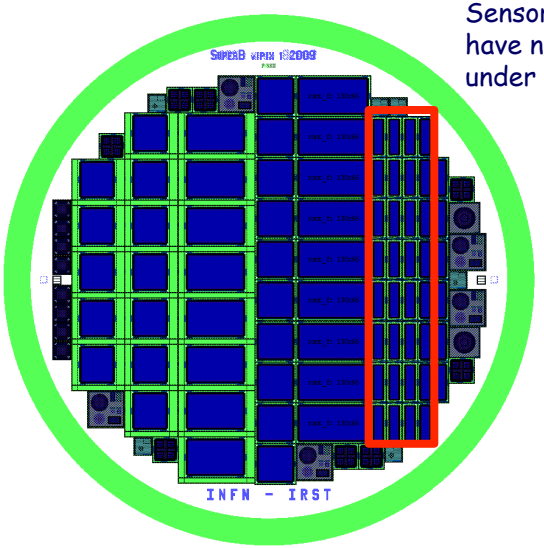




Vertically integrated layers

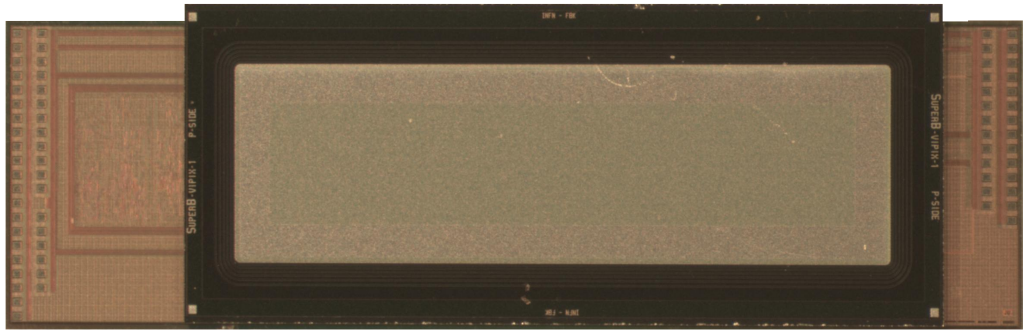
- Preliminary test of the T-Micro integration process performed on pre-existing readout chips (Superpix0) and high resistivity n-on-n pixel sensors (VPix1)





Sensors in the red box have no metal layers under the markers

- Front-end chips and a pixel sensor wafer shipped to T-Micro in Dec. 2012
- 5 vertically integrated chips now waiting for customs expenses to be paid



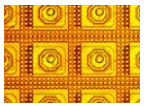
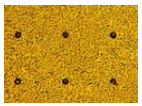
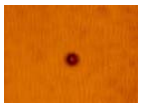
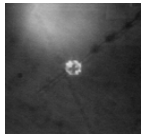
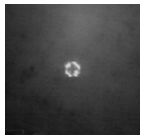
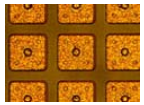
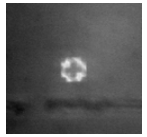
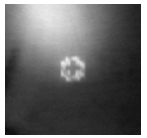
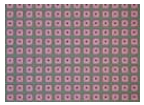
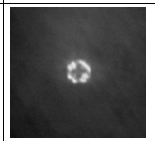
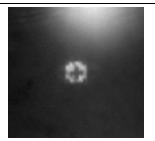
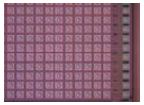
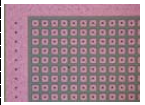
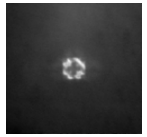
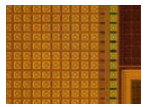
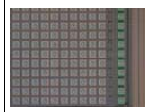
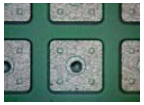
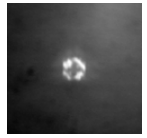
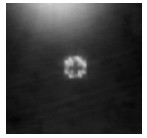
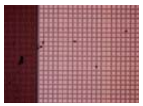
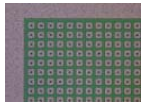
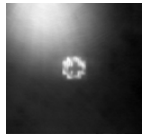
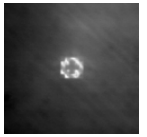
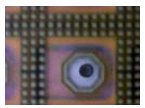
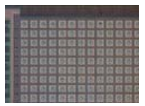
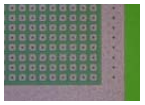
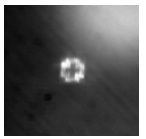
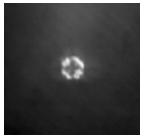
- Recall that a few samples of Superpix0 readout chips and VPix1 sensors have already been bump bonded with IZM

Surface inspection and alignment

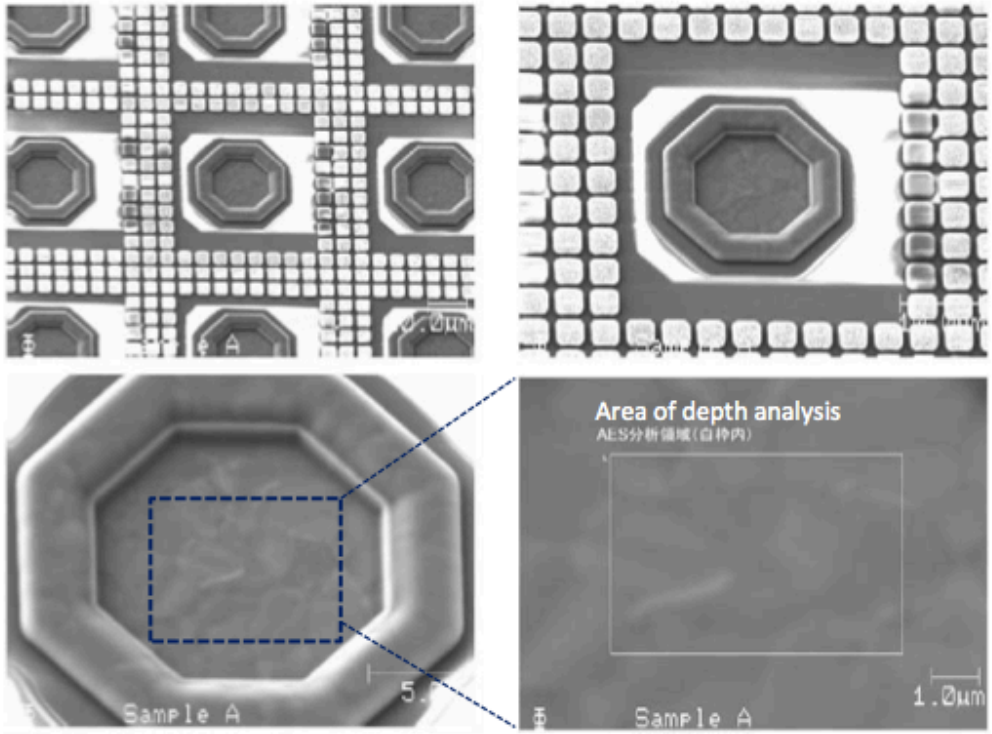
T-Micro

Result of Chip stacking

February 28,2013

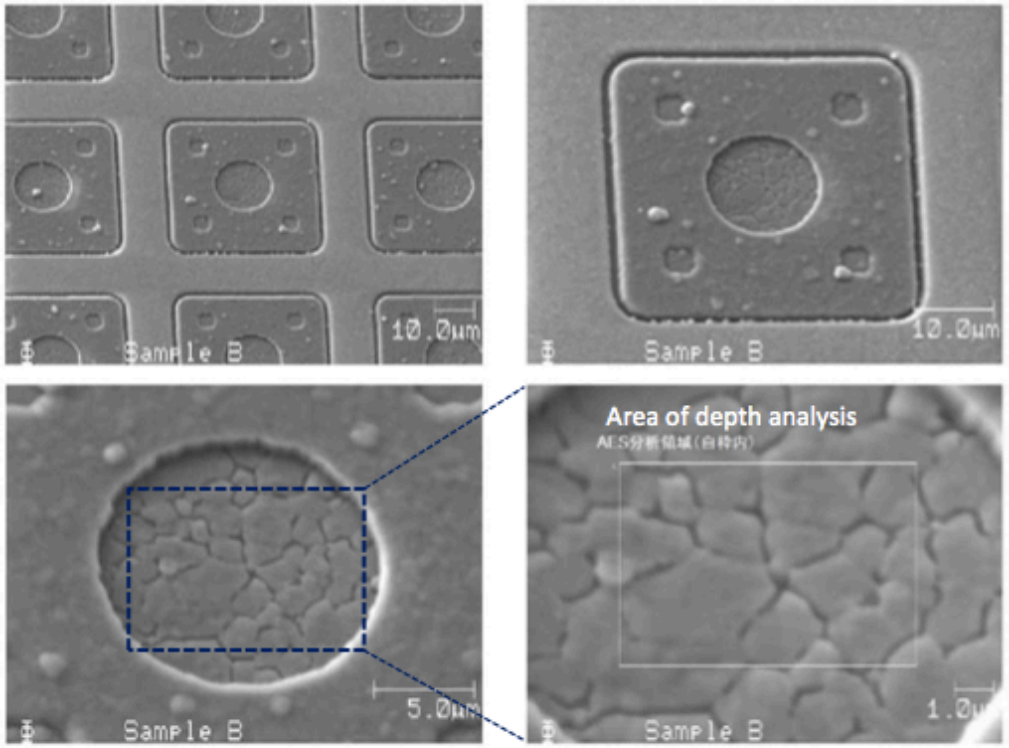
	after surface treatment (cleaning)		after bump lithography		after bump formation		after Stacking	Remarks
	ASIC Chip	Sensor Chip	ASIC Chip	Sensor Chip	ASIC Chip	Sensor Chip	(Two alignment mark images using IR microscope)	
Chip_01							 	Only for process optimization (in another chip tray with broken chips)
Chip_02							 	
Chip_03							 	
Chip_04							 	
Chip_05							 	
Chip_06							 	large alignment error
Chip_07							 	

Auger electron spectroscopy (AES analysis)

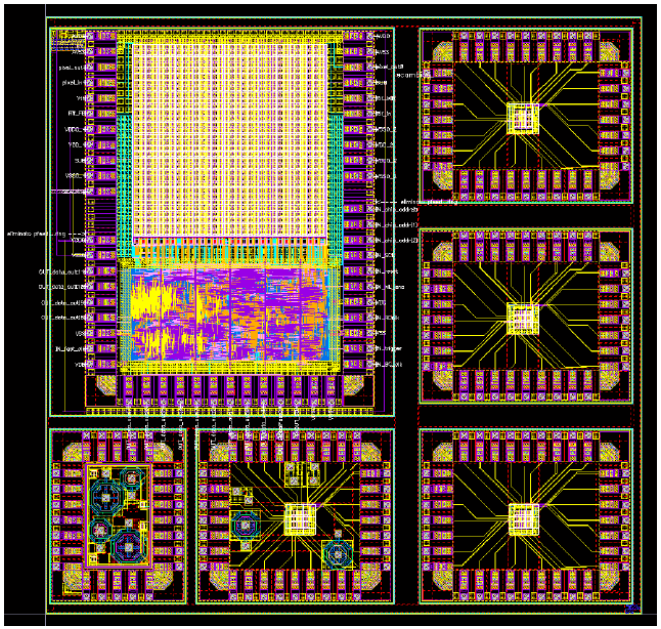


ASIC chip

Sensor chip



INMAPS chip thinning



- The aim is to understand whether and how the collection properties of quadruple well MAPS are changed by thinning the substrate (low material budget)
- Metallize (if needed) the chip backside after processing, try and increase depleted volume by uniformly applying a negative voltage to the backside

Processed chips

Codice	Numero	Descrizione del Chip
APS-12-HR	16	Chip Apsel4well con substrato di 12 um ad alta resistività
APS-12-LR	16	Chip Apsel4well con substrato di 12 um a bassa resistività
APS-05-LR	30	Chip Apsel4well con substrato di 5 um a bassa resistività

Chip thickness after processing

Numero	Codice Chip	Spessore finale [um]
10	APS-12-HR	25
10	APS-12-LR	25
6	APS-12-HR	50
6	APS-12-LR	50
15	APS-05-LR	25
15	APS-05-LR	50
5	MIMO	50