SOI Technology for High Energy Physics Applications

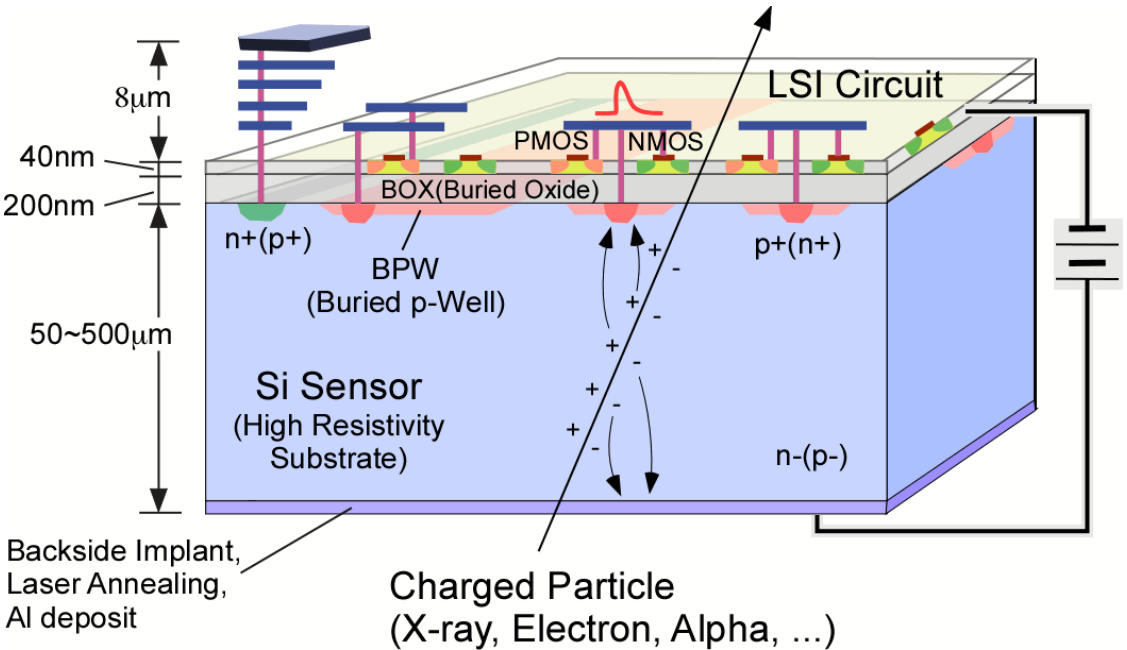
Akimasa ISHIKAWA

(Tohoku University)

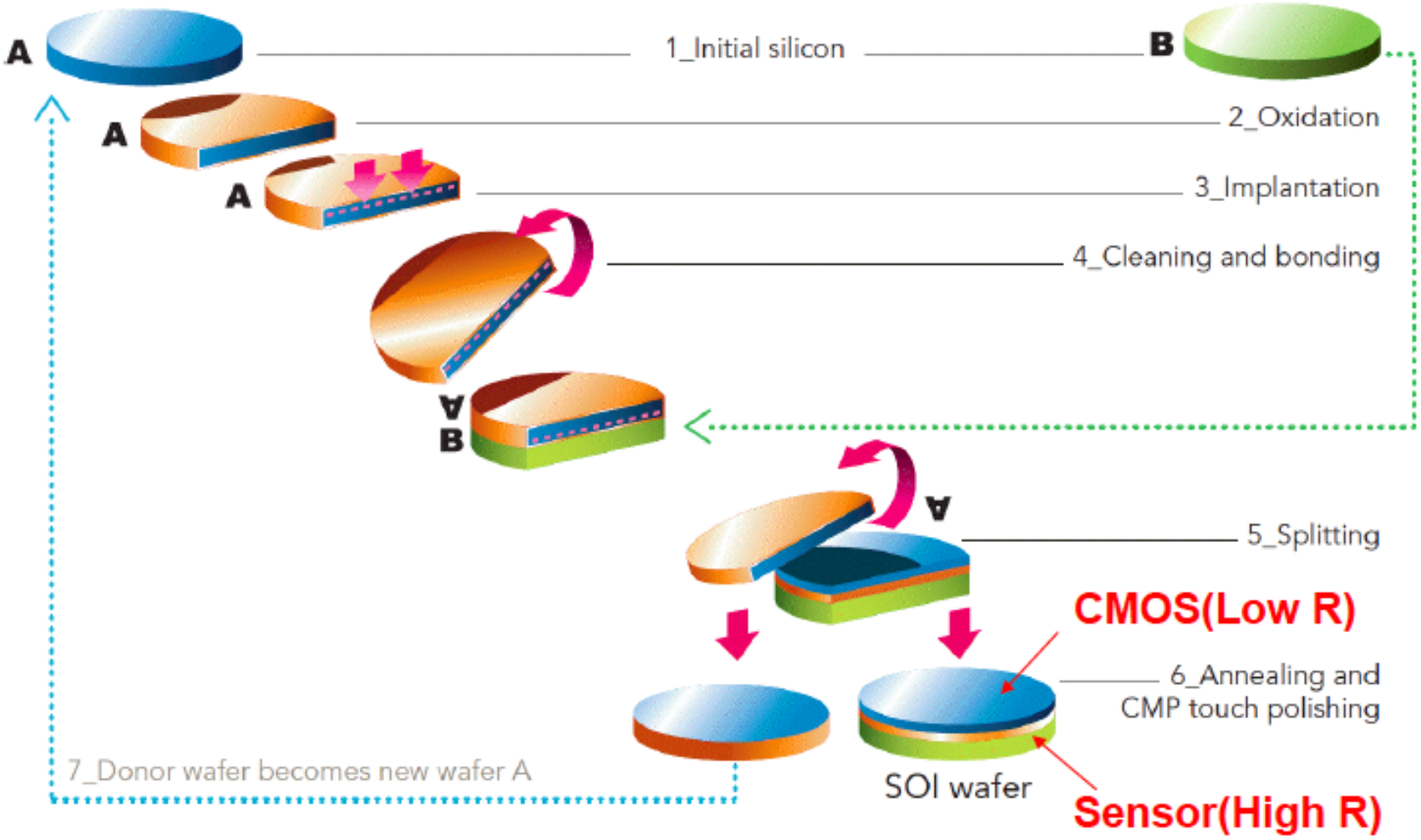
For the SOIPIX Collaboration

SOI Technology

- SOI detector is the monolithic detector which has sensor and data processing layers with a fine resolution
  - suitable for HEP.
- Silicon-on-Insulator (SOI) detector consists of three layers
  - Substrate Silicon sensor layer
  - Burried OXide layer (BOX layer)
  - Circuit CMOS layer

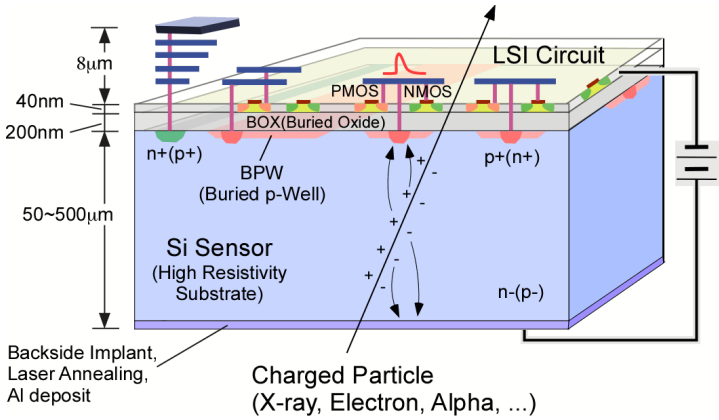


SOI Wafer Production (Smart Cut by SOITEC)



Feature, Pros and Cons of SOI for HEP

- Feature
  - No mechanical bonding for readout
  - On pixel processing with CMOS layer
  - Fully depleted sensor with low sense node C
- Pros
  - Small material → good resolution
  - Small pixel size → good resolution
  - Small parasitic capacitance → good S/N
- Cons
  - Back gate effect from sensor bias
  - Not-good radiation tolerance due to hole trapping in BOX layer
  - Crosstalk btw sensor and circuit
  - → these three can be solved by double SOI structure



Back gate effect can be also suppressed by Buried P-Well (BPW)

Three SOI Detectors for HEP

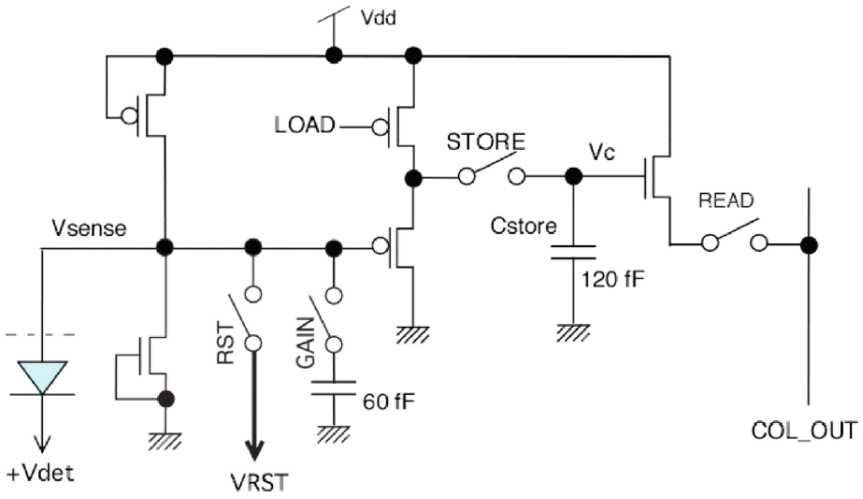
- INTPIX
  - General purpose integration type
- CNTPIX
  - General purpose counting type (Binary)
- PIXOR
  - Counting type (Binary)
  - aimed to replace the inner most layer of Belle II SVD
  - Intermediate structure of pixel and strip

Lapis Semiconductor Co Ltd. 0.2 μm FD-SOI pixel process

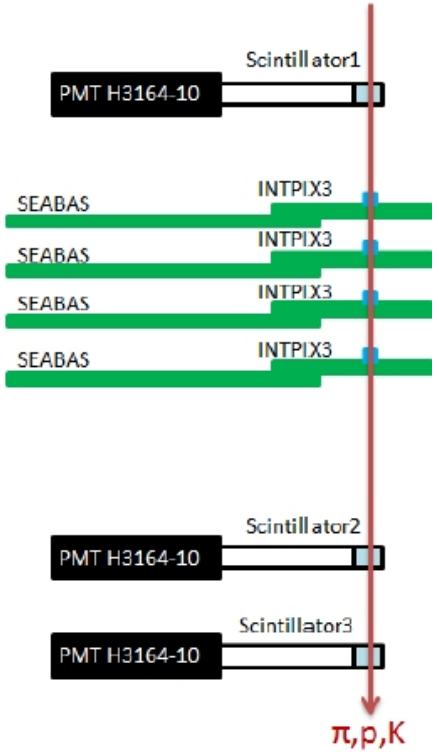
INTPIX

INTPIX

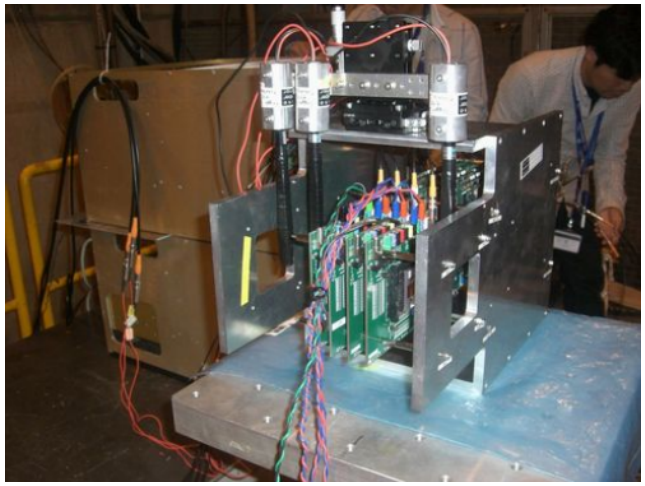
- Feature
  - Very simple data processing circuit, which consumes area, to reduce the pixel size for better resolution
  - Integration type
    - Smaller cross-talk
    - No timing information available ☹



INTPIX3e



- Parameters for INTPIX3e
  - Pixel size : 16um*16um
  - # of pixels : 192*192
  - Chip size 6mm*6mm
- Tested with high energy beam
  - 1GeV electron beam at Tohoku in 2010
    - Measurement of charged particles tracks with SOI for the first time.
  - 120GeV hadron beam at CERN SPS in Fall 2011
    - Multiple scattering effect can be ignored
    - Two types are tested
      - Thick sensor 260um
      - Thin sensor 100um
    - 4layer-configuration

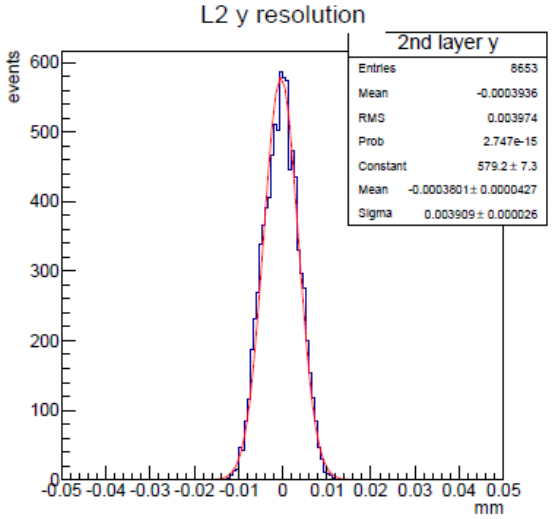


Beam Test Results for INTPIX3e

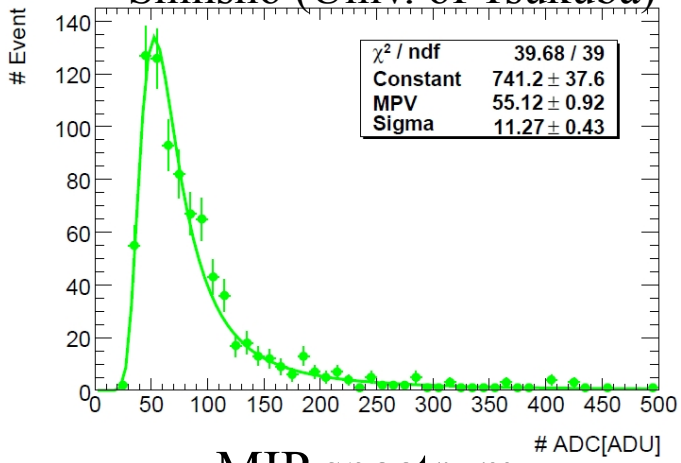
- Resolution with thick one
  - resolution achieved is 3.9um
    - Worse than expected
  - But we know that calibration was imperfect and could improve the resolution

- S/N with thin one
  - Thinned to 50um by Nihon Exceed Co.
  - S/N = 15

Katsurayama (Tohoku Univ.)



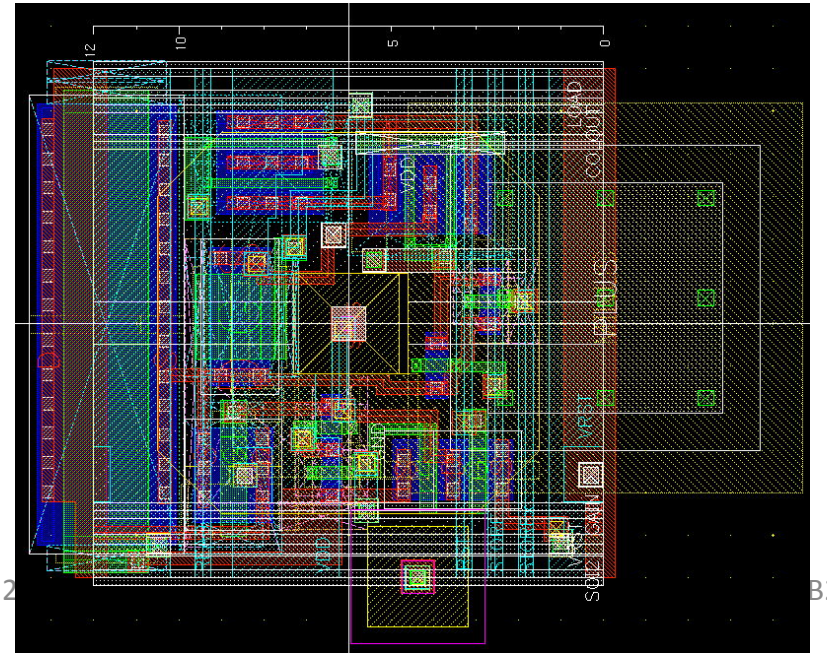
Shinsho (Univ. of Tsukuba)

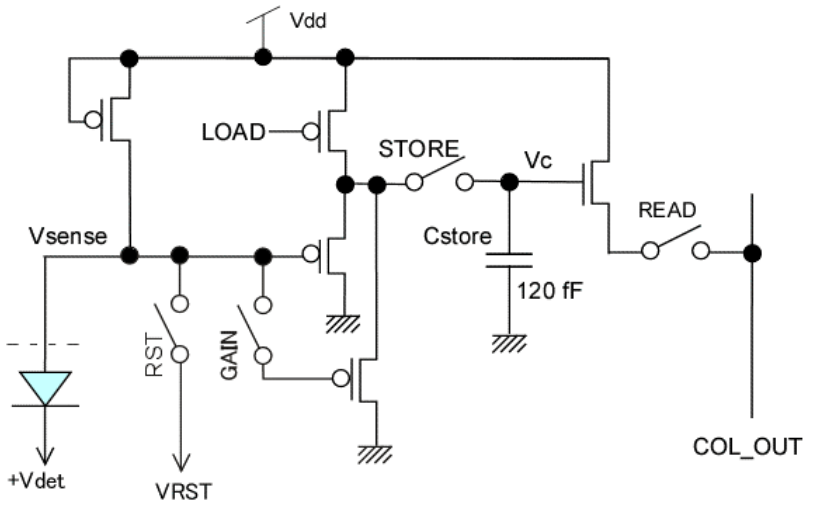


MIP spectrum

INTPIX6

- The newest version of INTPIX series submitted on Jan 2013
  - Pixel size : 12um*12um
  - # of pixels : 896*1408
  - Chip size : 12.2mm*18.4mm
- Smaller pixel size and larger chip
  - Aiming 1~2um resolution

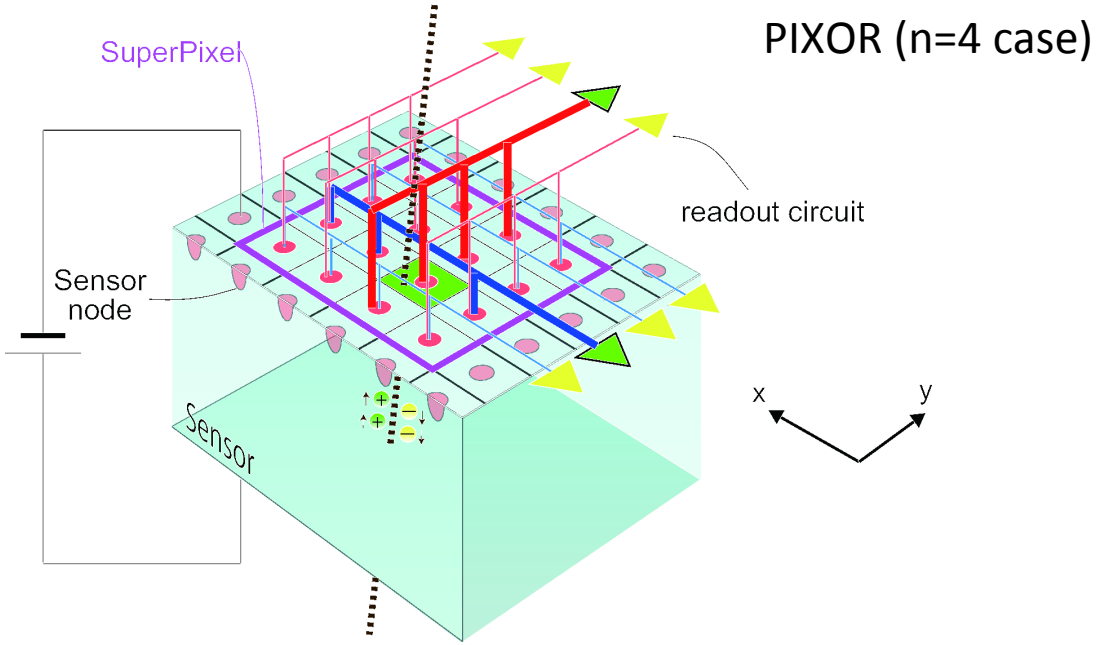




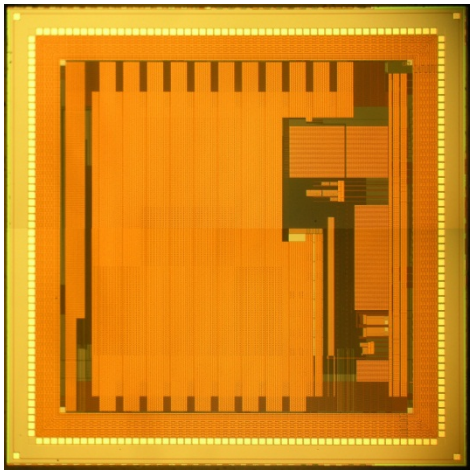
PIXOR

PIXOR

- The PIXOR (PIXel OR) readout scheme
  - In a small n by n pixel matrix (called Super-Pixel, n^2 channels), an analog signal from each pixel is divided into two directions (x and y).
  - N channels from n pixels in each directions are taken analog OR and processed by the circuit on the matrix in order to reduce readout channels (n^2 → 2n channels), and to make the pixel size smaller.
- Intermediate structure of pixel and strip



PIXOR1

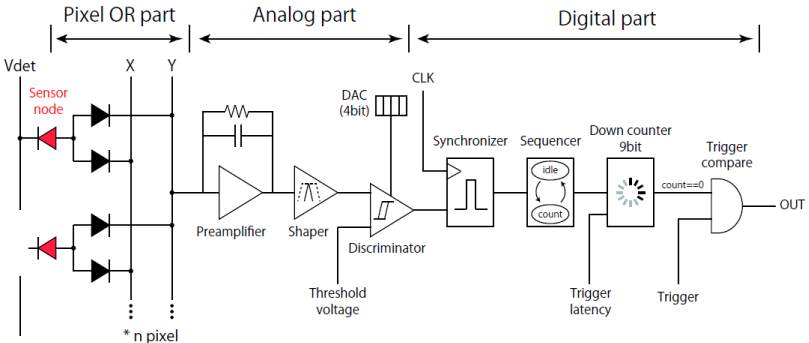


PIXOR1 Chip

- We have designed the first PIXOR chip

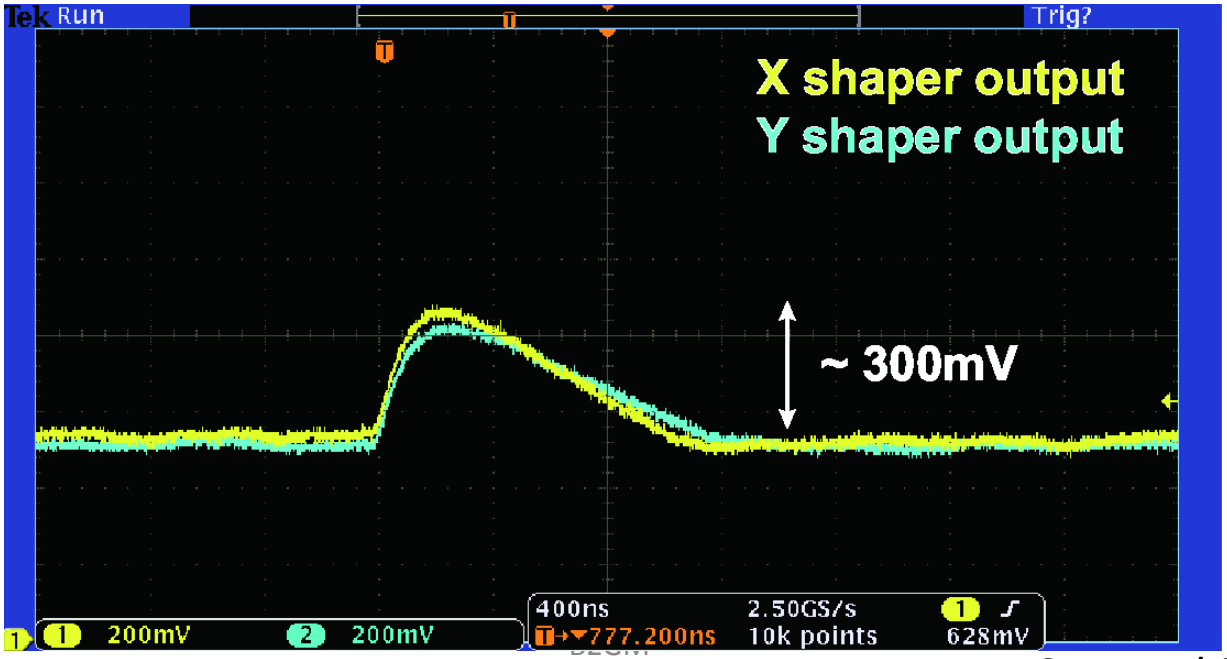
pixel size	25um*40um
# of “OR”ed channels	16
# of pixel in chip	5632
Chip size	5.6mm*5.6mm
trigger latency	5us

- Several TEGs (Test Element Group) in the chip
  - Analog/Discriminator signal-out from each “OR”ed channels.
  - Hit counter synchronized with clock and waits trigger signal for data transfer
    - All digital circuits are not on the pixel unfortunately.



PIXOR1 Analog readout

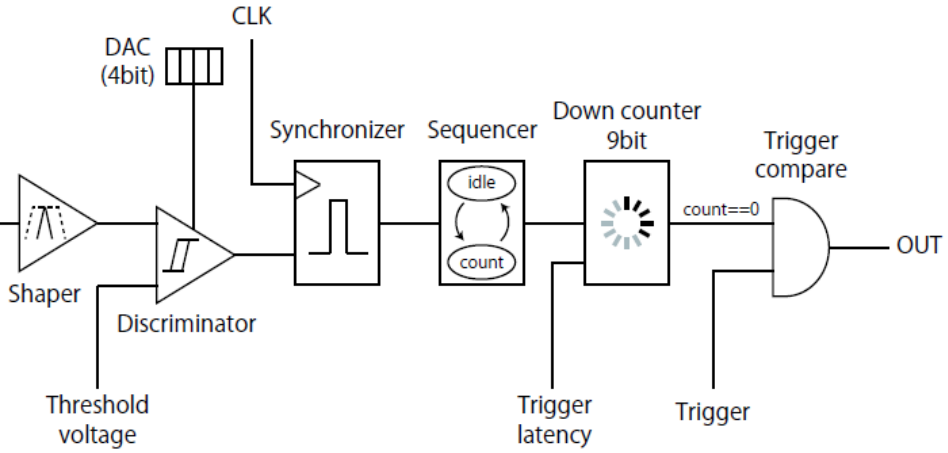
- Analog signals after pre-amp and shaper are checked with X-ray from Cd109
  - Almost same charges are readout with X and Y readout
- PIXOR scheme working fine!

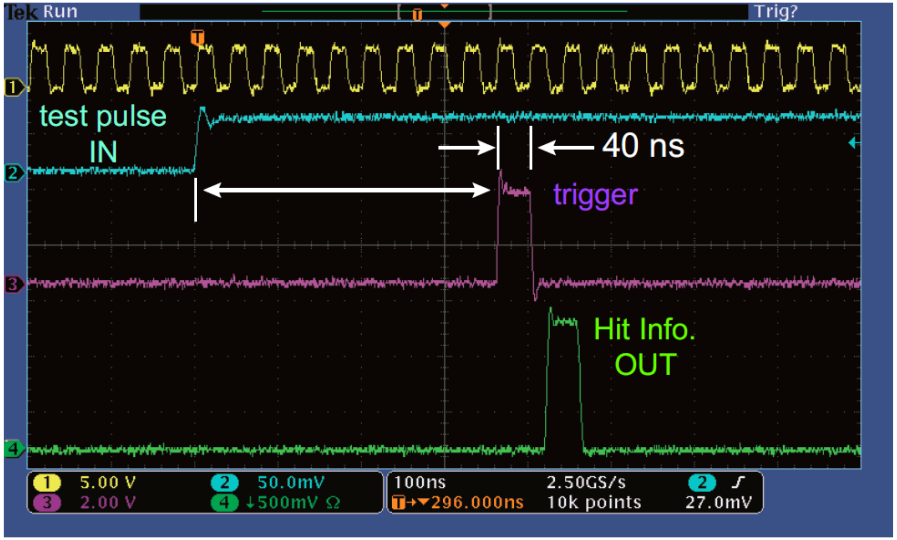


Sensor thickness 260um

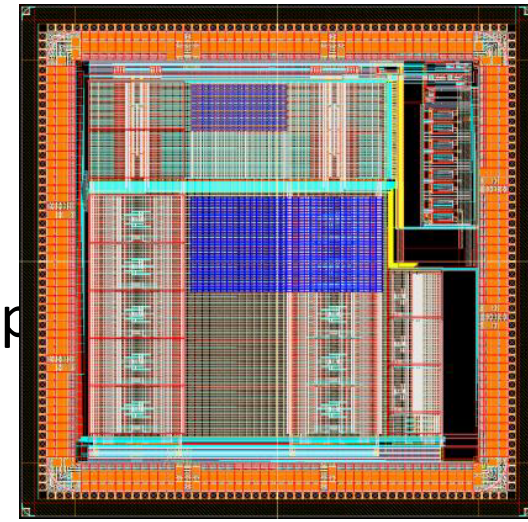
Trigger Logic

- Hit information after discriminator is stored in the buffer
- The nine-bit down counter starts counting the trigger latency time
- After the trigger latency, the hit information and trigger signal are compared, then the AND signal are sent to DAQ system.

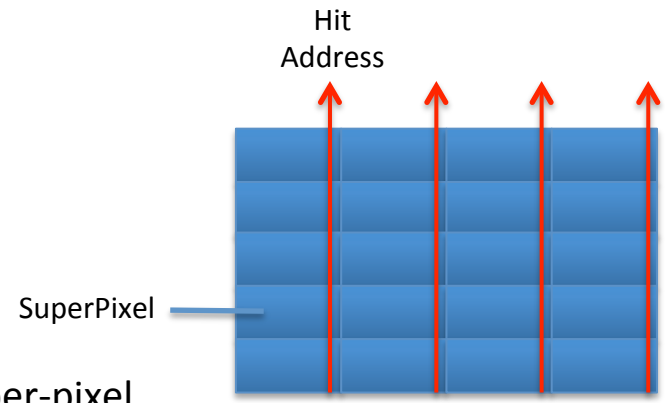




PIXOR2



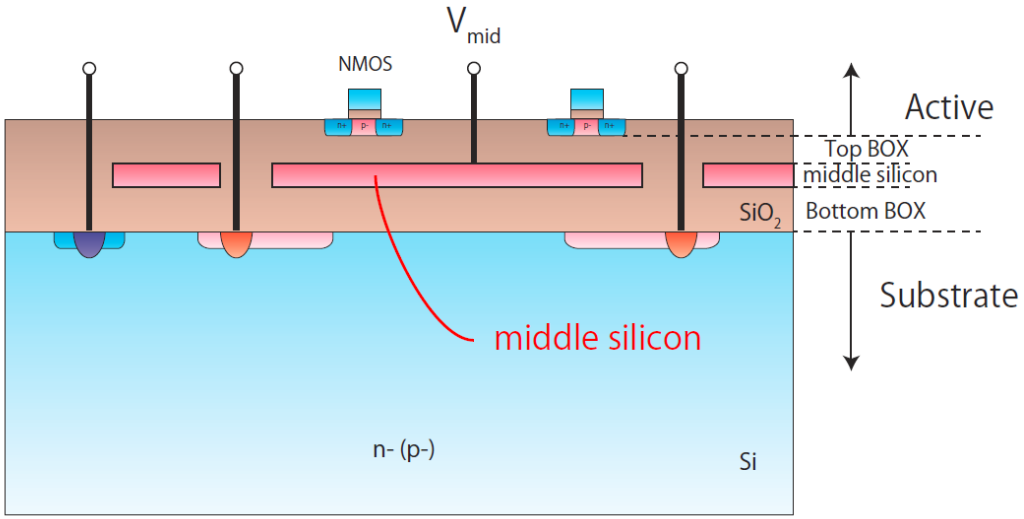
- PIXOR2 is designed for much more realistic chip
  - Only fired channels send hit address information
  - All digital circuit are on the pixel
- Parameters
  - Pixel size : 35um(r-phi)*70um(z)
    - The resolution should be 10um*20um
  - Size 6.3mm*6.3mm
  - # of “OR”ed channels : 16
- Added functionalities
  - Two hit counters
    - For multi hits in trigger latency
  - Address readout to speed up
    - Address in Super-PIXEL and Address for the Super-pixel
  - Mask-off capability



Double SOI Structure

Double SOI Wafer

LAPIS SEMICONDUCTOR

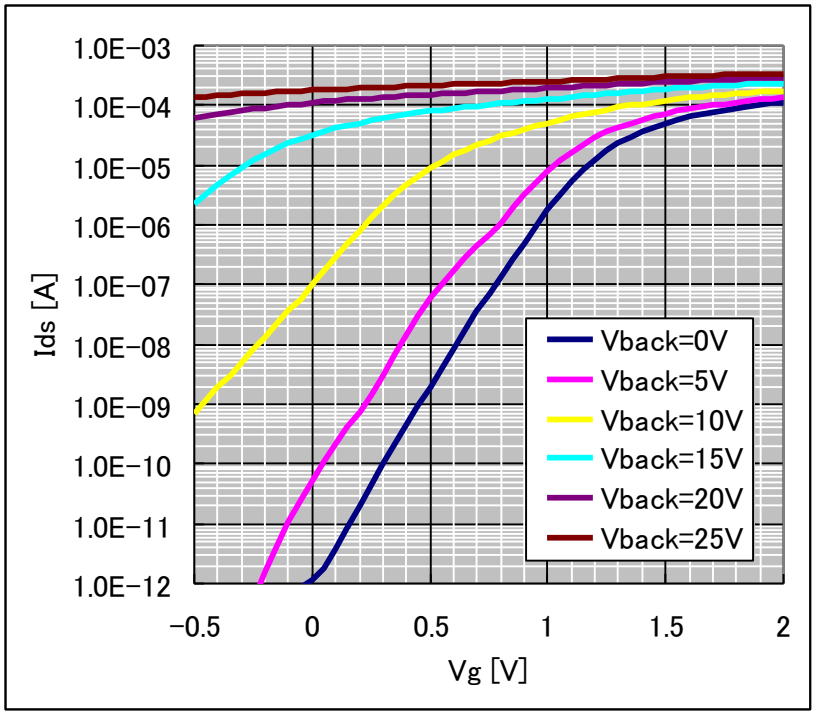


additional conduction middle silicon layer in BOX layer

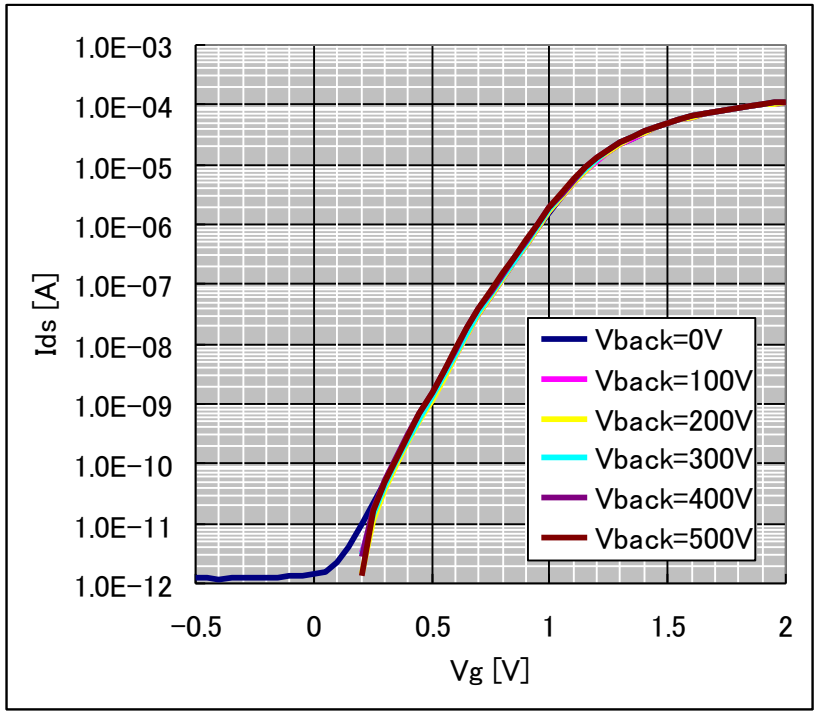
- Back gate effect
  - Shield transistors from bottom electric field
- Radiation Tolerance
  - Compensate electric field generated by the trapped hole in the BOX.
- Crosstalk
  - Reduce crosstalk between sensors and circuits.

Suppression of Back-Gate Effect with Middle-Si layer

a) Middls-Si Floating



b) Middle-Si = GND



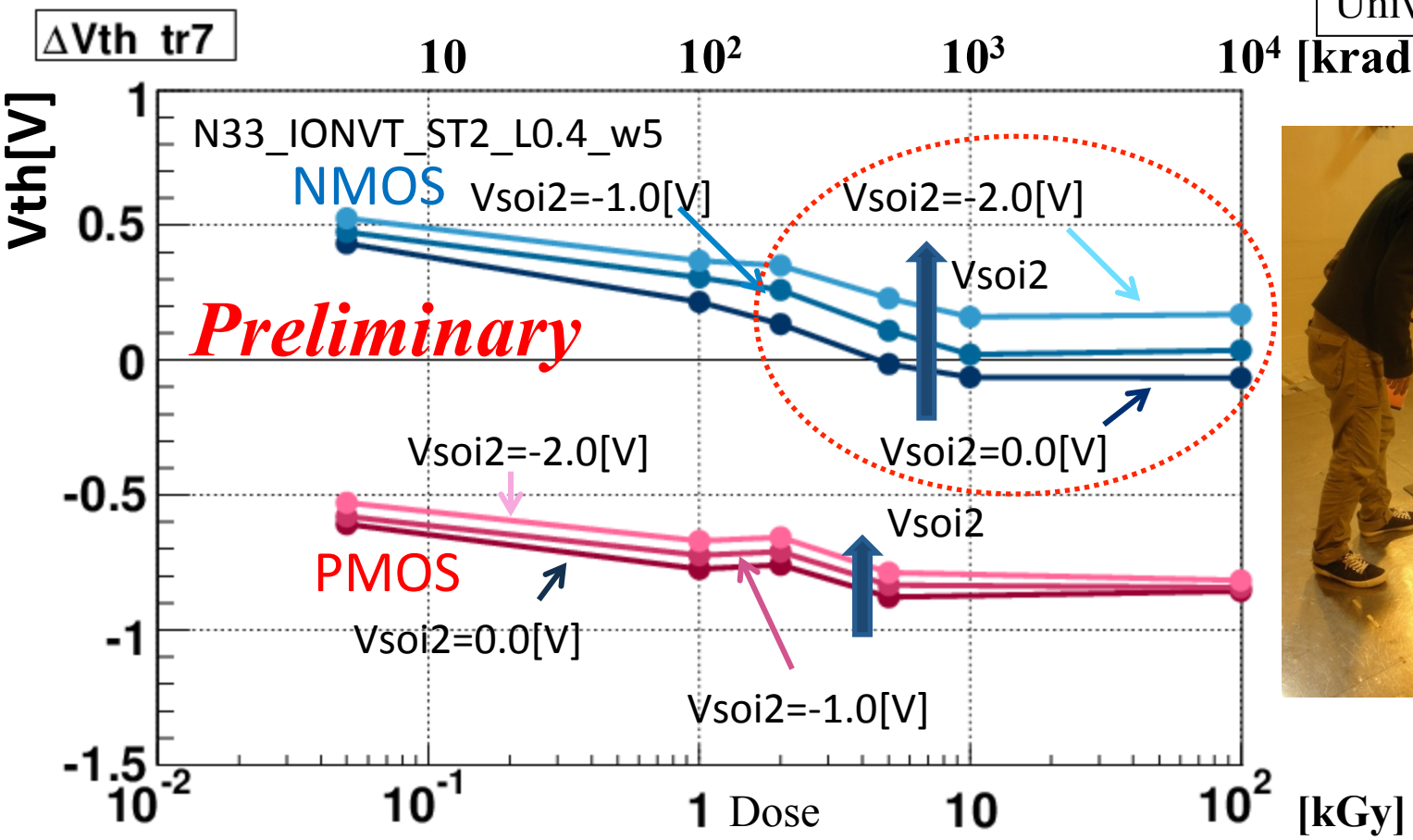
Back-Gate Effect is fully suppressed with the Middle Si Layer of fixed voltage.

Nch Core Normal-Vt
L / W = 0.2 / 5.0um
Vd=0.1V

Co-60 gamma-ray TID test @ JAERI/Takasaki

Double SOI Test Element Group (TEG) chip (AIST & KEK)
During irradiation, all the contacts are set to GND.

Univ. of Tsukuba

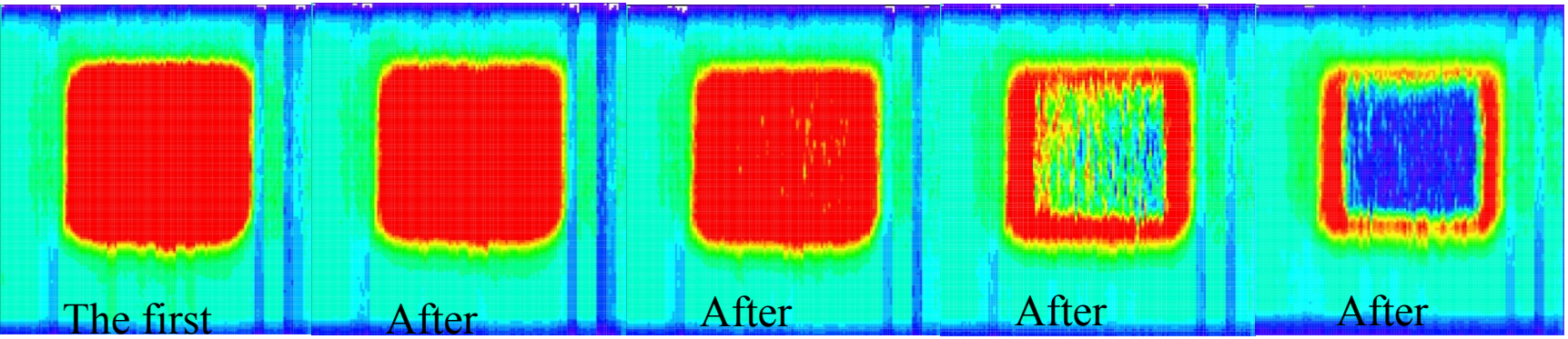


NMOS is ON at more than ~ 400 krad with Vsoi2=0V
NMOS works at 10Mrad with Vsoi2=-2V
PMOS works at 10 Mrad

Preliminary results of high dose X-ray irradiation test

Single SOI Total dose 54 krad

Signals disappeared



The first Irradiation (9krad/10sec)

After 18krad

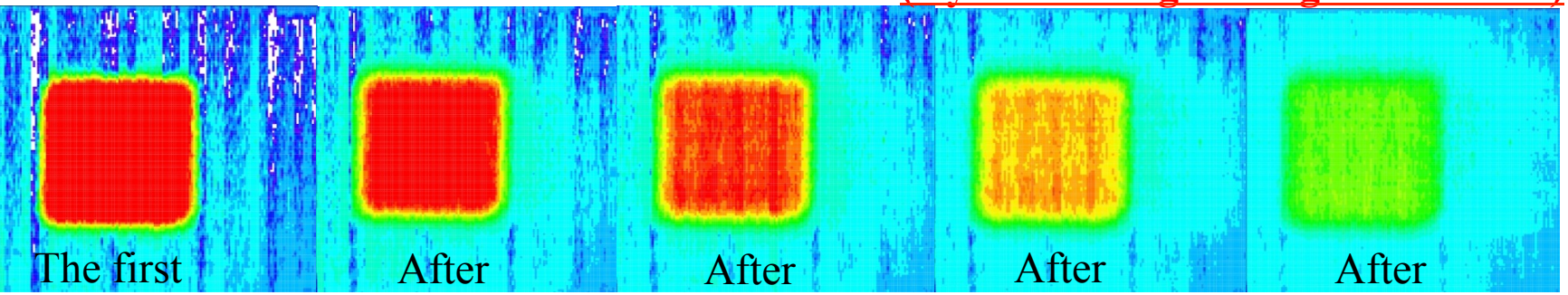
After 27krad

After 36krad

After 45 krad

Double SOI Total dose 810 krad

Signals still appear (Dynamic range changed narrower)



The first Irradiation (9krad/10sec)

After 90krad

After 180krad

After 360krad

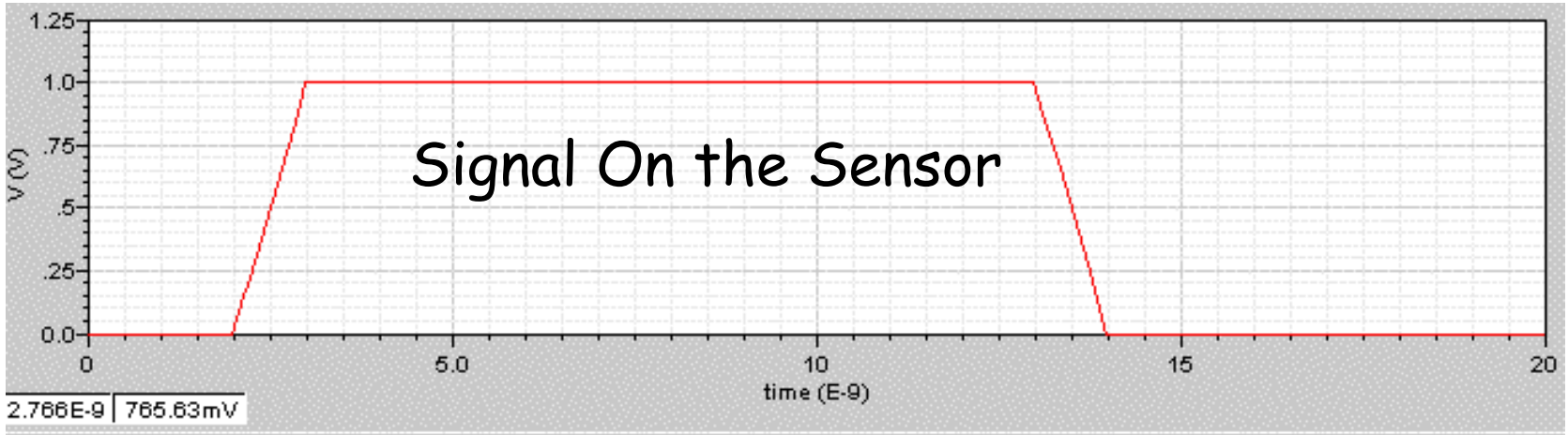
After 801 krad

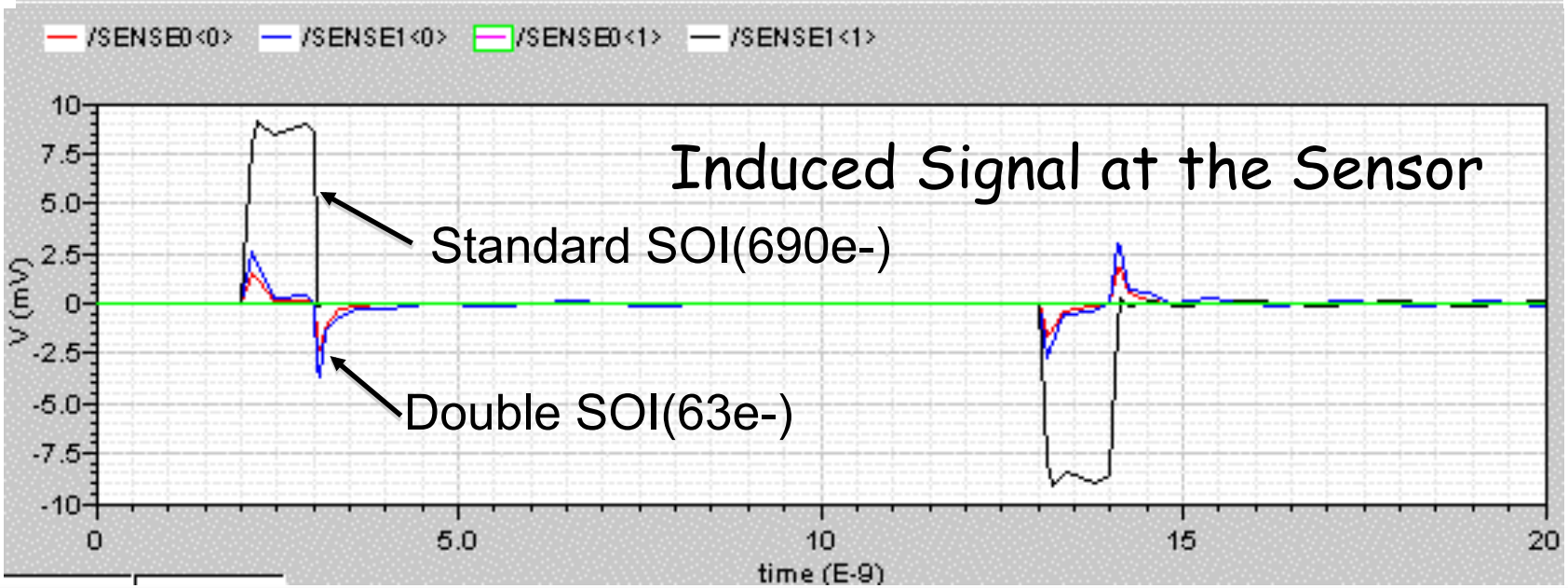
Caution!: INTPIX3g design has problem and has very low dynamic range!

* Middle SOI voltage = -2V

Cross Talk Simulation

To be tested with real chip





Cross Talk from the circuit to the sensor can be reduced 1/10, and signal shape will be bipolar. → disappear in charge amp.

Summary

- SOI technology is suitable for HEP applications
- Two SOI chips are designed for HEP
  - INTPIX for better resolution
    - INTPIX6 aiming for 1~2um resolution
  - PIXOR to replace most inner layer of Belle II SVD

- Double SOI structure to solve
  - Back gate effect
  - Radiation tolerance
  - Cross-talks