SuperPix0 Calibrations

Threshold Correction Study

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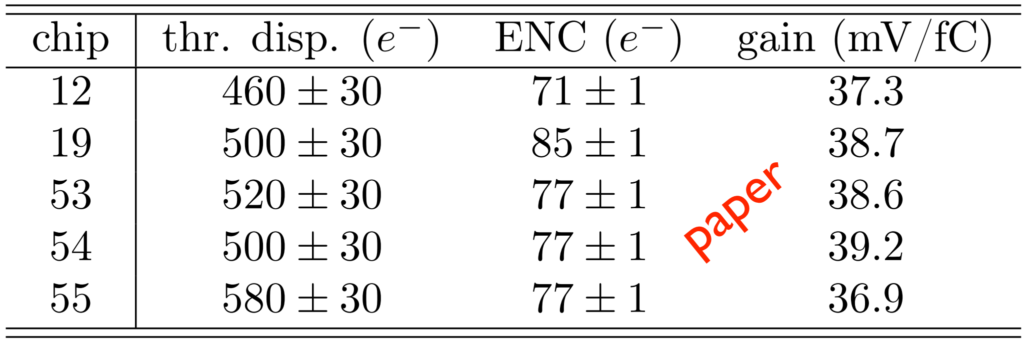
SuperPix0

- chip characterization in lab:
  - thr. dispersion & ENC computed in electrons *assuming a linear gain*:



chip	thr. disp. (e^-)	ENC (e^-)	gain (mV/fC)
12	460 ± 30	71 ± 1	37.3
19	500 ± 30	85 ± 1	38.7
53	520 ± 30	77 ± 1	38.6
54	500 ± 30	77 ± 1	39.2
55	580 ± 30	77 ± 1	36.9

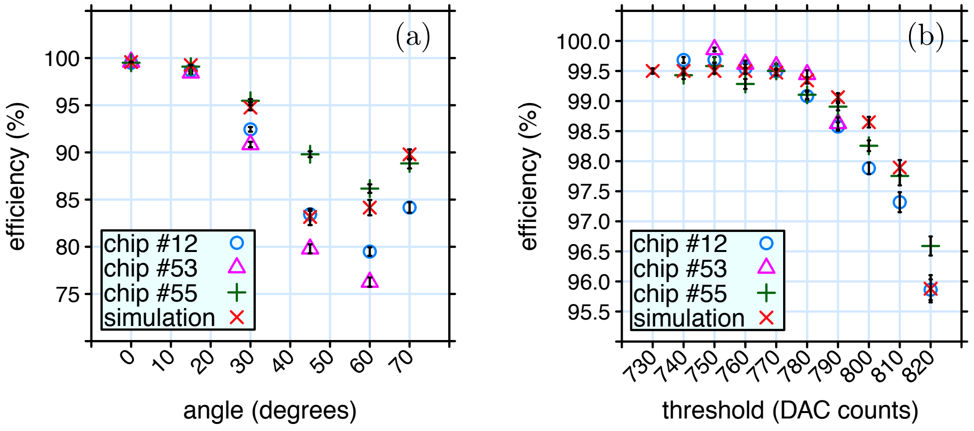
paper

Table 1: Lab characterization of the 5 chips tested during the test-beam.

- 2011 Testbeam:
  - scan in angle done with a threshold at **770** DAC, corresponding to 1/4 MIP *assuming a linear gain*:

Figure 9: Hit efficiency as a function of the angle of incidence of tracks when the pixel charge threshold corresponds to about 25% of a m.i.p. (left), and as a function of the threshold for normal-incidence tracks (right), for all detectors under test. The DAC values in the picture on the right correspond to a range from 12.5% to 40.6% of the charge released by a m.i.p.. Monte Carlo expectations are also shown.

on 200 μm Si:
1MIP = 16k e- = 2.6 fC
1/4MIP = 4k e- = 0.65 fC



Gain Calibration

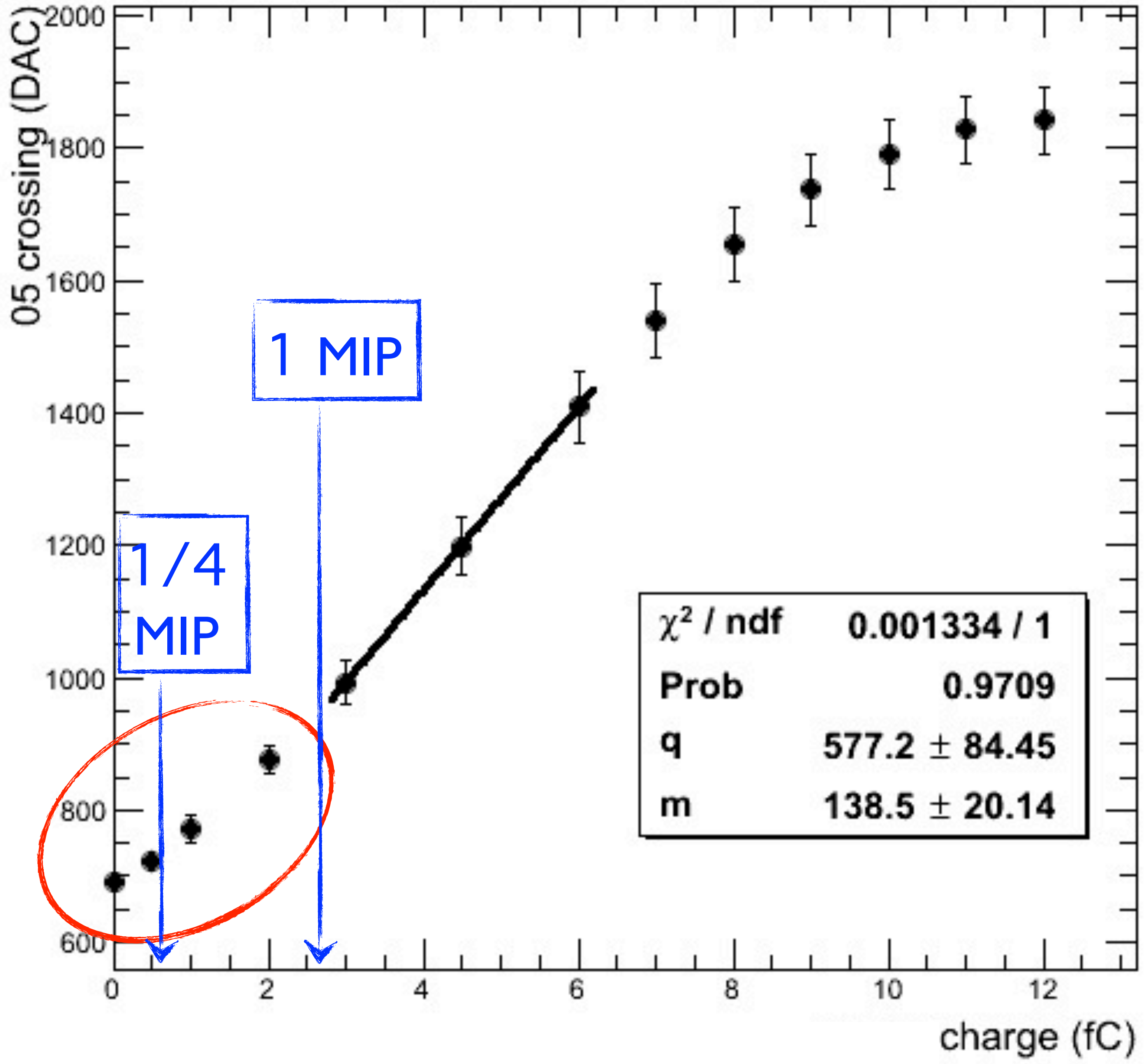
The gain for charges < 2.6 fC is not linear (due to a comparator malfunction):

- observed in chip1, ena20 (128 pixels)
- Vout = pre-ampl. output = voltage at 50% occupancy. Vout and baseline for each charge of each DUT is estimated as the average (over the enabled macrocolumns) of the mean of the distributions (of the pixels of a given macrocolumn)

we need to parameterize the gain at low injected charges to understand the threshold in terms of electrons

NOTE: DUTs are mounted on a different carrier and have been tested on a different board than chip1.

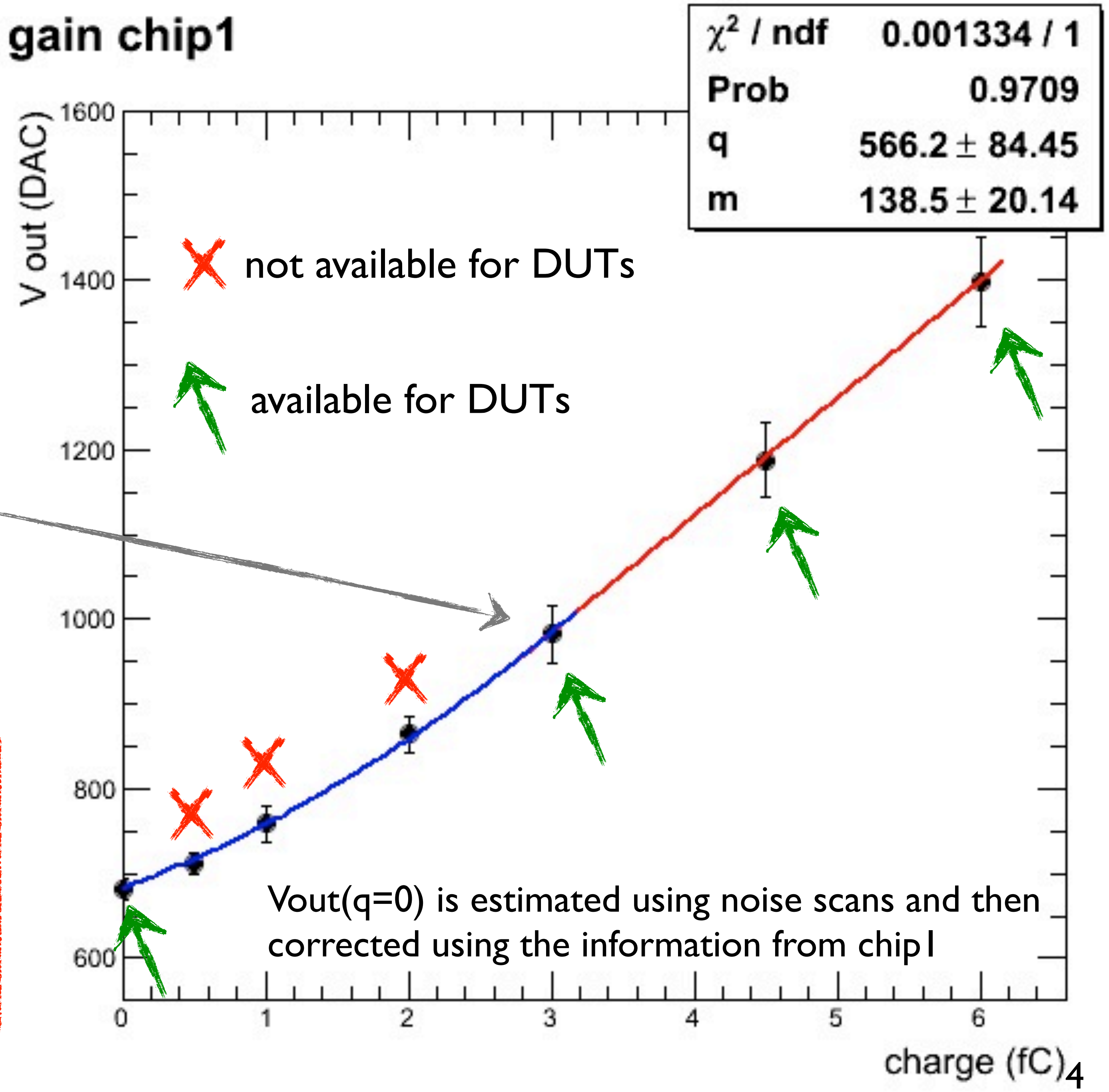
Vout(q) for chip1:



Procedure and Validation

1. define the curve y(x) in 2 regions
   - linear region: $y(x) = mx+q$
   - non-linear region: $y(x) = ax^2 + bx + c$
2. fit the linear region and extract m (*old* gain)
3. find a,b,c such that:
   - $y(0) = V_{out}(q=0)$
   - the curve is continuos in q'=3fC
   - the derivative is continuos in q'=3fC
4. shift the curve so that y(0) = baseline

Parameterization validated on chip1. The calibration will be further validated measuring Vout for q<2fC also for the DUTs

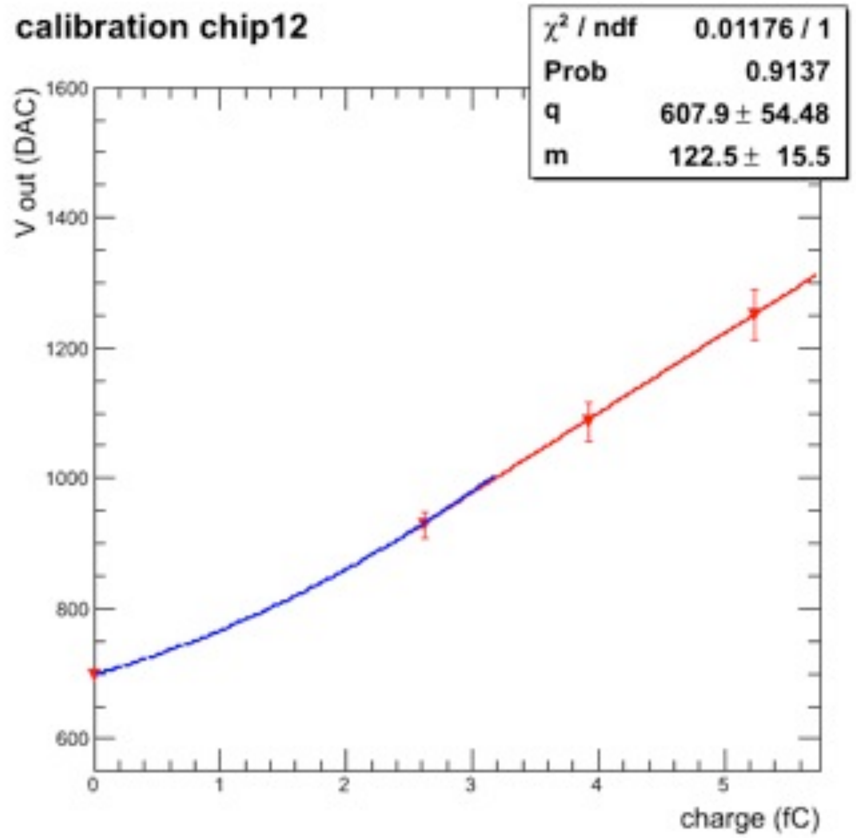


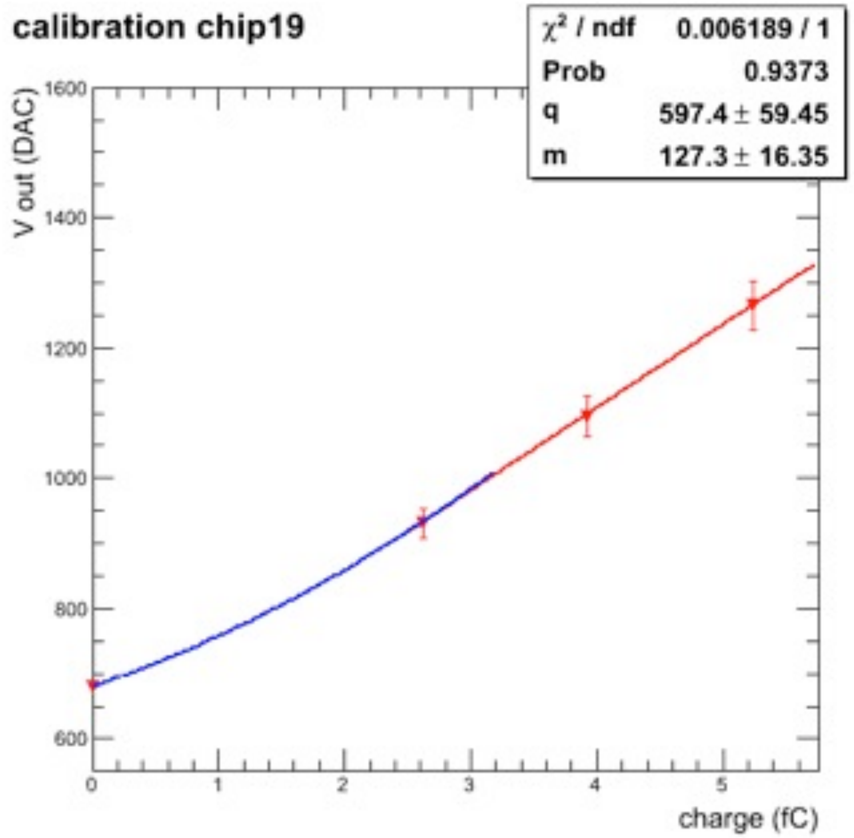
✗ not available for DUTs

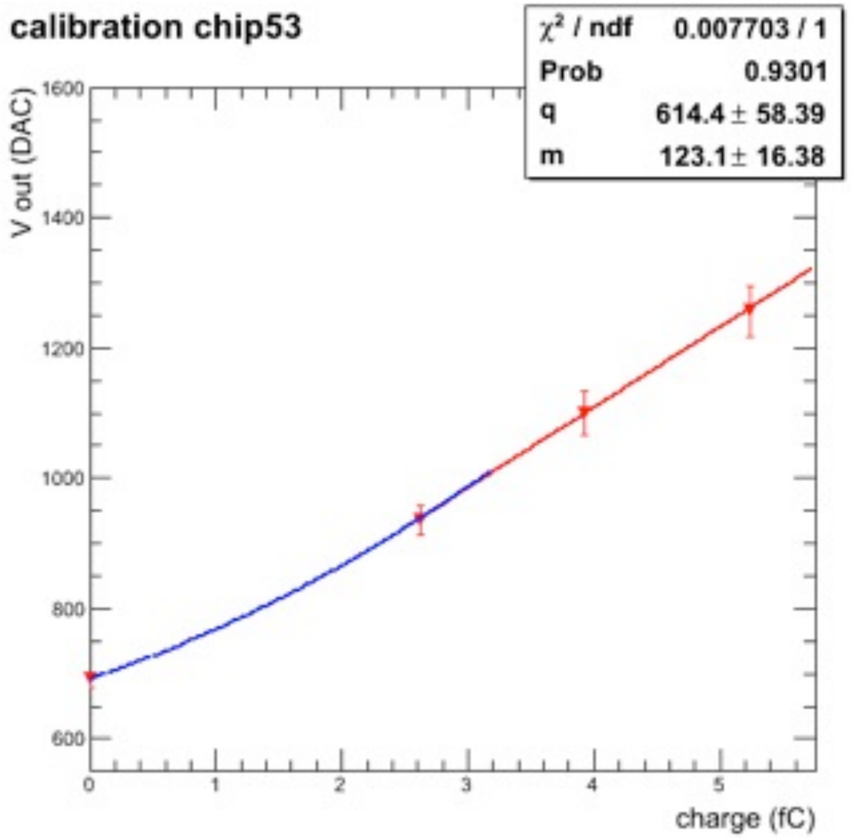
↖ available for DUTs

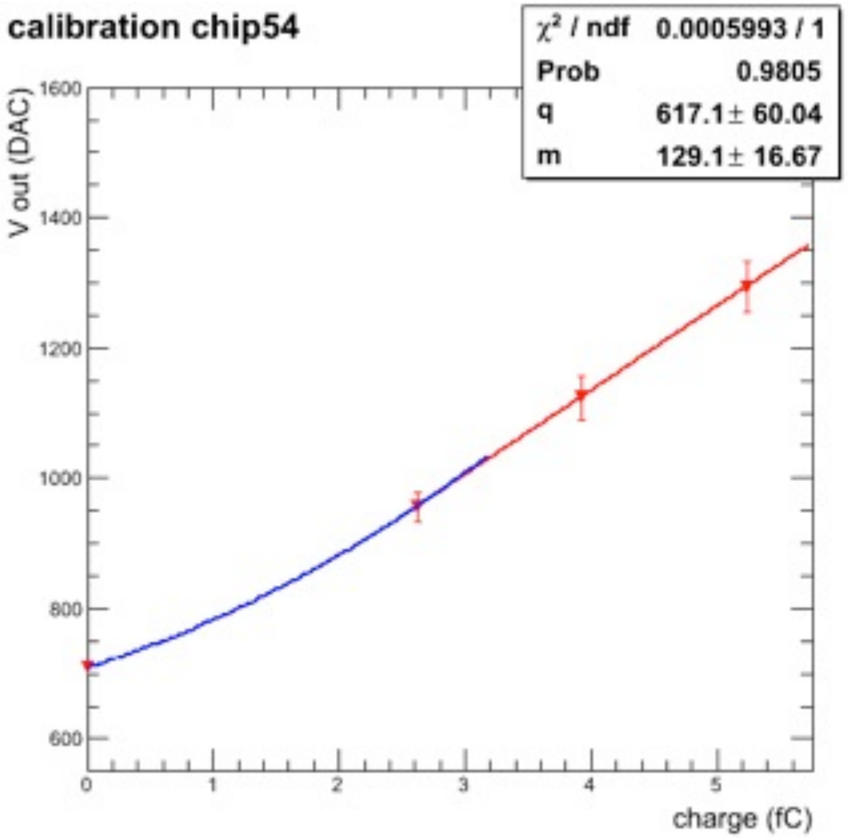
Vout(q=0) is estimated using noise scans and then corrected using the information from chip1

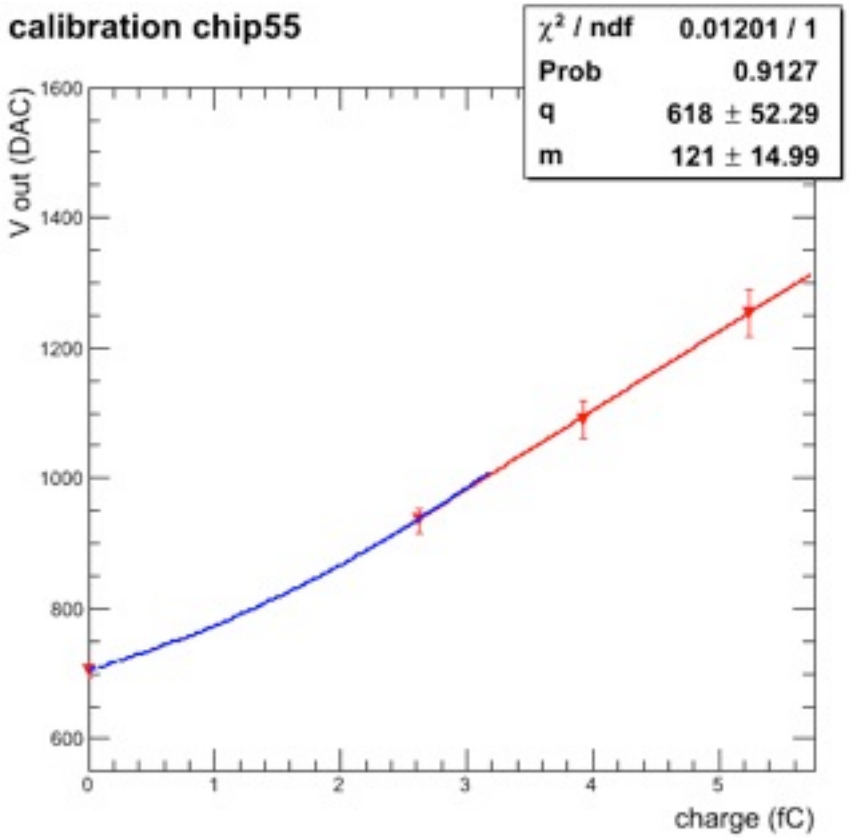
DUTs calibrations



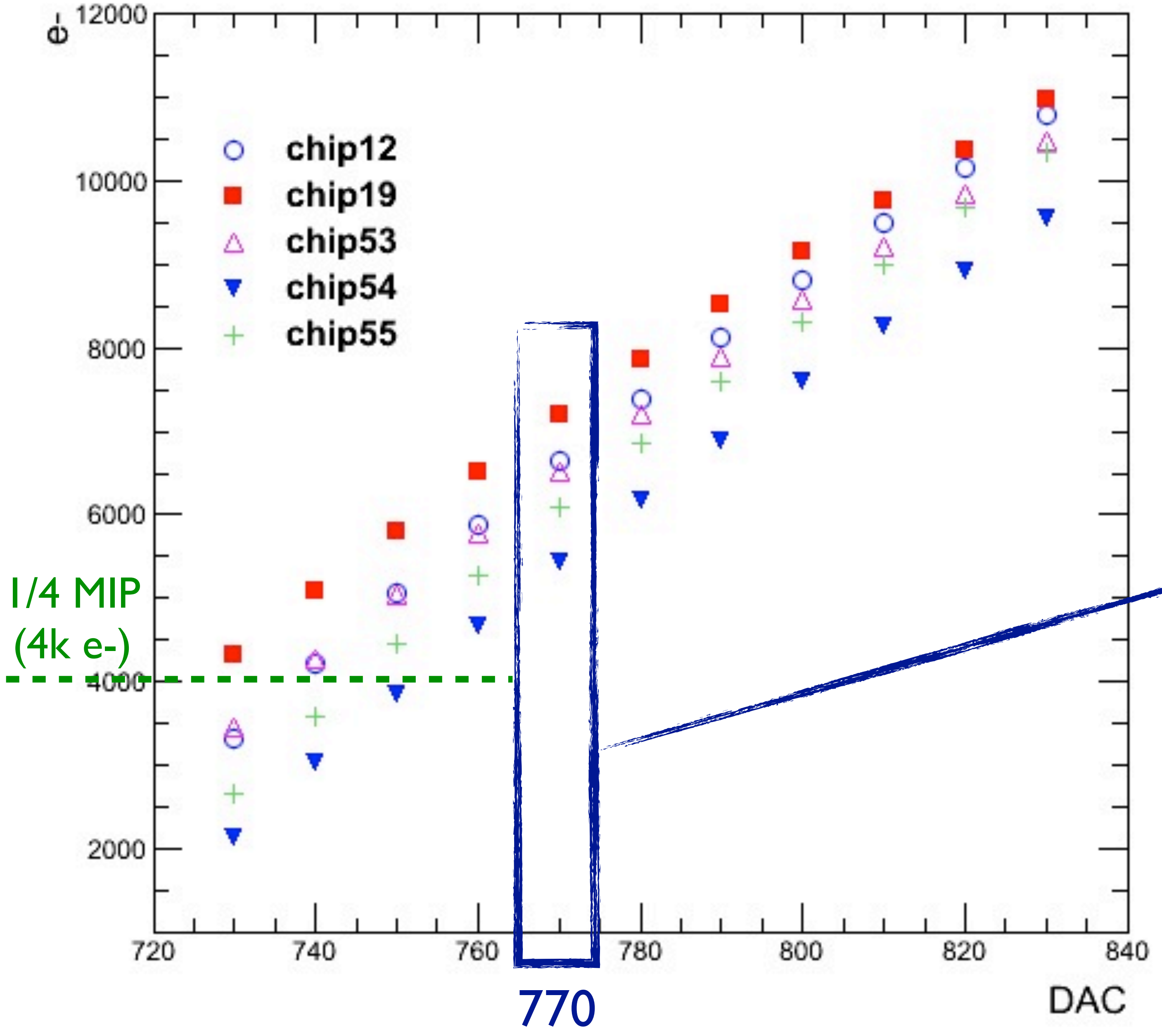








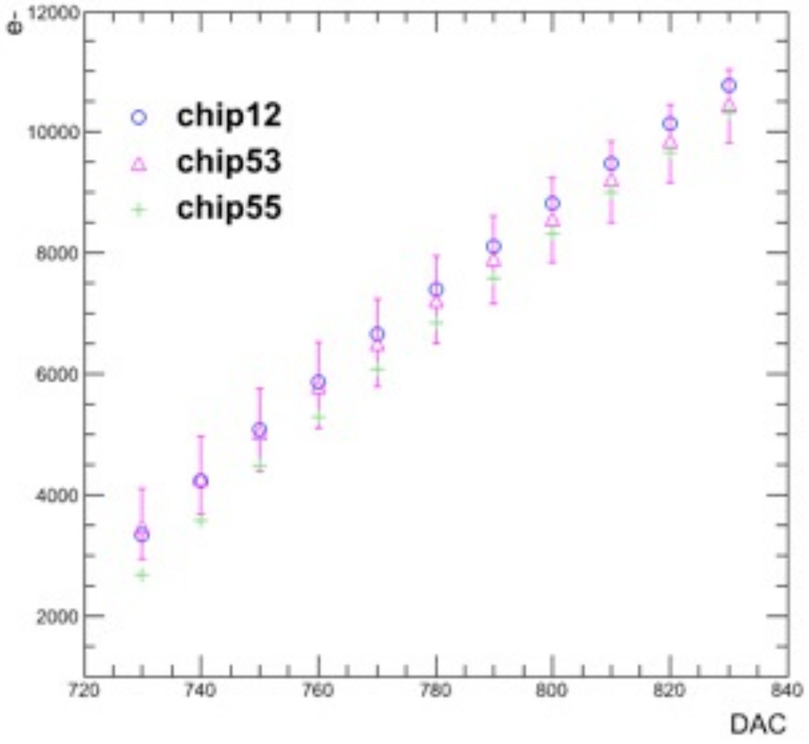
Threshold: from DAC to electrons



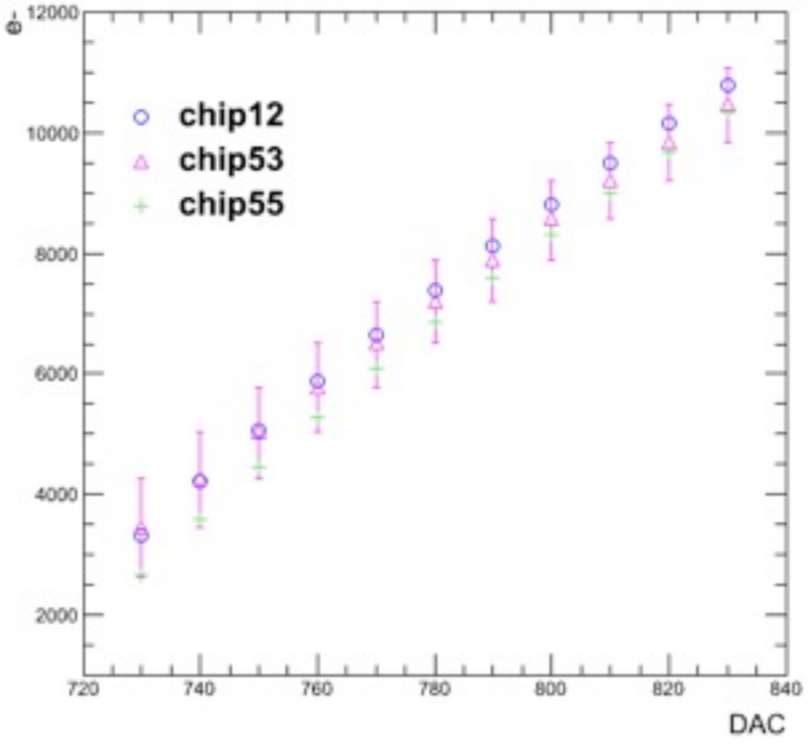
- the range of 730 – 820 DAC corresponds to:
  - chip12 → 3340 – 10800 e- = 20.9% – 67.5% MIP
  - chip53 → 3460 – 10500 e- = 21.6% – 66.5% MIP
  - chip55 → 2670 – 10300 e- = 16.7% – 64.4% MIP
- the threshold of 770 DAC corresponds to:
  - chip12 → 6650 e- = 41.6% MIP
  - chip53 → 6510 e- = 40.7% MIP
  - chip55 → 6090 e- = 38.1% MIP

Calibration Error Estimation

- vary the gain in the linear region by ±1σ and repeat points 3. and 4. of the procedure in slide 4
- example from chip53:
    - error ~ 520-740 e- (19% to 5% relative error).



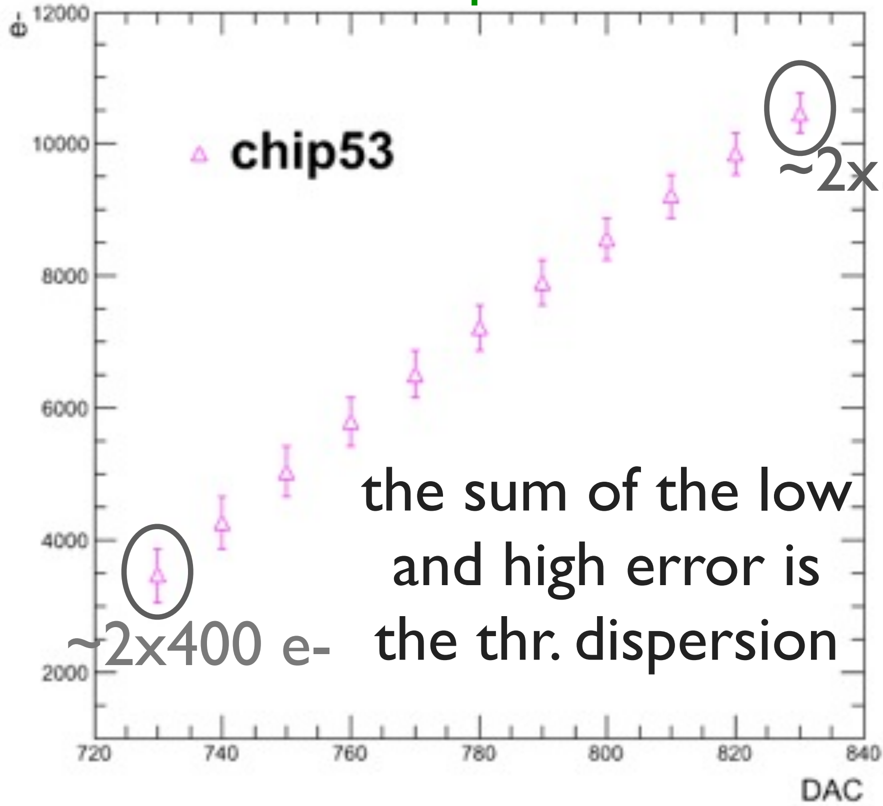
- vary the baseline by ±1RMS and repeat point 4. of the procedure in slide 4
- example from chip 53:
    - error ~ 630-830 e- (24% to 6% relative error).



ENC & thr. disp. re-evaluation

the value in mV is estimated as the RMS of the distribution of the baseline; need the equivalent in electrons to compare it to the noise. Since the gain depends on the threshold, the value of the threshold dispersion in electrons will also depend on the threshold:

threshold dispersion:



~2x300 e-

~2x400 e-

the sum of the low and high error is the thr. dispersion

currently reported on the paper (assuming linear gain):

chip	thr. disp. (e^-)	ENC (e^-)	gain (mV/fC)
12	460 ± 30	71 ± 1	37.3
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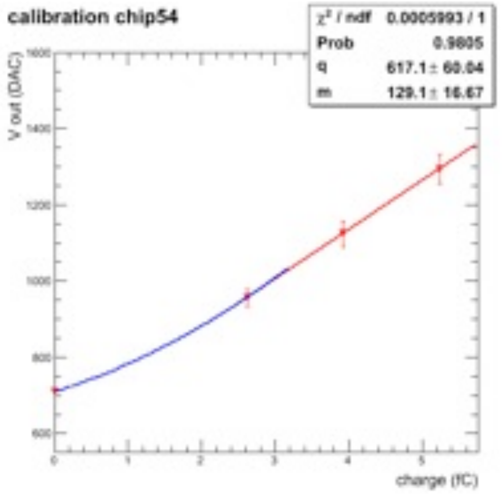
Table 1: Lab characterization of the 5 chips tested during the test-beam.

current value is underestimated, re-evaluate it using the new calibrations:



quote the linear gain, not mentioning the non linearity at small charges

corrected ENC & thr. disp.

DUT	baseline (DAC)	baseline RMS (DAC)	thr. disp. (e-) at 770 DAC	ENC (DAC)	ENC RMS (DAC)	ENC (e-)	linear gain (mV/fC)
chip12	697	9	680	1.4	0.3	158^{+60}_{-35}	$37.4^{+4.7}_{-4.7}$
chip19	679	10	674	1.7	0.3	164^{+53}_{-32}	$38.9^{+5.0}_{-5.0}$
chip53	691	10	710	1.6	0.3	150^{+50}_{-31}	$37.6^{+5.0}_{-5.0}$
chip54	708	10	750	1.6	0.5	163^{+61}_{-35}	$39.5^{+5.0}_{-5.0}$
chip55	704	11	860	1.5	0.3	166^{+59}_{-35}	$36.9^{+4.5}_{-4.5}$

NOTE: quoted errors correspond to variations on linear gain$^{+1\sigma}_{-1\sigma}$

currently reported on the paper (assuming linear gain):

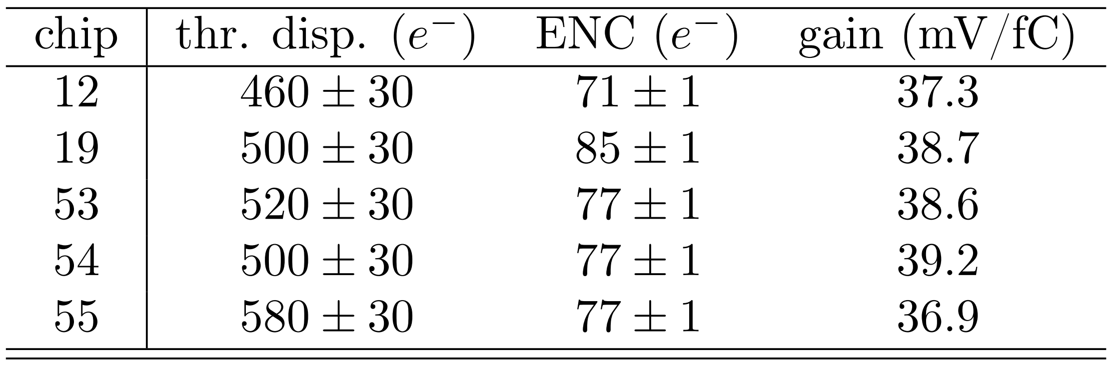


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Table 1: Lab characterization of the 5 chips tested during the test-beam.

now in agreement with post-layout simulations (150 e-)

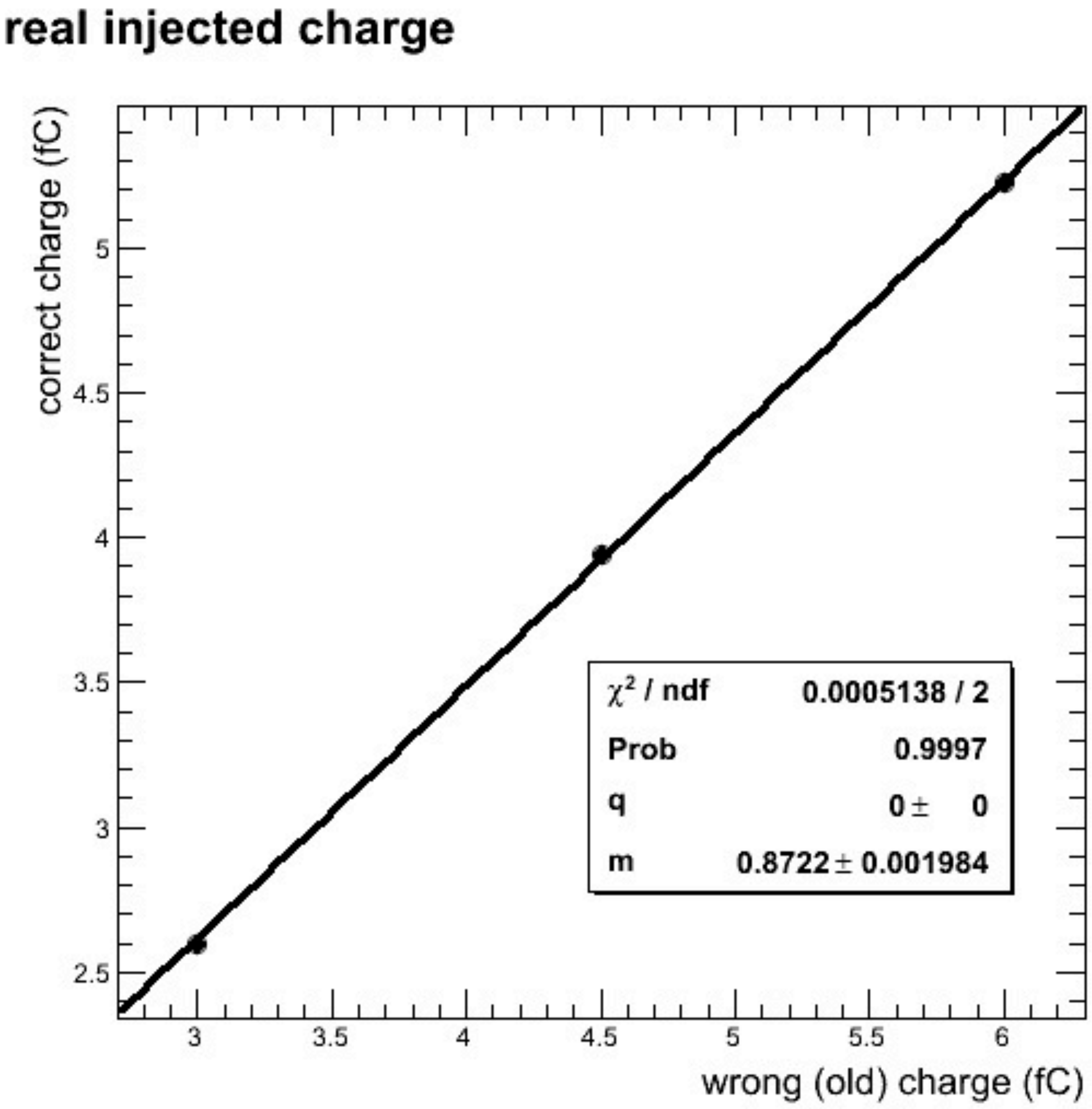
Corrections to the Paper

- Characterization of the chip in Lab:
    - Table1 and the text should be corrected
    - signal-to-noise is 100 (not 200)
- Testbeam Results:
    - the threshold of 770 DAC corresponds to:
        - chip12 → 6650 e- = 41.6% MIP
        - chip53 → 6510 e- = 40.7% MIP
        - chip55 → 6090 e- = 38.1% MIP
    - range of 730 – 820 DAC:
        - chip12 → 3340 – 10800 e- = 20.9% – 67.5% MIP
        - chip53 → 3460 – 10500 e- = 21.6% – 66.5% MIP
        - chip55 → 2670 – 10300 e- = 16.7% – 64.4% MIP
- Simulation:
    - check the values of the charge used to produce the points in Fig.9 and the charge estimated from Fig. 11.

back-up slides

Charge Scaling

- in the board where the DUTs have been tested we have a correction factor to get the actual ddp applied to the capacitance in the injection runs
- 3 useful points: 3, 4.5, 6 fC
- linear relation extracted with a fit:
    - y = mx + q
- fitting function constrained to cross the point (0,0)
- in this presentation, q’ stands for the *wrong* charge

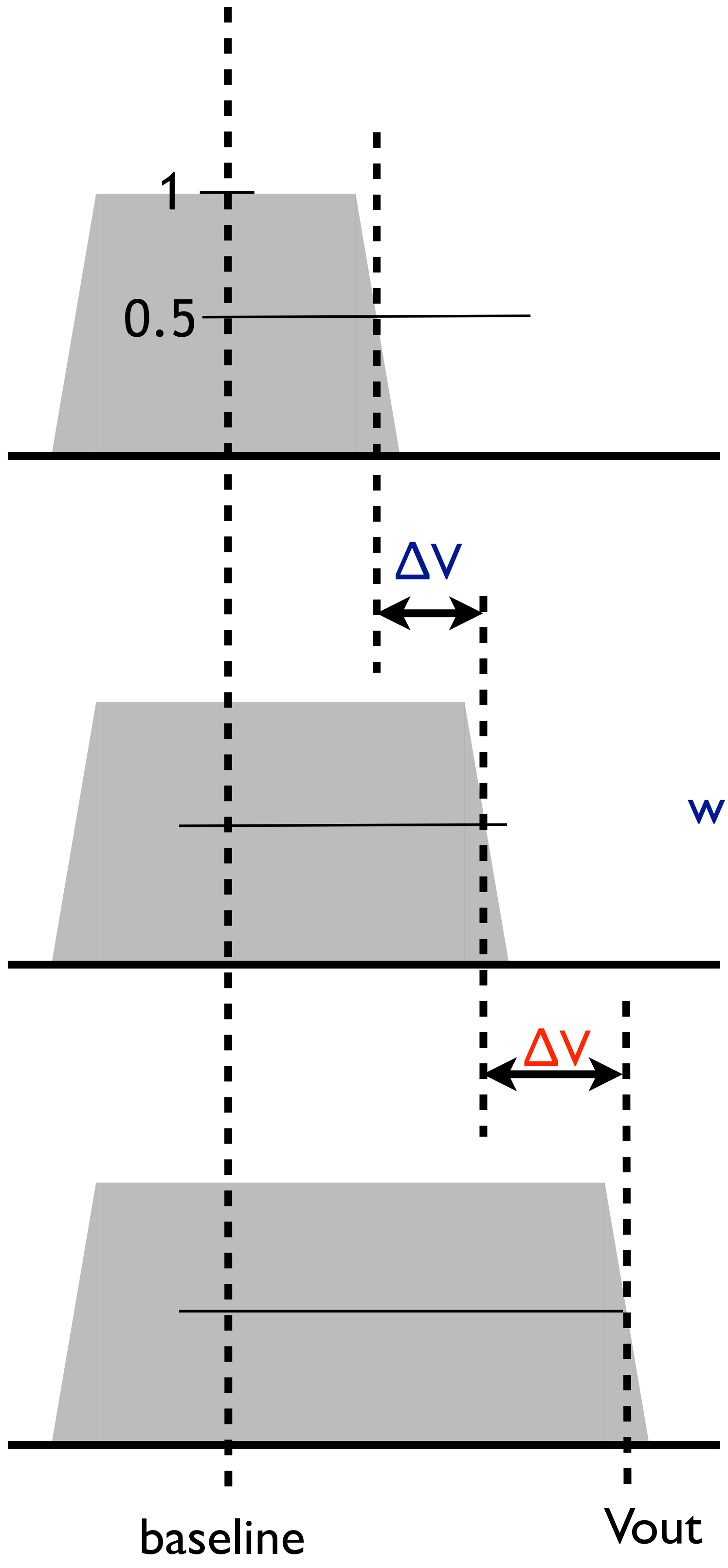


the DUTs

- for each chip we have studied 2/3 ena. For the 128 pixels in each ena we have:
    - inject scans: distribution of the Vout at q' = 3, 4.5, 6 fC
    - noise scan: distribution of the baseline and of Vout
- Vout and baseline of each DUT has been evaluated as the average (over the 2/3 ena) of the mean of the distributions (of the pixels of a given ena)

chip	ena	noise run	3 fC run	4.5 fC run	6 fC run
chip19	19	6	8	9	10
	24	7	26	27	28
chip12	6	11	7	8	9
	19	10	3	4	5
	30	12	13	14	15
chip53	6	1	4	5	6
	20	2	7	8	9
	30	3	11	12	13
chip54	6	3	4	5	6
	20	7	8	9	10
	30	11	12	13	14
chip55	6	3	8	9	10
	20	2	4	5	6
	30	7	13	14	15

occupancy curve



noise scan

injection scan
with q = 0

injection scan
with q > 0

ΔV = correction applied to
all chips to Vout(0) measured
with noise scans instead of inject scans.
Estimated from chip1 = +5 DAC.

ΔV/q = gain(q)