The SuperPix0 Small-Pitch Hybrid Pixel Detector with Fast Sparsified Digital Readout: Beam Test Results

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Abstract

A prototype hybrid pixel detector with 4096, 50×50 μm^2 pixels, 200 μm thick sensor and sparsified digital readout has been tested with a 120 GeV pion beam at the SPS H6 beam line at CERN. Efficiency and resolution have been measured as a function of both the discriminator threshold and the angle of incidence of the impinging particles. The capabilities of the custom data-push readout architecture have been tested as well. The viability of this technology for the full-luminosity upgrade of the layer 0 of the SuperB vertex detector is discussed.

Keywords: CMOS pixels, Charged particle tracking, Hybrid pixel detector, Data-push readout

1. Introduction

The SuperB B-Factory [1], a new concept asymmetric e^+e^- collider dedicated to heavy-flavour physics and expected to deliver unprecedented luminosities in excess of 10^{36} cm^{-2}s^{-1}, has been funded by the Italian Ministry of Education, University and Research in the framework of the 2011-2013 National Research Plan (Dec. 24 2010). Its reduced center-of-mass boost with respect to previous B-Factories (BaBar at SLAC and Belle at KEK) asks for a factor

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two improvement on typical vertex resolutions to fully exploit the accelerator potential for new-physics discoveries. In addition, the high luminosity and large backgrounds expected at SuperB determine stringent requirements in terms of granularity, time resolution and radiation hardness of all subdetectors and in particular, the vertex detector which is the closest to the interaction point.

The design of the SuperB Silicon Vertex Tracker follows the model of the BaBar SVT [4] but comprises both an extended coverage and an additional innermost layer, called layer 0, located at about 1.5 cm radius from the beam line. The layer 0 should offer a low material budget to minimize multiple scattering so as to meet the requirements on vertex resolution, and must be provided with a high-speed readout to minimize the acquisition dead-time. Intense R&D studies on various emerging technologies have been carried out to address further requirements such as a small pitch to guarantee a hit resolution at the level of 10 μm and to limit detector occupancy, the capability to withstand background hit-rates up to a few tens of MHz/cm^2, large signal-to-noise ratio and low power dissipation. Standard high resistivity silicon detectors with short strips (striplets) will be used for the layer 0 during the first period of operation, when the luminosity will be gradually increased to reach the design value. In fact, striplets offer a reasonably low material budget (about 0.2-0.3% X_0 for 200-300 μm silicon thickness) together with the required hit resolution. However, the detector occupancy becomes unaffordable at background rates larger than 5 MHz/cm^2 as expected at full luminosity, and a detector replacement is already scheduled after the first period of running.

This paper is focused on a prototype hybrid pixel detector named SuperPix0 and designed by the VIPIX collaboration as a first iteration step aimed at the development of a device to be used for the layer 0 upgrade.

Hybrid pixel devices are a well established technology in HEP experiments. The fully depleted high-resistivity sensors and the read-out integrated circuits are built on different substrates and then connected via high density bump-bondings. Hybrid pixel sensors usually provide high signal-to-noise ratio, high radiation tolerance and 100% fill factor. Furthermore, this technology offers the possibility to implement advanced in-pixel electronics such as low-noise amplification, zero suppression and threshold tuning without the problem of cross-talk between the readout logic and the sensor. The relatively large amount of material they are made of represents a disadvantage in terms of probability of particle scattering, although a reduction of material budget may become possible with the latest technology improvements [5]. The main novelties of our approach is the sensor pitch size (50$\times$50 μm^2) and thickness (200 μm) as well as the custom front end chip architecture providing a sparsified and data-driven readout. A prototype readout chip with 4096 cells arranged in a 32$\times$128 matrix was submitted for fabrication in standard 130 nm CMOS technology by STMi-

croelectronics. The sensor was fabricated by FBK-IRST[1] and interconnected with the readout chip by IZM[2] .

The paper is organized as follows: section 2 describes the sensor, the analog in-pixel logic, the digital readout architecture as well as the chip properties as determined in laboratory tests. Section 3 summarizes the main aspects of the beam-test setup and beam characteristics, and section 4 provides information about the trigger and DAQ infrastructure and performance. Data analysis, including telescope alignment, track reconstruction as well as the determination of the prototype efficiency, is described in section 5. A Monte Carlo modeling of the SuperPix0 chip is provided in section 6. Finally, conclusions are drawn in section 7.

2. The SuperPix0 Hybrid Detector

2.1. The High Resistivity Pixel Sensor

Pixel sensors are made from n-type, Float Zone, high-resistivity silicon wafers, with a thickness of 200 μm and a nominal resistivity larger than 10 kΩcm. Sensors are of the "n-on-n" type and were fabricated at FBK with a double-sided technology [6]. N^+ pixels are arranged in a 2d array of 32×128 elements with a pitch of 50 μm in both X and Y directions, for a total active area size of 10.24 mm^2 . All around the pixels is a large n^+ guard ring extending up to the cut-line. The electrical isolation between neighboring n^+ pixels has been obtained by means of a uniform p-spray implantation. A large p^+ diode is on the bias side: it has the same size as the active area and is surrounded by 6 floating rings. From electrical tests performed on wafers before bump-bonding (and connecting the sensors from the bias side only with a probe on the diode and a probe on the scribe line [7]), the total leakage current is about 1 nA, the depletion voltage is about 10 V, and the breakdown voltage in the order of 70 V, due to a relatively high p-spray dose. The pixel capacitance has also been estimated from measurements performed on a special test structure, and the resulting values are in the order of 50 fF (i.e. comparable to the capacitance contribution expected from the bumps).

2.2. The Analog Front End Cell

The in-pixel analog electronics is made of a charge processor (shown in Fig. 1) where the sensor charge signal is amplified and compared to a chip-wide preset threshold by a discriminator. The in-pixel digital logic, which follows the comparator, stores the hit in an edge-triggered set reset flip-flop and notifies the periphery readout logic of the hit. The charge sensitive amplifier uses a single-ended folded cascode topology, which is a common choice for low-voltage, high

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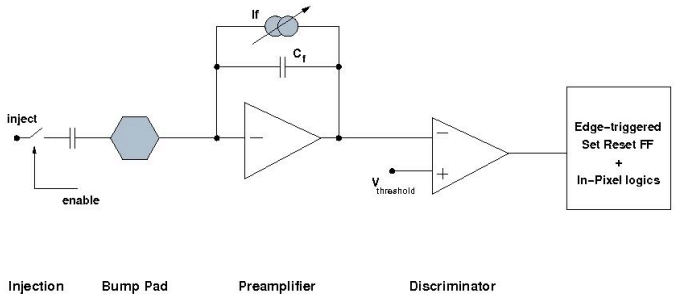

Figure 1: Block diagram of the analog front end electronics for the elementary cell of the SuperPix0 readout chip.

gain amplifiers. The 20 fF MOS feedback capacitor is discharged by a constant current which can be externally adjusted, giving an output pulse shape that is dependent upon the input charge. The peaking time increases with the collected charge and is in the order of 100 ns for 16000 electrons injected. The charge collected in the detector pixel reaches the preamplifier input via the bump-bond connection. Alternatively, a calibration charge can be injected at the preamplifier input through a 10 fF internal injection capacitance so that threshold, noise and crosstalk measurements can be performed. The calibration voltage pulse is provided externally by a dedicated line. Channel selection is performed by means of a control section implemented in each pixel. This control block, which is a cell of a shift register, enables the injection of the charge through the calibration capacitance. Each pixel features a digital mask used to isolate single noisy channels. This mask is implemented in the readout logic. The input device (whose dimensions were chosen based on [8]) featuring an aspect ratio W/L=18/0.3 and a drain current of about 0.5 μA, is biased in the weak inversion region. A non-minimum length has been chosen to avoid short channel effects. The PMOS current source in the input branch has been sized to have a smaller transconductance than the input transistor. For a detector capacitance of 100 fF, an equivalent noise charge of 150 e^- rms was obtained from circuit simulations. The noise contribution arising from the leakage current can be neglected for the leakage current range considered in the simulations (0-2 pA). 2 pA corresponds to ten times the anticipated leakage current for the pixel sensor. An overall input referred threshold dispersion of 350 e- rms was computed from Monte Carlo simulations. Since SuperPix0 is the first iteration step aimed at the development of a readout chip for small pitch hybrid pixel sensors, in this design only the main functionalities have been integrated in the pixel cell. Threshold dispersion is a crucial characteristic to be considered in order to meet the required specifications in terms of noise occupancy and efficiency. Therefore, circuits for in-pixel threshold fine-adjusting will be implemented in the next version of the chip. The analog front end cell uses two power supplies. The analog supply (AVDD) is referenced to AGND, while the digital supply is

referenced to DGND. Both supplies have a nominal operating value of 1.2 V. Since single-ended amplifiers are sensitive to voltage fluctuations on the supply lines, the charge preamplifier is connected to the AVDD. The threshold discriminator and voltage references are connected to both the AVDD and AGND. The in-pixel digital logic is connected to the digital supply. The substrate of the transistors is connected to a separate net and merged to the analog ground at the border of the matrix. The SuperPix0 chip has been fabricated in a six metal level technology. Two levels of metal have been used to route the analog signals, two for the digital ones and two for distributing the analog and digital supplies. The supply lines, at the same time, shield the analog signals from the digital activity. For nominal bias conditions the power consumption is about 1.5 μW per channel. More details on the design of the analog front end chip can be found in the literature [9].

2.3. Digital Readout Architecture

The SuperPix0 digital readout architecture is an evolution of the one adopted for the APSEL4D chip [11] and was originally designed to read out matrices of 320×256 pixels and sustain rates of 100 MHz/cm^2 . The same macro-pixel (MP) structure as described in [11] has been adopted, but with a different MP shape: 2×8 pixel rectangles replace 4×4 pixel squares in order to minimize the matrix mean sweeping time (MST) in the presence of hit-clusters as expected in the data. A further parallelisation level is achieved by dividing the matrix in sub-matrices of 32×64 pixels and providing each sub-matrix with an independent readout and a local data buffer. A final output stage retrieves data from all the readout buffers and compresses them into a single data stream. Hits are extracted from the matrix in a time-ordered way, which was not the case with the APSEL4D chip and which allows avoiding to add time information to each hit, thus reducing the total amount of data to be transferred. Finally, a new hit encoding algorithm is used that includes a data compression for clustered hits; in this way the output data band-width is significantly reduced with a negligible increase of logic gates.

Each MP is connected to the peripheral readout through two private lines used to send a "hit" information when at least one of the pixels in the MP is fired and to receive a "freeze" signal to prevent all the pixels within the MP from accepting further hits until the readout has been completed. The peripheral readout includes a time counter (BCO) which is incremented at the frequency of a programmable clock defining the time resolution of the detector. Its value is used to provide a time-stamp to each event. Whenever the BCO counter is incremented, the MPs that have been hit during the previous time window are frozen and their hit-map is stored inside a FIFO together with the associated time stamp. The list of active MPs is then used to extract hits from the matrix in a time-ordered way. A 32-bit wide pixel data bus is shared by the rows and driven by the columns of the pixel matrix. For each BCO, the readout is performed only on the columns in the corresponding MP list, one column per readout-clock cycle (down to 6 ns) independently of the pixel occupancy. Only

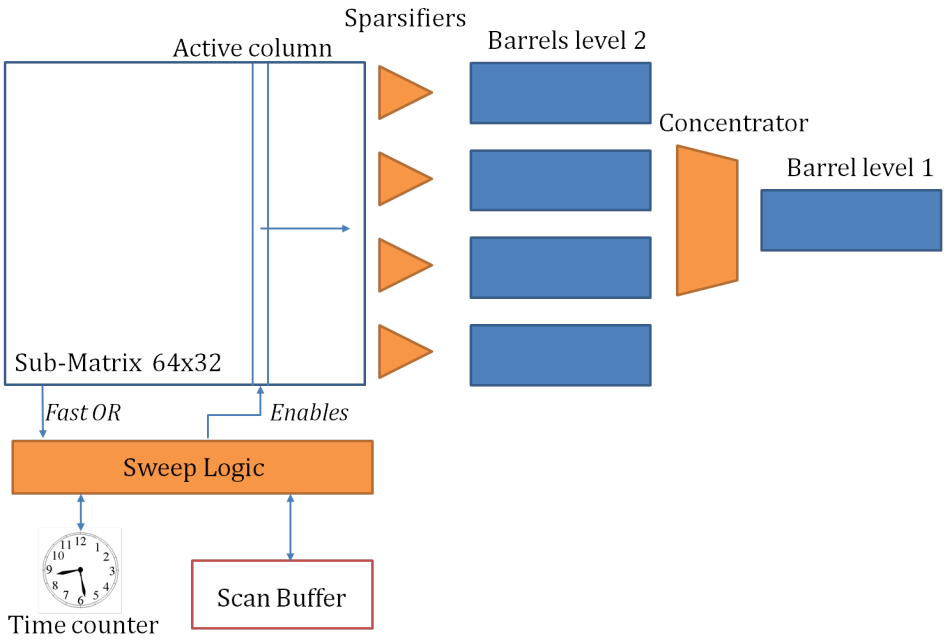

Figure 2: Schematics of the digital readout architecture.

pixels belonging to the fired MP are enabled to drive the corresponding lines of the pixel data bus. When compared to a continuous sweep over the matrix columns as performed with the APSEL4D chip, this technique slightly increases the mean pixel dead-time. On the other hand, simulations demonstrated that the rectangular MP geometry results in an overall improvement of performance with respect to the APSEL architecture for any fixed number of hits.

A schematics of the perifery digital logic is shown in Fig 2. As in the APSEL4D chip, the pixel data are encoded by the sparsifier elements. They create a formatted list of all the hits found on the pixel data bus and write it into a dedicated memory element called barrel. This component is a FIFO memory with multiple write ports (one for each word in the list) and a conventional single output port. A data concentrator controls the flux of data preserving the time-sorting of the hits.

Monte Carlo simulations have been performed on this architecture scaled to a 320×256 matrix in order to evaluate its performance. We measured efficiencies close to 98.5% running with a 60 MHz readout-clock (200 MHz on the output bus) and starting from the assumption of a 100 MHz/cm^2 hit rate. Whilst keeping in mind that the target time resolution for this architecture is 1 μs, an efficiency drop is observed with BCO lengths below 400 ns.

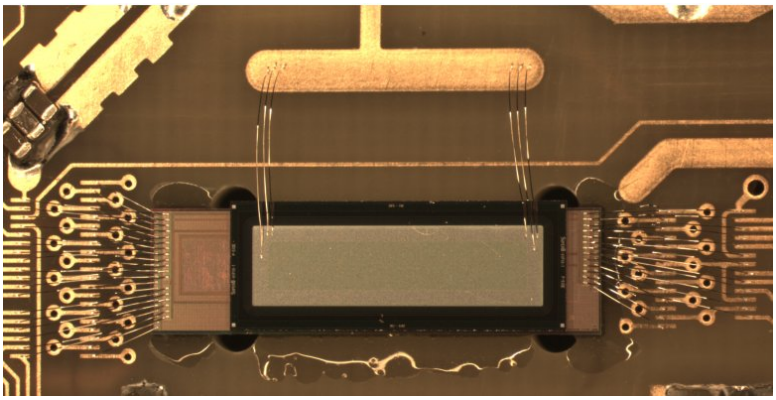

Figure 3: Photograph of the bump-bonded chip, the sensor matrix and the front end chip are visible as well as the bondings to the carrier.

2.4. Chip Characterization

Five chip matrices have been characterized in terms of noise, threshold dispersion and gain in various laboratory tests before the final trial on beam. The response of the sensors was analysed as well. A photograph of one of the front end chips connected by bump-bonding to the high resistivity pixel sensor matrix of 200 μm thickness is shown in Fig. 3.

The first laboratory checks identified a feature in the readout architecture causing the generation of spurious data on the output stream. The problem was fully understood and a special configuration was found to avoid it already in the current chip version, although at the expenses of a considerable reduction in the area of the matrix that can be used at the same time. In such a configuration and for continuous data taking only one fourth of the matrix at a time is activated, in the shape of an 8x126 pixel stripe. Calibrations and gain measurements are based on 4-column steps. These limitations, in conjunction with time constraints, allowed the laboratory characterization of the front end electronics of only 10-20% of the pixels in each matrix, depending on the chip.

The absolute calibration of the gain of the chip matrix was performed by using the internal calibration circuit described in 2.2, which allowed the injection of charges from 0 to 12 fC in each preamplifier. An average gain of 38 mV/fC was measured with a typical dispersion of about 6% inside the examined piece of matrix.

Noise measurements and an evaluation of the threshold dispersion were performed by measuring the hit rate as a function of the discriminator threshold. With a fit to the turn-on curve we obtain a pixel average equivalent noise charge (ENC) of about 77 e^- with 15% dispersion inside the matrix, and a threshold dispersion of about 500 e^-, which motivated the project of a threshold tuning

chip	thr. disp. (e^-)	ENC (e^-)	gain (mV/fC)
12	460 ± 30	71 ± 1	37.3
19	500 ± 30	85 ± 1	38.7
53	520 ± 30	77 ± 1	38.6
54	500 ± 30	77 ± 1	39.2
55	580 ± 30	77 ± 1	36.9

Table 1: Lab characterization of the 5 chips tested during the test-beam.

circuit at pixel level for the next submission. Threshold dispersion, ENC and gain values for each of the 5 chips characterized in the laboratory are reported in Table 1.

Both beta (^{90}Sr) and gamma (^{241}Am) radioactive sources were used in order to test the sensor response and the interconnections between the pixel electronics and the sensor. The hit rate as seen from the sensor matrix when exposed to ^{90}Sr is shown in Fig. 4. The illumination of the matrix is not uniform due to the

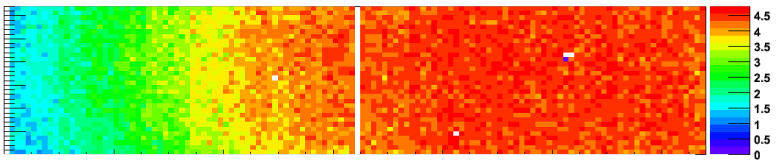

Figure 4: Hit rate (Hz) measured with chip 19 exposed to a ^{90}Sr source.

collimation of the source. The two blank columns were not scanned due to the aforementioned workaround in the readout scheme. All tested chips showed a very good quality of the interconnections at 50 μm pitch, as well as a responding sensor. Only four channels out of more than 20 thousands showed interconnection problems.

Continuous data acquisitions with pixel thresholds corresponding to less than 1/2 of the signal released by a minimum ionizing particle (m.i.p.) revealed another undesired effect ascribable to inter-pixel inductions, which can be avoided in next chip submission. Meanwhile, a solution has been found to profit of the high SNR ($\simeq$ 200) of the sensor during the beam test, allowing to lower the threshold down to 1/4 of a m.i.p. at the cost of 25% of the acquisition duty cycle.

3. Beam Test Setup

The beam test was carried out at CERN, at the SPS H6 beam line delivering 120 GeV pions in spills lasting 9.5 s and separated by about 40 s. In the region of the experimental setup the beam was characterized by widths of about 8 and

4 mm rms on the horizontal and vertical planes, respectively. As a reference telescope six planes of 2×2 cm^2, double-sided silicon strip detector with 25 μm strip pitch on the p-side and 50 μm pitch on the n-side [12] were used. The readout pitch was 50 μm on both sides. Three planes were placed before the devices under test (DUT), and three after them, at distances of 3.5 cm from each other and either 25 or 35 cm from the DUT, depending on their number: either one or two SuperPix0 chips could be accommodated in the beam-line. All detectors were placed on a custom motorized table with remote control. The reference telescope was used both to trigger events and determine the impact point of tracks at the DUT. Due to beam time constraints, only three out of the five aforementioned SuperPix0 chips were tested with beam. One chip at a time was used to study the dependence of the efficiency on the angle of the impinging particles, whereas either one or two chips were put in the beam line when studying the dependence of the efficiency on the value of the discriminator threshold. The schematics of both setups are shown in Fig 5.

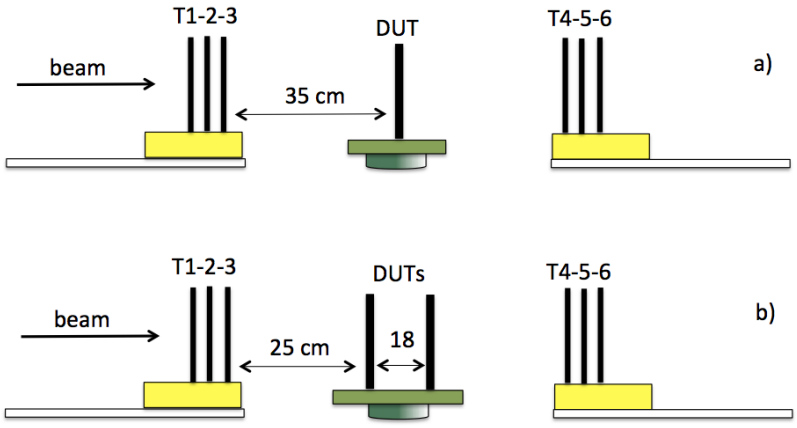

Figure 5: Test beam setup with either one (a) or two (b) detectors under test (DUT). The drawing is not in scale. T1...6 represent the double-sided telescope planes

4. Trigger and Data Acquisition

The DAQ infrastructure is very similar to the one described in detail in [10]. The main elements are two programmable VME 9U EDRO (Event Dispatch and Read-Out) boards [13, 14] organized in a master-slave configuration and responsible for programming the front end chips of both the telescope and the DUT. The master EDRO is connected to the first, third, fourth and last plane of the telescope. It generates and distributes to all elements both the readout and BCO clocks, as well as the triggers. These are based on hit multiplicity on each

side of the telescope planes connected to the master. The slave is connected to the remaining planes of the telescope and to the DUT. Both EDRO boards act as event builder, packing time-ordered information from the telescope and the DUT in events that are then sent out via optical links (S-link [15]) to a Robin card [16] on a remote PC where they are written to disk. Online monitoring is performed on another PC complementing the DAQ system. The programmable BCO clock defines the time resolution of the experiment by dividing the time in corresponding events. Its period can vary from 400 ns up to 500 μs. For all data collected during the beam-test the BCO period was set to 5 μs.

The DAQ software is built on the ATLAS TDAQ software infrastructure [17], which provides a complete environment with remote process control and communication, finite-state-machine, inter-process messaging, online monitoring and histogramming as well as a textual database infrastructure for run and front end configuration. The VIPIX team developed applications, plugins, configuration and monitoring programs specific to our EDRO boards and information stored in the raw events.

The analysis of the BCO information stored in each event allows the measurement of the trigger rate, together with the DAQ dead-time, over the duration of each spill. A maximum acquisition rate in the order of 40 kHz was observed. The data acquisition was dead-time free for the first half of each spill, when events could be buffered in the Robin card while waiting to be copied to disk. In the second half of each spill the DAQ rate was limited to roughly 20 kHz.

A total of about 324 million events with good data were collected with one or two SuperPix0 DUT over a period of 42 hours. For all data considered in this paper, the trigger minimum multiplicity was set to one in all trigger planes, resulting in a minimum request of eight hits distributed over four different planes, one hit per side.

5. Detector Performance

5.1. Silicon Telescope Alignment and Track Reconstruction

For each event, tracks are reconstructed from the silicon telescope hits. The same track-reconstruction software that was used for the analysis of a former test-beam [10] is employed, although here the track-finding algorithm is improved to use a variable number of telescope planes, since the beam test setup includes six telescope planes whereas four were used in the past.

Typically, triggered events have just one track, with one hit for each of the two sides in each of the six telescope planes. The global reference frame is set with the z axis along the beam direction, the x axis in the horizontal plane and the y axis in the vertical plane, pointing up. The p-side silicon strips measure the local detector coordinate u along x, while the n-side strips measure the local detector coordinate v along y. The reconstruction algorithm relies on the

fact that the telescope planes have high efficiency and low noise, and that most triggered events contain just one track with all its related hits, with nothing else but a very small number of noise hits. Adjacent fired strips are grouped in clusters, and the position of each cluster is calculated by weighting the strip positions with their measured charge. The clusters primarily consist of one or two strips, in similar proportions, as in a former beam test [10]. For each silicon detector, each u hit is combined with each v hit on the opposite side to define a local space point. All possible straight lines connecting the space-points of the two outer detectors are considered, together with the closest space-points in the intermediate detectors. All space point sets are then fitted to straight lines with a minimum χ^2 fit, using roughly estimated hit uncertainties as in a former data analysis [10]. A precise determination of the telescope resolution is not needed for the purposes of this study.

In order to fit tracks, the real positions and rotations of the inner telescope planes must be determined and accounted for. In a first phase, they are measured by using events where a single track is reconstructed, with hits on all sides of all telescope planes within 1 mm in the xy projection, and no requirements on the track-fit χ^2. Beam tracks are found to have an angular distribution that is close to normal incidence: 5.0 ± 0.2 mRad in xz plane, and 0.7 ± 0.2 mRad in the yz plane. In these conditions, data permit the determination of possible translations of the telescope-planes in xy, as well as their rotation angles around the z axis, whereas there is no significant sensitivity to possible displacements along z and rotations around x and y. Nominal positions and uncertainties are thus used on these coordinates.

The final telescope alignment is achieved by assuming that the first and the last telescope planes are placed at their nominal position and by minimizing the residuals of the hits in the inner planes with respect to the extrapolated fitted tracks. Residuals are defined as the difference between the u- and v-positions of each hit on the telescope planes and the u- and v-positions of the fitted track on the same planes. The alignment procedure is based on the measurement of the dependence of the mean residuals in the u and v views on both the u and v coordinates and is described in more detail in [10].

After telescope alignment, events with just one track, with hits on both sides of all six planes, and track-fit $P(\chi^2) \geq 10\%$ are selected. In a typical run, these requirements correspond to an overall efficiency of roughly 50% of all triggered events. The resulting data-set has position-residual distributions (averaged over all telescope planes) which can be approximately fitted with Gaussians with means consistent with zero and $\sigma = 5\,\mu$m and $\sigma = 9\,\mu$m in the x and y view, respectively. The p-side resolution is better than the u-side one because the presence of an additional floating strip improves the uniformity of the charge splitting among the readout strips.

Typical p and n-plane residual distributions are presented in Fig. 6 and show

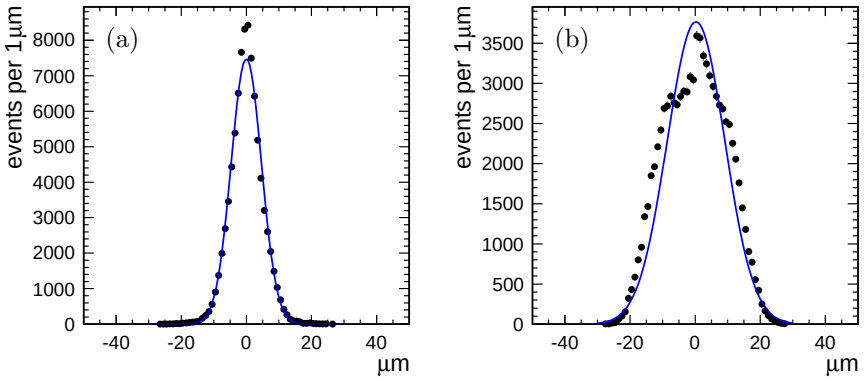

Figure 6: Typical residual distributions (points) between fitted tracks and hits in all telescope planes for the the p-side (a) and the n-side (b). The line represents a Gaussian fit. Tails are truncated because of the requirement on the track fit χ^2 probability described in the text.

sizable deviations with respect to a Gaussian shape, implying the presence of some systematic effects. We could not find evidences connecting these distributions to mis-bonded channels or the presence of insensitive strips. At any rate, the widths of the residual distributions indicate that track extrapolation to the devices under test are precise enough for the rest of the analysis.

5.2. Hybrid Pixels Efficiency and Resolution

The efficiency of the DUT is studied both as a function of the angle of the track with respect to the normal to the detector (angle of incidence θ) and as a function of the threshold used in the pixel charge comparators.

In order to vary the angle of incidence, the DUT are rotated in the xz plane from 0° to 60° in steps of 15°, and then up to a maximum of 70°. In runs at normal incidence, pixel charge thresholds are varied from 730 to 820 DAC counts, corresponding to a range from about 12.5% to 40.6% of the charge released by a m.i.p.. Relatively high thresholds are used in order to overcome the data-acquisition limitations of the prototype under test described in section 2.4. A different acquisition run with about one million events is taken for each condition.

Hits in the DUT are defined as clusters of fired pixels that are either adjacent or separated by up to one non-fired pixel along either u or v. The cluster u and v local positions are set to the unweighted averages of the u and v positions of the fired pixels. To associate hits in the DUT to the reconstructed track, we first study the residual distributions between the track extrapolation at the DUT and the cluster positions, so as to align the DUT in x and y by using the mean of the residuals. No alignment is performed in the angle around the z axis nor in the other degrees of freedom. After alignment, we observe

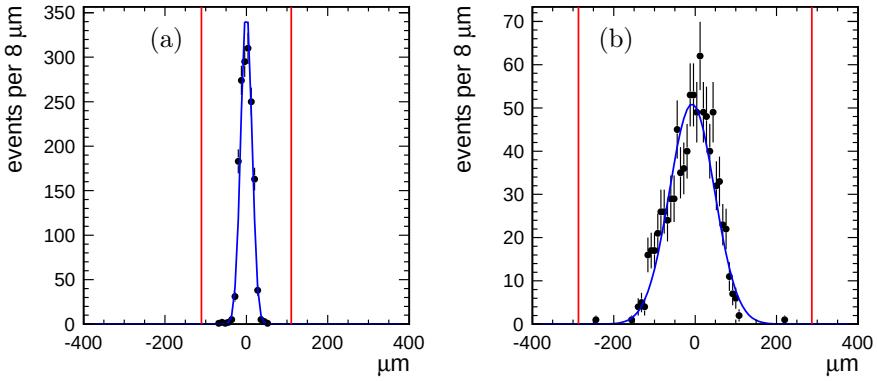

Figure 7: Example u-view residual distribution (points) for tracks hitting a hybrid pixel detector at normal incidence (a) and at 60° incidence angle (b). The line represents a Gaussian fit. The red vertical lines show the requirements on the residual to consider the hit associated to the extrapolated track.

centered and approximately Gaussian residual distributions with a negligible amount of noise hits. The residual distributions in the u-view for data collected with a pixel-charge threshold corresponding to about 25% of a m.i.p., at both normal and 60° beam incidence angle, are shown in Figure 7. The width of these residuals is driven by the DUT intrinsic resolution, which is nominally $50\,\mu\text{m}/\sqrt{12} \approx 14.4\,\mu\text{m}$ at normal incidence and increases with the incidence angle because the track ionization is distributed on a larger number of pixels, some of which may more easily be under threshold. Figure 8a shows the u-view residual width, as estimated by the σ of a Gaussian fit, as a function of the angle of incidence of tracks for the three pixel sensors under test as well as a Monte Carlo simulation, which is described in next section. From $\theta = 0$ to $\theta = 70°$, the residual width in the x-direction increases approximately from $10\,\mu\text{m}$ to $70\,\mu\text{m}$, because tracks release their ionization over an increasingly larger amount of pixels. This is confirmed in Figure 8b, which reports the average cluster size as a function of the incidence angle. In the y-direction, the residual width is larger than along x for normal incidence tracks, and ranges from $15\,\mu\text{m}$ to $19\,\mu\text{m}$. The larger y residual width is understood to originate from the larger uncertainty of the track extrapolation along y from the silicon telescope.

Hits in the DUT are associated to extrapolated tracks by requiring that they are closer than 4 times the (angle dependent) width of the residual distribution, plus $60\,\mu\text{m}$ to account for non-Gaussian tails caused by delta-rays. The detector efficiency is evaluated by dividing the number of tracks with at least one associated hit by the total number of tracks that extrapolate to the sensitive area of the DUT. The total number of such tracks intercepts on all SuperPix0 DUT is about 560,000. Due to fabrication defects, the prototypes are insensitive on 4 pixel columns at the center of the wafers in the u-view: this area is

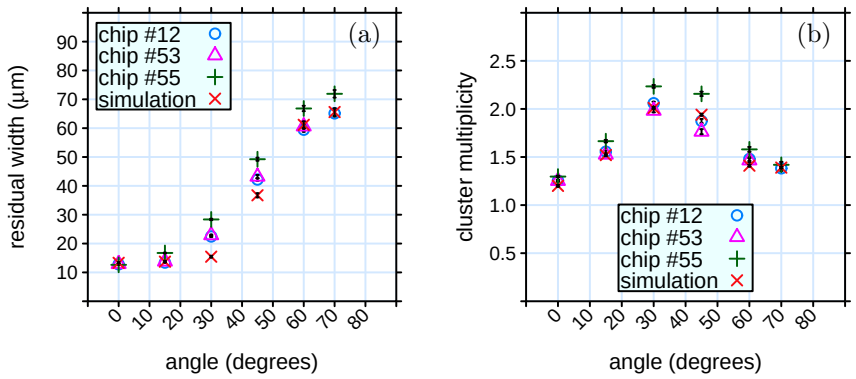

Figure 8: Width of the pixel residual distribution in the u-view (left) and average number of pixels per cluster (right) as a function of the angle of incidence of tracks, for the chips under test. Data were taken at a threshold corresponding to about 25% of a m.i.p.. Monte Carlo expectations are shown for comparison.

excluded from the sensitive area together with a safety margin corresponding to an additional 50 μm pixel spacing. To avoid border effects, the regions within 50 μm from the top and the bottom, and the regions within 150 μm from the left and the right borders of the detector are excluded as well. At non-zero track incidence, pixel detectors are observed to be inefficient in an area where their aluminum frame intercepts the beam particles before they reach the sensors. Although the extent of the effect along the x coordinate is well described by geometrical shadowing, the mechanism that causes the observed inefficiency is not understood. To obtain the DUT hit efficiency, the inefficient area related to the shadowing effect is also excluded. A Bayesan estimate of the efficiency and its uncertainty is obtained by using a Jeffreys' prior [**?**]. Similar results are obtained by using the naive estimators $\epsilon = k/n$ and $\sigma^2(\epsilon) = k(n-k)/n^3$, where k denotes the number of hit-associated tracks and n the number of tracks that extrapolate to the sensitive area of the sensors. The measured efficiency is shown on the left side of Fig 9 as a function of the angle of incidence of tracks for the three pixel sensors under test. Data were collected with a threshold of 770 DAC counts, corresponding to about 1/4 of the signal of a m.i.p.. The chip efficiency at normal incidence and as a function of the value of the charge threshold is shown on the right side of Fig. 9. Inefficiencies are uniformly distributed among pixels and no insensitive pixel was found. However the efficiency is found to depend on the distance of the track extrapolation to the center of the closest pixel in the y coordinate (Figure 10). Pixel sensors at the reference threshold, corresponding to 1/4 of a m.i.p., are close to full efficiency for normal-incidence tracks. More precisely, for this threshold and for smaller ones, an apparent maximum efficiency plateau at about 99.5% is reached. When the threshold is increased above the reference of 1/4 of a m.i.p., the data indicate a progressive and significant efficiency drop. The analysis also shows that the

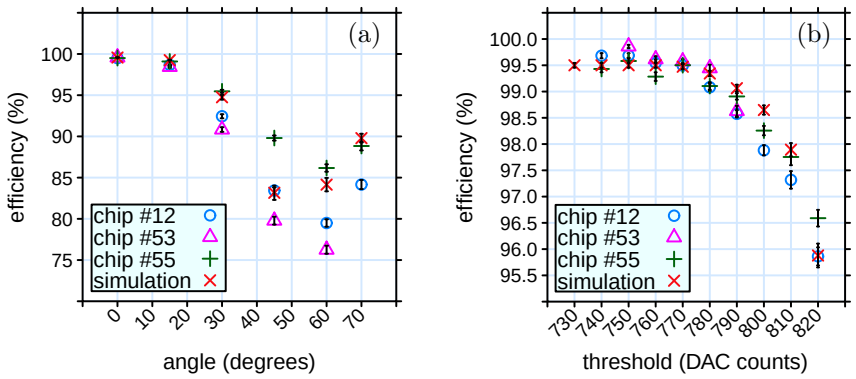

Figure 9: Hit efficiency as a function of the angle of incidence of tracks when the pixel charge threshold corresponds to about 25% of a m.i.p. (left), and as a function of the threshold for normal-incidence tracks (right), for all detectors under test. The DAC values in the picture on the right correspond to a range from 12.5% to 40.6% of the charge released by a m.i.p.. Monte Carlo expectations are also shown.

efficiency decreases considerably for non-zero angle of incidence. For all chips under test, the efficiency falls from ∼99.5% to a minimum of about 80% for 60° angle of incidence, and then moderately increases at 70°.

The efficiency drop with the track incidence angle and with the distance from the closest pixel center in the y coordinate is understood as caused by the fact that track ionization in the sensitive area of the detector is shared among a larger number of pixels: along the x coordinate because of the incidence angle, and along the y coordinate as the track hit moves from the pixel center to the pixel border. For increasing angles of incidence, the released ionization also increases because a larger amount of silicon is traversed. However, charge sharing among an increased number of pixels is such that the probability that all involved pixels remain under threshold increases, up to angles of incidence of about 60°. The moderate efficiency increase between 60° and 70° can be explained by the fact that the increase in the number of involved pixels prevails on the moderate reduction of average ionization per pixel.

6. Hybrid Pixels Response Modeling

The response of the SuperPix0 chip has been modeled fairly well using a coarse Monte Carlo simulation, which includes energy loss in silicon with a Landau distribution, charge splitting among the geometrically interested pixels, and the presence of a threshold comparator. On top of these features, an additional inefficiency of 0.5% has been introduced in order to match the apparent data efficiency saturation around 99.5%. A simple simulation cannot explain such a plateau, which is believed to be related to the limitations mentioned in sec-

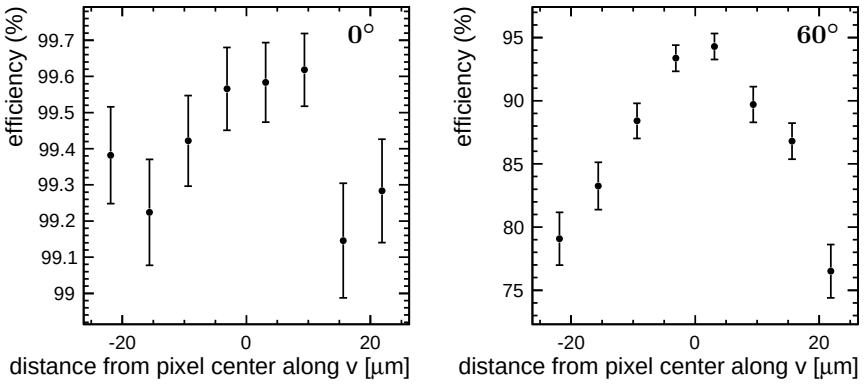

Figure 10: Hit efficiency as a function of the track extrapolation distance from the center of the closest pixel along the y coordinate, on the left for normal incidence tracks, and on the right for tracks at 60° incidence angle.

tion 2.4 and the related workaround in the readout scheme. The presence of noise and threshold dispersion has been tentatively simulated but was found to produce negligible effects, and it was turned off for the results that are shown here.

The Monte Carlo simulation proceeds as follows. First, straight line particle tracks at fixed specified incidence angle and uniformly distributed in x and y are generated. For each track, the segments corresponding to the traversal of each crossed pixel are calculated, and the related energy loss is randomly extracted from the distribution of the energy loss in Silicon, according to a Landau distribution whose mean and width parameters are taken from the literature [**?**].

Each pixel energy loss is evenly divided along $0.1\,\mu m$ steps within its segment, and each step energy loss dE is split between the affected pixel, the closest one in x and the closest one in y. The charge attributed to the closest pixel in x increases linearly from 0% for charge released exactly at the pixel center to 25% when approaching the border between two pixels in x, and the same happens along y. The remaining charge (larger or equal to 50%) is attributed to the hit pixel.

In an alternative approach the charge splitting is implemented as a 2D Gaussian distribution, with the σ parameter set such that tracks hitting the center of a pixel deposit 50% of their charge on that pixel. Both methods give similar results, but the first method appears to fit the data better.

Clusters, or hits, are built in the same way as for the data, e.g. two fired pixels are considered to be in the same cluster if there is at most one non-fired pixel between them in both u and v directions.

In order to compare the predicted behavior of the SuperPix0 chip with the data, for each configuration of threshold and angle of incidence realized at the beam test 10000 events are generated and analyzed as the data. As shown in Fig. 9, the dependence of the efficiency on the angle of incidence is reasonably

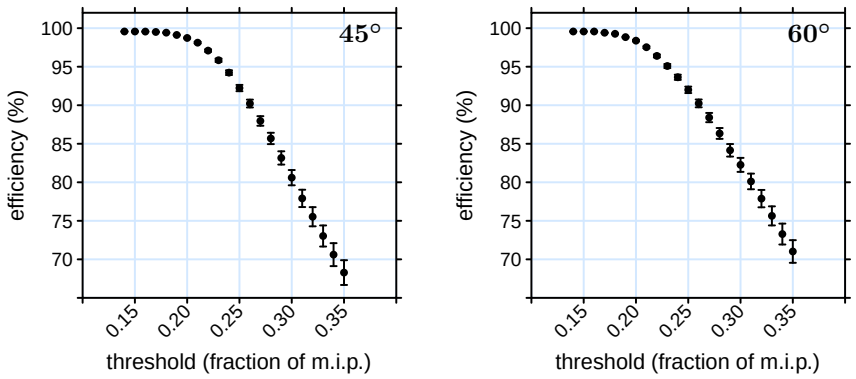

Figure 11: Simulated pixel detector efficiency for track incidence angle of 45° (left) and at 60° (right) as a function of the threshold. According to the simulation, the data were collected using an effective threshold equal to 29% of the ionization produced by a m.i.p.. The range of m.i.p. fractions from 0.15 to 0.35 corresponds approximately to the range of thresholds DAC counts from 725 to 789.

well modeled, although the minimum of the efficiency is predicted to be closer to 45° than to 60°. The simulation confirms that the efficiency dependence on the incidence angle can be explained by the combination of two effects: as long as the angle of incidence increases, the per-pixel collected charge decreases, but the number of affected pixels increases. As a consequence, the probability that *all* the pixels are under threshold first increases and then decreases. The simulation reproduces reasonaly well the dependence of the chip efficiency on the charge threshold (Fig. 9), and the dependence of the x residual distribution width and the cluster size on the incidence angle (Fig. 8).

To obtain an accurate fit to the data, the simulation has to shift the pixel thresholds by a fixed amount equal to 4% of a m.i.p. with respect to the values that were measured in laboratory tests (Section 2.4). Figure 11 shows the simulated efficiency at 45° and 60° when varying the threshold. According to the simulation, the pixels would be fully efficient (i.e. they would reach the apparent 99.5% efficiency plateau) for thresholds equal or smaller than 0.16 of a m.i.p.. This corresponds in the data to about 729 DAC counts or to a nominal threshold of about 12% of a m.i.p..

7. Conclusions

The VIPIX collaboration has tested three prototype SuperPix0 hybrid pixel detectors with a 120 GeV pion beam at the SPS H6 beam line at CERN. A telescope consisting of six double-sided silicon strip detectors was used to reconstruct tracks that were then used to evaluate the performance of the sensors under test.

The efficiency of the chips has been measured as a function of both the angle of incidence of the impinging particles and the threshold used in the pixel charge discriminators. Relatively high threshold settings were used to overcome some fabrication defects that were affecting the readout chain and are now fully understood. The width of the distributions of residuals between the position of detector hits and the pion impact points suggests the detector resolution is consistent with the expectation for a 50 μm pitch pixel detector with digital readout.

The chip efficiency for tracks at normal incidence is found to saturate at about 99.5% for charge threshold corresponding to less than 25% of the energy loss expected for a m.i.p.. This behaviour is believed to be due to an *ad-hoc* fix up implemented in the readout scheme to avoid the consequences of the aforementioned defects, already in the current version of the prototype. A significant efficiency drop is observed for non-zero angles of incidence, which is understood to be related to charge splitting among an increasing number of pixels.

A coarse Monte Carlo simulation is able to model reasonably well the features observed in the data and suggests that lowering the threshold to $\sim$12% of a m.i.p. would result in a sensor that is fully efficient at all incidence angles.

Conclusioni rispetto all'uso nel layer0 di SuperB?

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