

FTK integration in the ATLAS TDAQ the Vertical Slice

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INFN Frascati

ATLAS DETECTOR

Centre mass energy 14 TeV

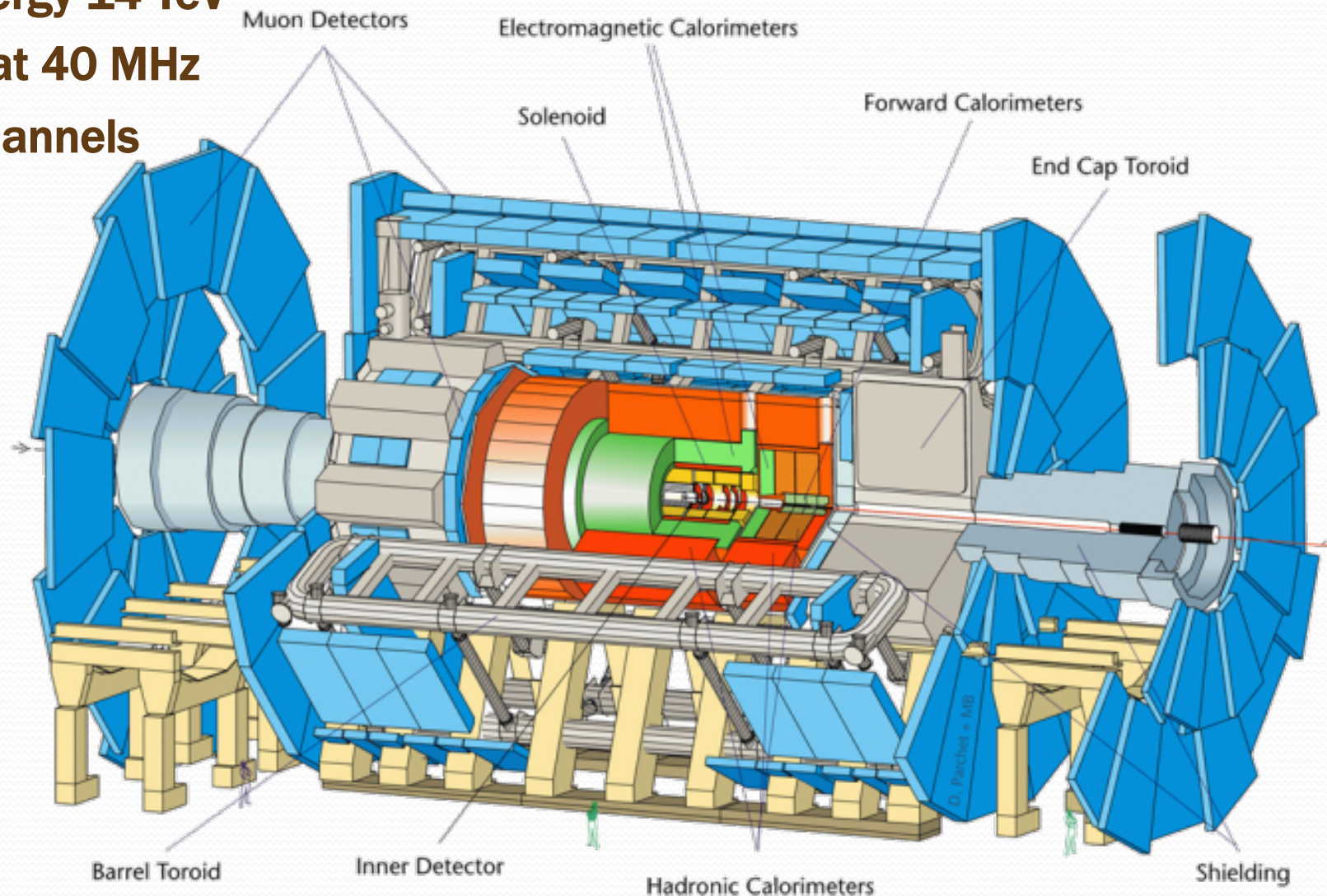
Bunch crossing at 40 MHz

140 000 000 channels

Weight 7000 t

Diameter 22m,

Length 46m



ATLAS DETECTOR

Centre mass energy 14 TeV

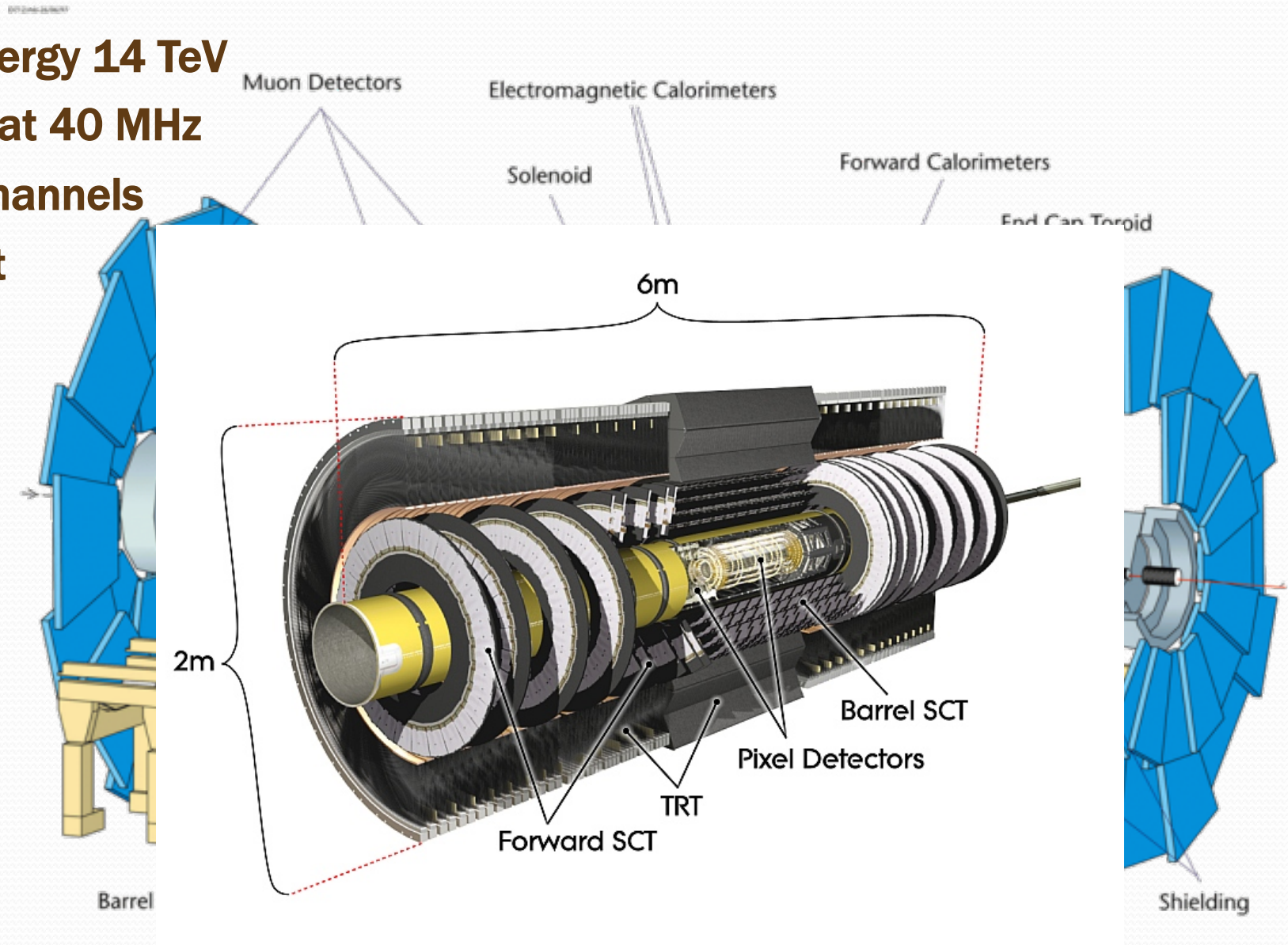
Bunch crossing at 40 MHz

140 000 000 channels

Weight 7000 t

Diameter 22m,

Length 46m





ATLAS Trigger-DAQ concept (1)

Latency

Rates

200 - 600 Hz



TDAQ slides courtesy of
K. Kordas and S. Kolos

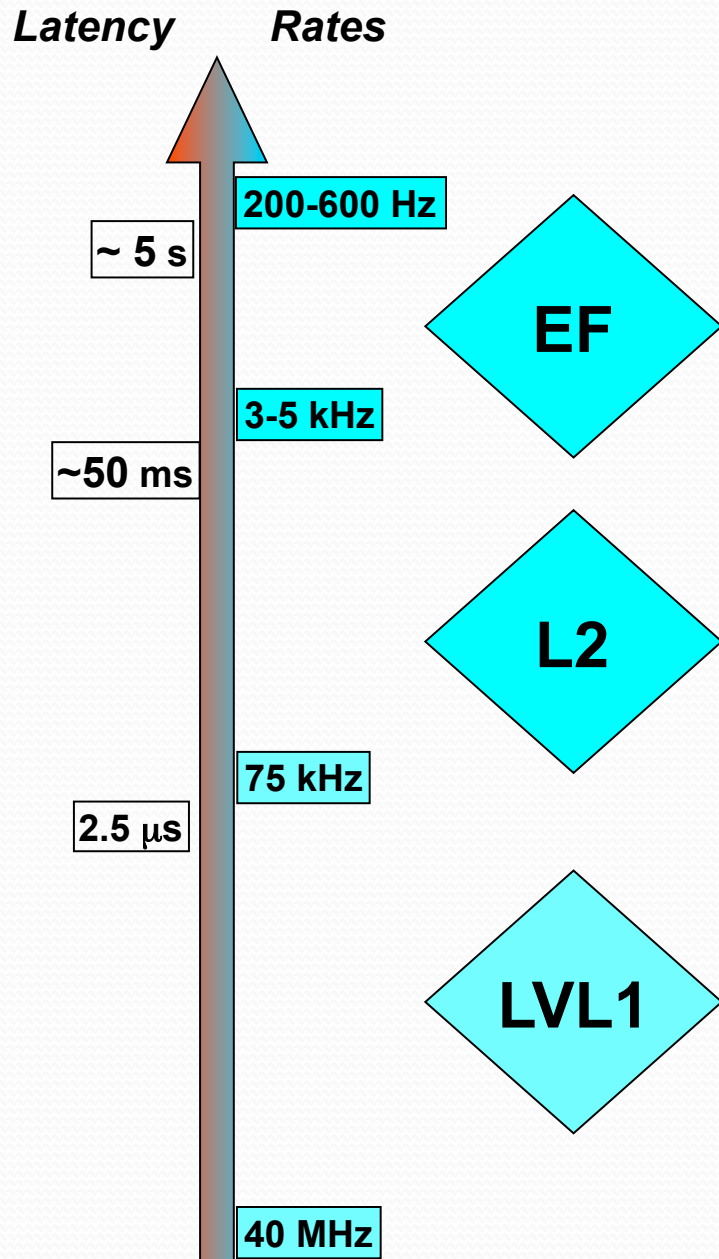
- ✓ The job of the Trigger and Data Acquisition (TDAQ) System:
 - ✓ Reduce 40 MHz bunch-crossing (~ 1 GHz of proton-proton interactions) to $O(400)$ Hz of recorded events
 - ✓ Transfer events from detector read-out to the mass storage

ATL-DAQ-CONF-2007-022; Nucl. Phys. B, Proc. Suppl. 172 (2007).
ATL-DAQ-CONF-2005-025; IEEE TNS V53, Issue 3, Part 1, (2006).

**40
MHz**



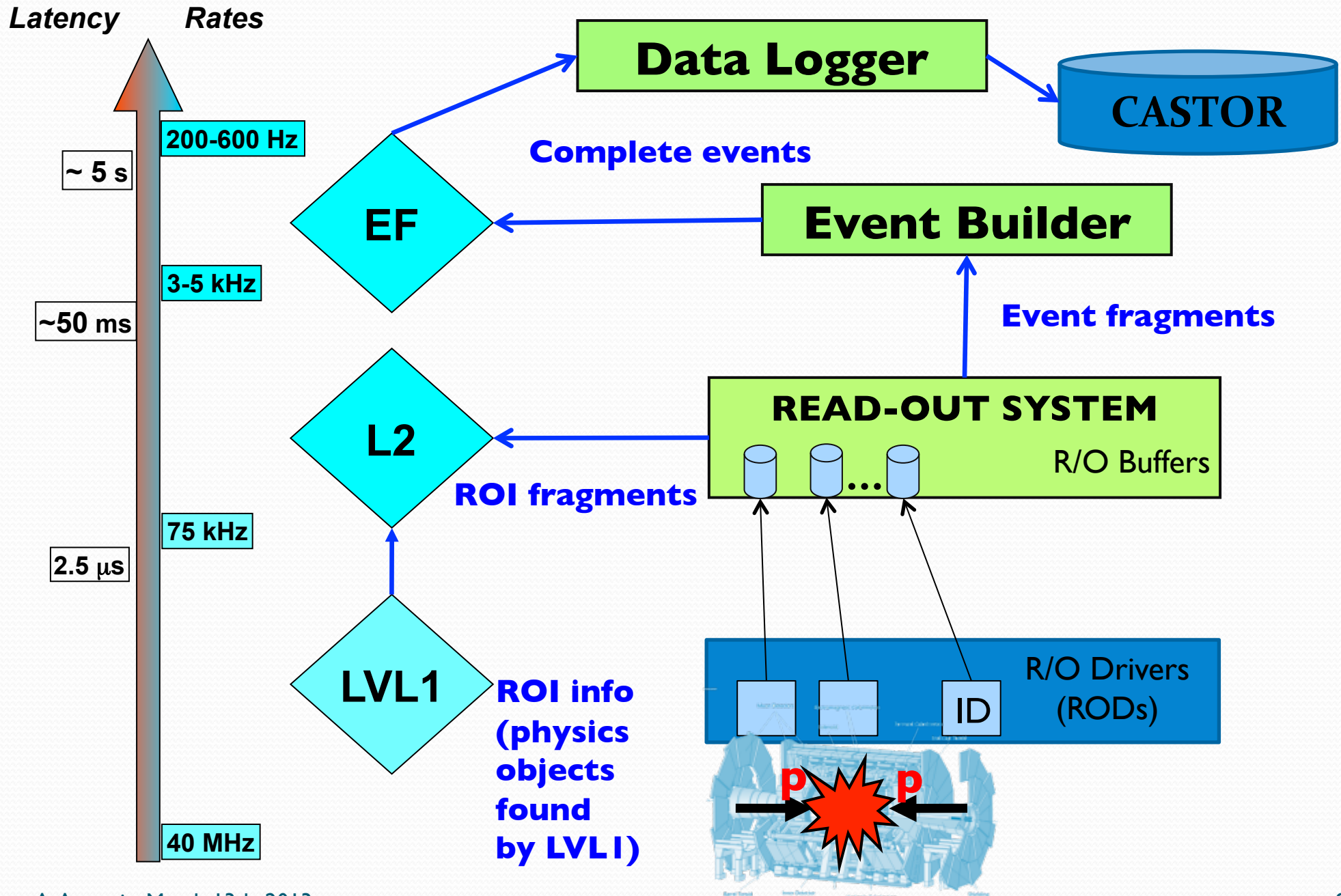
ATLAS Trigger concept



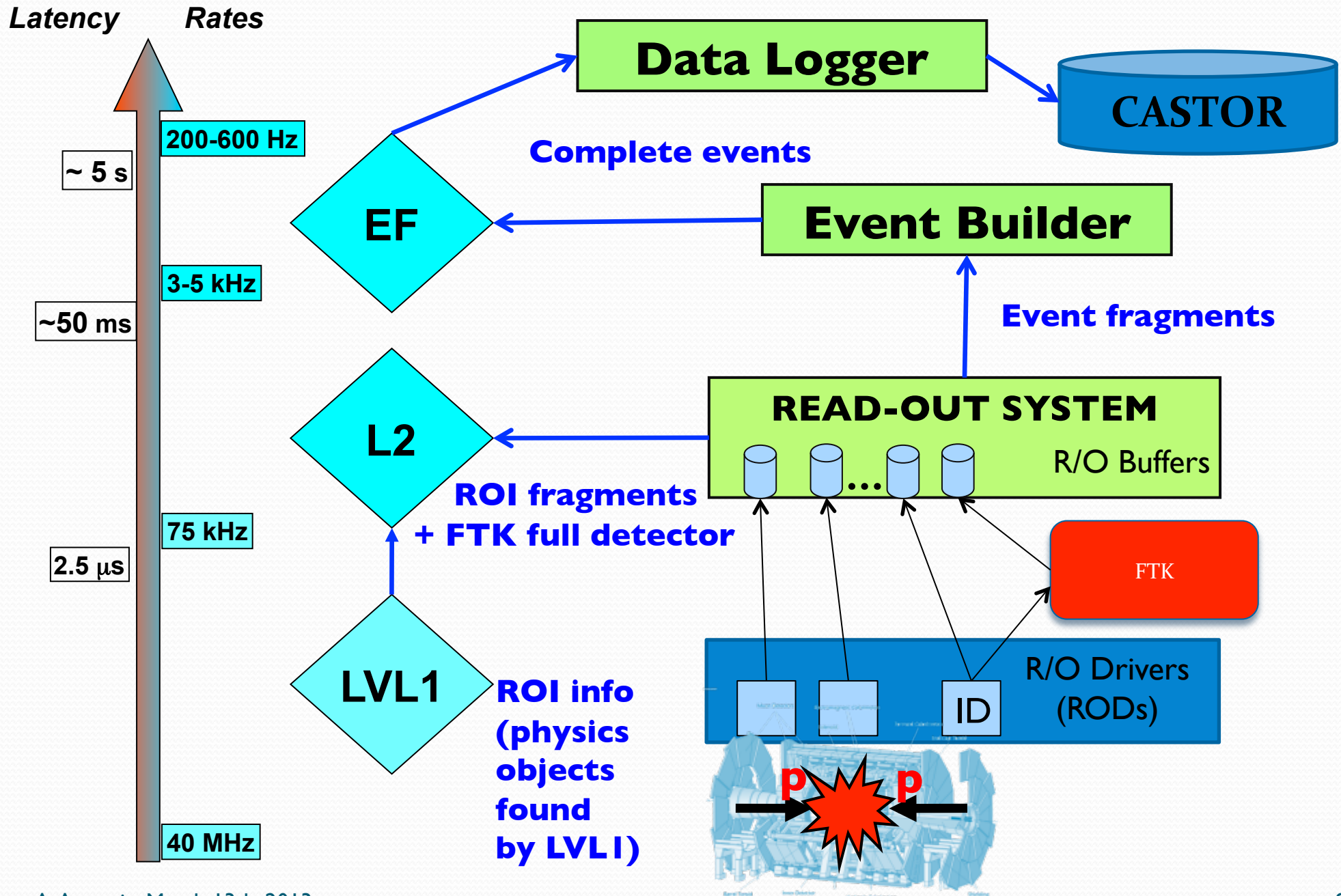
- ATLAS has 3 levels trigger system:
 - HW based LVL₁:
 - $40\text{MHz} \Rightarrow 75\text{kHz}$
 - SW based High Level Trigger (HLT):
 - LVL₂ trigger :
 - $75\text{kHz} \Rightarrow 3\text{-}5\text{kHz}$
 - Event Filter (EF) :
 - $3\text{-}5\text{kHz} \Rightarrow 200\text{-}600\text{Hz}$



ATLAS Trigger concept



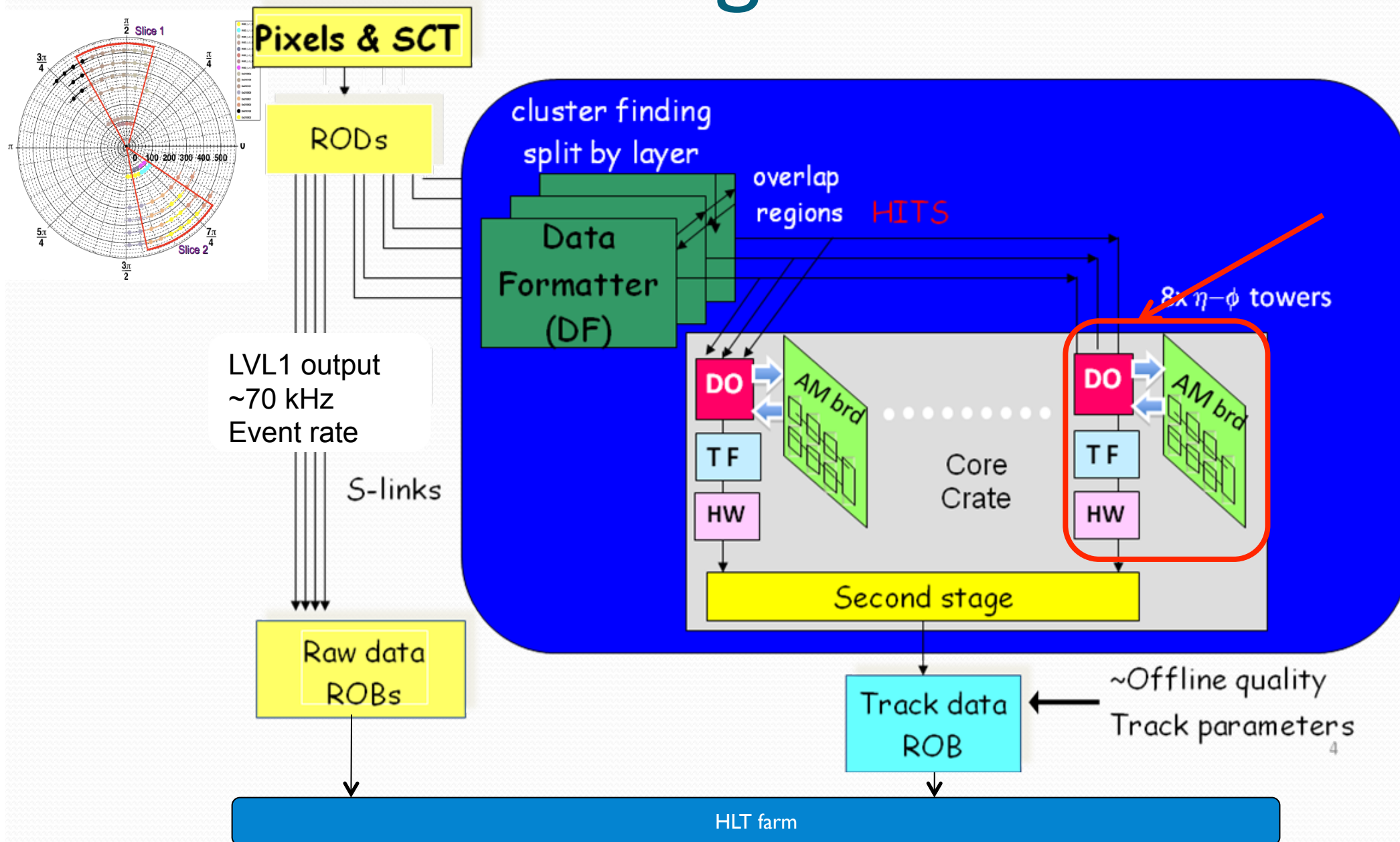
FTK in the ATLAS TDAQ



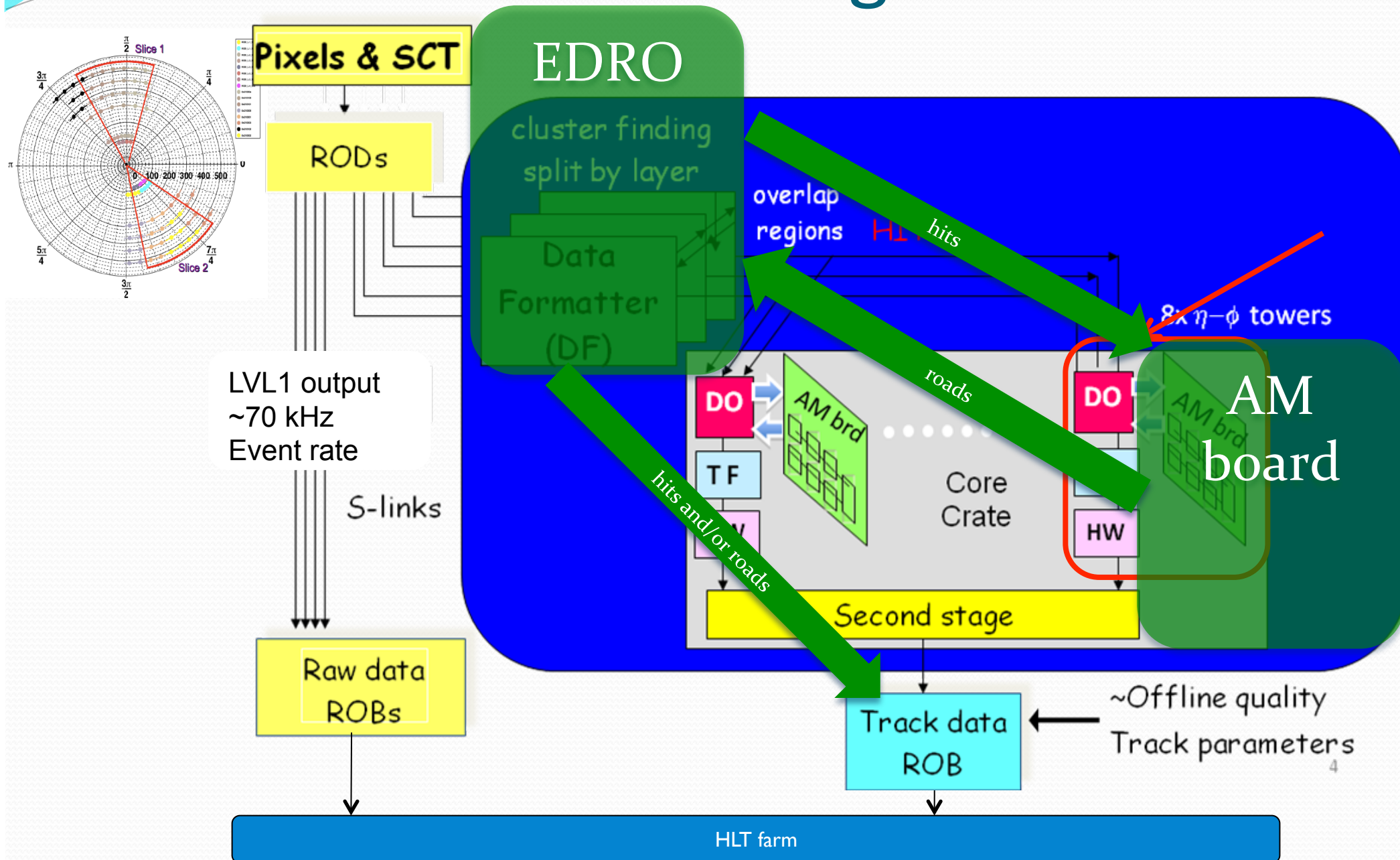
The FTK Vertical Slice (up to now)

- Install existing FTK prototypes at Point 1
- Execute the first part of FTK algorithm
 - pattern recognition to find low resolution roads
 - no track fitting (yet)
- Goals:
 - Verify integration of FTK prototypes with ATLAS TDAQ
 - Verify hardware under normal data taking conditions
 - Verify that real-time FTK output from collision data corresponds to FTK simulation

FTK block diagram



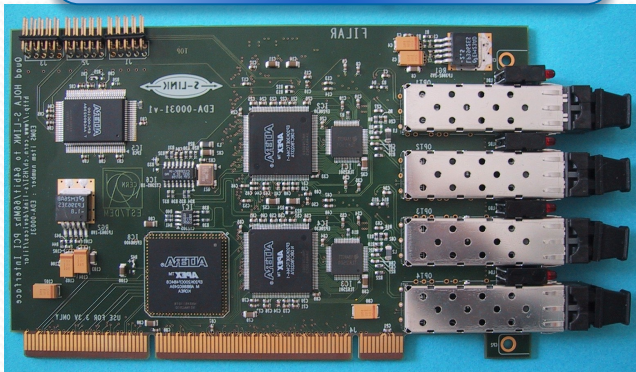
Vertical Slice block diagram NOW



QUEST/FILAR/ROBIN/ROS

QUEST

Slink data source
FILAR card w/ QUEST FW

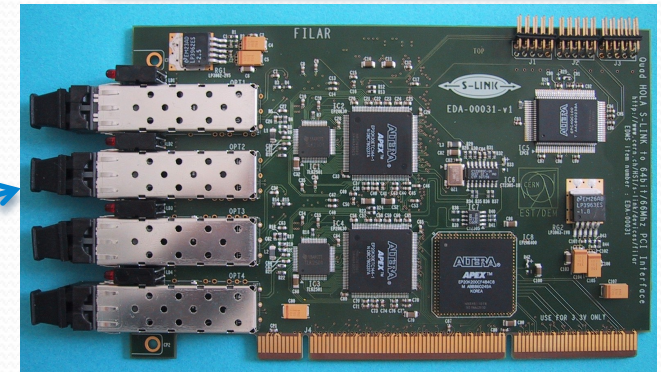


CERN S-LINK

<http://hsi.web.cern.ch/hsi/s-link/>

FILAR

Slink data receiver



FTK
VS

S-LINK I/O tools

ROBIN

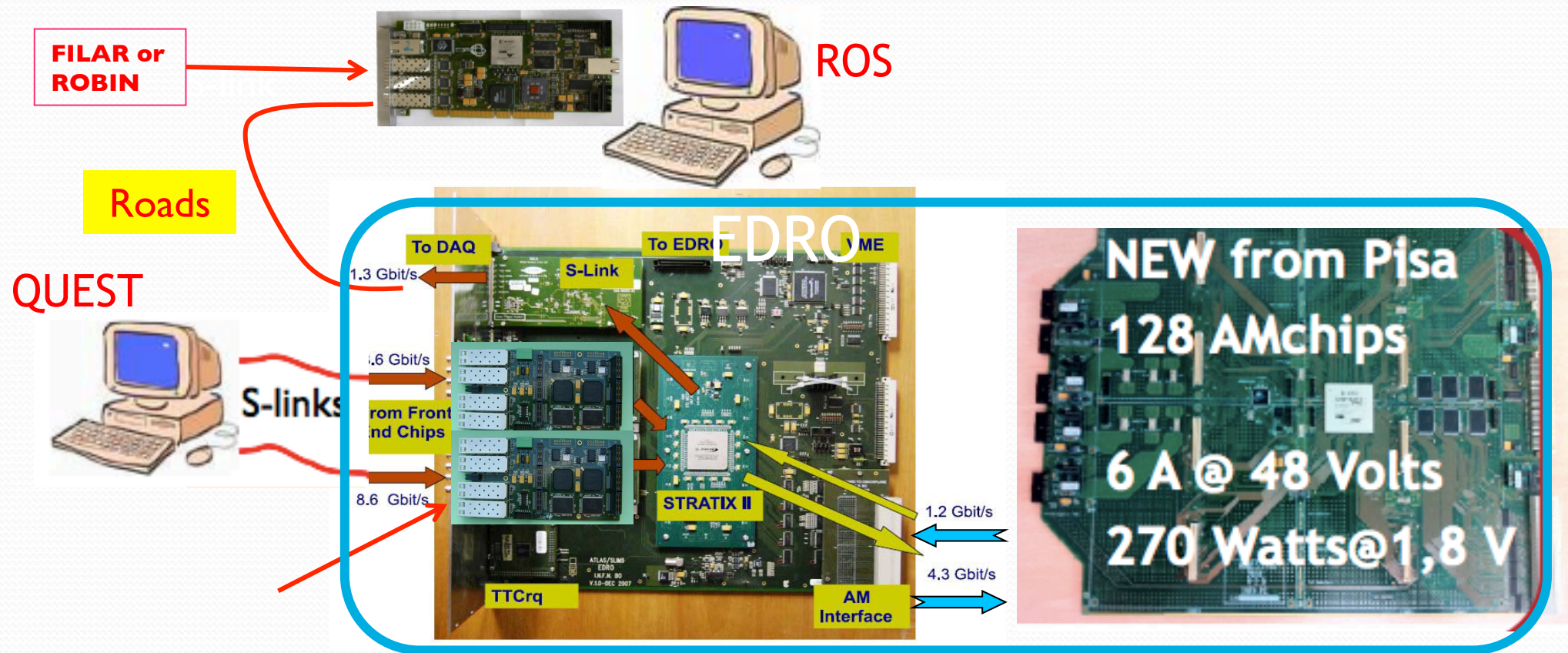
Slink data receiver

ROS PC

With ROBINS



QUEST → FTK_IM → EDRO → AM → EDRO → ROS



Test system in TDAQ lab 4 at CERN,
Pisa, Bologna, Waseda

HW Hit generation in EDRO → AM → EDRO → ROS

Test system in Bologna: sample run

TDAQ Rate

HW hit generation
inside EDRO

to exercise the system
at low and high rates

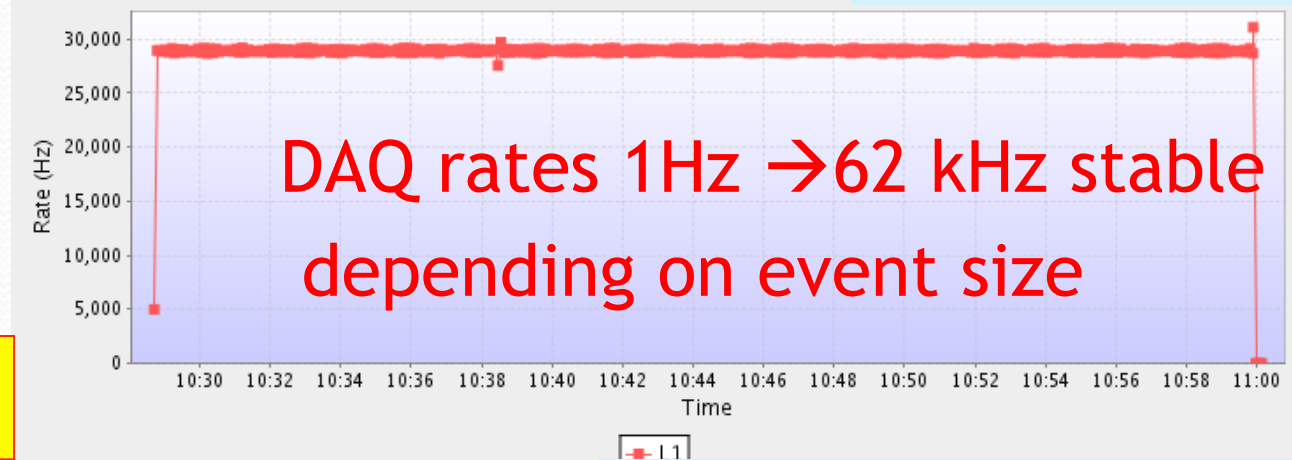
No TDAQ errors

Mean size ≈ 500 words

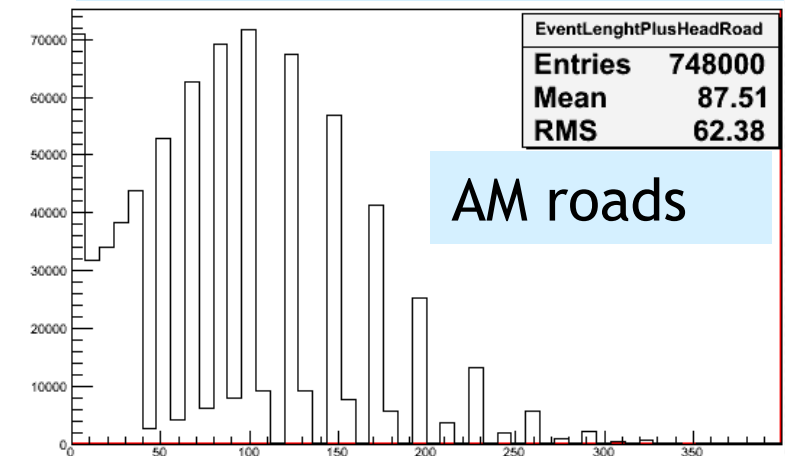
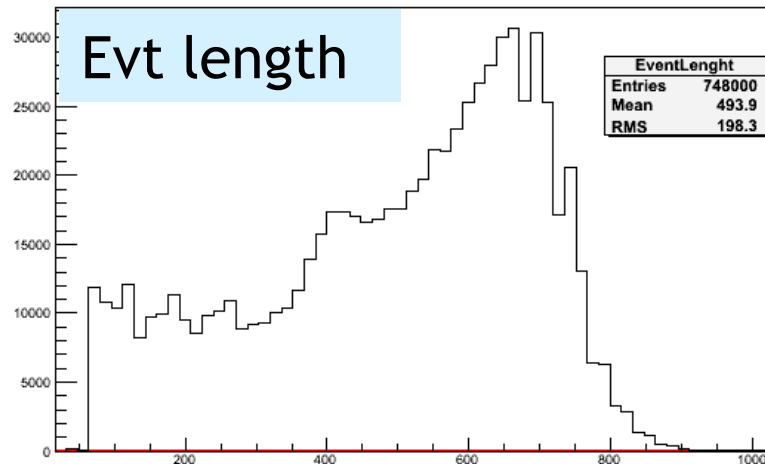
Mean roads ≈ 90

TDAQ rate: 28 kHz

**Repeat
with full
chain**



Online histograms

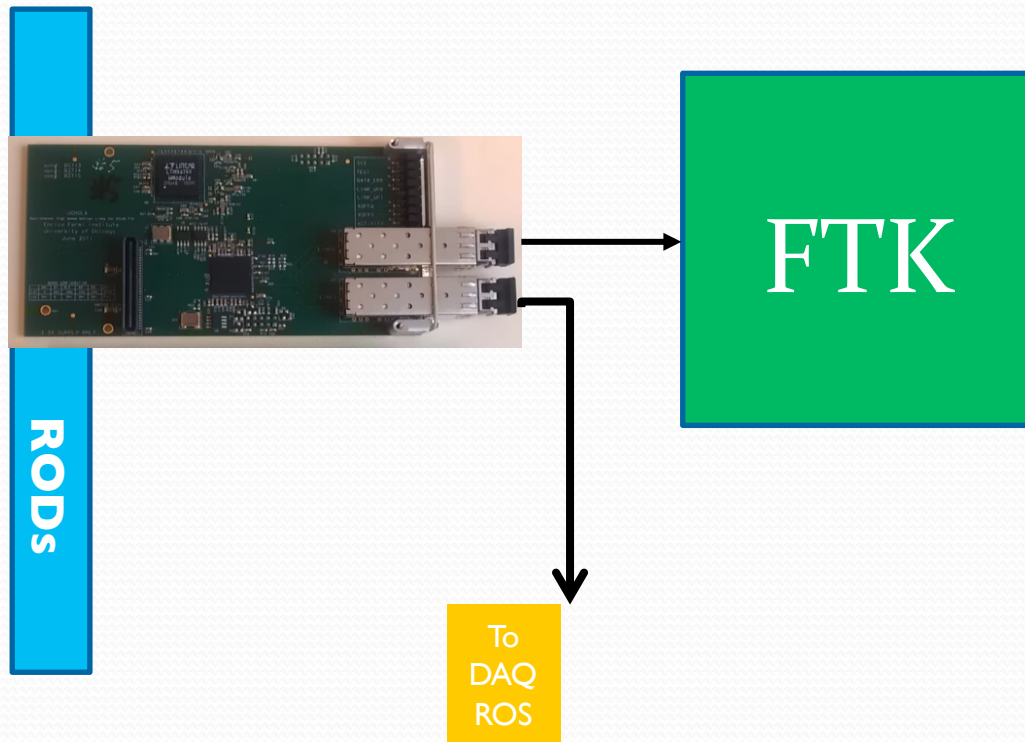


Comparison with offline analysis: on 100k events, 9M HW roads, 99% matched in simulation (missing roads due to event mixing, wrong data transfer or cuts), 0.1% missing End-Events.



FTK Vertical Slice at CERN

Dual-output HOLA



- Sends **SCT & pixel** data to **DAQ & FTK**.
- All required boards produced and tested.
- **32 boards** installed at **P₁**.

Installing the dual-output HOLAs

16 pixels + 16 SCT dual HOLAs and fibers installed

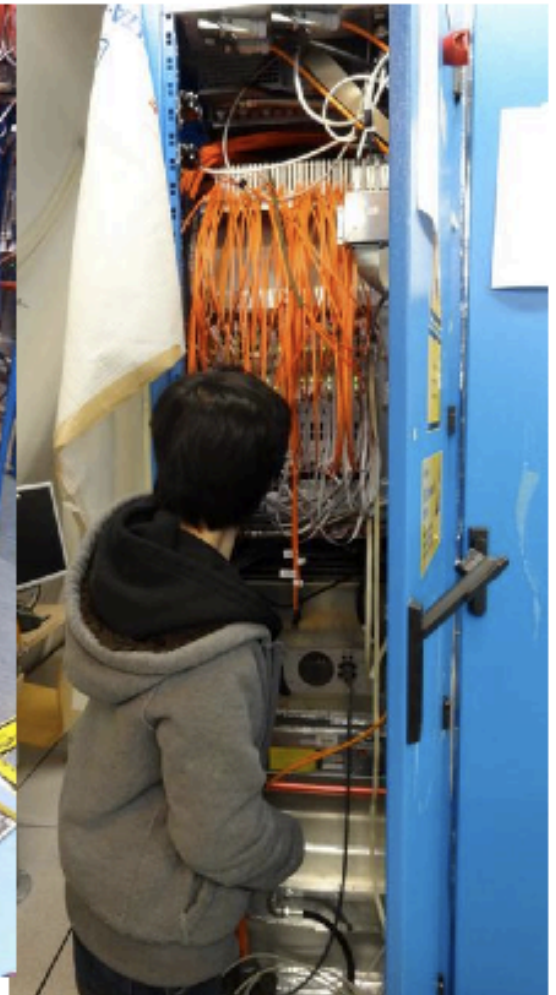
Preparing FILAR test PC that reads out the FTK link



Mounting dual-channel HOLAs on ROD-BOC boards

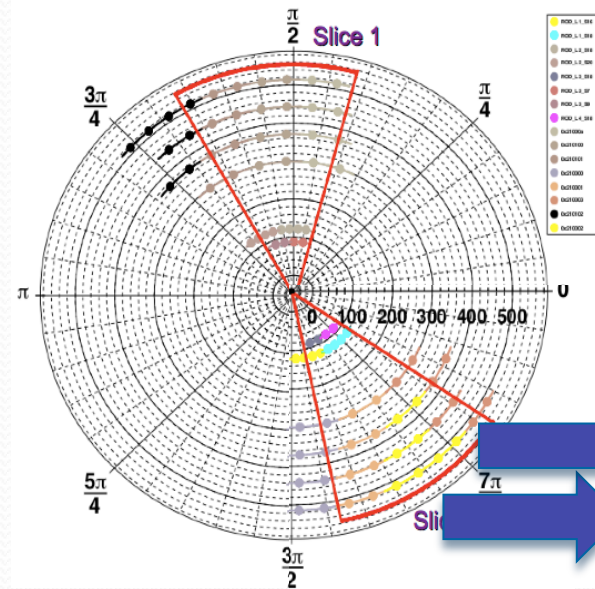
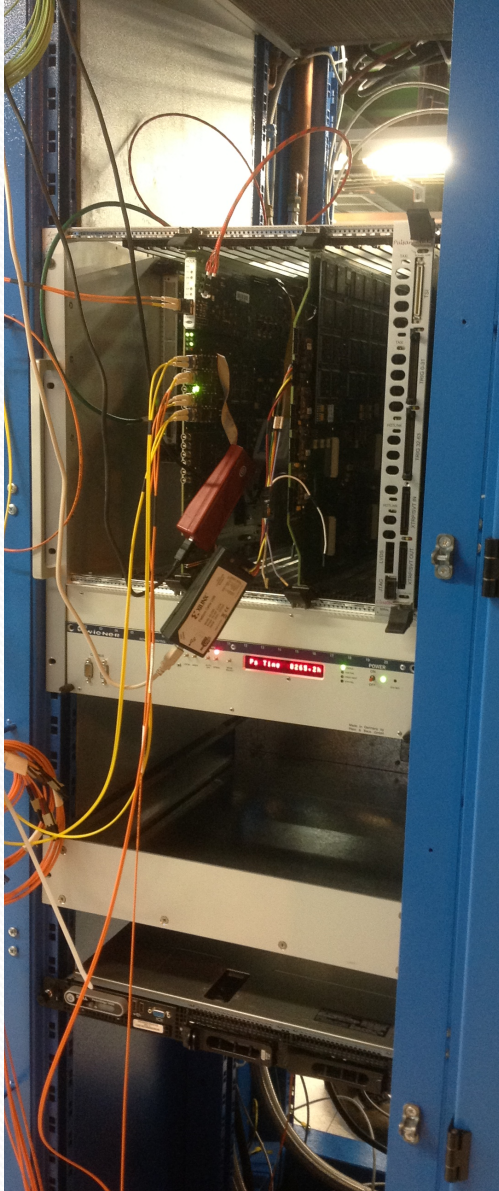


Connecting FTK fiber to the dual-channel HOLA

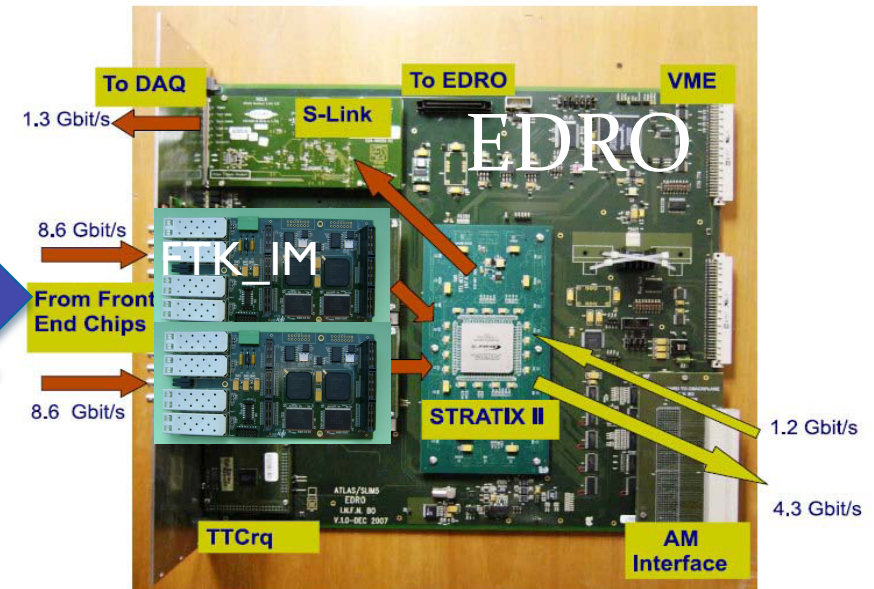


The FTK Vertical Slice in USA15

FTK prototypes in USA15



1 EDRO + 2 FTK_IM

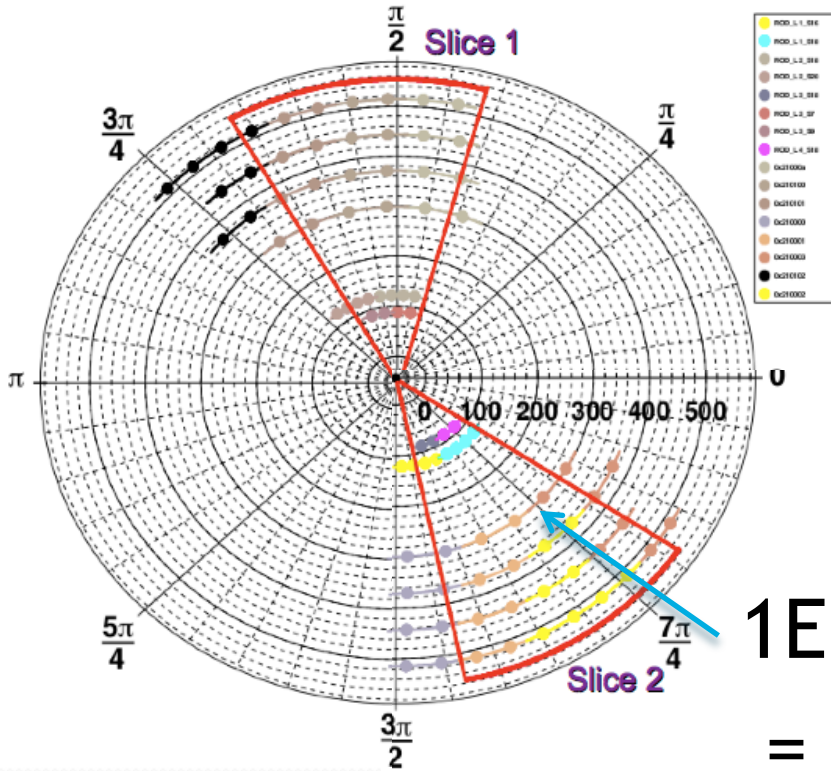


4 pix (L1, L2) + 4 SCT
RODs per tower ($0.3 < \eta < 1.15$)
Total 16 ROLs for 2 towers
Now 1 tower:
4 SCT or 4 QUEST inputs

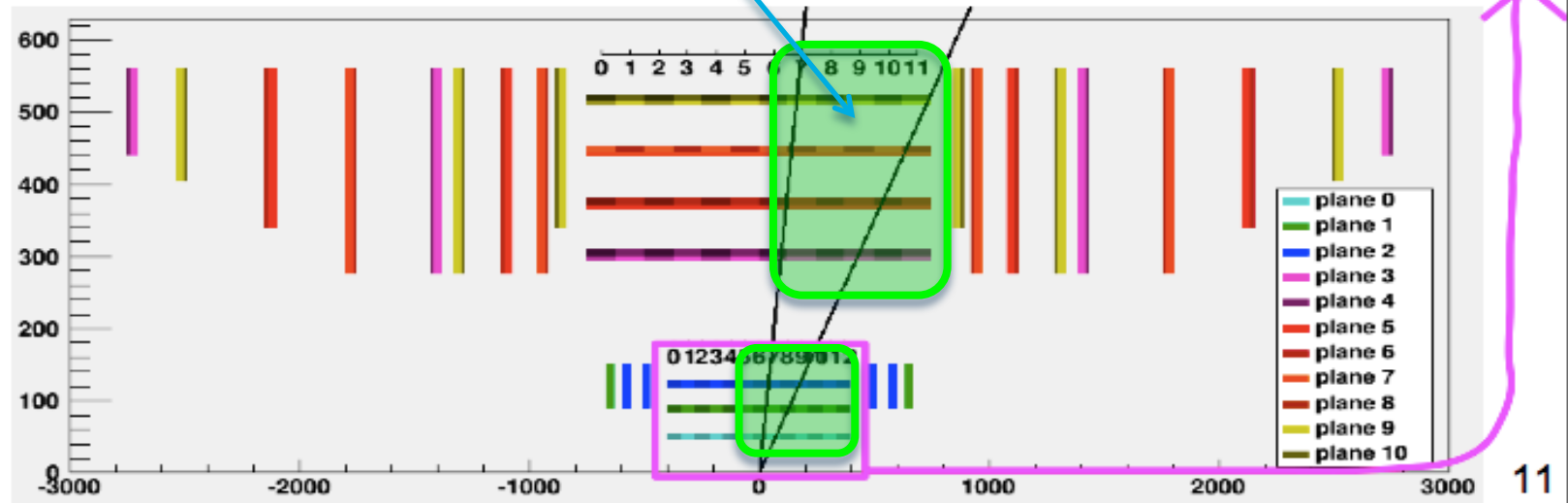
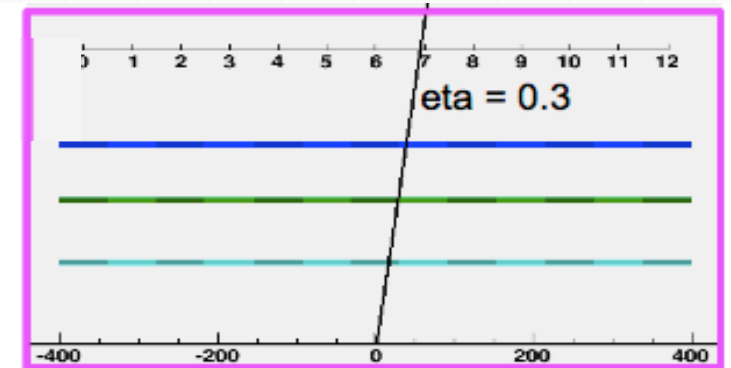


45degree phi towers ($0.3 < \eta < 1.15$)

4 pix (L1, L2) + 4 SCT
RODs per tower ($0.3 < \eta < 1.15$)
Total 16 ROLs for 2 towers



1EDRO+1AMB
= 1 tower



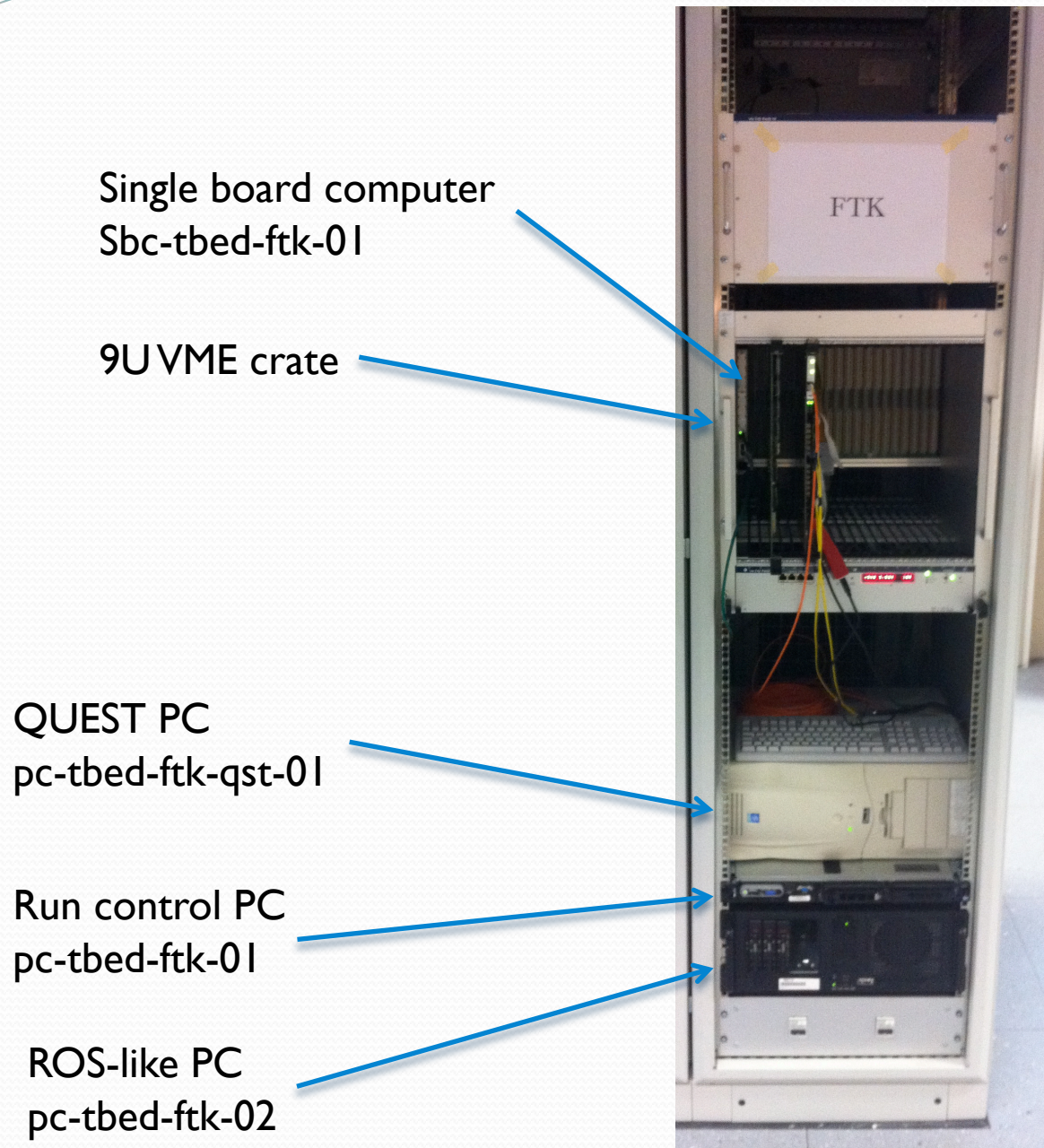
Current VS status

- Preparation of board prototypes and initial FW/SW development (Italy, Waseda, TDAQ lab 32 at CERN)
- Jan/Feb 2012: dual output HOLA installation
- Sep 2012:
 - Crate and boards moves to Point 1
- Sep-Oct 2012:
 - FTK system integrated in the ATLAS partition
 - Data pass-through (little processing)
- Oct-Dec 2012:
 - Developing SW and FW needed to find patterns w/ SCT
 - More TDAQ integration tests
- Jan-Feb 2013:
 - Inclusion in ATLAS partition for cosmics, stand-by and collisions
 - First pattern finds p-p collisions at $\sqrt{s} = 2.76$ TeV
 - More information in F. Lasagni's talk
 - Lot to TODO to get system ready for data taking

FTK Vertical Slice in lab4



FTK Vertical Slice in lab4



FTK configuration in OKS

The screenshot displays two windows from the OKS (Online Kernel Setup) application. The left window, titled 'Oks Data Editor', shows a list of schema files and data files. The right window, titled 'Oks Class : ReadoutModuleFTK', shows the configuration for the ReadoutModuleFTK class, including its objects and data files.

Oks Data Editor

Schema Files:

- /atlas/oks/tdaq-04-00-01/daq/schema/RODBusy.schema.xml
- /atlas/oks/tdaq-04-00-01/daq/schema/coca.schema.xml
- /atlas/oks/tdaq-04-00-01/daq/schema/core.schema.xml

Data Files:

File	Access	Rep
/atlas/oks/tdaq-04-00-01/bcm/segments/BCM_DQM_PM_tree.data.xml	read-only	none
/atlas/oks/tdaq-04-00-01/ctp/sw/L1CT_sw.data.xml	read-only	none
/atlas/oks/tdaq-04-00-01/daq/hw/hosts-bst.data.xml	read-only	none
/atlas/oks/tdaq-04-00-01/daq/hw/hosts-lv12.data.xml	read-only	none

Matching names of files: ☐ Match case ☐ Regular expression

Classes:

Name	Number of instances	Is abstract
ReadoutModuleFTK	1	No

Oks Class : ReadoutModuleFTK

Class: ReadoutModuleFTK

Objects:

UID	PhysAddress	EnableSpy	LookUpTables
Edro1	0	0x1	/det/tdaq/ftk/ftk_v2/ftk_edro_1/data/tower0_LUT_

Matching UIDs: ☐ Match case ☐ Regular expression

Oks Object : ReadoutModuleFTK@Edro1

Object ID: Edro1

Class: ReadoutModuleFTK

Data File: /det/tdaq/ftk/oks/daq/segments/FTK-Segment.data.xml

Data:

Attributes:

PhysAddress:

EnableSpy:

LookUpTables:

SimulatedHits:

PixelMap:

SCTMap:

IM_Prescale:

IM_MaxHits:

SimulatedTriggers:

OutBuf:

Close

HW configuration stored in OKS.
A few registers and a few "MAP" files
for each board.

FTK VS with run control

The screenshot displays the FTK VS software interface, which is used for managing the Run Control state and monitoring the execution of various segments. The interface is divided into several panels:

- Run Control State:** Shows the current state as **RUNNING**. It includes buttons for **SHUTDOWN**, **BOOT**, **TERMINATE**, **INITIALIZE**, **UNCONFIG**, **CONFIG**, **STOP**, **START**, **HOLD TRG**, and **RESUME TRG**. There are also indicators for **Beam Stable**, **Warm Start**, and **Warm Stop**.
- Run Information & Settings:** Displays the **Lumi Block** (3) and a table of **Level 1** and **Level 2** data. The table shows the **Number** and **Rate** for each level, as well as **Event builder**, **Event filter**, and **Recorded** counts.
- Run Control Segments & Resources:** A tree view showing the hierarchy of running segments. The **RootController** is the top-level segment, which branches into **FTK**, **RCD-FTK**, **ROS-FTK**, **FTK_AM:pc-ftk-l2pu-test-01**, **FTk_Am_App**, **L2-Segment-1:pc-ftk-l2pu-test-01**, **Top-LVL2-L2-Segment-1-Gatherer**, **L2SV-Segment-1:pc-ftk-l2pu-test-01**, **L2SV-1**, **L2-Segment-1-1:pc-ftk-l2pu-test-01**, **EBEF-Segment-1:pc-ftk-l2pu-test-01**, **DFM-1**, **LVL2ResultHandler-1**, **Top-EF-EBEF-Segment-1-Gatherer**, **EBF-Segment-1:pc-ftk-l2pu-test-01**, and **SFI-1**. All segments are marked as **RUNNING**.
- RootController:** A panel showing the **RootController** segment, which includes **HW**, **PMG**, and **Infrastructure** components.
- Subscription criteria:** A panel for selecting the severity of messages to be displayed. It includes checkboxes for **WARNING**, **ERROR**, **FATAL**, and **INFORMATION**, as well as an **Expression** field and a **Subscribe** button.
- Message Log:** A table showing the log of messages, with columns for **TIME**, **SEVERITY**, **APPLICATION**, **NAME**, and **MESSAGE**.

A blue callout box points to the **FTK** segment in the tree view, labeled "FTK segment". Another blue callout box is overlaid on the right side of the interface, containing the text: "Preliminary version of online software for HW configuration Integrated with runControl".

FTKSim for validation

- FTK vertical slice validated against FTKSim
- Offline FTKSim
 - Generates configuration files
 - Produce list of expected roads/tracks
 - See G. Volpi's talk
- Online FTKSim
 - Reproduces internal data and output data bit by bit
 - HW validation and debug
 - See F. Lasagni's talk

Test strategy

- Test prototypes at home institutions
- Bring prototypes to CERN and test at lab4
 - With quest
- Integrate prototypes in USA15
 - Standalone tests with quest
 - Parasitic tests with SCT and Pixels
 - FTK in a separate partition
 - Integrate FTK in ATLAS partition

Activity during Long Shutdown1

- Long shutdown 1 (LS1) until end of 2014
- Using VS rack in USA15 for prototype tests
 - Add ATCA crate
 - Include final FTK prototypes when available
- Prepare for FTK demonstrator installation
 - Install racks in USA15
 - Install dual-output HOLAs for Pixel and SCT
 - Install crates, fibers and services
- Install first production boards when available
- Commissioning



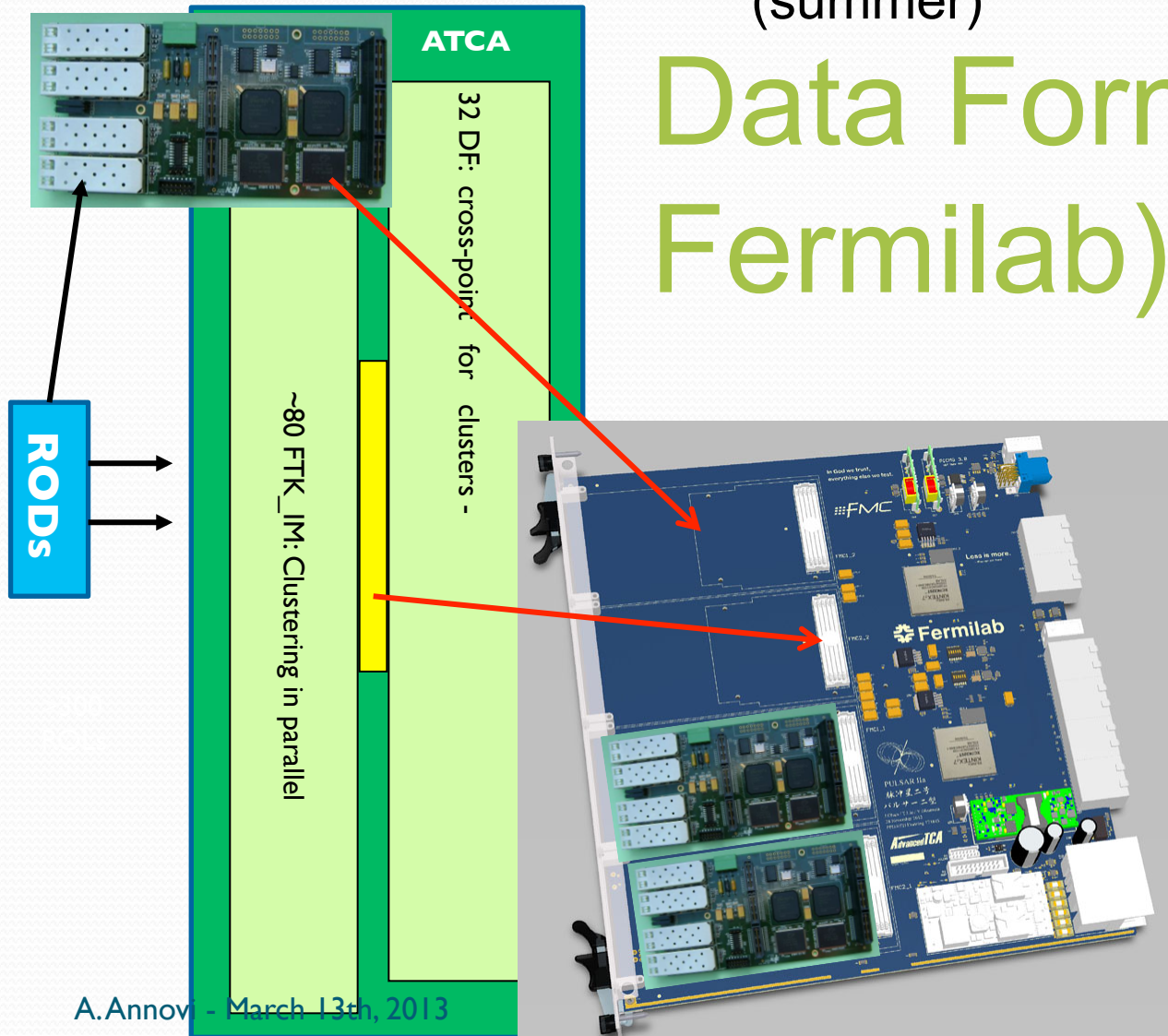
Cards to be integrated for first stage track finding

FTK input mezzanine (FTK_IM Frascati Waseda)

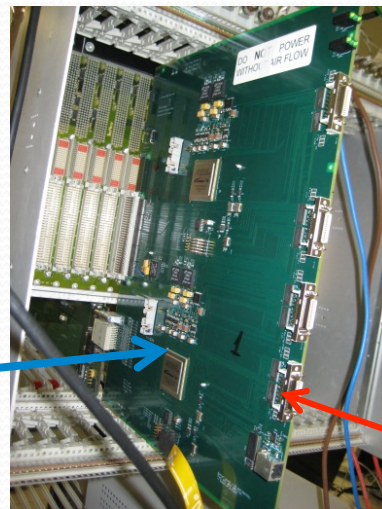
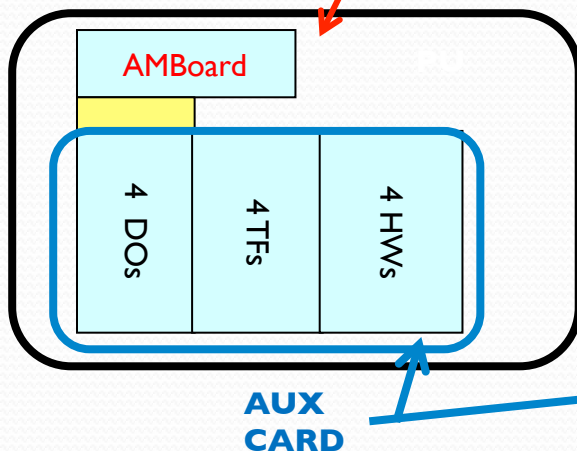
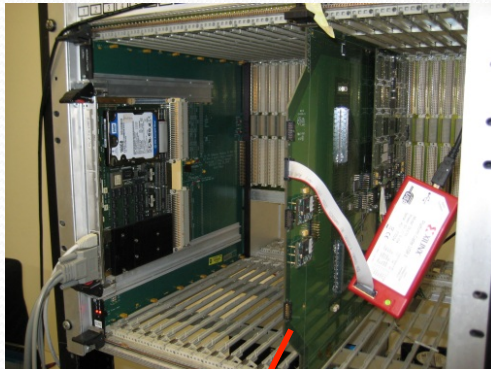
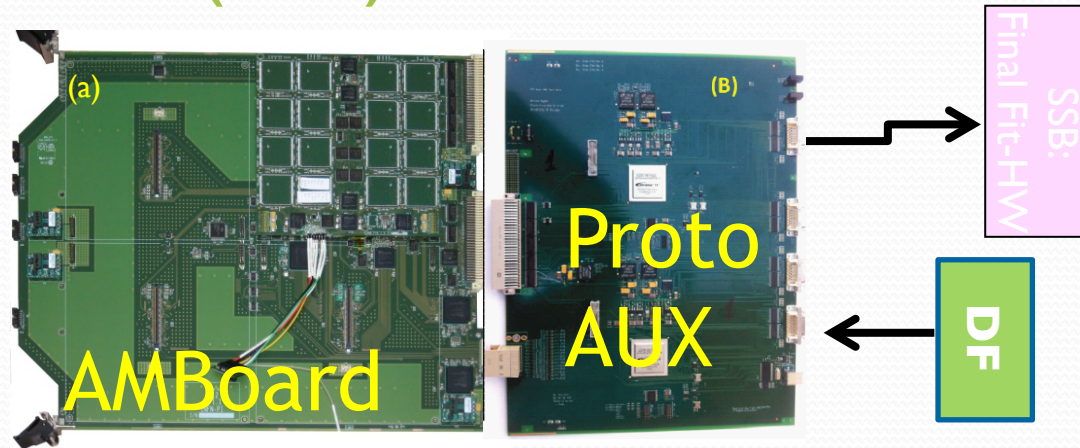
- 4 FTK_IM/DF receive ROD's data and do **cluster finding**.
- Prototypes **produced**, **tested**, and **used** @P1.
- Few **changes** needed for DF compatibility.
- Final Production after **tests** with IBL BOC (summer)

Data Formatter (DF - Fermilab)

- Distributes found clusters to 64 FTK η - ϕ towers. **ATCA** for complex fiber-to-tower mapping.
- Designed and **being manufactured**.
- First task: test high speed serial data transfer and ATCA control functionality. Firmware being written.



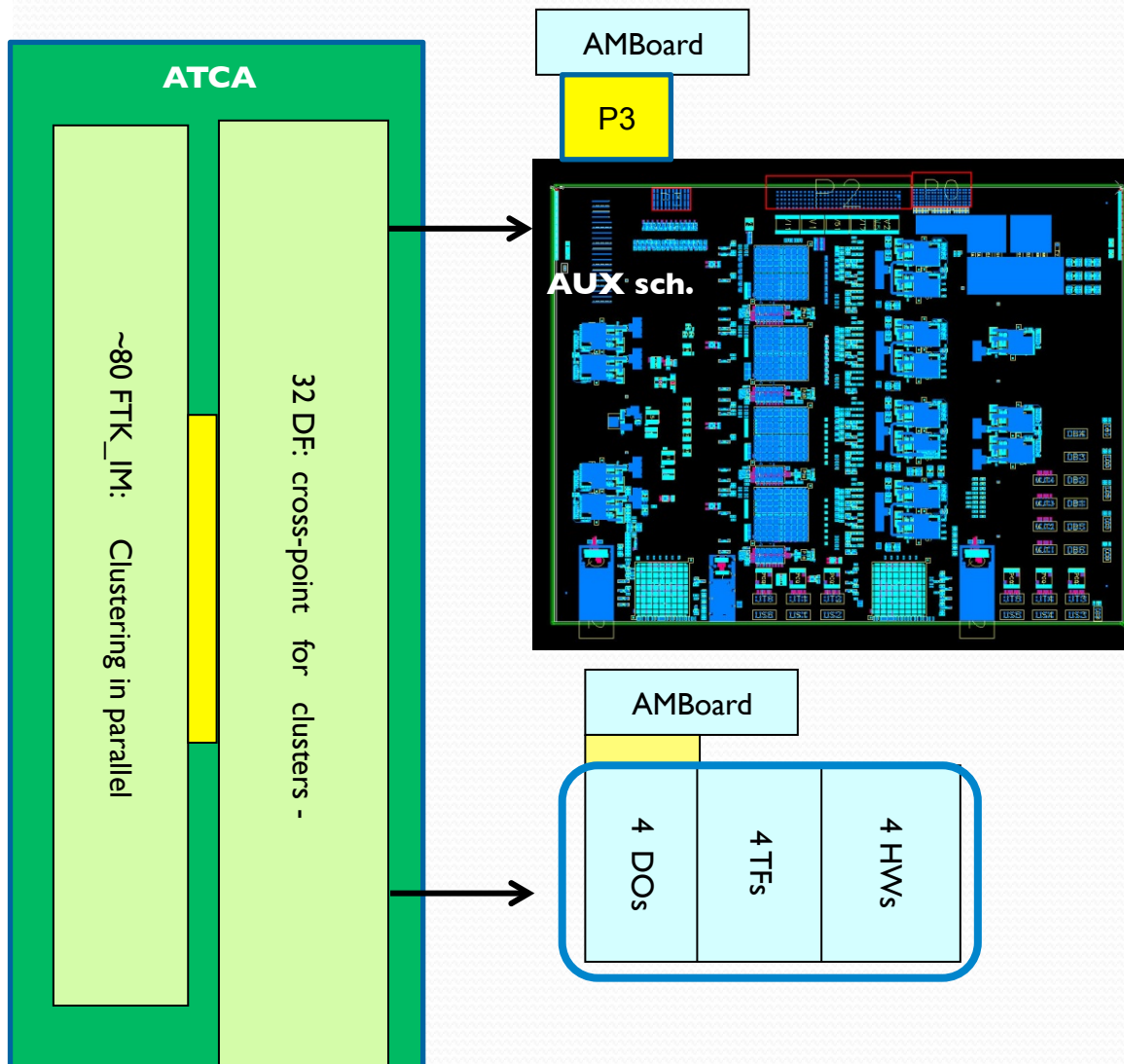
FTK Processor Unit (PU)



- 128 PUs do **pattern matching** and the **1st stage track fitting**.
- A PU consists of an **Associative Memory VME board** (a)(AMB-Europe) and a large **Auxiliary Card** (b) (AUX-UoC) behind it.

tested

The final AUX (UoC)



- Receives **DF data**, sends **coarse hits to AMB**, receives back **roads**, and does the **1st stage fitting** (8 layers).
- **Final board design** close to completion.
- **Firmware written**; testing/integration in progress.
- Engineering review in March.
- **Produce** prototype in April.

Summary

- FTK VS with early prototypes integrated integrated in ATLAS TDAQ
- Starting planning of activity for LS1
 - Integration of final FTK prototypes
 - Preparing for FTK demonstrator
 - Get the system ready for data taking
- Installation of FTK demonstrator in 2015