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LAMB: Hardware & Firmware

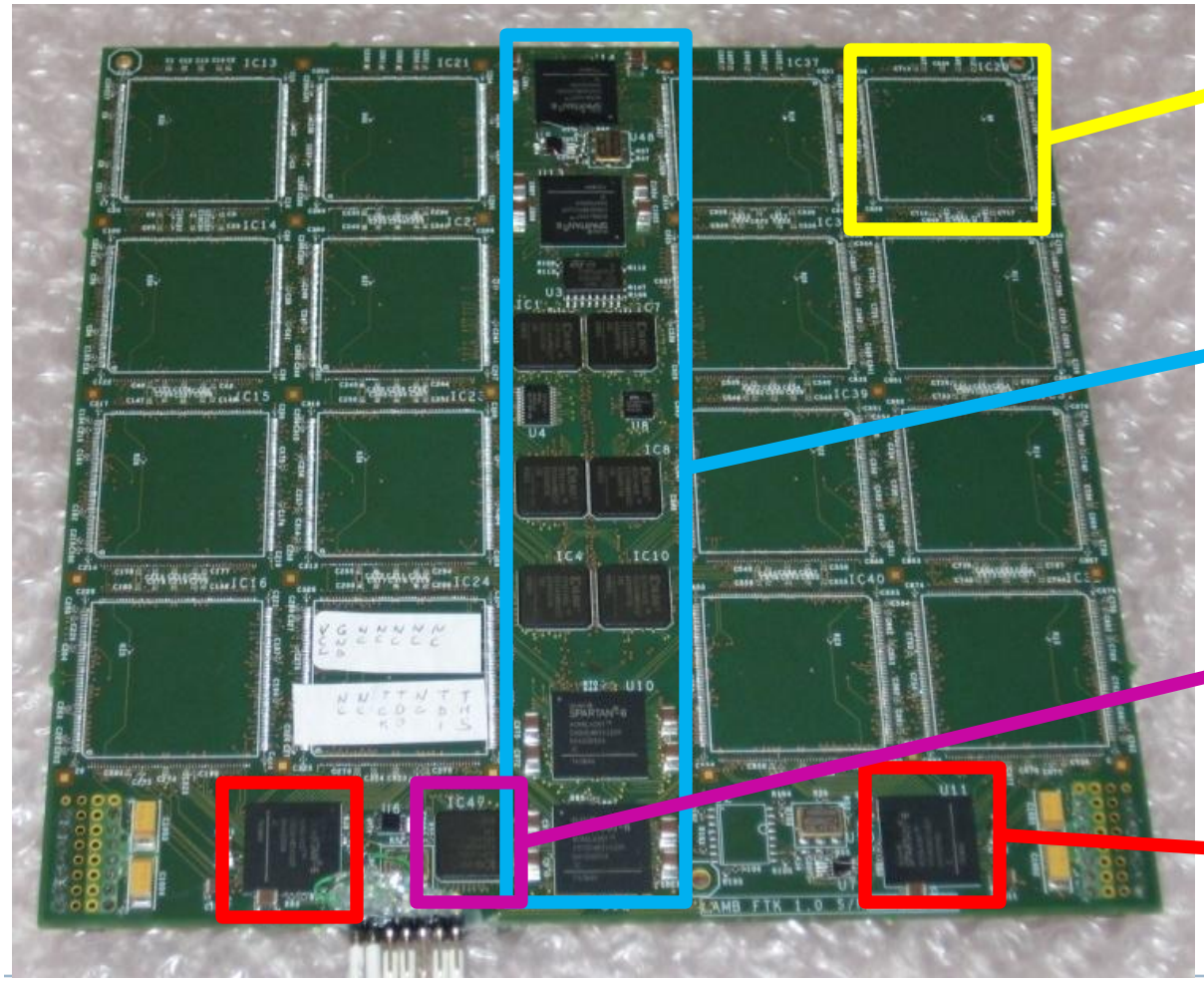
FTK Workshop – Pisa 13/03/2013

Outline

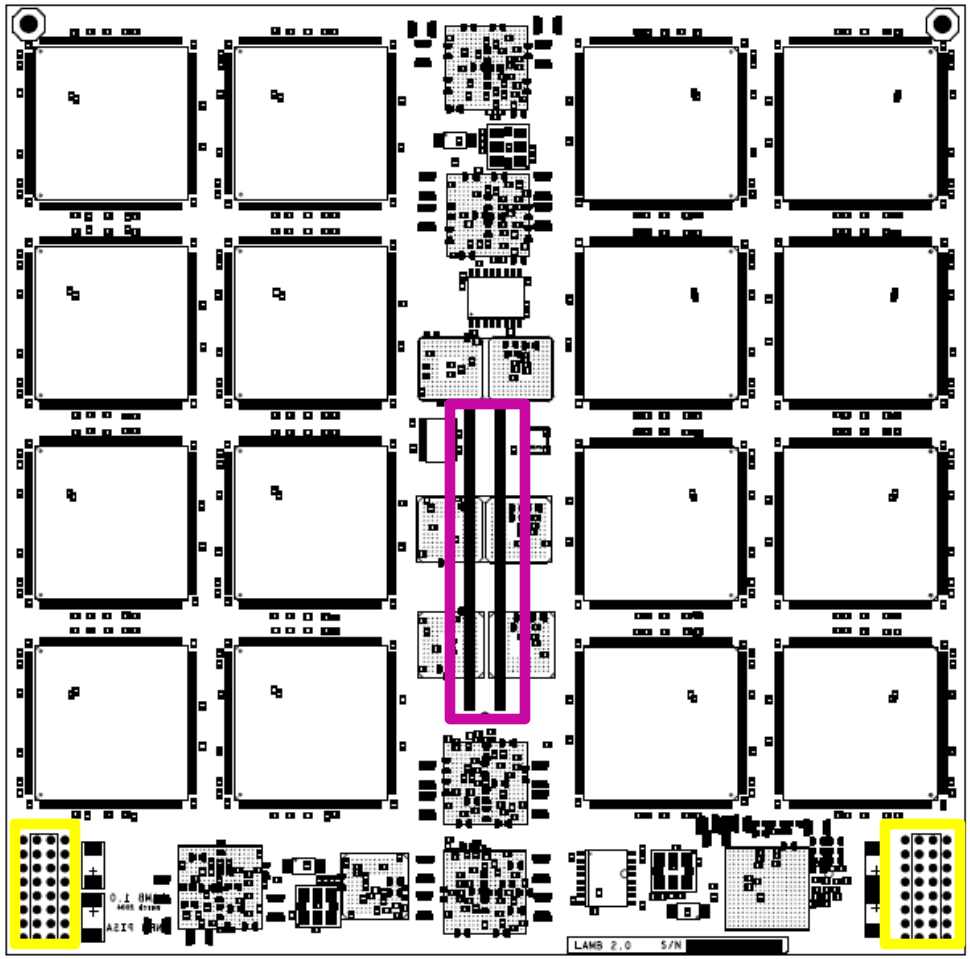
- Local Associative Memory Bank (LAMBFTK)
- Hardware description of LAMBFTK
- Firmware implementation of LAMBFTK
- Evolution of the board: serial link processor (LAMBSLP)

AM system: Local Associative Memory Bank (LAMB)

- Some definition of the board…



LAMBFTK – Interface and Power



Core voltage @ 1.2V

I/O voltage @ 3.3V

Input signal

4 bus parallel (0,1,3,5)

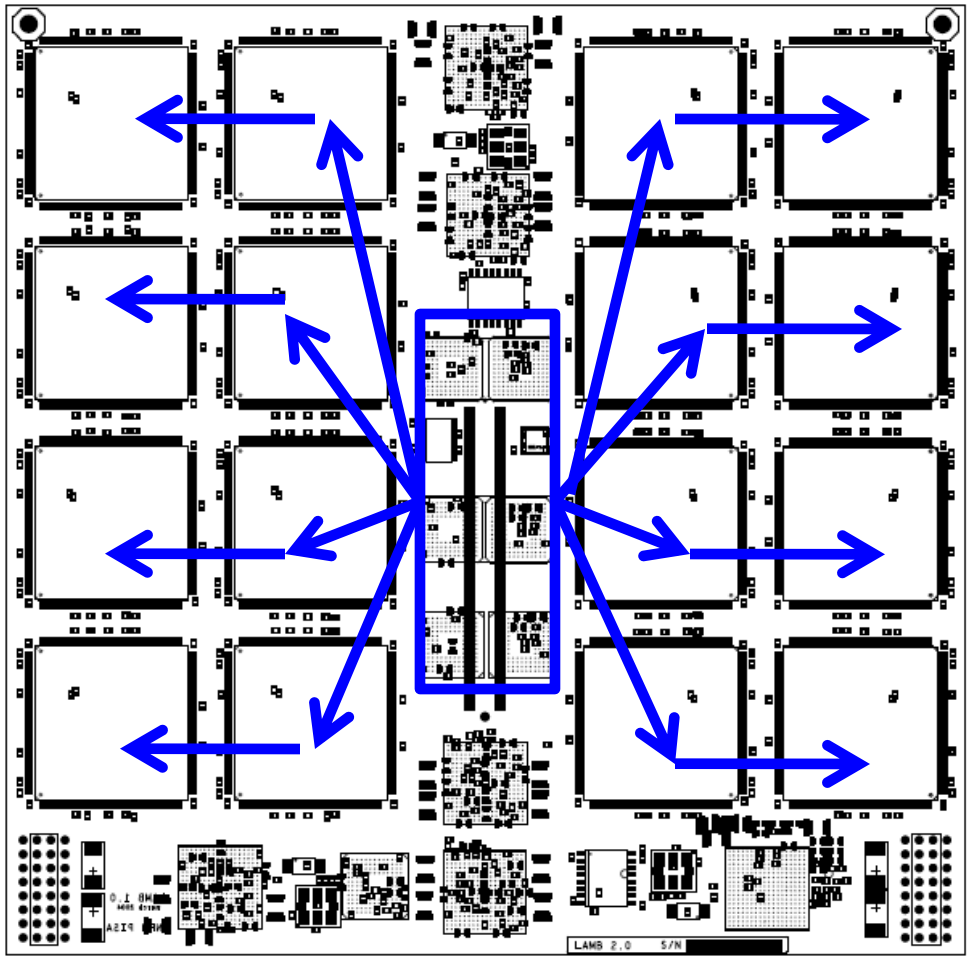
4 bus serial(2,4,6,7)

Output signal

2 from the right part

2 from the left

LAMBFTK – Parallel Busses Distribution

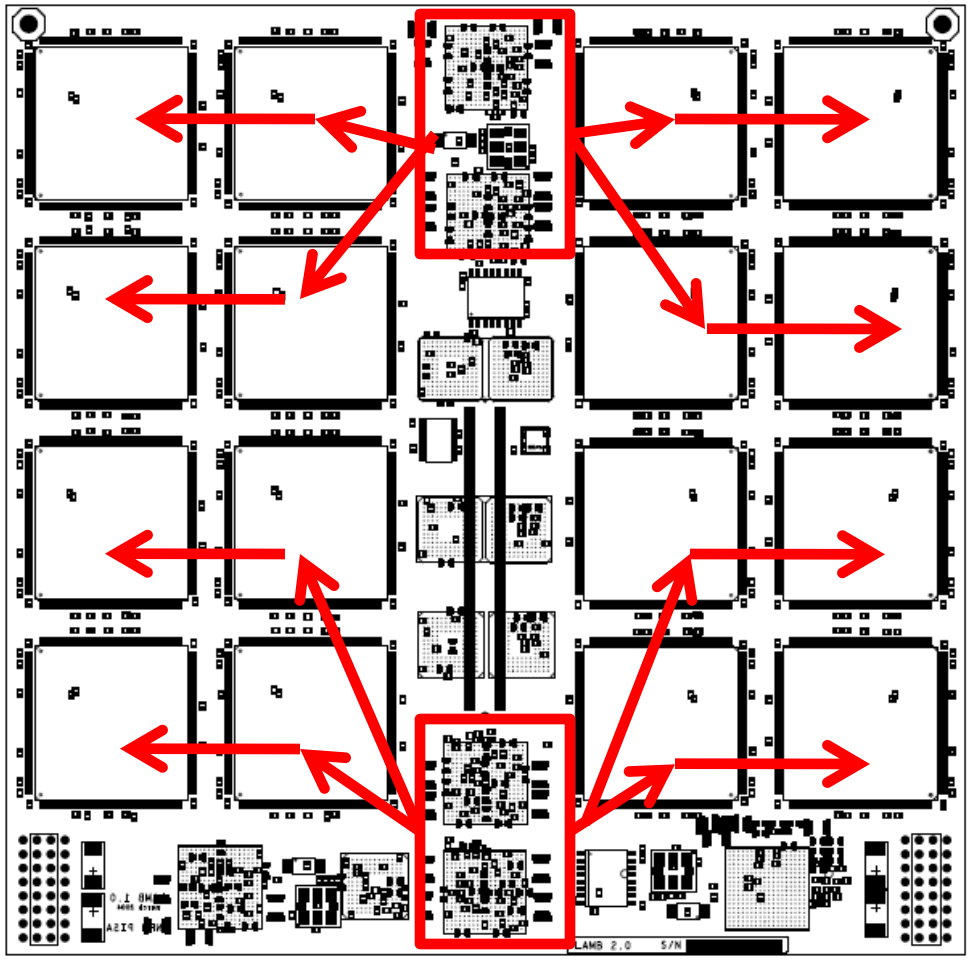


Core voltage @ 1.2V

I/O voltage @ 3.3V

CPLD – Input Distributor for parallel buses
4 bus parallel (0,1,3,5)
XC95144XL

LAMBFTK – Serial Busses Distribution



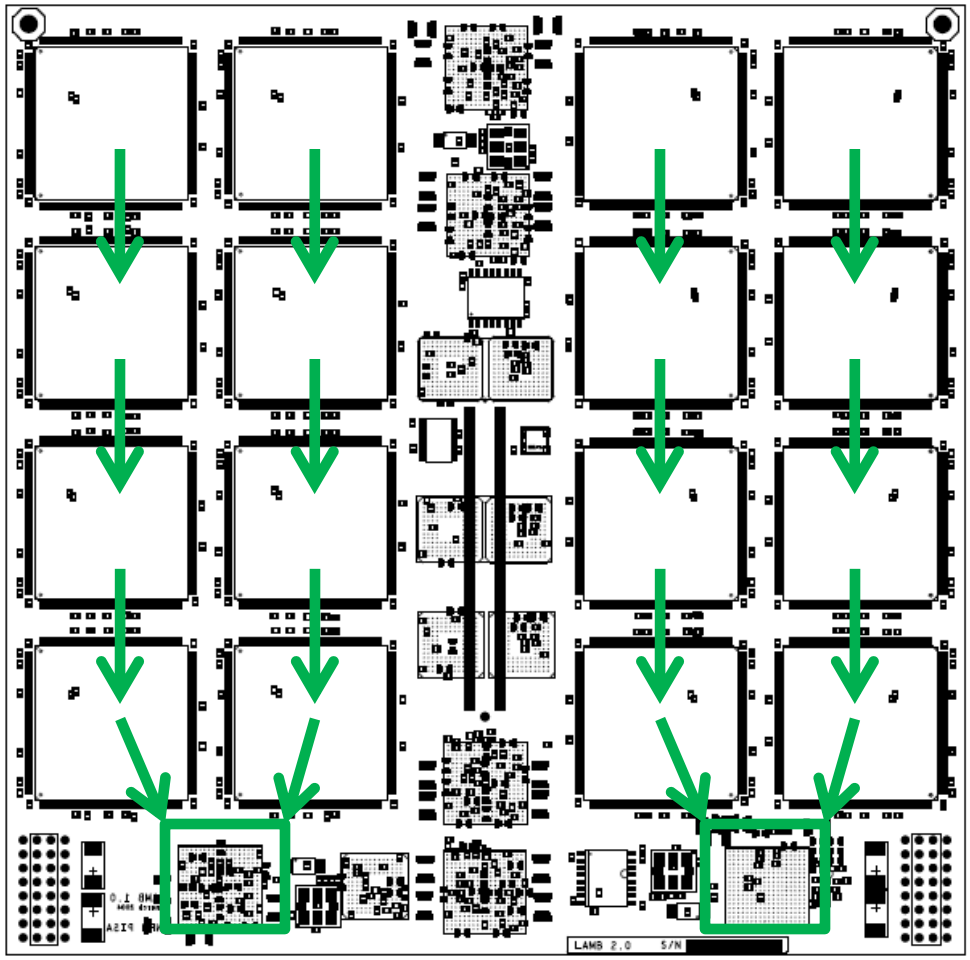
Core voltage @ 1.2V

I/O voltage @ 3.3V

CPLD – Input Distributor for parallel buses
4 bus parallel (0,1,3,5)

Spartan 6 – Distributor for serial buses
4 bus serial(2,4,6,7)
GTP transceiver

LAMBFTK – Road data flow



Core voltage @ 1.2V

I/O voltage @ 3.3V

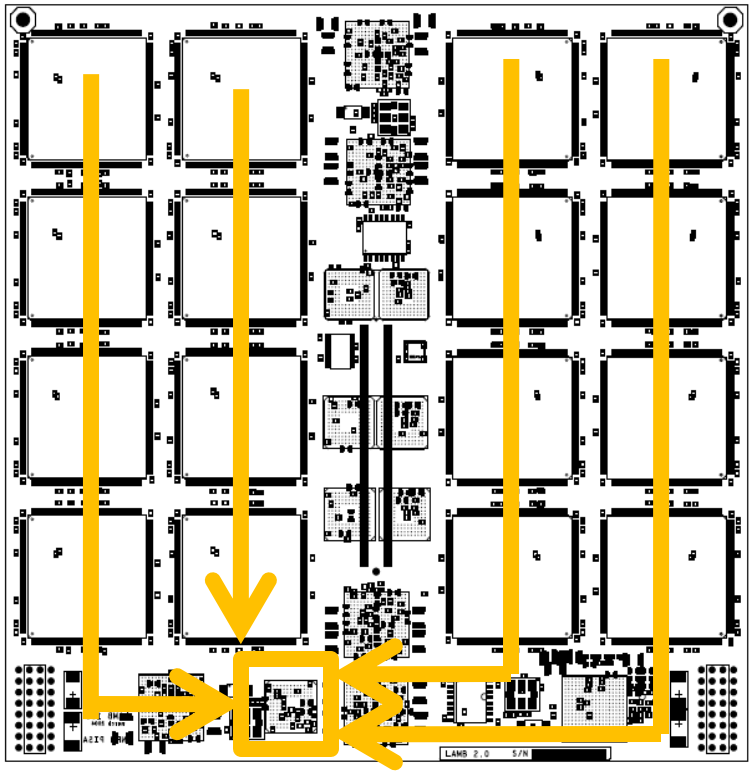
CPLD – Input Distributor for parallel buses
4 bus parallel (0,1,3,5)

Spartan 6 – Distributor for serial buses
4 bus serial(2,4,6,7)

Spartan 6 – GLUE for output road

LAMBFTK – JTAG AMchip connection

- The AMchips are connected in 8 JTAG chain controlled from the BSCAN chip.



4 JTAG chain of 4 chip on the top and on the bottom of the board

The BSCAN chip manages each JTAG chain distributing the TMS, TCK, TDI and TDO

The BSCAN manages the conversion from the VME protocol into JTAG protocol

LAMBFTK – Firmware development

- The logic of the board is very simple
  - controls the data distribution of the input buses to the AMchip
  - Manage the handshake with the AMchip and merge the 8 flows into 4 output streams
- A control of the Spartan-6 FPGA GTP Transceivers need to be implemented for the serial link connections

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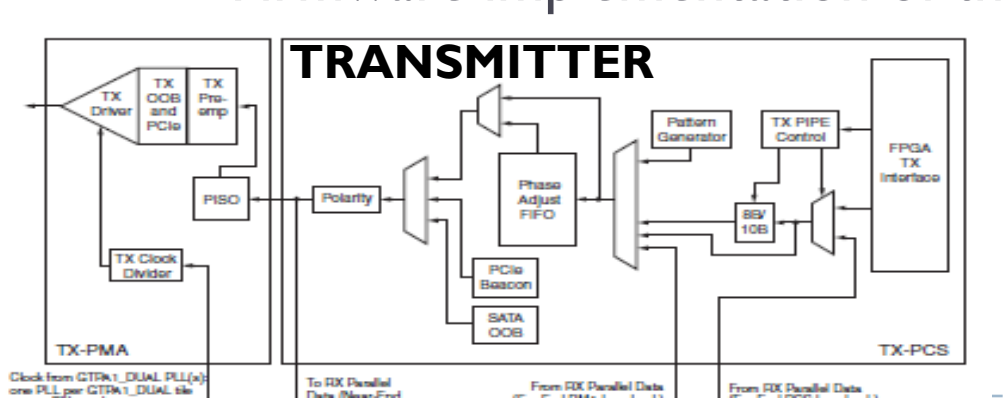
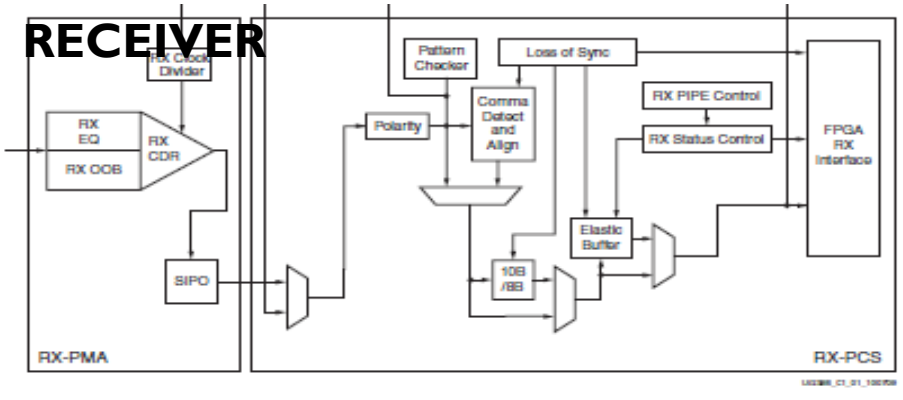
- A control of the Spartan-6 FPGA GTP Transceivers need to be implemented for the serial link connections
  - Definition of a protocol between transmitter and receiver
  - Firmware implementation of the TX and RX transceiver



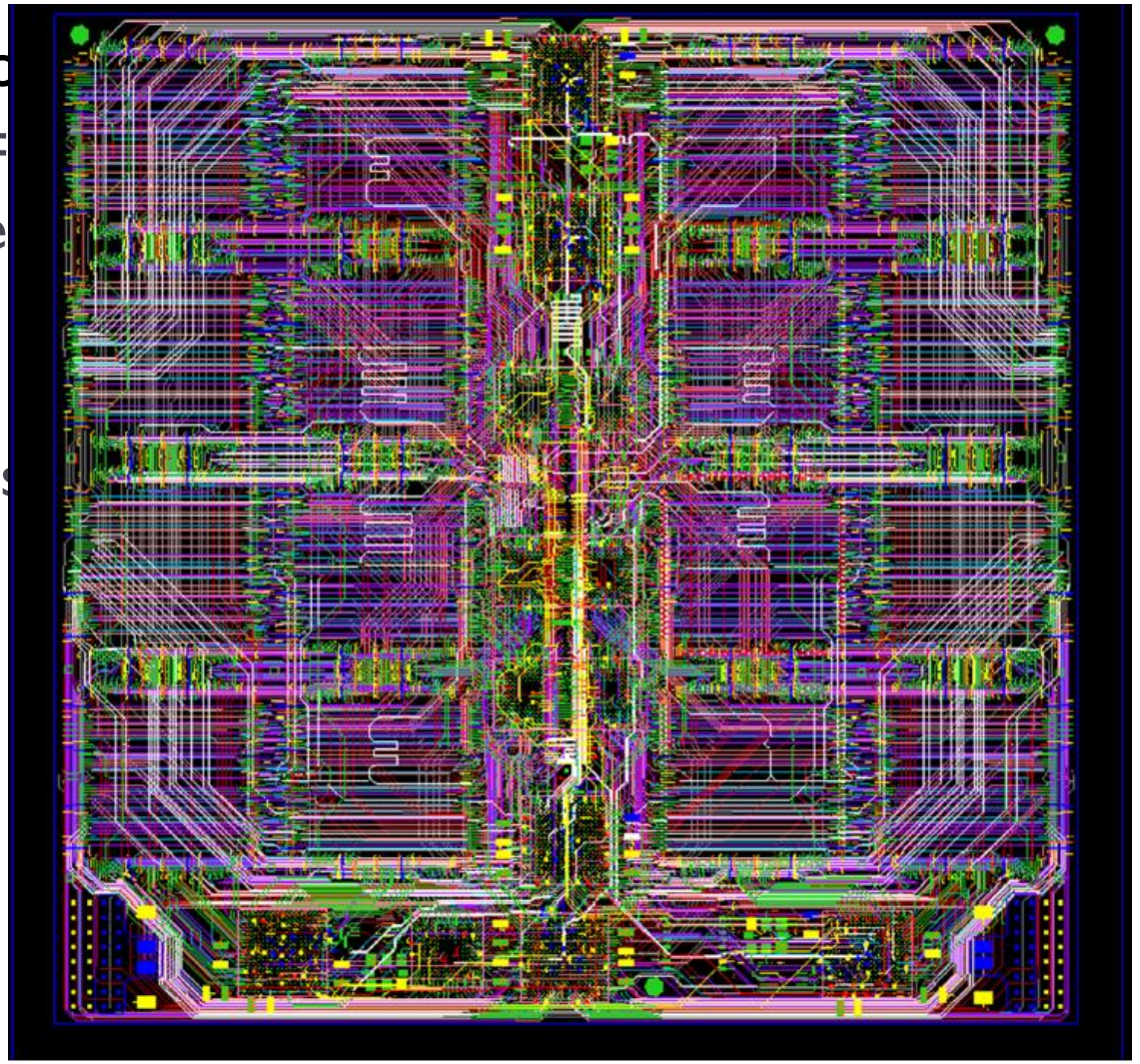


LAMBFTK: critical issue

- Complexity of the board:
  - High number of the FPGA and CPLD: for the mixed standard in I/O (parallel and serial)
  - Routing of the board of the all parallel data to the AMchips: each AMchip receives all the busses in parallel

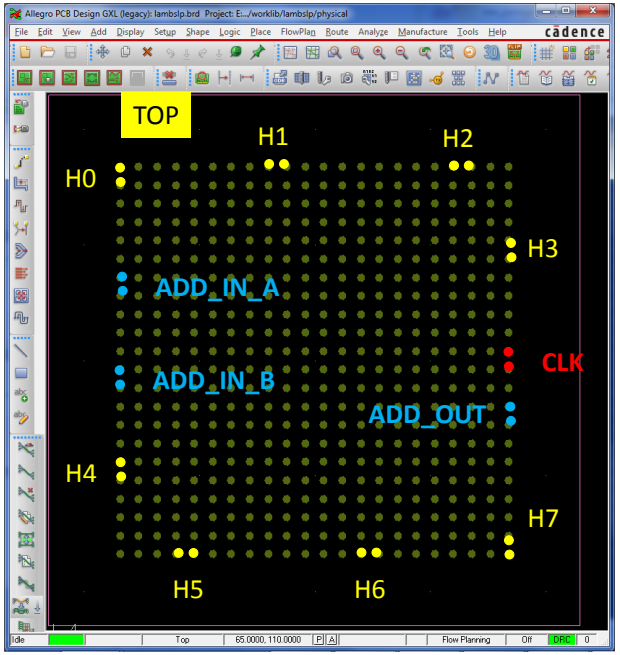
Problem…

- Complexity of the bo
  - High number of the F in I/O (parallel and se
  - Routing of the board each AMchip receives
  - **8 routing plane**
  - **8 power plane**

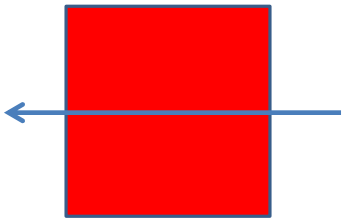


LAMBSLP: Serial link LAMB

- The new version of the board is totally based on the serial link connection
- The new AMchip will have 8 input serial link for the hit and 1 output serial link for the road



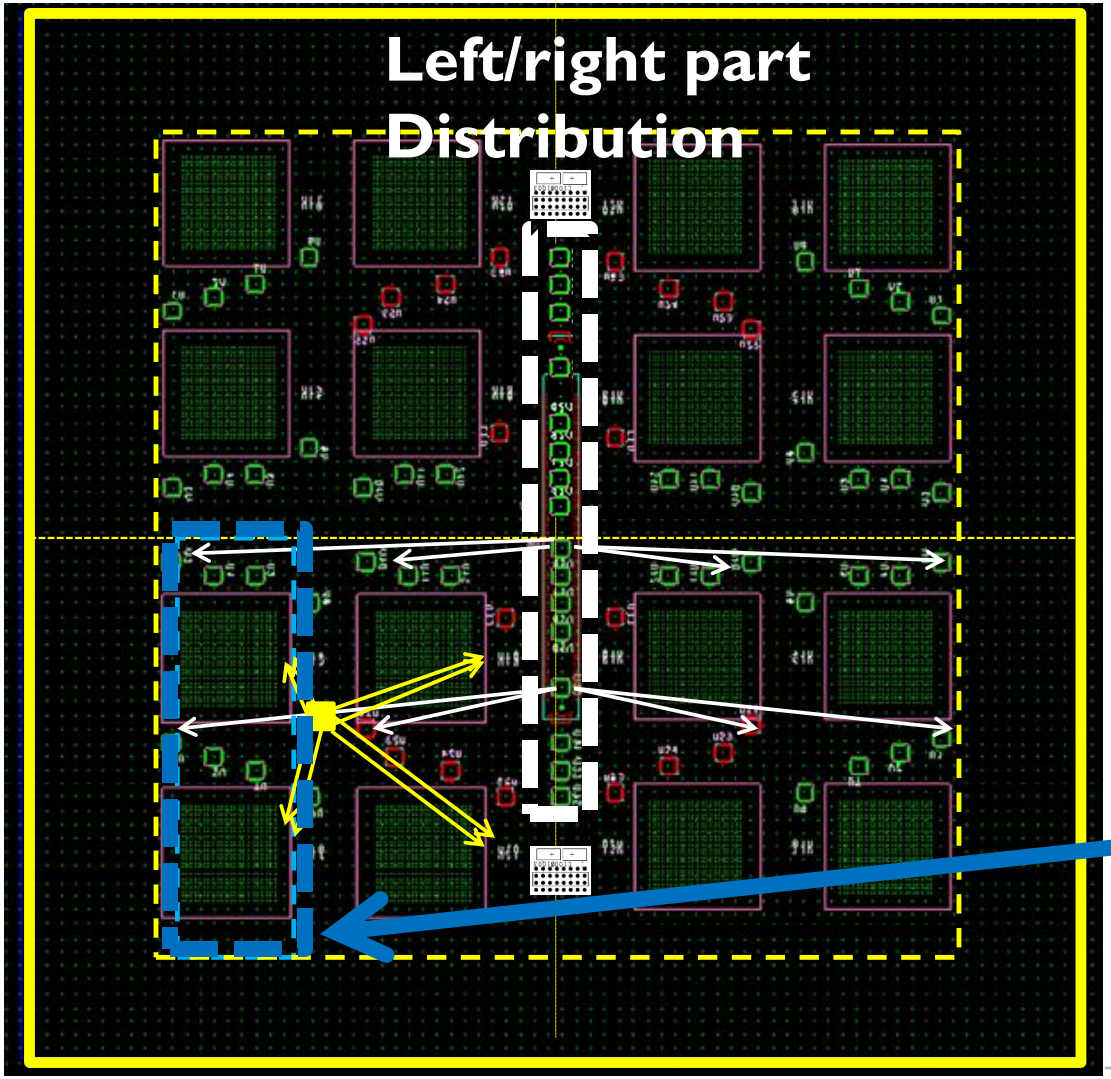
Bottom mirrored around Horizontal line



The LAMBSLP will hosts again **32 AMchip** maintaining the same structure of the old board

A list of issue in the design of LAMBSLP

LAMBSLP: Serial link LAMB



Component placement

- AMchip
- Fan-out buffer

Place 32 AMchip

- 16 on the top
- 16 on the bottom.

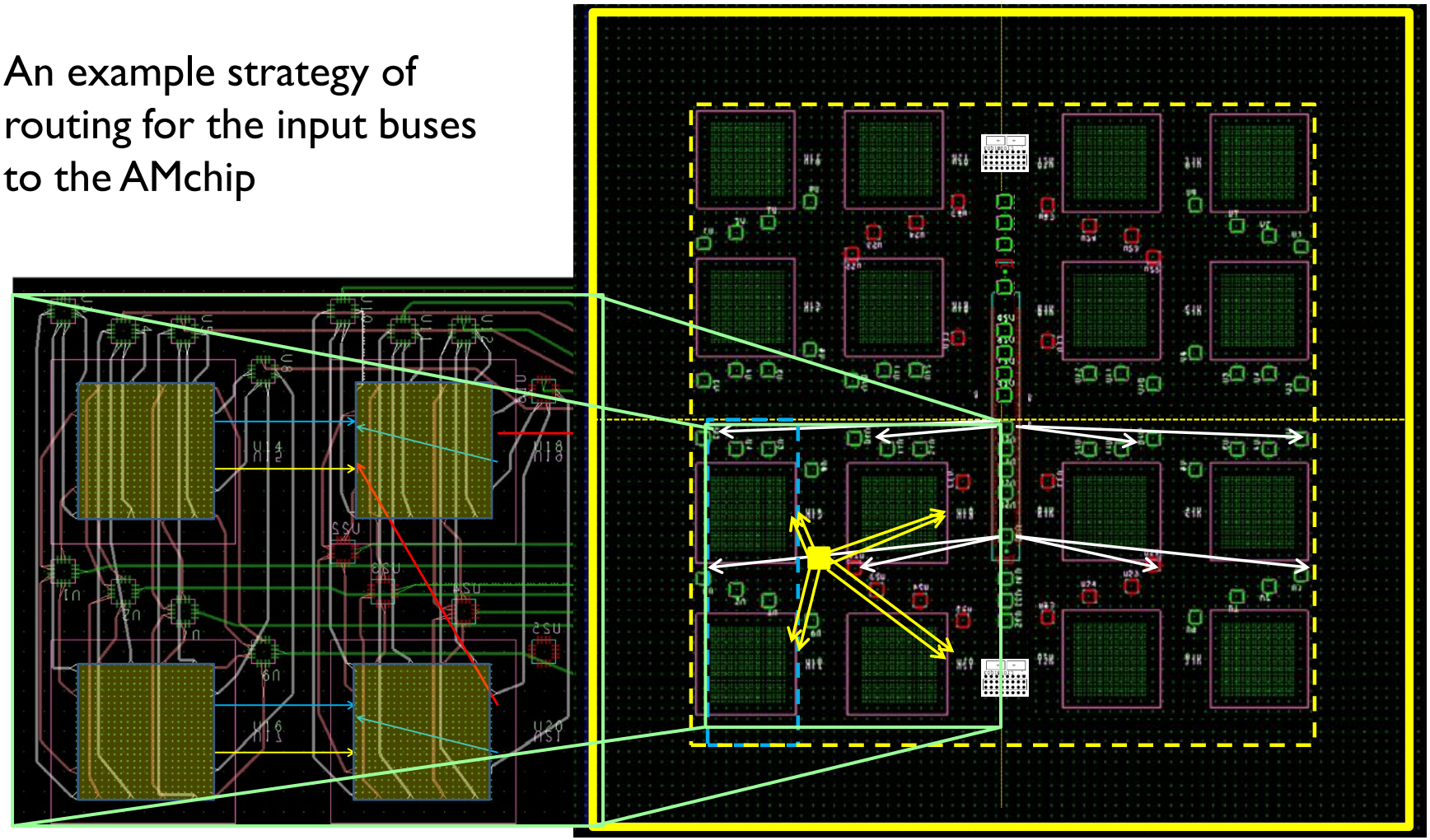
Input data distribution

Chain of two fan-out buffers (1:4 CML (SY58020U Micrel))

1. distribute the input bus to the left/right part of the LAMB (blank arrow)
2. replicate one bus to four AMchip (blue box)

LAMBSLP: Serial link LAMB

An example strategy of routing for the input buses to the AMchip



LAMBSLP: Serial link LAMB

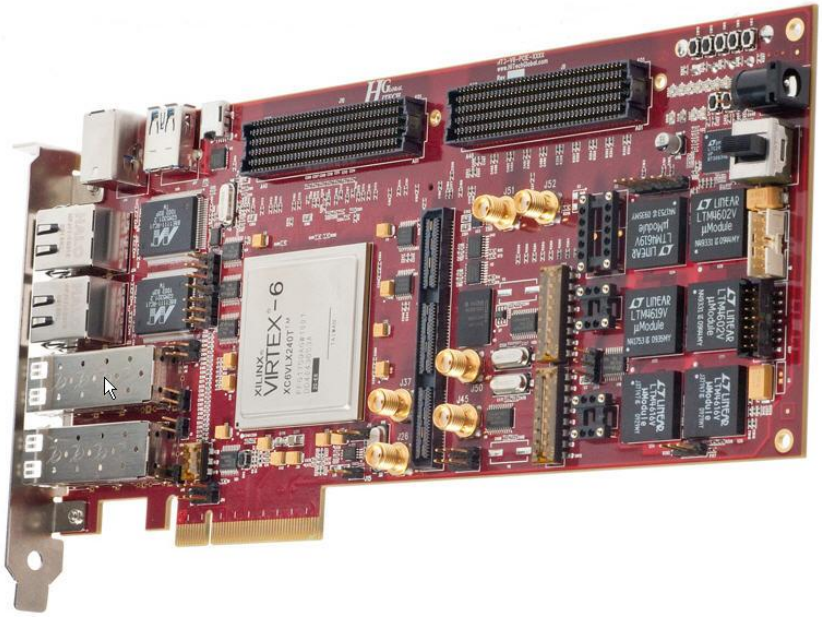
- Power distribution network
  - AMchip will need a core voltage of 1.2V for the Silicon Creation IP Serializer/Deserializer
  - 1 V for the core of the AMchip
  - Voltage 2.5V for the I/O for both FPGAs and AMChips
  - **~2 W per chip**

- The LAMBSLP needs to be squeezed with respect the size of the LAMBFTK
  - DC-DC converters and eventual filters.

LAMBSLP: Serial link LAMB

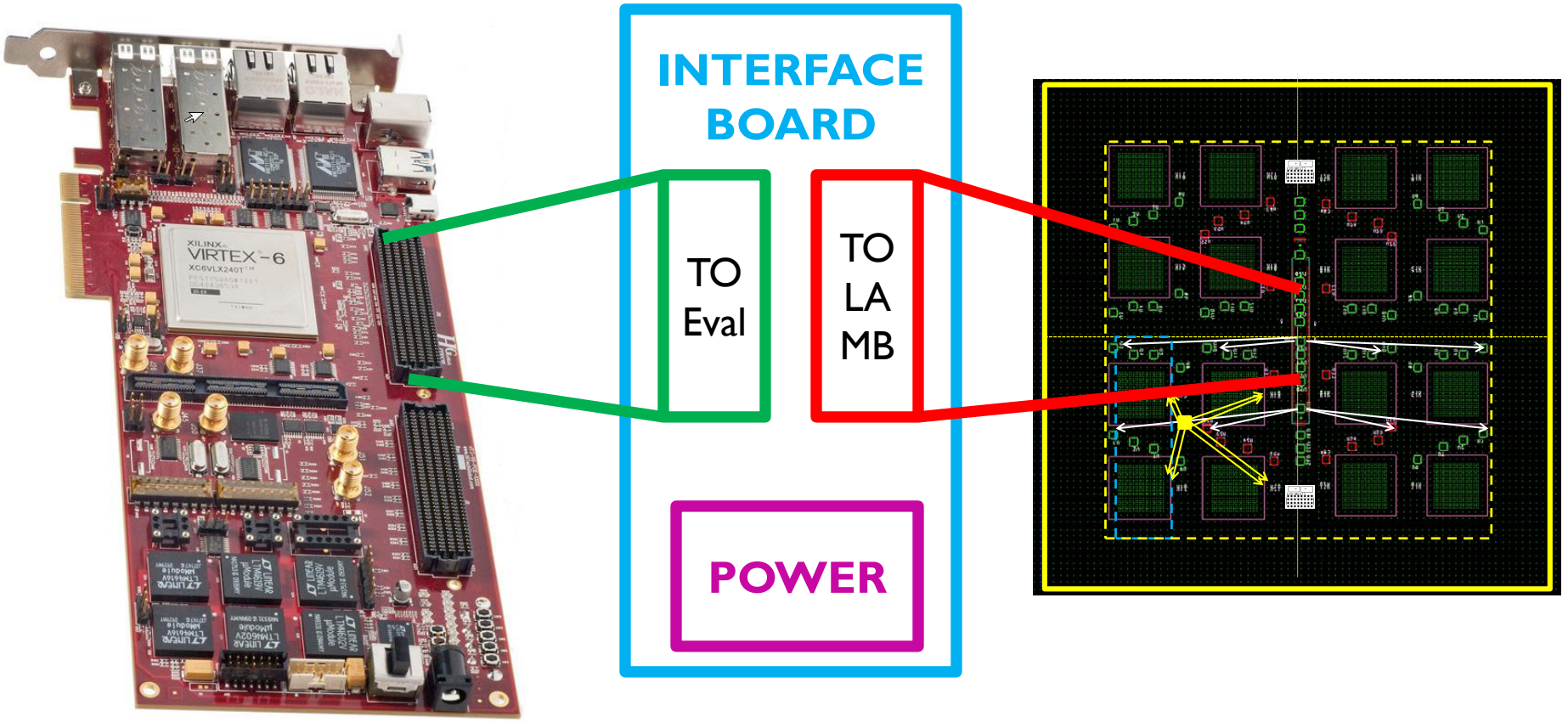
- The interface connector for the I/O signals is
  - High speed/high density open pin field
  - Power distribution

- This connector is select to interface the board with the Xilinx evaluation board
  - Few number of the pin to give all different voltage power to the board

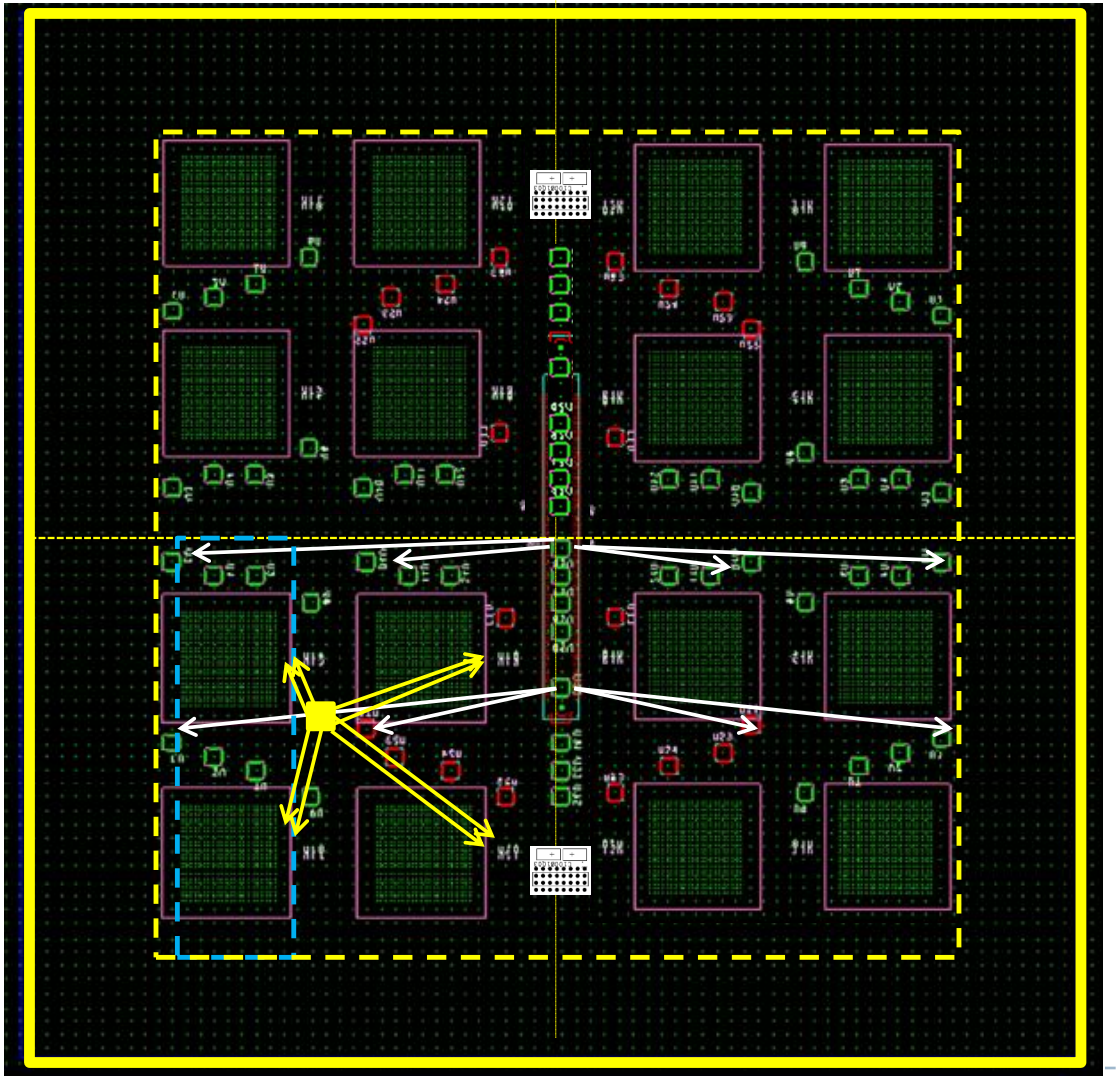


LAMBSLP: Serial link LAMB

- An interface board need to be development to interface the evaluation board and the ALMBSLP board



LAMBSLP: Serial link LAMB



Clock distribution

- Each AMchip receives a single LVDS input clock, a low jitter signal.

- The local signal clock is generated by a quartz placed in the middle of the four chips

- The yellow box shows the quartz and a fan-out buffer to provide the clock to all the 8 chips in the LAMB fourth