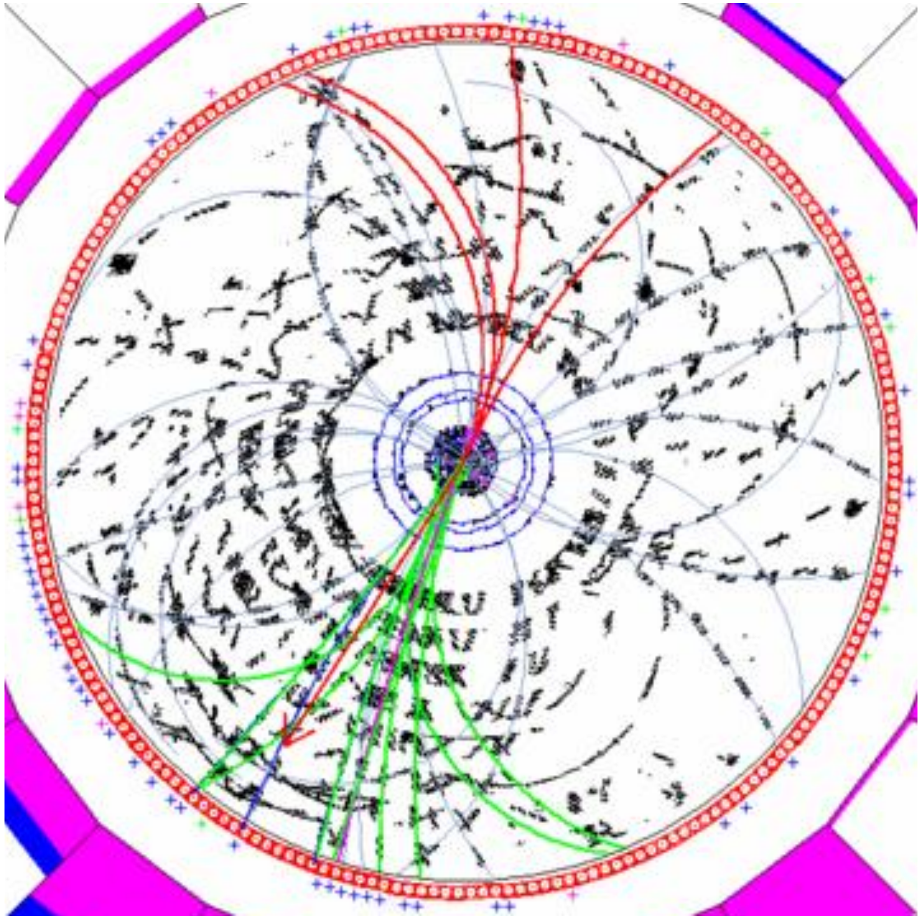
Variable Resolution and ternary cells

Alberto Annovi

Istituto Nazionale di Fisica Nucleare
Laboratori Nazionali di Frascati

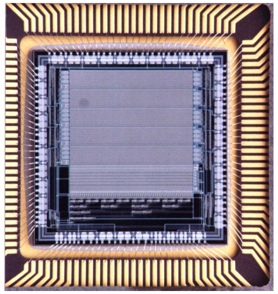
Associative Memories

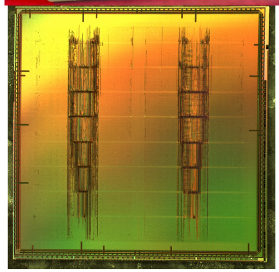
- First AM for HEP idea
  - M. Dell'Orso, L. Ristori
    VLSI Structures for Track Finding
    NIM A **278, 436 (1989)**
- First application: SVT @ CDF
  - Profit of drift chamber track seed
  - System started with 12*32k patterns

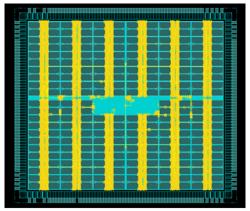


We discuss the architecture of a device based on the concept of *associative memory* designed to solve the track finding problem, typical of high energy physics experiments, in a time span of a few microseconds even for very high multiplicity events. This "machine" is implemented as a large array of custom VLSI chips. All the chips are equal and each of them stores a number of "patterns". All the patterns in all the chips are compared in parallel to the data coming from the detector while the detector is being read out.

AM technological evolution







- (90's) **Full custom VLSI chip -** 0.7μm (INFN-Pisa)
- **128 patterns, 6x12bit words each**

F. Morsani et al., "The AMchip: a Full-custom MOS VLSI Associative memory for Pattern Recognition", IEEE Trans. on Nucl. Sci., vol. 39, pp. 795-797, **(1992).**

On the opposite side: **FPGA** for the same AMchip

P. Giannetti et al. "A Programmable Associative Memory for Track Finding", Nucl. Intsr. and Meth., vol. A413/2-3, pp. 367-373, **(1998).**

G Magazzù, 1st standard cell project presented @ LHCC (1999)

Standard Cell 0.18 μm → 5000 pattern/Amchip

SVT upgrade total: 6M patterns

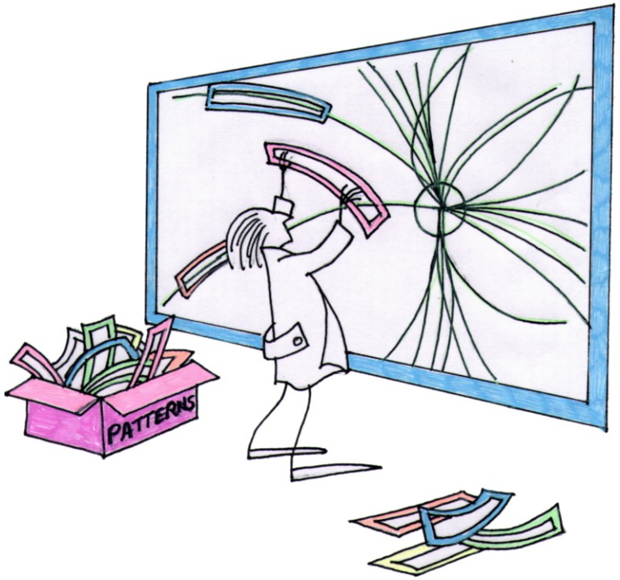
L. Sartori, A. Annovi et al., "A VLSI Processor for Fast Track Finding Based on Content Addressable Memories", **IEEE TNS**, Vol 53, Issue 4, Part 2, Aug. **2006**

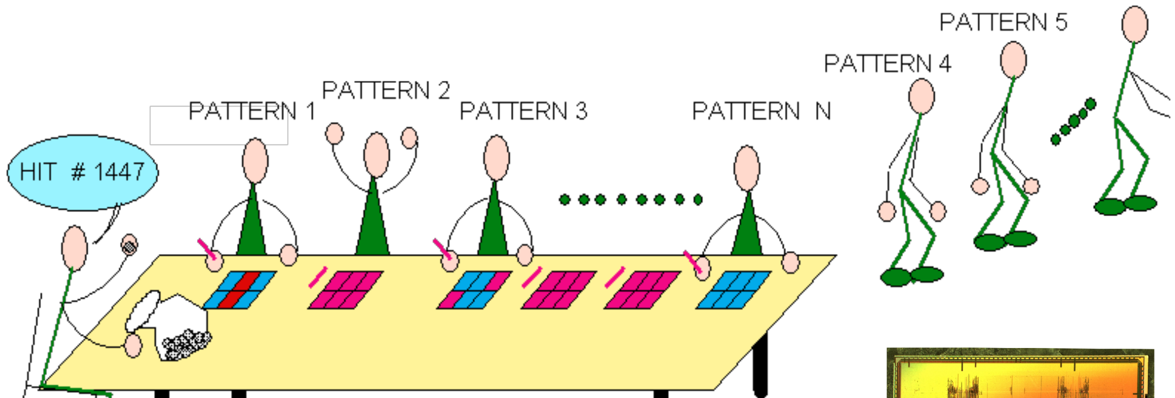
AMchip04 – 8k patterns in 14mm2, 65nm tech.
Power/pattern/MHz ~50 times less. Pattern density x12.
First variable resolution implementation.

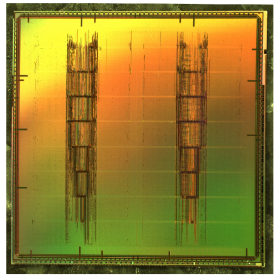
F. Alberti *et al 2013 JINST* ***8 C01040***, ***doi:***10.1088/1748-0221/8/01/C01040

FTK algorithm:
Pattern recognition & Track fitting

- Pattern recognition – find track candidates with enough Si hits

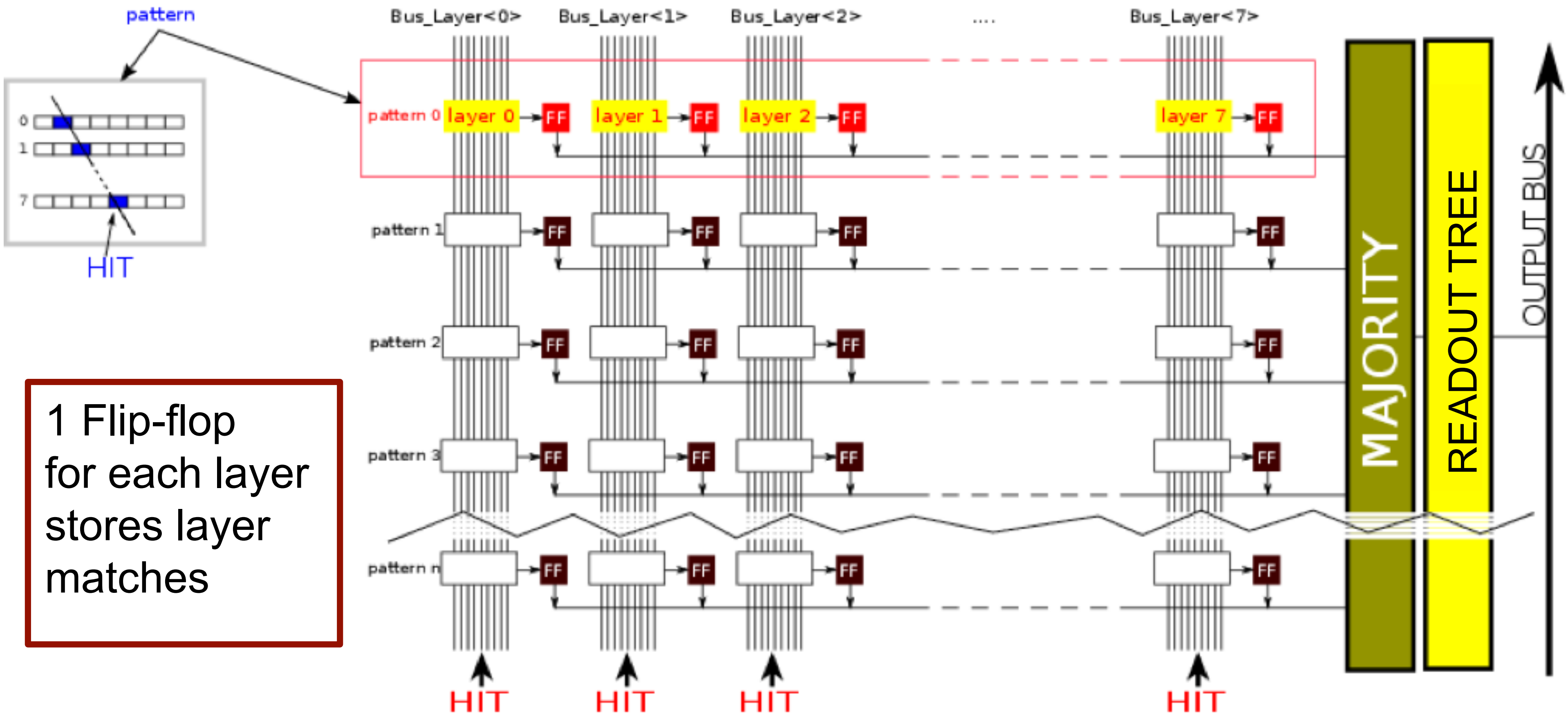






  - O(10^9) prestored patterns simultaneously see the silicon hits leaving the detector at full speed.
  - Based on the Associative Memory chip (content-addressable memory) initially developed for the CDF Silicon Vertex Trigger (SVT).

AM working principle



1 Flip-flop for each layer stores layer matches

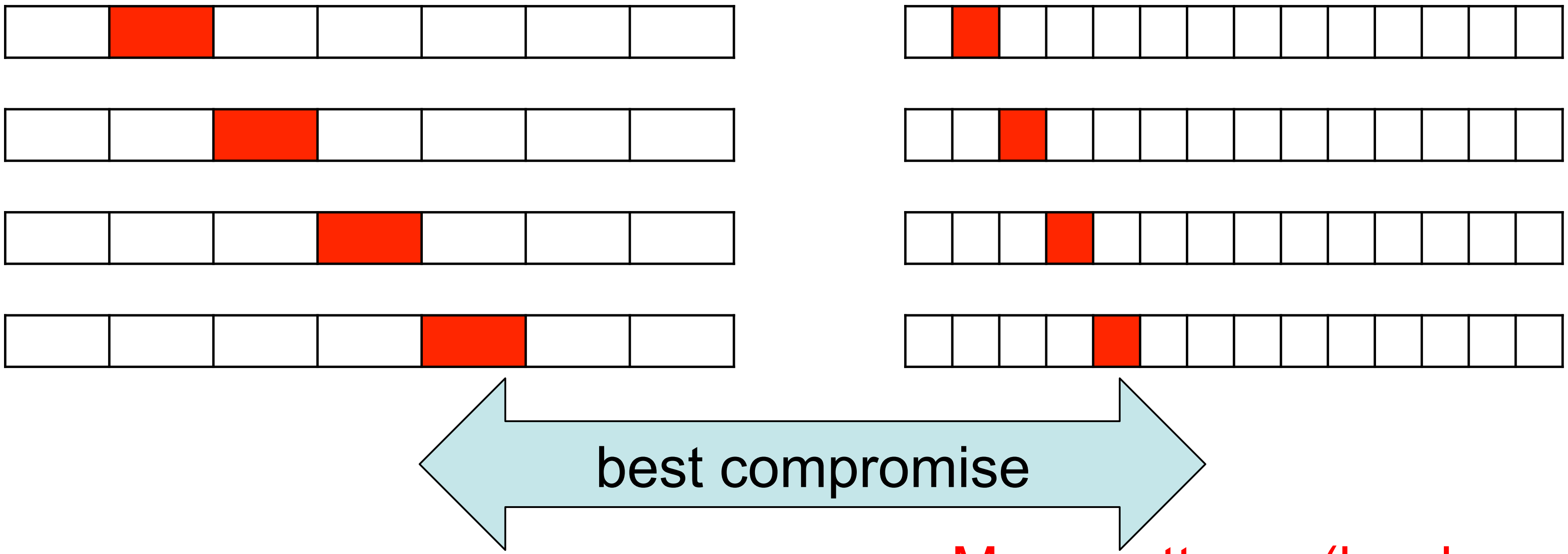
All patterns compared in parallel with incoming data. Look for correlation of data received at different times. (Feature unique to AMchip)

Fast pattern matching. Flexible input: position, time, objects…

Generatig the pattern bank

Wide patterns

Thin patterns



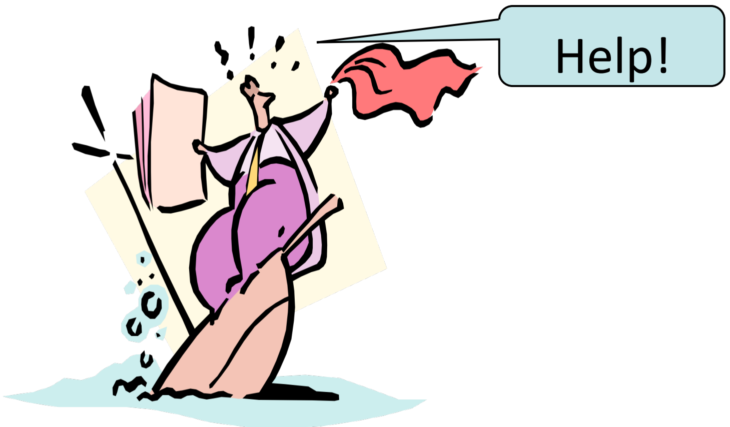
High efficiency
with less patterns (hardware)
BUT more fakes

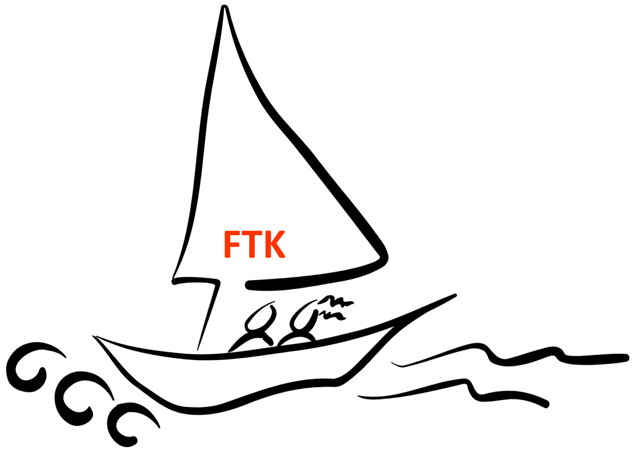
More patterns (hardware)
for same efficiency
less fakes
In FTK fakes are workload
for track fitter.

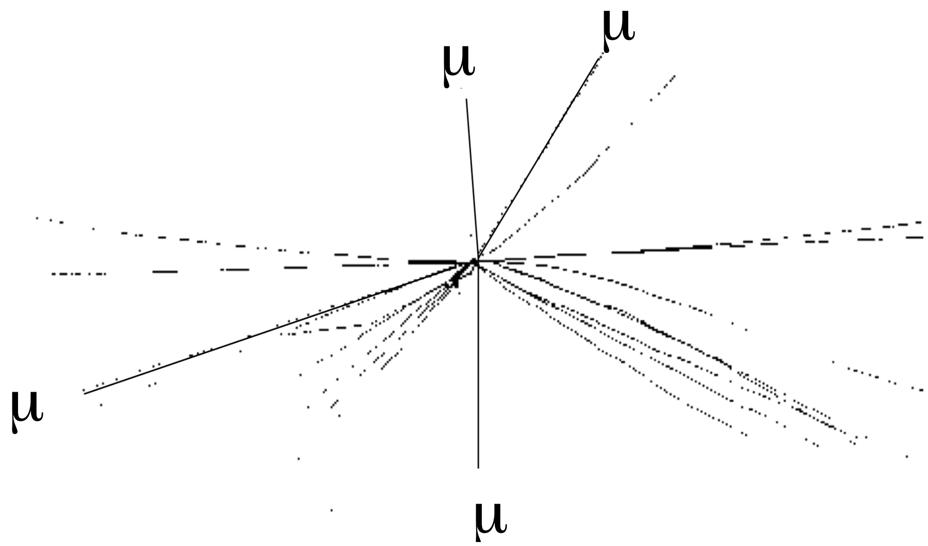
AM at LHC

30 minimum bias events + H->ZZ->4μ

Where is the Higgs?



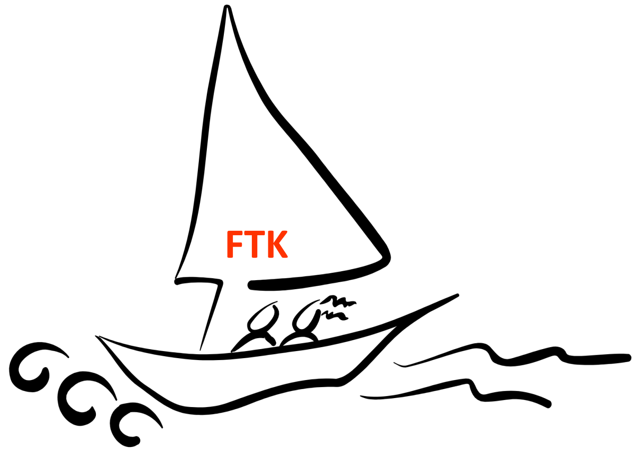


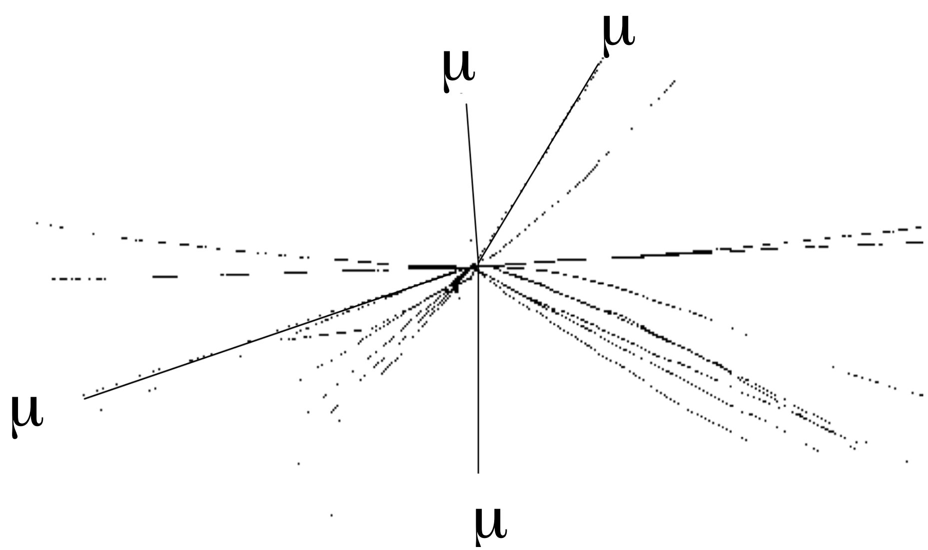


Tracks with P_t>2 GeV

AM at LHC

- Silicon only tracker
- High luminosity → high detector occupancy
- Thousands of tracks / bunch crossing
- For AM to reduce information
  - Need thin AM resolution
  - Need billions of patterns
  - Requires lot's of Amchip…





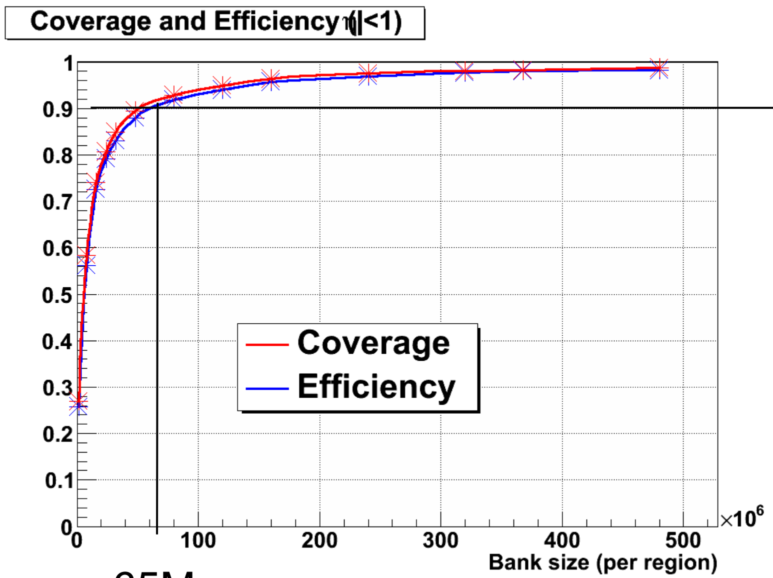
Tracks with P_t>2 GeV

Pattern efficiency

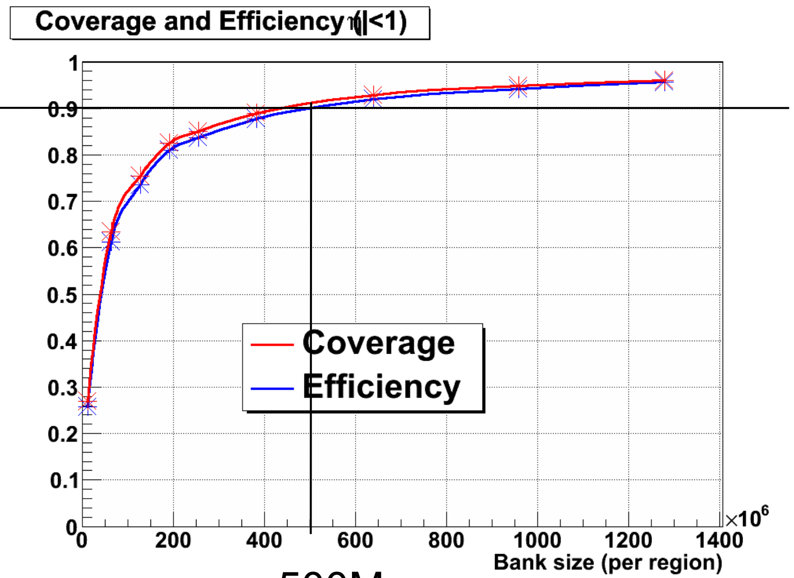
ATL-UPGRADE-PROC-2011-004

Pattern size
r-ϕ: 24 pixels, 20 SCT strips
z: 36 pixels

Pattern size (half size)
r-ϕ: 12 pixels, 10 SCT strips
z: 36 pixels



65M



500M

90%

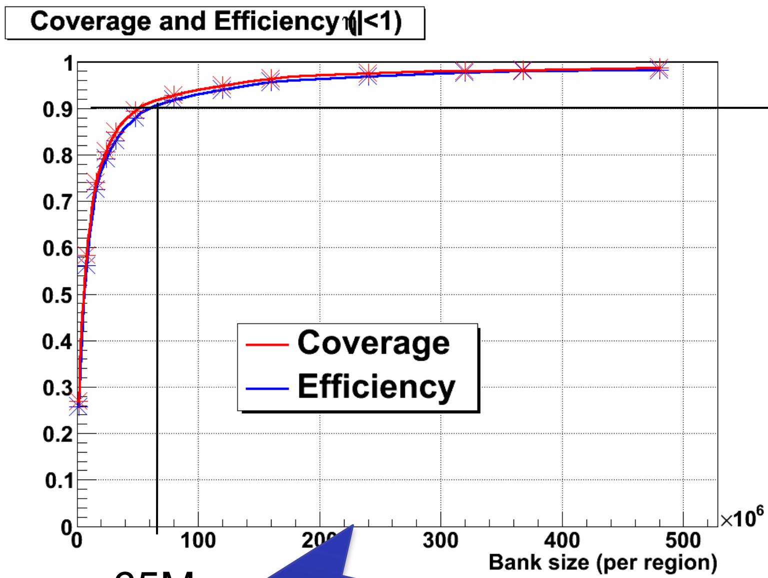
# of patterns in Amchips (barrel only, 45 ϕ degress)

<# matched patterns/event @ 3E34> = 342k

<# matched patterns/event @ 3E34> = 40k

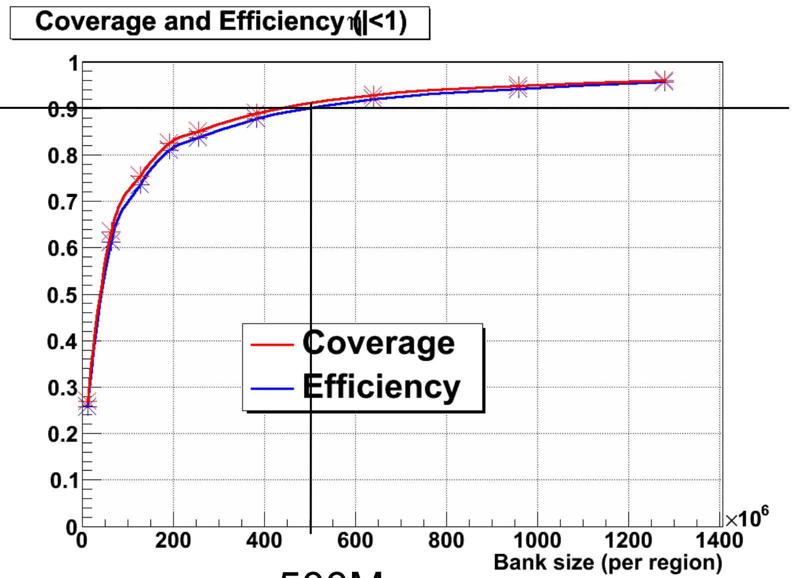
Pattern efficiency

Pattern size
r-ϕ: 24 pixels, 20 SCT strips
z: 36 pixels



65M

Pattern size (half size)
r-ϕ: 12 pixels, 10 SCT strips
z: 36 pixels



500M

90%

o… (barrel only, 45 ϕ degress)

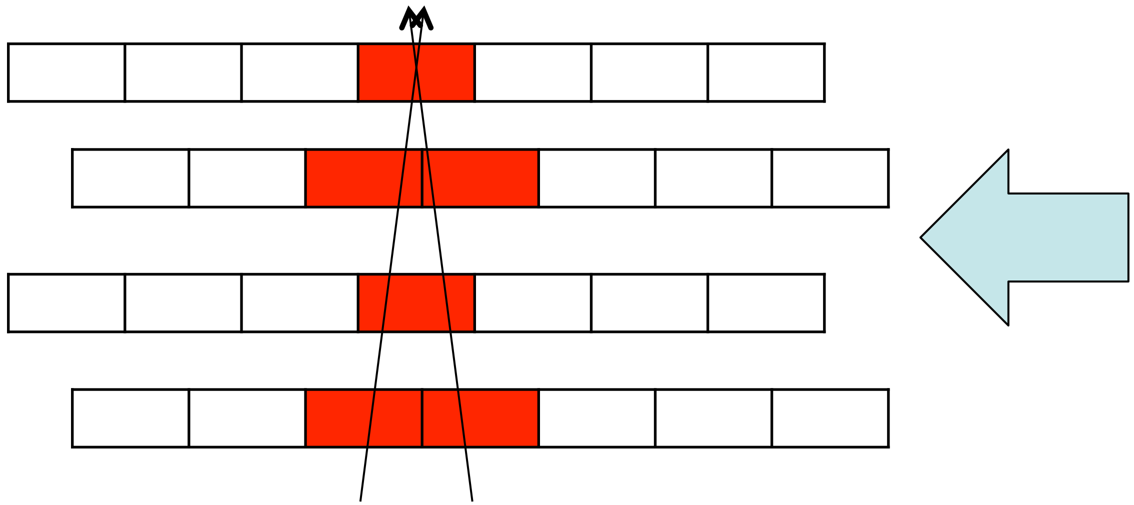
Want this

<# matched patterns/event @ 3E34> = 342k

…atched patterns/event @ 3E34> = 40k

discretiziation effects

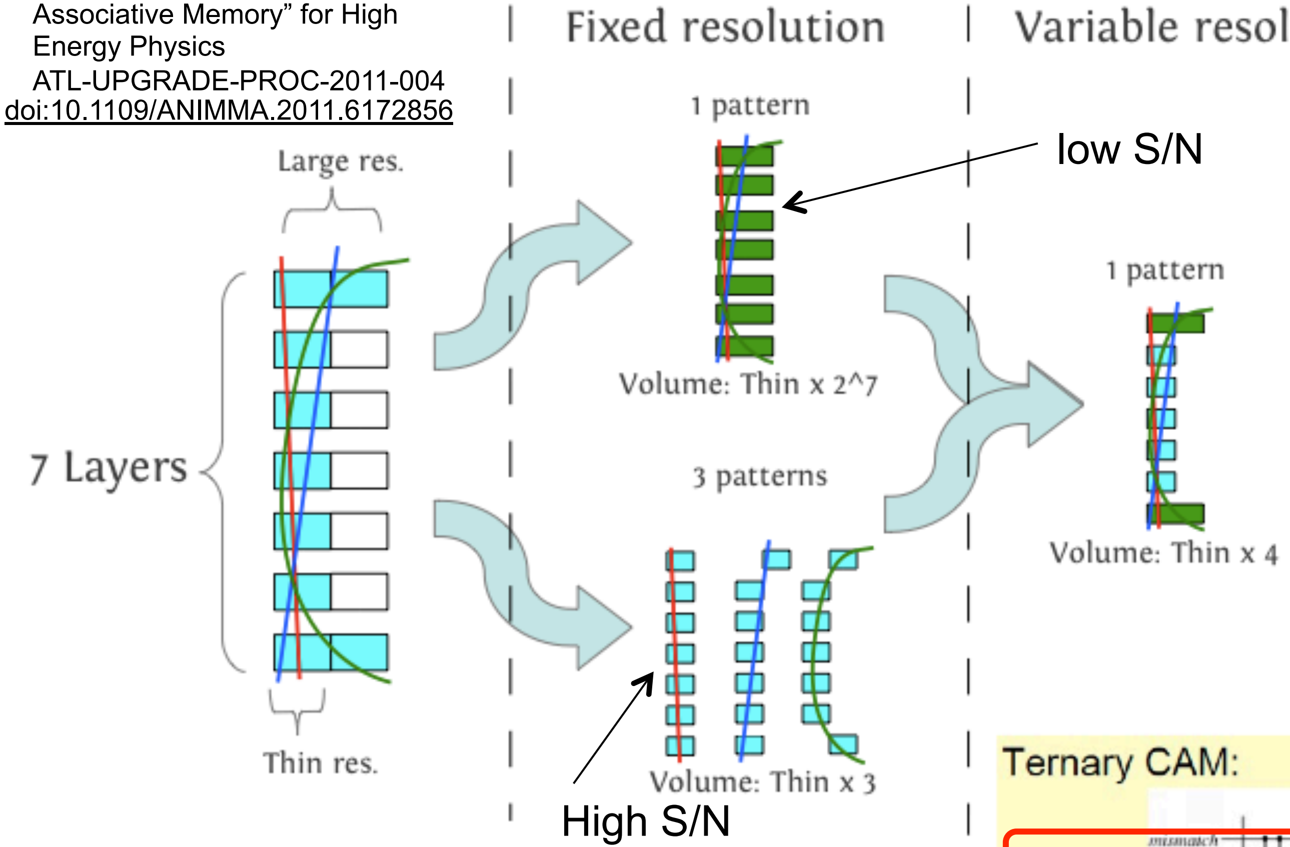
Layers are not aligned



Would use 4 patterns locations instead of 1 without variable resolution

AMCHIP04: VARIABLE RESOLUTION

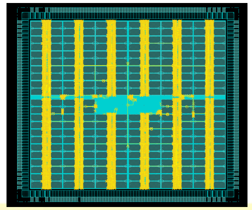
A new “Variable Resolution Associative Memory” for High Energy Physics
ATL-UPGRADE-PROC-2011-004
doi:10.1109/ANIMMA.2011.6172856

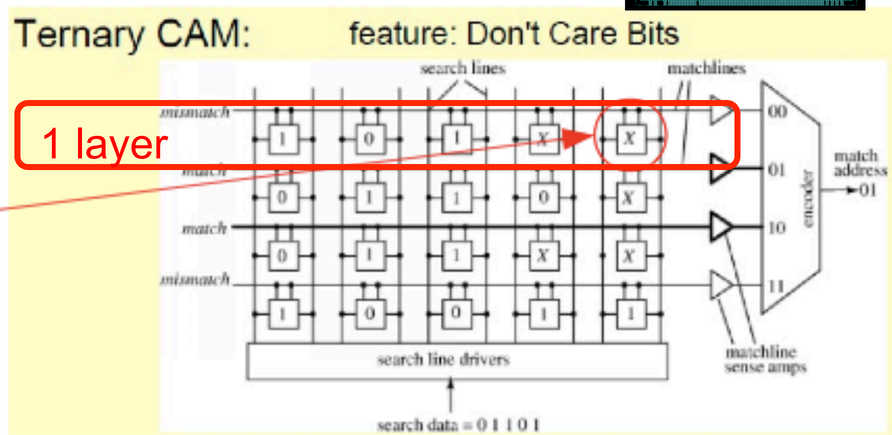


Good rejection and occupy only one pattern location.

Per-pattern choice of optimal resolution.

AMchip04





We can use **don’t care** on the least significant bit when we want to match the **pattern layer @ Large resolution** or use all the bits to match it **@ Thin resolution**

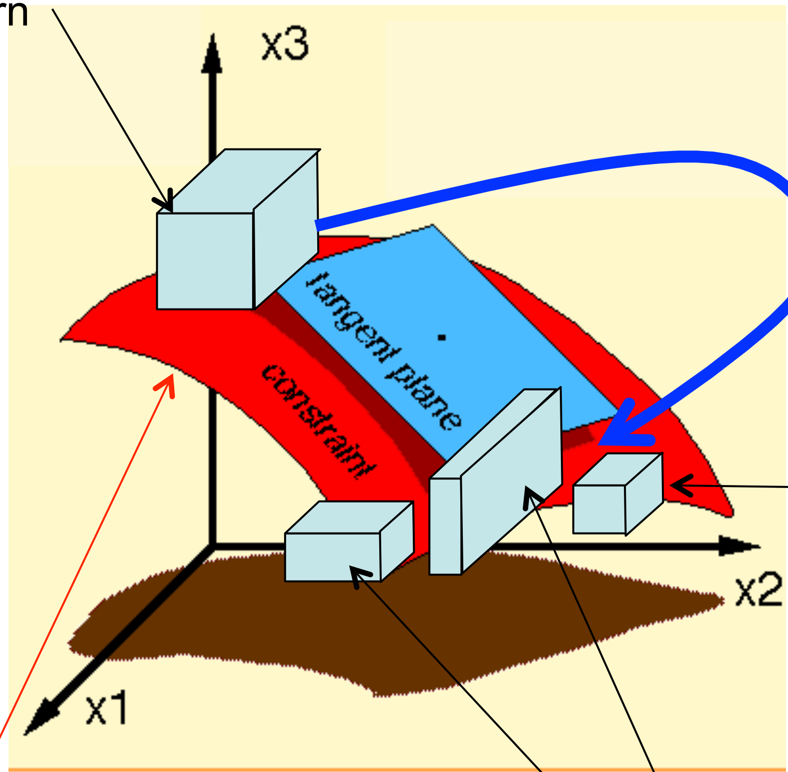
Coincidence window is programmable layer by layer and pattern by pattern

The patterns: a different point of view

5 strip + 3 pixel layers
→11 coordinates
→11D hit coord. space

The pattern bank:
- cover the track manifold with patterns.
- covered space outside manifold → fakes.
- variable resolution → dramatically improves S/N

Large pattern



A factor of 2 on each side
→a factor 2^11 less volume
→O(1/2048) less fakes!!
… forgetting correlated hits

Thin pattern

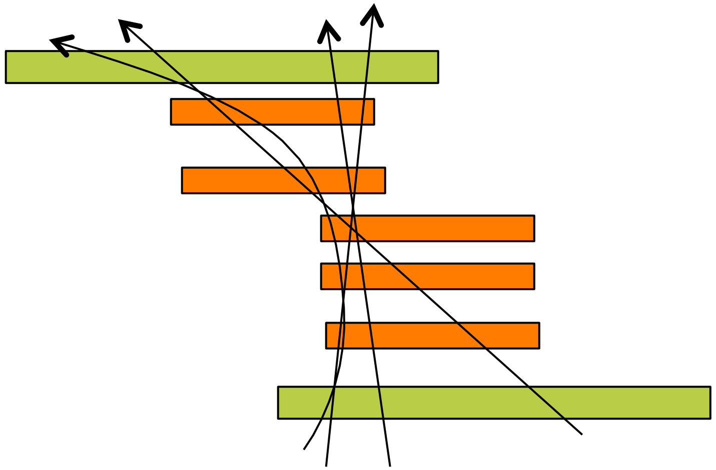
Fixes resolution patterns → fixed aspect ratio

5D track manifold

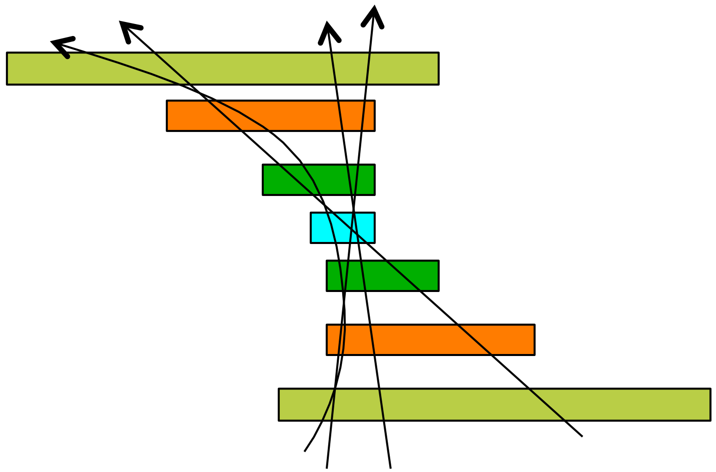
Variable resolution patterns

Many bits variable resolution

1 bit variable resolution



3 bit variable resolution



1 pattern
Volume 4*
Volume 2^(7*2)*4* = 2^16

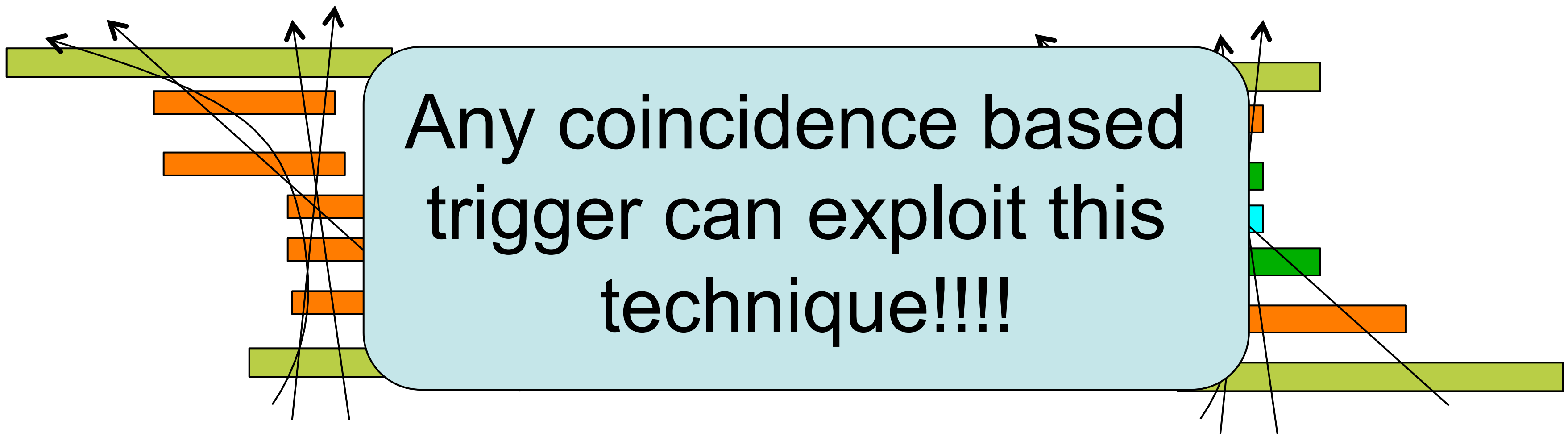
1/16 less volume
less fakes!!!

1 pattern
Volume 1/4*
Volume 2^12

Many bits variable resolution

1 bit variable resolution

3 bit variable resolution

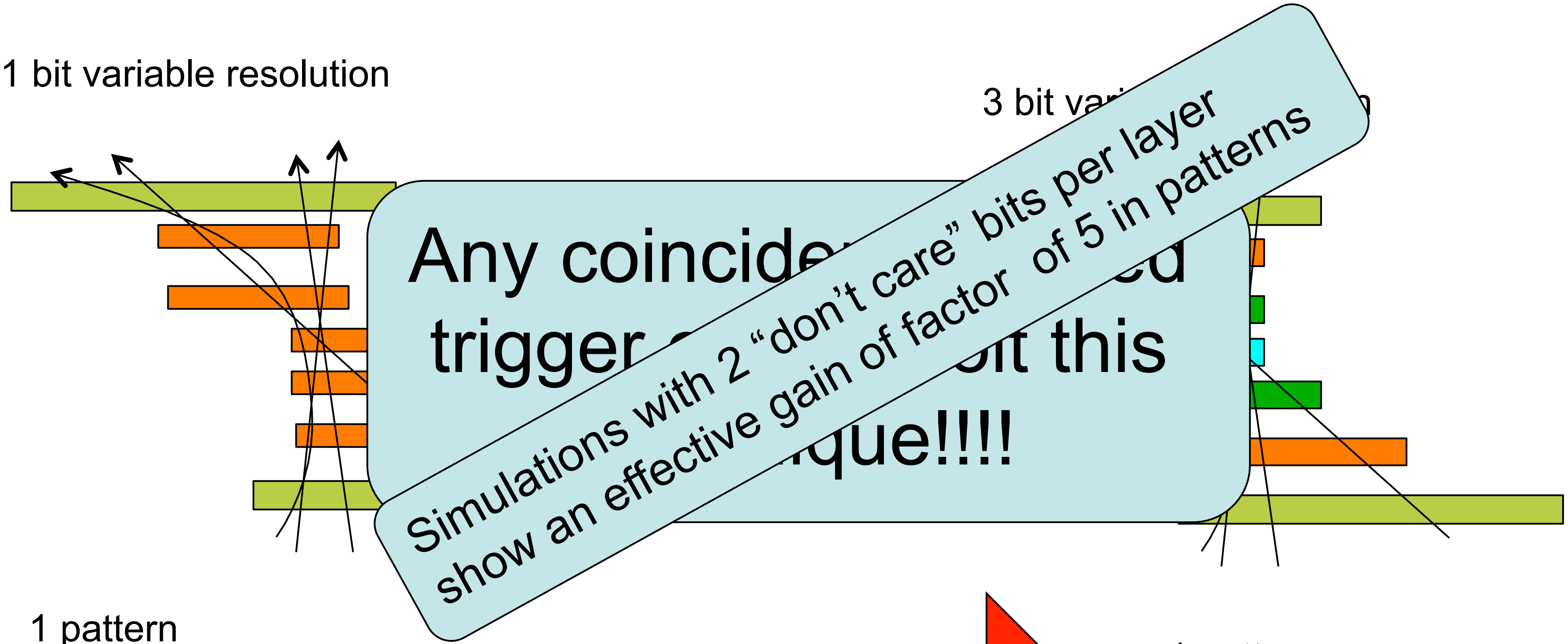


1 pattern
Volume 4*
Volume 2^(7*2)*4* = 2^16

1/16 less volume
less fakes!!!

1 pattern
Volume 1/4*
Volume 2^12

Many bits variable resolution



1 pattern
Volume 4*
Volume 2^(7*2)*4* = 2^16

1/16 less volume
less fakes!!!

1 pattern
Volume 1/4*
Volume 2^12

Ternary CAM Cell with two NOR type cells

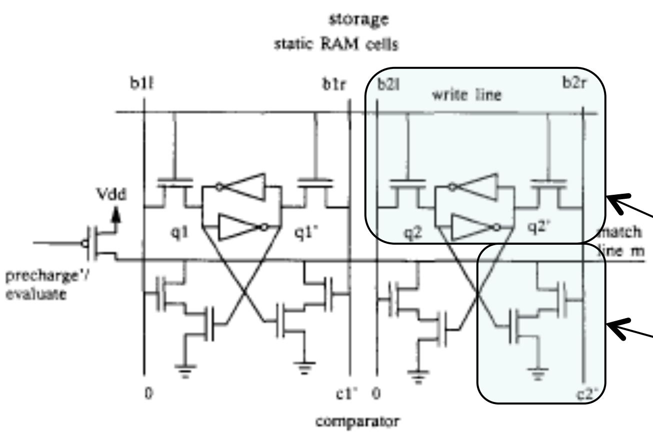


Fig. 8. Two adjacent static binary CAM cells.

SRAM cell stores one bit

Half comparator: compares one value only

Images from: "*Encoding Don't Cares in Static and Dynamic Content-Addressable Memories*", Sergio R. Ramirez-Chavez, IEEE Transactions on circuits and system-II: Analog and Digital Signal Processing, Vol. 39 NO. 8, August 1992

Ternary CAM Cell with two NOR type cells

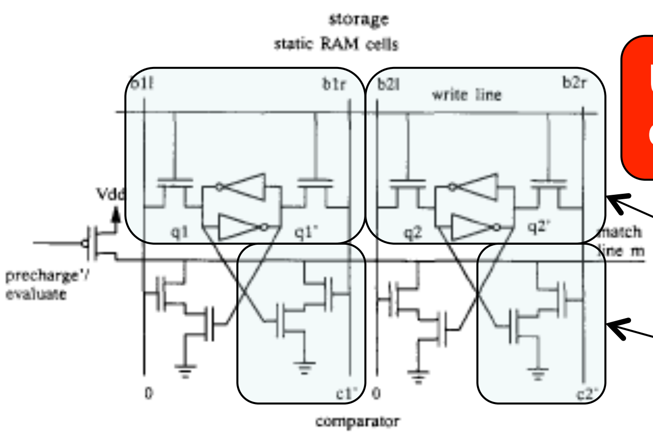


Fig. 8. Two adjacent static binary CAM cells.

Use 2 bits to encode 3 values

2 SRAM cells

2 Half comparators

Can use from 3 to 6 ternary cells per layer.
Variable resolution 1-8 up to 1-64.

Images from: "*Encoding Don't Cares in Static and Dynamic Content-Addressable Memories*", Sergio R. Ramirez-Chavez, IEEE Transactions on circuits and system-II: Analog and Digital Signal Processing, Vol. 39 NO. 8, August 1992

Ternary CAM Cell with two NOR type cells

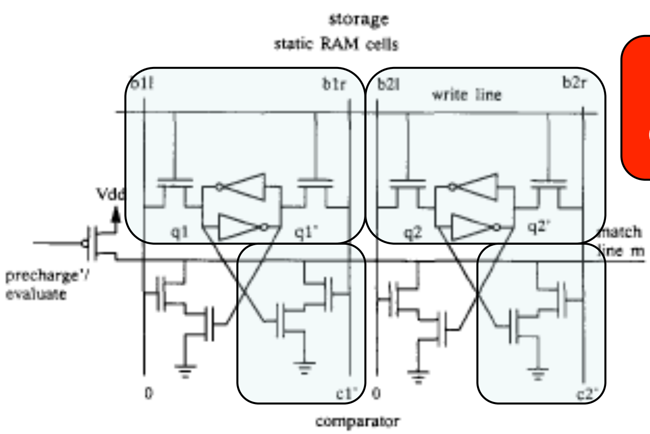


Fig. 8. Two adjacent static binary CAM cells.

Use 2 bits to encode 3 values

storage scheme
stored values

	q1q2
0	01
1	10
*	00

(a)

Each cell does half comparison

retrieval scheme
presented values

presented ternary value	c1c2	encoded value in the bit lines of two binary static CAMS. b1l	b1r	b2l	b2r	binary CAM equivalent operation l	r
0	01	0	1	0	0	0	M*
1	10	0	0	0	1	M	0
*	11	0	0	0	0	M	M

*M is the masking of a bit operation common in commercial binary CAMS.

(b)

Can use from 3 to 6 ternary cells per layer.
Variable resolution 1-8 up to 1-64.

Fig. 9. Encoding and retrieval schemes for don't-care in two static binary CAM's cells with masking capability. (a) Encoding scheme. (b) Retrieval scheme.

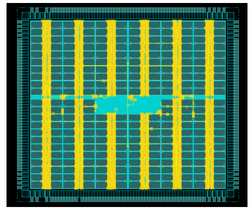
Two bitlines always set to 0

Images from: "*Encoding Don't Cares in Static and Dynamic Content-Addressable Memories*", Sergio R. Ramirez-Chavez, IEEE Transactions on circuits and system-II: Analog and Digital Signal Processing, Vol. 39 NO. 8, August 1992

CAM cell configuration

- 18 CAM bits per layer: 4 NAND and 14 NOR
  - NOR pairs can make a ternary cell
- Default 12 bits + 3 ternary (minimum)
  - 15 bits per input bus (maximum)
  - (14:7) NOR, (6:3) 4 NAND, (2:0) 3 NOR-pairs
- 6 bits + 6 ternary (maximum)
  - Use only 12 bits per input bus
  - (11:10) NOR, (9:6) 4 NAND, (5:0) 6 NOR-pairs
- Ternary cells (NOR pairs) mapped to LSBs
- NAND cells are mapped to LSBs after the ternary cells, when they don't match small power consump.

AMchip04



Input buses
15 bits each

Summary

- Introduced an innovative AM algorithm
  - Resolution variable layer-by-layer and pattern-by-pattern
- Equivalent to a factor 3-5 extra patterns or more
  - Not fully exploited yet
- Any coincidence based trigger can profit