**SEVENTH FRAMEWORK PROGRAMME**
**THE PEOPLE PROGRAMME**

# *Annex I - "Description of Work"**

## PART A:

**Grant agreement for: Industry-Academia Partnerships and Pathways**
**Call identifier: FP7-PEOPLE-2012-IAPP**

**Project acronym:** FTK
**Grant agreement no.:** 324318

**Project full title:** Fast Tracker for Hadron Collider Experiments

**Date of approval of Annex I by REA:** 24/09/2012
**Project start date:** 01/02/2013

**Duration of the project: 48 months**

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**** This Annex I refers to the 2012 PEOPLE Work Programme (European Commission C(2011)5033 of 19 July 2011)***

# A.1 Project abstract

**Keywords:** trigger, online tracking, pattern matching, content addressable memories, FPGA, VLSI, real-time, electronics, Higgs.

**Abstract:**
This project aims to develop an extremely fast but compact processor, with supercomputer performances, for pattern recognition, data reduction, and information extraction in high quality image processing. The proposed hardware prototype features flexibility for potential applications in a wide range of fields, from triggering in high energy physics to simulating human brain functions in experimental psychology or to automating diagnosis by imaging in medical physics. In general, any artificial intelligence process based on massive pattern recognition could largely profit from our device, provided data are suitably prepared and formatted.
The first goal consists in demonstrating the system can perform online track reconstruction of full events at the highest luminosities of the LHC and SLHC) at CERN, beyond the limits of any existent or planned device and despite the overwhelming confusion due to the very high track multiplicity and the exceedingly large event pile-up. With this goal we participate to the construction and the test for an high precision real-time tracker built for the ATLAS experiment: the Fast Track (FTK) processor. FTK can improve the capability of the ATLAS detector to select interesting events reach of heavy leptons or quarks within the enormous LHC background. It uses FPGA and ASIC chips to implement, real-time, complex track reconstruction algorithms. The track's trajectories are reconstructed in 3D, in few dozens of microseconds and the quality of the parameters is almost offline. FTK will increase the ATLAS discovery capability.
In parallel we will pursue challenging R&D & new real time computing ideas for more complex applications. A new industry-academia cooperation will reinforce the FTK team making it suited for such applications. The knowledge transfer will significantly increase the research quality and overall RTD capability and competitiveness of the partners, opening new scientific directions for our technology dissemination.

# PART B:

# B.1 List of participants

| Beneficiary Number | Beneficiary short name | Commercial Sector *(Y/N)* | SME *(Y/N)* | Country | Scientist in charge | Month Enter-Exit Project |
|---|---|---|---|---|---|---|
| 1 | UniPisa | N | N | Italy | Dell'Orso | M1-M48 |
| 2 | CAEN | Y | Y | Italy | Petrucci | M1-M48 |
| 3 | CERN | N | N | Switzerland | Formenti | M1-M48 |
| 4 | AUTH | N | N | Greece | Kordas | M1-M48 |
| 5 | PRIELE | Y | Y | Greece | Mermikli | M1-M48 |
| 6 | CNRS [1] | N | N | France | Calderini | M1-M48 |
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| | | | | | | |

[1] The work program related to the CNRS partner will be performed at the Laboratoire de Physique Nucléaire et des Hautes Energies (LPNHE) in Paris.

# B.2 S&T Quality

## B.2.1. Objectives of the research programme

The Physics programme at CERN's Large Hadron Collider (LHC) has been extremely successful since the early phase of data taking in the year 2010. The LHC detectors were designed to search for new discoveries in the head-on collisions of protons of extraordinarily high energy. The origin of mass, extra dimensions of space, unification of fundamental forces, evidence for dark matter candidates in the Universe are among the most interesting searches.
Moreover, the LHC upgrade, currently called the Super LHC (SLHC), will provide continuously increasing instantaneous luminosity, and will widen our capability to search new phenomena that are beyond the scope of our current theory of matter and energy, the Standard Model (SM). In the next few years an impressive harvest of data will be collected at the LHC and at the same time R&D at the technological frontier will be pursued for SLHC.
The proponents of this project are active essential participants of both events. These experiments will have a fundamental impact on physics and technology for the next 20 years. There are good reasons to expect that these new areas of research will have heavy quarks as well as tau leptons – the so-called third fermion generation - in the interesting events. These third generation objects will be excellent probes to search for New Physics.
Tracking devices, and in particular the Silicon devices that are becoming the predominant tracking technology, play an essential role in the identification of the third fermion generation. On the other hand the electronics required to process the signals from the detectors is taking a very important role, and it must be state of the art. The most interesting processes are very rare and hidden in an extremely large level of background. Implementing the most powerful selections in real time is therefore essential to fully exploit the physics potential of experiments where only a very limited fraction of the produced data can be recorded. A drastic real-time data reduction must be obtained. This makes on-line event reconstruction a critical component at any hadron collider experiment. A multi-level trigger is an effective solution for an otherwise impossible problem at LHC. The level-1 (L1) trigger is based on custom processors and reduces the rate from 40 MHz to ~100 kHz . The level-2 (L2) is based on standard CPUs. The L2 output rate is ~3 kHz. The Level-3 (L3) selection, called Event Filter in Atlas (EF) is performed by CPU farms, which write to tape about 200 events/s (at LHC L2 and L3 can also be called High Level Trigger, HLT).
This project directly addresses the main technological challenges of hardware and software necessary to identify heavy flavour objects and jets with a tau lepton. These are tracking issues at detector and trigger level. Addressing the challenging physics goals at the terascale requires a high degree of detector sophistication and significant technological breakthroughs in: (a) new developments in Silicon tracking technologies for thin, radiation-hard sensors; (b) sophisticated triggering and real time processing; (c) use of very deep sub-micron electronics
The high-occupancy environment experienced at the LHC and even more at the SLHC, will require a huge computing power to reconstruct very complex events with hundreds of particles emanating from the proton-proton collisions happening every 25 ns at the heart of the detector. The increase in luminosity of accelerators will require highly segmented and radiation-hard sensors. Given the difficulty to fully deplete the sensors under those conditions and considering the importance of material budget in the quality of track reconstruction, a new development of thin sensors is necessary. We propose collaboration between research companies active in high energy physics and research institutions to face these challenging future conditions.
**The first important goal** of this project is the realization and optimization of the Associative Memory (AM) system to make it work in the FastTracker (FTK) processor for the Atlas experiment at LHC and its future evolution for **new applications**. FTK is a high-performance "super-processor" based on the combination of two innovative technologies: powerful FPGAs

(Field Programmable Gate Arrays) working with standard-cell ASICs (Application-Specific Integrated Circuits), the Associative Memory (AM) chips, for utmost gate integration density. Optimal partitioning of complex algorithms on a variety of computing technologies has been already proved to be a powerful strategy, which turned the past hadron collider experiment CDF at the Tevatron accelerator in the Fermilab Laboratory, near Chicago (USA) into a major player in the field of B-physics, on par with dedicated experiments operating at e+e- colliders.
**A complementary and secondary goal** is the participation to the development of new sensors and electronics for the upgrade of the Silicon tracker of the ATLAS experiment. The sensors should be able to provide charge collection efficiency still larger than 50% even in condition of partial depletion at an equivalent fluence of 1016 neq/cm2 (neq: neutron equivalent).
**There are also important reasons, outside High Energy Physics (HEP), for the research proposed in the present program.** Our approach to use powerful modern electronics is extremely flexible and its spread outside the realm of HEP would be extremely beneficial. The strategy of the "optimal mapping of a complex algorithm in different technologies" is a general approach that can speed up enormously any calculation by providing a high degree of parallelism. Handling complex electronics components (dedicated AM chips and FPGAs) is less straightforward than programming a multi-core CPU, since it requires availability of FPGA hardware and knowledge of computer-aided-design (CAD) tools. For this reason we think that the HEP development in this area is important to show the potential of these devices and to spread the skills needed to use them with top efficiency. There are already examples showing that the use of a tuned combination of CPUs and FPGAs could expand not only in HEP, but also in other academic and even non-academic fields, for example in financial applications. The “Workshop on High Performance Computational Finance” is an instance of the many occasions for discussing FPGA acceleration techniques in the financial domain.
These techniques could be very important in the area of medical imaging for real-time diagnosis, when the patient is under examination. The computing power is still a limiting factor for some high quality applications. High-resolution medical image processing, for example, demands enormous memory and computing power to allow 3D processing in a limited time. The same approach could be incisive for astrophysical and meteorological calculations, for robotic automation, for security applications. It could be essential for neurophysiologic studies of the brain. **This is a goal of our proposal, a study to apply our technology outside HEP.**
The use of the associative memory processor for brain studies is particularly fascinating. The most convincing models that try to validate brain functioning hypotheses are extremely similar to the real time architectures developed for HEP. A multilevel model seems appropriate also to describe the brain organization to perform a synthesis certainly much more impressive than what done in HEP triggers. The AM pattern matching has demonstrated to be able to play a key role in high rate filtering/reduction tasks. We can test the AM device capability as the first level of this process, dedicated to external stimuli preprocessing. We follow the conjecture of reference [Punzi & Del Viva (2006) Visual features and information theory JOV 6(6) 567]: the brain works by dramatically reducing input information by selecting for higher-level processing and long-term storage only those input data that match a particular set of memorized patterns. The double constraint of finite computing power and finite output bandwidth determines to a large extent what type of information is found to be “meaningful” or “relevant” and becomes part of higher level processing and longer-term memory. The AM-based processor will be used for a real-time hardware implementation of fast pattern selection/filtering as studied in these models of human vision and other brain functions.
We could apply this filtering function to medical images, to extract the salient features and apply fast but complex reconstruction algorithms to them. We would measure the extracted features in a very short time and automatic fashion providing a computer-diagnosis. The reduction of execution time of image reconstruction to be applied after the AM filtering

function, would exploit the computing power of parallel arrays of Field Programmable Gate Arrays (FPGAs) as we do in FTK to find clusters of contiguous pixels above a certain programmable threshold. As we process them producing measurements that characterize their shape, we can measure quantities of interest in medical applications like the size of the found spots, how circular or irregular the spot is. The algorithm can be extended to 3-D images.
Also the development of sensors and related electronics has the inter-sectorial aspect of the medical physics. Solid state detectors have been used in medical imaging for many years for early diagnostic in cancerology. Digital images provided by this kind of sensors can also be processed with pattern-recognition algorithms to increase the diagnostic capability.
**The long-term goal** of this research is to increase the importance of parallel computing based on dedicated real-time techniques, disseminating them to a large scientific community.

## B.2.2. Research methodology and approach

FTK is a second generation processor, much more ambitious than its progenitor, SVT, built for the CDF experiment. FTK reconstructs all events coming out of the L1 (100 kHz) to provide into few dozens of microseconds all the tracks with transverse momentum above 1 GeV to the L2. The power of FTK is mainly based on the AM chip. The same AM technology can be used also at L1, even in much more adverse conditions. All the LHC experiments, ATLAS, CMS and even LHCb, are thinking to it for SLHC. Let's compare the Tevatron and LHC machines to explain the increase of complexity of events and, as a consequence, of the tracking detectors. The CDF collision rate was ~2 MHz and at the instantaneous luminosity (ILum) of $3\times10^{32}$ $cm^{-2}$ $sec^{-1}$ the average number of soft, not-interesting interactions per bunch crossing (pile-up) was 6 (396 ns bunch spacing). The LHC environment is much more demanding: a bunch spacing of 25 ns at high ILum ($10^{34}$ $cm^{-2}$ $sec^{-1}$) produces ~25 pile-up interactions. The LHC upgrade (SLHC), with the recently proposed scenario of 50 ns bunch spacing, will produce a pile-up of hundreds of events at the ILum of $5x10^{34}$ $cm^{-2}$ $sec^{-1}$.
Today we can exploit a very important advantage to face the increased complexity: on the technological side, (a) the detector granularity is strongly increased (the SLHC silicon projects are an extreme result in this direction), (b) the digital electronics is becoming so powerful that the difference between the performance of the algorithms executed in real-time and in the offline analysis is significantly reduced, even in the extremely hard conditions of high data rates and limited processing time. Since the background suppression needed at trigger level is becoming similar to that of the usual offline analysis, the offline quality is required already at trigger level. Our goal is "online exploitation" of the full silicon detector resolution: it is challenging, but it is not impossible. Let's see how we plan to do it.
The FTK tracking algorithm is subdivided into 2 sequential steps of increasing resolution. In step 1 the dedicated VLSI device, the AM, finds track candidates with low spatial resolution, called roads. In step 2, the real tracks are searched within the roads and fitted to determine their parameters with the best resolution (sigma(IP)=35 • m, sigma (1/PT) = 0.3 % and sigma($\phi$0)=1 mrad). Tracks with PT>1 GeV/c are finally selected to tag secondary vertexes or to search for hadronic taus or to perform high quality track-based isolation of muons, electrons and gammas.
The AM performs the most CPU intensive part of the pattern recognition, exploiting dedicated highly parallel structures. It exploits the idea of a pattern matching algorithm based on pre-calculated and stored track candidates, which are compared in parallel with the actual event. It has to solve a very difficult problem since the silicon detector has millions of channels and the number of track candidates is very large (~$10^9$). For this reason a high density dedicated chip has been developed for the AM. FTK includes important pre/post processing functions, complementary to the intensive pattern recognition performed by the AM. Pre-processing corresponds to (a) cluster finding in the silicon data, performed by ATCA boards called Data Formatters (DF); (b) smart database for immediate retrieval of full resolution detector clusters associated to roads found by the AM, performed by Data Organizers (DO). Post-processing includes (a) the track fitting performed by Track Fitters (TF) and (b) duplicate-track cleanup performed by the Hit Warrior (HW). The most important function is the track fitting, which refines the candidate tracks in order to determine the track parameters with the full detector resolution. The TF makes use of methods based on local linear approximations and learn-from-data techniques for online misalignment corrections. The fit calculation consists of scalar products. The FTK simulation shows that the approximations, made to be fast, do not significantly affect the fit performance.

The event processing is highly parallel into all online tracking processors, with the detector segmented into towers. Our main goal is to build the Processor Unit (PU) that pipelines all the functions needed by a high quality real time tracker. This is the processor core. A full coverage online tracking for ATLAS at the Phase 1 instant luminosity is estimated to require 8 9U VME crates with 16 PUs each (128 PUs), using the best technology available today. In addition to that, two ATCA crates of Data Formatters are necessary to cluster the raw hits coming from the detector and to provide the correct data to each PU. The main DF processing device is the FTK Input Mezzanine, (FTK_IM), a data concentrator-processor for pixel and strip silicon detectors. It performs online clustering for uni- (strips) and bi-dimensional (pixel) detectors. Different clustering approaches will be studied and implemented on FPGAs.
The FastTracKer (FTK) has been approved recently by ATLAS for a Technical Design Report (TDR) submission in 2013 and to build a small demonstrator taking data in 2015. FTK is today mainly a collaboration between Italy and USA with a smaller contribution from Japan. If the demonstrator is successful, FTK will be enabled for a large production and will be a trigger upgrade for the LHC Phase1 (Phase I, up to $L = 2x10^{34}$ $cm^{-2}$ $s^{-1}$ and 40-80 pileup events). The Italian funding agency, INFN, has taken the responsibility to fund the PCBs and chip costs for the AM system in the demonstrator, but no money is provided for man-power costs, neither for future tests and commissioning periods, neither for further developments. The EU funds would provide the complementary contribution to push further this research, involve new Institution and Companies in an area that is in quick expansion, where new manpower and organization capabilities are strongly needed.
In parallel we need to gain experience on the modern TDAQ systems to face early the integration problems such a complex device could meet. Atlas is allowing us to test the integration of the FTK functions in the experiment, today, well before production. We plan early parasitic commissioning (no impact on normal ATLAS data taking, thanks to a duplicated additional output fiber provided for FTK by the tracking front-end) of a small proto-FTK, based on existing prototypes and able to reconstruct tracks inside a narrow azimuthal slice (tower) of the detector. The FTK output can be written to the calibration stream for offline studies. We call this proto-FTK a “vertical slice” because it will be small (operating on a slice of the detector) but functionally complete from the detector inputs up to the track output available for the L2 CPUs. The vertical slice will continue to exist as a test stand for new prototypes while the FTK demonstrator will start to take data in 2015.
In addition a new R&D is planned for the FTK evolution necessary for the many new foreseen applications, like online tracking at L1 and use of the AM for image processing. Time for FTK production after the TDR approval will be quite long, because of the LHC schedule, so even the FTK final production could profit of the electronic and algorithm advancement we plan to pursue in the next years. While the demonstrator will convince the collaborations of the FTK capabilities, we will provide modern, much more powerful prototypes (AMBSLP), fully tested in the vertical slice, ready to substitute the FTK default one (AMBFTK) in the final production.

**The Serial Link Processor (SLP): a new Processor Unit for many different uses.**

In the R&D area our goal is to build a new Processor Unit called "Serial Link Processor" or SLP. The SLP has many points in common with the past developments: it pipelines all the functions needed by high quality real time tracking (AM, DO, TF, HW); it will occupy a single VME slot, and will consist of a 9U VME board, the AMBSLP, along with an AUX card on the back of the crate, built by the USA FTK collaboration. The two future boards will exchange data through the P3 connector.
The AMBSLP, the object of the European research, will perform pattern recognition (128 AMchips on it). The AMBSLP has the same modular structure of the AMBFTK. It consists of 4 smaller boards, the Local Associative Memory Banks (LAMB). Each LAMB contains 32 AM chips, 16 per face. The AM chips come in LQ208 packages, and contain the stored patterns with the readout logic. They are connected into eight 4-chip pipelines on each LAMB. The found roads flow down in the 8 pipelines and are collected and merged into 4 parallel output streams by two readout logics called GLUEs. The SLP has a flexible control logic placed inside powerful FPGA chips (Xilinx). The FPGA flexibility allows to use the same architecture in different applications characterized by short- or long-latency trigger decisions, with the only exception of the LAMB, which needs to be specialized. In the case of long-latency (SLP2 for L2 trigger or seeding of the offline tracking or image processing) very large associative memory banks can be obtained pipelining boards and AM chips. For low-latency applications (SLP1 for L1 trigger) we reduce the pipelines as much as possible. We will develop a unique motherboard for all possible conditions, and two types of LAMBs , one for long-latency and one

for low-latency applications. In the second case GLUE chips will be placed in the center of "stars" of AM chips directly connected to them, reducing significantly the latency for road readout.
The SLP innovation consists in the use of high speed serial links everywhere in the system. The AM system is today overloaded by the enormous traffic of words flowing to the AM chips. Eight TTL 15 bit buses bring hits to the SLP with a consequent enormous fan out problem (128 AM chips). This is made even more complex by the board output traffic that in the LHC high luminosity will become extremely demanding and will require a larger number of output buses (16), of larger words (32 bit). A redesign of the boards and a new AM chip equipped with serializers, deserializers & differential I/O are required. The chip development is funded by INFN. Serial links will provide important advantages:
1. Gain in flexibility: data words with variable size could be delivered and collected without changes to the boards. Robustness is gained, since the LVDS connection is more robust against noise & cross talk.
2. We can push the transmission frequency into new ranges, far from what we faced in the past.
3. The board routing will be optimized and much less crowded. In particular the LAMB reorganization for L1 application, where direct connections are required between the many AM chips and the readout controllers (GLUEs) would not be possible using a large TTL road bus for each AM chip.
4. The necessary number of pins for signals in the AM chip package will be reduced. This is important because the AM chip silicon area has to increase in the future by a factor of 10, to contain a much larger number of patterns with no change of the package size. Unfortunately also the needs of the chip in terms of VCC and GND pins increases correspondingly, while the package we have (LQ208) is totally occupied by the many necessary TTL buses. Serialized I/O will provide space for VCC and GND pins.
5. The connection between the AMBFTK/AMBSLP and the AUX board is implemented with a very compact, high performance P3 connector, while in the past the AMBoard needed complex connections with the other boards. No backplane is anymore necessary.
**Appropriateness of research methodology and approach.** Our research methodology is based on the idea of a "continuous evolution". Our final goals are very challenging, so we need to advance per steps. For this reason we organize our work in such a way that design, tests and commissioning are performed in parallel, instead of executing them sequentially as usually is done. It is important that test results and commissioning provide a feedback on design before the system is frozen for a large production.
This working plan is extremely ambitious. The methodology of parallel design, tests, commissioning and future R&D is very demanding in terms of manpower and infrastructures. In addition the interest for this technology, as explained above, is quickly expanding. New studies are necessary for L1 and outside-HEP applications. It is particular relevant to have the possibility to involve new institutions and new companies that can learn about the project in the development phase and be fundamental in the future at the production and running time. The work is organized in 5 areas, or **work packages (WP)**.
**WP1**, "**Prototype Construction & Production validation**", leaded by PRIELE, includes board and FPGA firmware design, PCB construction and assembly, standalone test for a first validation. It is important that the designer can participate also to the first tests, before his product is integrated on the complete system. The board design is based on Cadence tools while the firmware is developed with the Xilinx CAD. The board assembly is complex, especially for the LAMB mezzanine that holds 32 AM chips, 12 Xilinx chips, and 8 devices for clock distribution in a small space. LAMBs, motherboards and FTK_IM mezzanines will be produced. The experience gained on prototypes will allow PRIELE to assembly the FTK boards at production time and validate them at the company before commissioning.
**WP2**, "**Infrastructures and Integration**", leaded by CAEN, first of all takes care of crates, power supplies and space for integrated lab tests. We use 9U VME crates with custom VME VIPA backplane, 48V power source and large DC-DC converters from 48 Volts down to 1.2 V to provide the needed power for 128 AMchips per board. The board has 4 DC-DC converters, each one providing a maximum of 25 A at 1.2 Volts, for a total of 100 A and a maximum power of 120 W. Each AM board has a weight of 2 Kg, so the crate has to support a total weight of 40 kg. Cooling and mechanical tests will be performed. The air flow must be sufficient to keep cold the boards. Each rack will contain two crates, each one provided of its own power supply. The power supply has to be transparent as much as possible to air flux. The whole system will be collected in a single place, including parts developed by USA. There realistic experimental conditions will be reproduced and tests enough complex will be performed with Monte Carlo data to guarantee the hardware is complete and can run flawlessly. Software will be developed to monitor and control the processor. The detector data will be produced in the lab by a "pseudo front-end" (a CPU). Data will be delivered via S-link from a mezzanine inserted in the CPU.

**WP3**, "**Commissioning**", leaded by CERN, closes the research path described above. After tests in the laboratory, the new hardware will be moved to the experiment and will spy real data during normal data taking. In fact commissioning implies the insertion in the experiment, the development of monitoring and control software compatible with its rules, long tests to validate the system, data taking and data understanding.
**WP4** is "**Architecture Simulation**", leaded by UniPisa. It is just software, but it has an important impact on hardware choices. A complex package, FTKsim has to simulate the hardware on Monte Carlo data, or real data. It is used to optimize the hardware design, to specify, build and test the internal data paths needed for the LHC high luminosity, to determine the optimal size of the AM system, to produce the Physics case. The simulation is an essential part of all tests since it allows to predict the hardware output, starting from the inputs, to validate the hardware (sometime the simulation) functionality.
**WP5**, "**Image Processing**", leaded by UniPisa, is a new very interesting atypical working area. We will use our AM-based Processor to process static images and movies in real time. We will check the capability of the AM to extract from the images and from a movie the relevant features and substantially suppress the not-relevant information. The images have to be formatted in the right way to provide data for the AM system. For static images groups of 3x3 pixels (black and white) are detected in the images and each particular configuration constitutes a 9-bit pattern. . For films we need to add a third dimension, the time, so the patterns becomes 3x3x3, made of 27 bits (128 million possible configurations). All found patterns will be sent to the AM and their frequency will be measured by the FPGA that controls the board. The pattern frequency is the determinant feature to decide if a pattern is relevant or not. After this learning phase, the relevant patterns will be downloaded in the AM bank and the processor will be ready to filter the images/movies selecting only ~5% of the input data (a maximum number of 1.5 million patterns can be downloaded today). The AM system always monitors the pattern frequencies and if the distribution changes the list of good patterns is updated. The mezzanine FTK_IM, developed to process bi-dimensional pixel detector data, could process the AM output, the filtered image.
**WP6** is "**Silicon Detector R&D**", leaded by CNRS. This WP has a reduced role compared to the electronics tasks, however it provides a solid link with the evolution of the on-going R&D for the silicon sensors and the front-end readout electronics in view of the high luminosity upgrade of the LHC. This link is important for FTK since a constant dependence connects the evolving features of the future tracker (segmentation, geometry, expected hit efficiency, noise, readout speed) with the future of the FTK architecture. CAEN will collect together competencies about the different aspects of the detector and the processing system. To resist in the high-radiation environment of the SLHC interaction region, new pixel sensors are being developed. The p-type bulk is being investigated and this is expected to improve the radiation tolerance (no type-inversion) and the cost of the process. In facts the layout of n-in-p pixel sensors requires the guard ring region to be on the same face of the pixels, basically giving a much cheaper single-side process with respect to the sensors presently used. After radiation damage, the maximum achievable depletion region will be reduced to a fraction of the detector thickness and consequently the signal size will be reduced. The sensors will be back-thinned considerably (well below the 300um, and possibly even below 200um if the technology evolution will allow to reach this in the next few years). The sensors will be operated at below-zero temperature to keep the leakage current to a still acceptable level of a few uA per sensor at -10C. The segmentation will also be reduced. The phi coordinate will follow closely the limit given by the interconnection technology (the present pitch is 50um but this will be reduced to at least 35um) while the pixel length in eta will probably be constrained by the consequent area of the cell and the component density of the readout electronics. Prototypes of a chip in 65nm CMOS process are being developed for the readout chip, to increase the component density of the readout chip and to allow a further reduction of the sensor pixel size. In all this, the power dissipation will play an important role and the high voltage distribution system will be one of the key ingredients in the evolution of the detector design. Even if the detector is operated at a below-zero temperature, a power supply system able to provide 1KV tension at a maximum current of about 10mA per channel will be necessary, with excellent temperature stability and excellent ripple/noise specifications even at full current. The test-stand for the module evaluation will be assembled at CAEN in Viareggio, Italy, to test how the CAEN devices can perform in these difficult conditions. The silicon sensors with their readout electronics will be used with the CAEN high- and low-voltage distribution system. CAEN has a long-tradition as one of the leader producers.

# B.3 Transfer of Knowledge

## B.3.1. Quality and Importance of the Transfer of Knowledge programme

There is a large exchange of knowledge in our research work, since this application is generated by the growing interest on this technology and the enlargement of the FTK collaboration. We have a very rich program of secondments characterized by some peculiarities. First of all many physicists and engineers will be exchanged among the participant institutions, some of them working on the same items. This is justified by the fact that the project is complex and an important goal of this application is the transfer of competencies to new teams that should be strong enough to support all the new applications and developments. The new components of the collaboration have a first period dedicated to learn the technology, followed by a second period where they will become the leading actors of a new application or a working package. The new teams need a significant number of participants to face the effort of the development of a new application. A second feature of our plan is frequent splitting of secondments in multiple periods. This is justified by a scientific program with multiple phases of design, construction, test and commissioning. Transfer of knowledge (ToK) is optimized with multiple periods, as explained below. The multi-return-mechanism will ensure each time efficient ToK back into the organisation of origin of the seconded staff, spreading the experience to the whole group.

Particularly important is the ToK to CAEN & PRIELE. The FTK project has been developed in a very long time (R&D started in 1989) with a very low budget per year. One reason for such a slow increase of budget has been the large diffusion of the CPU-farm based trigger strategy at LHC. The FTK research field had to compete with the predominant idea that commercial devices were the best choice to perform the FTK tasks. FTK was never allowed to assign part of the design to a company, because of the high costs. CAEN itself never participated to FTK in the past, even if it would have been natural given its experience in the field and its small distance from Pisa, the place where FTK was born. The LHC data taking and the machine working conditions changed this scenario. The large number of secondary interactions (high pile-up) that characterized the 2011 run and will increase in the future favour the FTK very powerful parallel architecture. The increase in precision necessary for future measures requires huge samples collected in extremely hard conditions. This gives increasing importance to parallel computing and dedicated real-time techniques. Not only was FTK recently approved for the TDR, but even more ambitious applications are now conceived. FTK has to evolve from its status of R&D. Now that the project is slowly moving from design and prototyping to production we really need the collaboration of companies with a wide experience in test, integration and commissioning of many complex boards. The complexity increase of FTK compared to SVT at CDF, requires this level of organization also for future possible expansions at CMS or LHCb and spin off outside HEP. In addition a new market is opened to these companies. Intensive, parallel computation based on FPGAs and specific VLSIs is again a field where electronics has an enormous potential. This is obviously very interesting for the SMEs participating to this network.

Here we describe the need of ToK inside each WP.

WP1 production & development – A flux of information is necessary inside the WP1, from the institutions already expert of tracking, as UniPisa, to the new collaborators, AUTH, CNRS and the PRIELE SME. The new Academia collaborators were mainly involved in detector construction in the past (AUTH for muon detectors, CNRS for silicon detectors). Now they are interested to start their activity in the trigger sector and in particular in the real time track reconstruction applied to their detectors. Also PRIELE manufactured electronics for CMS and did not have specific experience in online tracking in the past. On the other hand AUTH and CNRS have been in ATLAS for a long time, and PRIELE had experiences in CMS, while the UniPisa FTK researchers only recently joined the ATLAS collaboration. The experience of AUTH, CNRS and PRIELE about the LHC experiments will be valuable for the new group that has to integrate a challenging device in the already installed and working detector. PRIELE offers also a wide experience in electronics design & development as well as in manufacturing prototypes and/or mass production, in particular for space, defence and CERN applications, that is electronics constructions to function in hard environments. This could be a unique

training opportunity for secondments and recruitments visiting PRIELE. Also AUTH and CNRS have a strong electronic division with significant FPGA expertise, so exchanging design experiences will certainly be worthwhile. This large availability of different design skills will increase the initial FTK project goals, the research quality and the overall RTD capability and competitiveness of all the partners. Contacts among the research institutions and the PRIELE SME are guaranteed by the large number of secondment months. UniPisa experienced personnel has planned some months of the first year at PRIELE to (a) start the prototype design, (b) install the FTK test stand to check the assembly quality before the delivery of boards to integration (c) and also to collaborate on firmware and PCB design for the SLP2 prototype. They will also come back to PRIELE in the 3rd and 4th years for the final FTK small productions after the FTK demonstrator success. The seconded ERs will bring back to UniPisa their experience and will share it with other researchers opening their minds towards new opportunities, becoming familiar with practice in industrial routine. Similarly ESRs and ERs will be seconded from AUTH to PRIELE and viceversa. PRIELE and AUTH will collaborate for the design of boards and also the development of firmware. PRIELE secondments to Pisa will have the same goal. During the first year they will work on the system for L2 (SLP2) with the help of UniPisa and after that they will apply their acquired knowledge to L1 (SLP1), starting from the last quarter of the 2nd year. PRIELE engineers will profit of the high level tools (Cadence) available at the Universities and CERN. Coming back home they will transfer the knowledge to the company to reinforce it in its leading role of the WP1. Secondments dedicated to a certain job are split among collaborating Institutions to increase the connections among all the participants. For example the PCB design of the SLP2 will start in UniPisa with the secondment of a CAD expert engineer from PRIELE to work with FTK expert personnel. It will continue at PRIELE with the collaboration of both and personnel from AUTH. The same will be done for the SLP1.This scheme is certainly the best way to reinforce the collaboration of the team, trained on a strong common background. The designers will spend time working together in different places, practicing different realities. CERN will have a particular role for the prototype design since they will provide important trainings. The Electronic Service at CERN belongs to the accelerator sector but it has the typical organization of a company. They provide very professional service for board design based on the Cadence tools. Designing with them the future FTK boards will be a wonderful opportunity to learn all the Cadence details/functionality. This is the goal of the recruitment there. The Electronic Service will recruit an engineer (ER, less than 10 years experience) with advanced experience in the area of hardware real time tracking processors and initial experience of Cadence board design. The engineer will work in the electronic service, learn at the best level the use of Cadence tools and transfer the acquired knowledge about the tracking project. He/she will work also for the tests of the prototypes and will also gain commissioning experience. His/Her career will certainly profit from this valuable experience at CERN. Also AUTH will recruit one ER (less than 10 years experience) to work on online pattern recognition applied at Level 1 for the muon upgraded system. He/she will have to be expert of AM technology and its simulation, to reinforce the AUTH expertise in this field.

WP3 – Commissioning @ CERN. Commissioning of such a complex device in such a complex experiment & hard environment, already built & running is new for everybody within and also outside our collaboration. For this reason it is important to start early and proceed with small steps. All of us will learn gradually from the experience in the experiment. However CAEN has much more experience than the others, as far as infrastructure installation, security rules and procedures are concerned. CAEN will provide valuable support to researchers that will work there. At the same time CAEN will directly experience on the experiment the new field of application of advanced parallel and dedicated computing. It will acquire all the necessary expertise to help maintaining and expanding this system in the future years of LHC data taking. This continuous exchange of expertise will be achieved with the secondment of a high qualified CAEN engineer. He will participate to the 3 commissionings in the last 3 years. A PRIELE engineer (ESR) will be trained both by CERN and UniPisa experienced personnel and he/she will participate to the design of FTK tests and commissioning.

WP2 – WP4 Integration at CAEN & simulation (red and black in Schedule Table). This is a real training for all participating institutions. The exchange of experience and knowledge is maximum: we will collect all the results of all tests performed at each individual Institution to test the entire system of boards working together. This is the synthesis of all the individual efforts. For this reason we schedule a large number of secondment months there from all the research institutions involved in WP1 except

CERN that will offer similar experience in commissioning. The secondment includes MERs, ERs and ESRs. The more experienced staff will guide and supervise the ESRs and ERs work. We will have a significant group from AUTH coming the 1st and 2nd years to work with FTK experts. After the experience of the first year on the AMBFTK, the 2nd year they will become expert of serial links in the SLP2 and they will be able to discuss L1 architectures. CNRS expert personnel will advance in the tests in alternative periods, working with the UniPisa people that will guarantee the contact with the previous experience. The 4th year the AUTH group will come back for the SLP1 tests. This will complete their effort and the success of these tests will be the transfer of knowledge. CAEN offers large enough infrastructures to allow this effort and will provide its competence to lead it. The integration will provide a common experience and background that will be brought back home to prepare a competent and coherent collaboration, ready to produce powerful super-processors. The secondments at PRIELE and CAEN will also be ideal to exchange information about simulation studies and developments. UniPisa will recruit an ER (less than 10 years experience) with software (C++), GRID and online hardware dedicated tracking expertise. He/she will have to be expert of FTK simulation, an item that is not currently supported at UniPisa.

WP5 – Image processing (violet in Schedule Table) Finally the AM system will be used by UniPisa for Image Processing. An ER (less than 10 years experience) with specific expertise in this field will be recruited by UniPisa the last year. He/she will have to be expert in C++ software and AM technology to adapt the existing AM system to the need of this application. The collaboration with CAEN in this work package is conceived to transfer knowledge to a company that could be interested in future applications if the system turns out to be successful. AUTH is also interested in WP5, since their electronic division is expert in image processing. However, given the complexity of the L1 system they plan to build for muons, they prefer to not officially participate to this WP.

WP6 – Silicon Detector R&D. This package foresees secondments of a CNRS silicon detector expert to CAEN, to test CAEN power supply market for silicon detectors at SLHC. The work is diluted in the project 4 years, even if it could be executed in a much shorter time. We choose this strategy because the main goal of this work package is to keep the FTK collaboration, in particular CAEN, in contact with the detector R&D evolution, that will be important in all the years of our project, given the fact that these detectors are studied for LHC Phase II, scheduled after 2020. For this reason CNRS's secondment is split with large time intervals, even if in total it amounts to only 4 months. An ER with more than 10 years experience will be recruited the second year by CNRS to work on both subjects Silicon R&D and online tracking. He should have expertise of silicon detectors and of hardware for online tracking. He will participate to the pixel R&D and the running of the FTK test stand that will be installed at CNRS to allow firmware and test developments in Paris.

## B.3.2. Role of exchanged/recruited staff within the ToK programme

The ToK will be guided by experienced researchers, physicists and engineers. They have wide experience in experiments and in electronics development as well as trigger and data acquisition (TDAQ). We describe here the personnel that will be seconded, their role in the ToK plan and more in general in the project.

UniPisa has the responsibility and most expert engineers of the AM system. They worked for several years to the SVT design, its test and commissioning and after that to the development of the 3 second generation prototypes designed for FTK. The AMBFTK board, currently under design for the new AM chip, is the third existing prototype and will be used in the FTK Demonstrator. UniPisa has also experienced physicists that had an important role in the construction, commissioning and operation of SVT at CDF and trigger coordination. They will transfer knowledge of the FTK project outside UniPisa with their secondments, in particular to PRIELE to make them sufficiently expert to lead the Production of new prototypes.

The other key person holding a large experience on SVT and FTK is at CNRS (recently recruited by CNRS). He had an important role in the SVT upgrade as responsible of the Giga Fitter, a single board that replaced the old 12 Track Fitters and performed $10^9$ track fits per second. He had also a key role in developing the FTK simulation package, designing the AMchip, and organizing the vertical slice environment for tests.

In AUTH there are the two expert physicists that will be deeply involved in the Micromegas detector for the upgrade of the muon spectrometer at SLHC, including the Level 1 trigger application. Their curricula demonstrate the quality of their research, their interest in the ATLAS upgrades, but also their need of learning in the area of FTK applications. Their past work includes activities on different detector areas: the construction of the chambers of the muon spectrometer, work on the electromagnetic liquid Argon calorimeter simulation, work on the ATLAS TDAQ and GRID applications. They participated to analyses studies, including b-physics, measurement of the mass of the top quark, searching for penguin decays of B mesons, with a recent interest in Di-boson, Higgs and physics beyond the Standard Model, with coordination roles. The results of their research have been published in hundreds of papers in international scientific journals and conference proceedings.
The last experienced researchers that will participate to the project are from CAEN and CNRS. The CAEN engineer has been power supply designer for nuclear physics in CAEN and now is vice-coordinator of the power supply system design for LHC experiments. In 2004 he became the person in charge for the entire power supply system of all the 4 LHC experiments. Since 2009 he is the CAEN responsible for regional, national and international funded projects. He has the perfect background to learn about FTK, to lead the integration WP and to help in commissioning at CERN. The physicist from CNRS is the ATLAS/SLHC LPHNE group leader, had a leading role in the Babar silicon vertex design, test and commissioning.
In addition a team of ERs and ESRs will be seconded together with the experienced group. They provide the manpower necessary to face the big project effort. FTK is a great opportunity to gain an important position in this emerging technology that will offer opportunities during its expansion in ATLAS and other experiments.

# B.4 Implementation

## B.4.1. List of Work Packages

| Work package No | Work package title | Lead Beneficiary | Type of activity | Start-End month |
|---|---|---|---|---|
| 1 | Prototype Construction & Production Validation | PRIELE | RTD | M1-M42 |
| 2 | Infrastructure & Integration | CAEN | ToK | M1-M48 |
| 3 | Commissioning | CERN | RTD | M12-M48 |
| 4 | Architecture Simulation | UniPisa | RTD | M1-M48 |
| 5 | Image Processing | UniPisa | RTD | M25-M48 |
| 6 | Silicon Detectors | CNRS | RTD | M1-M48 |
| 7 | Outreach | AUTH | DISS | M1-M48 |
| 8 | Workshops & Trainings | AUTH | TR | M1-M48 |

## B.4.2. Work Packages description

| **Work package number** | **1** | **Planned start date:** | M1 |
|---|---|---|---|
| **Work package title** | Prototype Construction & Production Validation | | |
| **Beneficiary short name** | PRIELE | | |

**Objectives**

**O.1.1. Construction of SLP prototypes**

**O.1.2. ToK to PRIELE for board assembly and validation before integration or commissioning**

**O.1.3. Standalone validation of SLP prototypes**

**O.1.4. Standalone validation of FTK production**

**O.1.5. ToK between research institutions about AM technology**

**Description of work**

**T.1.1.** Installation of an FTK test stand at PRIELE and AUTH for board validation tests & ToK

**T.1.2.** Design of SLP2 PC boards (schematic capture, layout & routing with Cadence tools)

**T.1.3.** Design of SLP2 firmware (HDLs language and use of Xilinx CAD)

**T.1.4.** SLP2 PCB construction

**T.1.5.** SLP2 assembly at PRIELE

**T.1.6.** Standalone validation of SLP2 at PRIELE before integration at CAEN

**T.1.7.-T.1.11.** Same tasks for SLP1 as T1.2-T.1.6 for SLP2

**T.1.12.** Validation of 1st FTK production

**T.1.13.** Validation of 2nd FTK production

**Deliverables and Milestones**

**D.1.1.** SLP2 prototype constructed at PRIELE – delivery date M12

**D.1.2.** 1st FTK production assembled at PRIELE – delivery date M32

**D.1.3.** SLP1 prototype constructed at PRIELE – delivery date M36

**D.1.4 .** 2nd FTK production assembled at PRIELE – delivery date M42

**M.1.1.** SLP2 prototype validated at PRIELE - M12

**M.1.2.** FTK Technical Design Report: Atlas evaluation of FTK prototypes - M12

**M.1.3.** 1st FTK production validated at PRIELE – M32

**M.1.4.** SLP1 prototype validated at PRIELE – M36

**M.1.5.** 2nd FTK production validated at PRIELE – M42

**Seconded Fellows**

**MER 1** (GPF 21) – From Partner UniPisa to PRIELE – Month 7 to 8

Expertise: AM system responsibility; PC board and firmware design; quality assurance.

Tasks where involved: T.1.1, T.1.2, T.1.3 (M.1.1 SLP2 validated at Priele); T.1.12 (M.1.3 FTK prod)

**MER 2** (GPF 22) – From Partner UniPisa to PRIELE – Month 8 to 9; Month 23-24.

Expertise: AM system; PC board and firmware design; quality assurance.

Tasks where involved: T.1.1, T.1.2, T.1.3 (M.1.1 SLP2 validated at Priele);

**ER 3** (GPF 23) –From Partner AUTH to PRIELE – Month 5 to 6; 10 to 11; 20 to 21

Expertise: automated low power instrumentation systems; energy consumption estimation; PC board implementation.

Tasks where involved: T.1.2, T.1.3 (M.1.1 SLP2 validated at Priele); T.1.7, T.1.8 (M.1.4 same SLP1)

**ER 4** (GPF 24)– From Partner AUTH to PRIELE – Month 11 to 12

Expertise: Design of Reconfigurable Processors.

Tasks where involved: T.1.3 SLP2 firmware (M.1.1)

**ER 5**

(GPF 2) From Partner PRIELE to UniPisa – Month 5 to 6

(GPF 17) From Partner PRIELE to AUTH – Month 8 to 9

Expertise: embedded devices and firmware

Tasks where involved: T.1.3 SLP2 firmware (M.1.1)

**ER 6**

(GPF 1) From Partner PRIELE to UniPisa – Month 3 to 4; Month 26 to 27; Month 29 to 30

Expertise: schematic capturing and physical layout of multilayer PCBs

Tasks where involved: T.1.2 SLP2 PC design (M.1.1); T.1.7 SLP1 PC design (M.1.4)

(GPF 18) From Partner PRIELE to AUTH – Month 22 to 23

Tasks where involved: T.1.7 SLP1 PC design (M.1.4)

**ER 7** (GPF 19) - From Partner PRIELE to AUTH – Month 31 to 32

Expertise: setting up test kits and run functional tests on PCBs and/or electronic devices

Tasks where involved: T.1.11 SLP2 tests at Priele (M.1.4)

**ESR 8** (GPF 3) - From Partner PRIELE to UniPisa – Month 14 to 15

Expertise: setting up test kits and run functional tests on PCBs and/or electronic devices

Tasks where involved: T.1.12 SLP2 firmware (M.1.3)

**Recruited Fellows**

**ER 9** (GPF 20) –Partner AUTH– Month 13 to 36 (note: ER 9 fellow also active in WP3, WP4)

Expertise: AM technology

Tasks where involved: T.1.7, T.1.8, T.1.11 SLP1 PCB & firmware design, tests (M.1.4)

**ER 10** (GPF 14) –Partner CERN– Month 32 to 43 (note: ER 10 fellow also active in WP3)

Expertise: AM technology

Tasks where involved: T.1.7, T.1.8, T.1.11 (M.1.4) SLP1 PCB & firmware design, tests at CERN

**Risk Analysis**

**M.1.1.** Risk: SLP2 validation fails; it looses the possibility to be used in the FTK demonstrator. Action: (a) the demonstrator can be based on existing AMBFTK boards; (b) SLP2 design will be fixed and a second prototype built.

**M.1.2.** Risk: Atlas review of entire FTK system fails (extremely unlikely). Action: this project continues on R&D items to be used for longer-term goals (L1 applications for muons, for Phase II LHC upgrade, and Image Processing outside HEP); productions D.1.2 and D.1.4 will be dropped.

**M.1.3.** Risk: major fault found in produced boards. Action: investigate and solve the problem, then repeat the production. In this case we will propose to ATLAS a later commissioning to be approved by the experiment.

**M.1.4.** Risk: SLP1 validation fails; it looses the possibility to be used in the Atlas phase I upgrade. Action: evaluate the opportunity to continue L1 R&D for a second prototype during the last year.

**M.1.5.** Risk: major fault in production due to factory responsibility. Action: propose to ATLAS a later commissioning to be approved by the experiment.

| **Work package number** | **2** | **Planned start date:** | M1 |
|---|---|---|---|
| **Work package title** | Infrastructures & Integration | | |
| **Beneficiary short name** | CAEN | | |

**Objectives**

**O.2.1. Infrastructure construction and validation: racks, crates, power supplies, cooling system**

**O.2.2. Integration of prototypes from Europe, Japan and USA, validation before production**

**O.2.3. Software development for system control, monitoring, and test**

**O.2.4. ToK between CAEN and research institutions for integration, commissioning, and maintenance**

**O.2.5. ToK between research institutions about FTK technology for any kind of applications**

**Description of work**

**T.2.1.** Installation of a vertical slice (VS) at CAEN for board integration, validation tests & ToK

**T.2.2.** Prototyping of a CAEN power supply for the final crate (5kW)

**T.2.3.** Software development for tests of the VS

**T.2.4.** Tests and validation of the baseline FTK system for the demonstrator

**T.2.5.** Tests and validation of the SLP2-based system

**T.2.6.** Tests and validation of the SLP1-based system

**T.2.7.** Tests of cooling and mechanics of a rack with complete final crates

**Deliverables and Milestones**

**D.2.1.** VS infrastructure at CAEN for FTK demonstrator integration – delivery date M6

**D.2.2.** FTK demonstrator fully integrated with old power supply - delivery date M12

**D.2.3.** CAEN power supply ready for integration - delivery date M18

**D.2.4** FTK cooling and mechanical tests completed - delivery date M20

**D.2.5.** SLP2 fully integrated - delivery date M20

**D.2.6** SLP1 fully integrated - delivery date M48

**M.2.1.** FTK demonstrator running flawlessly at CAEN – M12

**M.2.2.** SLP2-based FTK running flawlessly at CAEN – M20

**M.2.3.** Infrastructure (crate, cooling, power supplies, mechanics) validated – M20

**M.2.4.** Comparison and choice between FTK baseline and SLP2 systems – M20

**M.2.5.** SLP1-based FTK running flawlessly – M48

**Seconded Fellows**

**MER 1** (GPF 7) – From Partner UniPisa to CAEN – Month 10 to 20, Month 29, 33

Expertise: Integration responsibility; test, firmware design; quality assurance.

Tasks where involved: T.2.1., T.2.3., T.2.4., T.2.5. (M.2.1., M.2.2. FTK demo & SLP2 running flawl.)

**MER 11** (GPF 8)– From Partner AUTH to CAEN – Month 4 to 5, Month 39 to 40.

Expertise: Trigger and Data acquisition

Tasks where involved: T.2.4. FTK demo tests (M.2.1.); T.2.6 SLP1 tests (M.2.5)

**MER 12** (GPF 9)– From Partner AUTH to CAEN – Month 41 to 42.

Expertise: Grid and muon detectors

Tasks where involved: T.2.6 SLP1 tests (M.2.5)

**ESR 13** (GPF 10)– From Partner AUTH to CAEN – Month 38 to 40

Expertise: Grid and data acquisition

Tasks where involved: T.2.6 SLP1 tests (M.2.5)

**ER 4** (GPF 11)– From Partner AUTH to CAEN – Month 4 to 5, Month 16 to 17

Expertise: Design of Reconfigurable Processors.

Tasks where involved: T.2.4. FTK demo tests (M.2.1.); T.2.5. SLP2 tests (M.2.2.)

**ER 19** (GPF 12)– From Partner AUTH to CAEN – Month 4 to 5, Month 15 to 17

Expertise: multiprocessing systems design and methodology for application, implementation and hardware/software co-design

Tasks where involved: T.2.4. FTK demo tests (M.2.1.); T.2.5. SLP2 tests (M.2.2.)

**ER 14** (GPF 13)– From Partner CNRS to CAEN – Month 7 to 8, Month 12 to 13, Month 20 to 21, Month 36 to 37.

Expertise: AM system, firmware, tests, software and GRID

Tasks where involved: T.2.4. FTK demo tests (M.2.1.); T.2.5. SLP2 tests (M.2.2.), T.2.6 SLP1 tests (M.2.5)

**Risk Analysis**

**M.2.1** Risk: problems detected in the FTK demonstrator. Action: Solve the problems and move commissioning start at CERN to a later date (maximum delay allowed by contingency is 8 months).

**M.2.2** Risk: problems detected in the SLP2-based FTK. Action: Choose baseline technology

**M.2.5** Risk: major problems in the SLP1-based FTK. Action: This system is not suitable for ATLAS Phase I

| **Work package number** | **3** | **Planned start date:** | M12 |
|---|---|---|---|
| **Work package title** | Commissioning | | |
| **Beneficiary short name** | CERN | | |

**Objectives**

**O.3.1. Infrastructure Installation and validation at point 1: racks, crates, power supplies, cooling system**

**O.3.2. Board installation and validation**

**O.3.3. Running control and functional monitoring**

**O.3.4. ToK between CAEN and research institutions for board commissioning and maintenance**

**O.3.5. ToK between research institutions about FTK technology for any kind of future application**

**Description of work**

**T.3.1.** Installation of Infrastructures, validation tests & ToK

**T.3.2.** Installation of boards (SLP2 or FTK baseline) for the demonstrator

**T.3.3.** Tests and validation of the FTK demonstrator

**T.3.4. T.3.5 as T.3.2, T.3.3.** for the first production

**T.3.6. T.3.7. as T.3.2, T.3.3.** for the second production

**Deliverables and Milestones**

**D.3.1.** FTK demonstrator commissioned – delivery date M22

**D.3.2.** FTK first production commissioned – delivery date M34

**D.3.3.** FTK second production commissioned - delivery date M46

**M.3.1.** FTK demonstrator running flawlessly inside Atlas– M24

**M.3.2.** FTK first production running flawlessly inside Atlas – M36

**M.3.3.** FTK second production running flawlessly inside Atlas – M48

**Seconded Fellows**

**ESR 8** (GPF 15)– From Partner Priele to CERN – Month 18 to 19

Expertise:

Tasks where involved: T.3.1. (M.3.1.) FTK Demo commissioning

**MER 14** (GPF 16)– From Partner CAEN to CERN –Month 18 to 19, Month 33 to 34, Month 43 to 44

Expertise:

Tasks where involved: T.3.1., T.3.2, T.3.3. FTK demo comm & 1$^{st}$, 2$^{nd}$ FTK comm.. (M.3.1.), (M.3.2)

**Recruited Fellows**

ER 10 (GPF 14) –Partner CERN– Month 32 to 43 (note: ER 10 already inserted in WP1, also active in WP1)

Expertise: AM technology

Tasks where involved: T.2.6., T.2.7., (M.2.3.) commissioning at CERN

**Risk Analysis**

**M.3.1., M.3.2., M.3.3.** Risk: any kind of failure at level of commissioning will produce the same action: understand the problem and fix it, requiring extra time to Atlas for the final activation.

| **Work package number** | **4** | **Planned start date:** | M1 |
|---|---|---|---|
| **Work package title** | Simulation | | |
| **Beneficiary short name** | UniPisa | | |

**Objectives**

**O.4.1. Definition of L1, L2 architectures optimizing the physics reach**

**O.4.2. Validation of tests: production of test vectors to validate HW configurations**

**Description of work**

**T.4.1.** SW simulation of the HW details of the FTK demonstrator

**T.4.2** Production of test vectors for the FTK demonstrator

**T.4.3.** Production of test vectors for the SLP2 based FTK

**T.4.4.** Study of high level event selection algorithms based on FTK tracks

**T.4.5.** Study of the L1 Muon Trigger architecture

**T.4.6.** Production of test vectors for the SLP1 based FTK

**Deliverables and Milestones**

**D.4.1.** - FTK Demonstrator detailed simulation - delivery date M9

**D.4.2. –** Test Vectors for the FTK demonstrator - delivery date M10

**D.4.3.** - Test Vectors for the SLP2 based FTK - delivery date M16

**D.4.4.** - Trigger table for FTK demonstrator with performance prediction – delivery date M25

**D.4.5.** - SLP1 architecture simulation - delivery date M28

**D.4.6.** - SLP1 detailed simulation - delivery date M38

**D.4.7.** - Test Vectors for the SLP1 based FTK - delivery date M42

**M.4.1.** FTK Demonstrator simulated in its general architecture – M6

**M.4.2** Predicted trigger performances meet Atlas requirements – M26

**M.4.3.** Approval of SLP1 architecture in Atlas – M30

**Seconded Fellows**

**MER 12** (GPF 9) – From Partner AUTH to CAEN – Month 15 to 16.

Expertise: Grid and muon detectors

Tasks where involved: T.4.1 SLP1 simulation and architecture studies & tests (M.2.5)

**ESR 13** (GPF 10)– From Partner AUTH to CAEN – Month 15 to 17

Expertise: Grid and data acquisition

Tasks where involved: T.4.1 SLP1 tests (M.4.1)

**Recruited Fellows**

**ER 15** (GPF 4) – Partner UniPisa– Month 10 to 29

Expertise: FTK system simulation, FTK architecture

Tasks where involved: T.4.3.-T.4.6.

**Risk Analysis**

**M.4.1.** Risk: general simulation not ready. Action: increase manpower to satisfy test vector deliveries.

**M.4.2** Risk: predicted trigger performances do not meet Atlas requirements, FTK could be rejected. Action: FTK productions could be dropped, R&D program would continue

**M.4.3.** Risk: SLP1 architecture rejected by Atlas . Action: correct the architecture to satisfy Atlas requirements and propose the architecture for later Phase II Atlas upgrades.

| **Work package number** | **5** | **Planned start date:** | M25 |
|---|---|---|---|
| **Work package title** | Image Processing | | |
| **Beneficiary short name** | UniPisa | | |

**Objectives**

**O.5.1.** Test AM real time capability to extract relevant features of natural and medical images

**O.5.2.** Evaluate the impact on medical imaging and diagnosis

**O.5.3.** Evaluate the impact on robotic automation

**Description of work (brief description; possibly broken down into tasks)**

**T.5.1.** Installation of a separate crate and AM system at CAEN for image processing

**T.5.2.** Production of software and firmware for image formatting and system training

**T.5.3.** Evaluate performances of natural still image processing

**T.5.4.** Perform tests on moving image processing

**T.5.5.** Perform tests on medical image processing

**Deliverables and Milestones**

**D.5.1.** Infrastructure at CAEN for Image Processing – delivery date M26

**D.5.2.** Software & firmware ready for training and image processing - delivery date M30

**D.5.3.** Performances of natural still image processing - delivery date M34

**D.5.4.** Results of tests on movie processing - delivery date M40

**D.5.5.** Results of tests on medical image processing - delivery date M48

**M.5.1.** Hardware still-image processor running flawlessly – M34

**M.5.2.** Filtering and data reduction of natural movies running flawlessly – M40

**M.5.3.** Procurement of medical image data – M42

**Recruited Fellows**

**ER 16** (GPF 5) – Partner UniPisa– Month 26 to 43

Expertise: AM system, FTK architecture, image processing

Tasks where involved: T.5.2., T.5.3., T.5.4., T.5.5.

**Risk Analysis**

**M.5.1.** Risk: Hardware still-image processor not working as expected. Action: understand the problem and fix it, reducing the time available for users inside the project time window.

**M.5.2.** Risk: the movie processing is not producing the expected results. Action: try more to understand problems and fix them, reducing the time available for medical image processing

**M.5.3.** Risk: we fail to procure medical image data. Action: drop this part of the program.

| **Work package number** | **6** | **Planned start date:** | M1 |
|---|---|---|---|
| **Work package title** | Silicon Detector | | |
| **Beneficiary short name** | CNRS | | |

**Objectives**

**O.6.1. CAEN Power supply (PS) optimization for Phase-II LHC pixel detectors**

**Description of work**

**T.6.1.** Setup of a test bench for PS performance evaluation at CAEN

**T.6.2** Mesurements on PSes equipped with undamaged readout chips (FEI4 devices)

**T.6.3.** Optimization of PSes with irradiated devices

**T.6.4.** Tests with optimized PSes

**Deliverables and Milestones**

**D.6.1.** Test bench – delivery date M12

**D.6.2.** Standard characterization – delivery date M24

**D.6.3.** Optimized power supplies and their characterization - delivery date M34

**M.6.1.** ATLAS review of CAEN power supplies – M32

**Seconded Fellows**

**MER 17** (GPF 6) –– From Partner CNRS to CAEN – Month 8 to 9, Month 31 to 32

Expertise: silicon detector development, test, commissioning and maintenance.

Tasks where involved: T.6.1.-T.6.4. (M.6.1)

**Recruited Fellows**

**MER 18** (GPF 25) – Partner CNRS– Month 6 to 17

Expertise: silicon detector, AM system

Tasks where involved: T.6.1.-T.6.4. (M.6.1); will work also on WP2 T.2.5. SLP2 tests (M.2.2.), T.2.6 SLP1 tests (M.2.5)

**Risk Analysis**

**M.6.1.** Risk: Atlas is not interested to the proposed CAEN power supplies solution. Action: try to change the solution to meet Atlas requirements.

| **Work package number** | **7** | **Planned start date:** | M1 |
|---|---|---|---|
| **Work package title** | Outreach | | |
| **Beneficiary short name** | AUTH | | |

**Objectives**

**O.7.1. Communication promotion between the scientific community and the general public**

**O.7.2. Awareness of science increase**

**Description of work**

**T.7.1. IAPP project open days**

**T.7.2 Workshop days**

**T.7.3. Summer school weeks**

**Deliverables and Milestones**

**D.7.1.** IAPP project open days – delivery dates M7, M19, M31, M43

**D.7.2.** Workshop days - delivery dates M5, M17, M29, M41

**D.7.3.** Summer school weeks – delivery dates M6, M18, M30, M42

**D.7.4.** World wide web site for dissemination – delivery dates M6, M18, M30, M48

**M.7.1. – M.7.3** Verification of open day results – M8, M20, M32

**M.7.4. – M.7.6** Verification of workshop day results – M6, M18, M30

**M.7.7. – M.7.9** Verification of summer school week results – M7, M19, M31

**Risk Analysis**

**For all milestones:** Risk: the outreach result of the proposed action has been unsatisfactory. Action: fix the problems for a better result at the next event.

| Work package number | 8 | Planned start date: | M1 |
|---|---|---|---|
| Work package title | FTK Workshops and Trainings | | |
| Beneficiary short name | AUTH | | |

**Objectives**

**O.8.1. Communication promotion between the participants to the project**

**O.8.2. Offer a suitable environment for trainings, to facilitate the sharing of knowledge and culture between the participants**

**O.8.3 Improve the chance of career opportunities to the project young researchers**

**T.8.1.** Organize FTK Workshops:

(a) FTK Kick-off Workshop at UniPisa, mainly to provide FTK knowledge to the new collaborators

(b) FTK Workshop at PRIELE (beginning 2nd year), particularly focused on WP1 & WP2 results.

(c) FTK Workshop at CERN during 2nd year, particularly focused on commissioning results (WP3).

(d) FTK Workshop at CNRS during 3rd year, particularly focused on WP6.

(e) FTK Workshop at CAEN near the end of 4th year, to discuss all the project results, included WP5.

**T.8.2.** Organize trainings**:**

(a) "The AM system": kick-off at UniPisa, for specific experience. Possible hands-on activity in Lab

(b) "Embedded System Design Using FPGA Technology", "VHDL Verification Techniques" and "Design Exploiting FPGA Resources" with lab sessions, at AUTH.

(c) "Silicon Photomultiplier read out-SIPM", "Past experience at LHC", "Overview of EU projects" offered by CAEN.

(d) "Technology: (a) CERN practical experience for the development of high density electronics boards, (b) kow-how for quality assurance practices in board manufacturing", with visit to the TE-MPE-EM infrastructures.

(e) **"**Experience on silicon detectors: evolution from LHC to SLHC" at LPNHE (Paris), with visit to the lab and learning to work in clean rooms.

(f) "Overview of the PRIELE projects" at PRIELE: knowledge of the company and its organization.

**T.8.3. Provision of courses in transferable skills. For example project management, language and presentation skills, IPR, ethics, ...**

**Deliverables and Milestones**

**D.8.1.** FTK Workshop – delivery dates M1, M13, M19, M29, M46

**D.8.2.** Trainings - delivery dates M1, M5, M9, M19, M29, M47

**D.8.3**. World wide web site for dissemination – delivery dates M6, M18, M30, M48

**M.8.1.** Evaluation of ToK between participants and results of trainings - M25

**Risk Analysis**

**M.8.1.** Risk: ToK has been unsatisfactory during the first two years. Action: find solutions to be applied during the last two years.

## B.4.3. List of milestones and project deliverables

| Milestone no. | Milestone name | Lead beneficiary short name | Delivery date | Comments |
|---|---|---|---|---|
| M.4.1. | Demo general simulation ok | UniPisa | M6 | Demonstrator simulated architecture ok |
| M.1.1. | Slp2 prototype ok at Priele | PRIELE | M12 | SLP2 prototype validated at PRIELE |
| M.1.2. | Prototypes Atlas Review | PRIELE | M12 | Atlas evaluation of FTK prototypes |
| M.2.1. | Demonstrator ok at Caen | CAEN | M12 | Demonstrator runs flawlessly at Caen |
| M.2.2. | Slp2 ok at Caen | CAEN | M20 | SLP2 runs flawlessly at CAEN |
| M.2.3. | Infrastructure ok at CAEN | CAEN | M20 | Infrastructure validated |
| M.2.4 | Compare_technologies | CAEN | M20 | Compare and choose technology |
| M.3.1. | Demonstrator ok at Atlas | CERN | M24 | Demonstrator runs flawlessly in Atlas |
| M.4.2. | Trigger_performance_ok | UniPisa | M26 | Predicted trigger performances ok |
| M.4.3. | SLP1 architecture review | UniPisa | M30 | Approval of SLP1 architecture in Atlas |
| M.1.3. | 1st production ok at Priele | PRIELE | M32 | 1st production validated at PRIELE |
| M.5.1. | HW still-image processor ok | UniPisa | M34 | HW still-image processor runs flawlessly |
| M.3.2. | 1st production ok at Cern | CERN | M36 | 1st production runs flawlessly in Atlas |
| M.1.4. | SLP1 prototype ok at Priele | PRIELE | M36 | SLP1 prototype validated at PRIELE |
| M.6.1. | CAEN PS Atlas review | CNRS | M32 | CAEN power supply Atlas review |
| M.5.2. | Natural movies processed by AM | UniPisa | M40 | AM filtering of natural movies ok |
| M.5.3. | Medical images for AM | UniPisa | M42 | Procurement of medical image data |
| M.1.5. | 2nd production ok at Priele | PRIELE | M42 | 2nd production validated at PRIELE |
| M.3.3. | 2nd production ok at Cern | CERN | M48 | 2nd production runs flawlessly in Atlas |
| M.2.5. | SLP1 ok at Caen | CAEN | M48 | SLP1-based FTK running flawlessly |
| M.7.1.- M.7.3. | Open Days results | AUTH | M8, M20, M32 | Verification of open day results – |
| M.7.4. – M.7.6. | Workshop days results | AUTH | M6, M18, M30 | Verification of workshop day results |
| M.7.7. – M.7.9. | Summer schools results | AUTH | M7, M19, M31 | Verification of summer school week results |
| M8.1. | ToK and training results | AUTH | M25 | Evaluation of ToK between participants and results of trainings - |

| Del. no. | Deliverable Title | Nature | Dissemination level | Delivery date |
|---|---|---|---|---|
| D.2.1. | VS infrastructure at CAEN for FTK demonstrator integration | R | RE | M6 |
| D.4.1. | FTK Demonstrator detailed simulation | R | RE | M9 |
| D.4.2. | Test Vectors for the FTK demonstrator | R | RE | M10 |
| D.2.2. | FTK demonstrator fully integrated with old power supply | Pub | PU | M12 |

| | | | | |
|---|---|---|---|---|
| D.1.1. | SLP2 prototype constructed at PRIELE | Pub | PU | M12 |
| D.6.1 | Test bench | R | RE | M12 |
| D.4.3. | Test Vectors for the SLP2 based FTK | R | RE | M16 |
| D.2.3. | CAEN power supply ready for integration | R | RE | M18 |
| D.2.4. | FTK cooling and mechanical tests completed | R | RE | M20 |
| D.2.5 | SLP2 fully integrated | Pub | PU | M20 |
| D.3.1. | FTK demonstrator commissioned | Pub | PU | M22 |
| D.6.2. | Standard characterization | R | RE | M24 |
| D.4.4. | Trigger table for demonstrator with performance prediction | Pub | PU | M25 |
| D.5.1. | Infrastructure at CAEN for Image Processing | R | RE | M26 |
| D.4.5 | SLP1 architecture simulation | Pub | PU | M28 |
| D.5.2. | Software & firmware ready for training and image processing | R | RE | M30 |
| D.1.2. | 1st FTK production assembled at PRIELE | R | RE | M32 |
| D.3.2. | FTK first production commissioned | Pub | PU | M34 |
| D.5.3. | Performances of natural still image processing | Pub | PU | M34 |
| D.6.3. | Optimized power supplies and their characterization | Pub | PU | M34 |
| D.1.3. | SLP1 prototype constructed at PRIELE | Pub | PU | M36 |
| D.4.6. | SLP1 detailed simulation | R | RE | M38 |
| D.5.4. | Results of tests on movie processing | Pub | PU | M40 |
| D.4.7. | Test Vectors for the SLP1 based FTK | R | RE | M42 |
| D.1.4. | 2nd FTK production assembled at PRIELE | R | RE | M42 |
| D.3.3. | FTK second production commissioned | Pub | PU | M46 |
| D.2.6 | SLP1 fully integrated | Pub | PU | M48 |
| D.5.5. | Results of tests on medical image processing | Pub | PU | M48 |
| D.7.1. | IAPP project open days | R | PU | M7, M19, M31, M43 |
| D.7.2. | Workshop days | R | PU | M5, M17, M29, M41 |
| D.7.3. | Summer school weeks | R | PU | M6, M18, M30, M42 |
| D.7.4 D.8.3 | World wide web site for dissemination | R | PU | M6, M18, M30, M48 |
| D.8.1. | FTK Workshops | R | RE | M1, M13, M30, M46 |
| D.8.2. | Trainings | R | RE | M1, M5, M9, M19, M29, M47 |

# B.4.4. Management structure, organisation and procedures

## B.4.4.1. Network organization and management structure

**- Organization of the network (task delegation, reporting)**

Progress reports, Mid-term report, periodic reports and final report is responsibility of the coordinator. They will be based on the WP reports. The financial statements (Form C) and the certificate on the finantial statements are responsibility of both the coordinator and the participants. The coordinator will delegate to an external person the preparation of documents necessary for financial reports and production of mandatory certificates.

**- Supervisory board composition, function and competences. Rules for internal co-ordination, monitoring and reporting**

The management scheme of the network consists of two boards: the Steering Committee that will be primarily responsible for the financial and administrative aspects of the network and the Scientific Board that will be in charge of the scientific operation of the network, the implementation of the training program and the recruitment processes in consultation of the Steering committee.

o Steering committee (SC): it will be responsible of the financial management of the project and the dissemination issues. They will play a consultant role in the selection of the network researchers. One member of the Steering committee will be appointed as gender officer. The gender officer will also be present during the selection procedure of the researchers. Each partner will appoint their representative to the SC who will be chosen to have a longstanding experience and international reputation in leading research teams and multi-institute projects, in order to guarantee the smooth operation of the network. The seconded/recruited researchers will also appoint their representative to the SC.

o Scientific Board (SB): the Scientific Board will (a) ensure the implementation of the network's scientific and training program, (b) monitor the progress of the research teams, (c) ensure good communication and exchange of information among the teams (d) be responsible for the recruitment process in consultation with the SC. The composition of the SB will consist of the representative of each participant institution, the work package managers (see below) and the seconded/recruited researchers' representative.

o Work Package managers: for the implementation of the milestones and deliverables of each WP, one manager per WP is appointed.

The Steering committee and the Scientific Board will be chaired by the project coordinator and both will vote for a deputy coordinator.

**- Rules for effective decision making including contingency planning**

We will follow the working plan description with its deliveries and milestones and risk analysis. Any deviation with that should be discussed with Atlas, to generate a proposal to be submitted to REA. The proposal will be discussed and voted by the SB before going to REA.

**- Methods and tools for effective network communication**

We will create and maintain a dedicated webpage also for the ongoing research. All our meetings will use the Indico software. Secure access to both the webpage and the Indico pages is guaranteed. In addition, the communication among the partners is assured through telephone-conferences, videoconferences and a dedicated e-mailing list. All these tools will be extensively used throughout the execution of the project. The communication among the members of the partner institutes will be further enhanced during the various workshops and tutorials, which will bring together many experts from different institutes. Once per year, a conference-like meeting will take place with a wide participation of the network partners and presentations of latest results. The seconded/recruited researchers of the network will be especially encouraged to contribute in the organization of these events.

**- Meeting calendar for management including mid-term review**

The Steering committee will meet twice per year (M5 and M11 of each year) to deal with administrative issues of the project. The SB will meet regularly every four months (M3, M7, M11 of each year) to assess the progress in the research and training aspects of the project and communicate the results of the closed sessions to all members of the network. The SB will submit a report on project progress to the SC, after each SB official meeting (each 4 months). The meetings on M11 of each year will be important to prepare the report to the REA.

The WP managers will report regularly to the SB on the progress of the project paying special care to match milestones and deliverables. A written report will be provided to the coordinator one month in advance of each due report to the REA.

**According to the Special Clause 5 bis of Article 7 of the Grant Agreement, a mid-term review meeting must be organised, preferably during month 20-22 of the project. The venue and organisation of this meeting will be of the responsibility of the coordinator, and the timing and location of the meeting must be agreed with the REA project officer.**

**B.4.4.2. Financial management**
All the categories have a clear expenditure path, well defined by the list of secondments and recruitments and by "The Marie Curie Actions FP7 Financial Guidelines".
Each participant will provide the expenditure details to the coordinator one month in advance of each financial report.

**B.4.4.3. Recruitment strategy**
The recruitment of the ERs will follow the European Charter for researchers and the Code of Conduct for their Recruitment. The posts will be widely advertised to the international scientific community via scientific magazines and websites, including compulsory publication on Euraxess. The positions profile are already established within the network by the project very well defined needs and will be centrally advertised. .
The curriculum vitas of the candidates will be circulated to all members of the Institute Board and a short list will be drawn based on their input. The short- listed candidates will be invited for an interview either to the host institute or to CERN, whichever is less costly. We will try to group the interviews when possible, to minimize traveling costs, or perform them via telephone conferencing.

**B.4.4.4. Gender aspects**
One member of the *Steering committee* will be appointed as gender officer. The gender officer will also be present during the selection procedure of the researchers to reach a recruitment target of 40% women researchers in the project.
The consortium will include in the agreement a Gender Action Plan to achieve gender balance within the workforce, to monitor the working conditions, to raise the gender awareness, to promote women in science. In particular we plan to obtain: (a) family friendly working conditions; (b) female speakers at the project training events, workshops, conferences; (c) specific invitations to female students to visit the FTK laboratories; (d) network with CERN women organization.

**B.4.4.5. Intellectual property**
IPR strategy will be in line with grant agreement provisions.
Publication policy will follow the FTK and Atlas rules: each publication on specific piece of hardware or software will be signed by people that worked on the content of the publication and their supervisors, while results on integrated systems will be signed by the whole FTK collaboration. Publications with Atlas data will be signed by the Atlas collaboration.

***B.4.4.6. Subcontracting (if applicable)***
*Not applicable*

***B.4.4.7. Third parties (other than subcontractors) (if applicable)***
*Not applicable*

***B.4.4.8. Small Equipment for SMEs (if applicable)***
*Not applicable*

# B.5 Impact

## B.5.1. Impact towards the policy objectives of the programme

**The expected results of the project how to assess them. -** We expect applications in all the fields where a huge computing power is necessary for fast real time results. Examples are astrophysical and meteorological calculations, robotic automation, or security applications, but our first expectation is innovation of the LHC experiments data taking and a widening of the physics possibilities in future collider experiments. Real-time analysis (few microseconds latency) of complex events is emerging in a field where large farms of CPUs have been believed the only solution.

For what concerns more closely the hardware, we expect a new prototype of the SLP, reliable, capable of supporting even the first level latency of selection at ATLAS and other experiments. The processor will have a modular, expandable and configurable structure. To be effectively used at its best, the power of SLP must be accompanied by a I/O architecture adequate to the huge flow of real-time data. Serial connections are a relevant item to this project offering bandwidths of 10 Gb/s. The expected results are the validation of algorithms aware of the internal structure of the device, and able to increase by orders of magnitude the overall reliability of the circuits. However, even with the use of highest speed serial channels, the I/O poses severe limitations to the overall performance of SLP in applications with high data flow, such as those on the pixel detectors of new generation. An expected result is the validation of highly parallelized implementations of cluster-finding and adaptive algorithms to reduce in a smart way the amount of data to be transferred (FTK_IM). As far as the adaptive algorithms are concerned, those adopted by the visual system and then optimized by the natural evolution, are expected to have the best performances. For Phase II at LHC we should transfer the algorithms inside the detector itself, an "intelligent" experimental apparatus.

An expected important result is in the field of vision: the capability to automatically analyze (without external supervision) static natural images and movies in real time, extracting highly compressed (over 95%) representations but still full of all the salient features of the original image. Such a device is important for the validation of the algorithm and to prove its effective chance of implementation. In fact, models are in general accurate and elegant, yet very hard to implement. The realization would allow automatic real time analysis of artificial images such as x-rays or satellite images. Without requiring expert supervision, our algorithm allows for an automatic tuning and continuous adaptation. These studies will provide inputs to (a) researchers that aim to understand neural mechanisms involved in early stages of visual analysis in humans; (b) to better understand nature and function of human physiology, giving a boost to this field.

**Immediate and longer term benefits of the proposed collaboration - how the project/programme will foster new collaborations and how the proposed collaboration might continue beyond the lifetime *of the project.* -** The FTK project exists since 1998 with no contacts or collaborations with the commercial sector. This European project gives the academia sector the capability to meet for the first time with the commercial one, building a new team with complementary expertises able to optimize and to bring to production and commissioning our FTK processor first and more complex evolutions after. We will export the technology in new more challenging directions. The use of AM for level 1 muon selections will be faced already during our project. This effort can be used for the more challenging task of full tracking at level 1, an item to which CMS and LHCb are thinking already today.

**Contribution to the career prospects and employability of the researchers**

The training will be performed in the framework of the development of an advanced technological system. The researchers in the FTK project will have the opportunity to be trained in UniPisa, AUTH and CERN in a peak technology subject, cooperating in a multinational environment. In parallel, they will get the satisfaction to watch part of their individual effort to become a prototype, in the advanced production environments of PRIELE and CAEN, to be commissioned at CERN, to become a product to be used in other Detectors all over the world. Having about 500 institutions, active partners around the world, CERN provides momentum to the training and qualifications offered that none can doubt about. Industry will have a key role in training, providing qualitative training to the researchers dealing with applied techniques and practices, creating preconditions to acquire someone advanced skills and unique experience. Researchers have the opportunity to experience working in industry and they will gain a better insight with regard to their potential career paths. Moreover our SMEs show a large variety of

ongoing projects outside HEP, many of them funded by FP7. This is a very interesting source of trainings for the Academia researchers, an important stimulus to create spinoff. For this reason we decided to dedicate some trainings on the SME experience on their research outside HEP.
Organization and continuous discussions are the bases of the high research productivity of the relatively small, but excellent research groups participating to the network. Each member has individual responsibilities and is required to discuss its work weekly with the rest of the correlated group. Seminars in front of the whole scientific community of each institute are periodically required, a strong stimulus to acquire clarity, independence, management capability, and presentation skills. We care to provide a stimulus to improve "leadership capability". Presentations at conferences are strongly encouraged. All the participating institutions are intellectually very active and offer seminars and possible interactions on a wide range of topics in high energy physics, technological areas related to the experiments/accelerators, and also in totally different fields. The fellow work will have the opportunity to be presented to a large and international scientific community. Independence and management capabilities are strongly encouraged and rewarded.
The ERs and ESRs will have a personal supervisor, with whom they will establish a career development plan, followed up, discussed and updated regularly. Given the healthy participation at each institute in the network of the experienced staff, good supervision is guaranteed. The progress of ERs will be followed closely and the supervisor, in the spirit of maximizing their career prospects, will make suggestions/corrections. They will be strongly advised to take an active role in training and outreach activities. A 6 month planning of their work is foreseen and a yearly report to the institute on their progress will be given. The supervisor on the basis of the importance of their scientific results, will advise on the ERs participation in workshops and conferences. High priority will be given to ERs presentations within the network, in collaboration meetings and international conferences.

## B.5.2. Plans for exploitation of results and Dissemination strategy

**Strategy for the dissemination and exploitation / commercialisation of the results**

The outcome of the dissemination could provide new applications and new research activities, that will also reinforce our team. Some examples are listed here:

(a) LHC experiments: we continuously disseminate our developments in workshops, conferences, publications, proposals, fighting to let understand people the importance of our new computing technology.

(b) If processing of static images and movies by our associative memory will be successful, we will look for possible applications, in addition to medical applications already mentioned: (1) Satellite or video-camera real-time image processing to diagnose possible accidents or dangerous situations in critical positions, continuously monitored. The processor, attached to the video-camera could be able to recognize immediately a movement or a change in the image and set an alarm. We plan to understand the possible applications as real time alarm. (3) Programs searching a large database to recognize features like for example faces or monuments are today quite slow. Providing the compression of information offered by the AM to all data base images, would make these programs much faster. We will discuss our results with researchers working in this field to look for their interest.

**Industrial or commercial routes envisaged for the exploitation of the results by the commercial sector participants.** - PRIELE and CAEN will gain an important role not only for the production and commissioning of FTK in Atlas, but also for the possible following evolutions. Both the two SMEs will have the opportunity to become the main places where assembly and preliminary tests will be performed for future productions, they will be also able to produce firmware and test procedures, and the maintenance of the hardware (a lot of boards if there will be the transition from Level 2 to Level 1 full tracking). WP6 opens also a new opportunity for CAEN, if its power supplies will be easily adapted to silicon detectors in future SLHC applications.
As required by the grant agreement Annex II, the coordinator will ensure that all publications and presentations by members of the project - including all funded fellows - acknowledge the EU financial support received. This acknowledgement should specifically refer to the Marie Curie Industry-Academia Pathways and Partnerships (IAPP) action, as well as the project number and acronym.

## B.5.3. Outreach activities

WP7 and 8 are dedicated to outreach, transfer of knowledge and training activities. We plan one annual occasion for each of the listed corresponding deliveries:

**IAPP project open day**: the FTK labs will be open to the public to show the racks, crates, boards and chips developed by the collaboration. Teachers (the fellows in particular) in front of posters in the lab will describe the importance of the real time analysis performed on FPGAs (a new type of computing) to make sophisticated decisions in few microseconds, for HEP experiment triggers as well as for other applications outside HEP. We will describe the programmable logic power based on real time parallel computing and the importance of "pipelining" and "parallelism" with examples as being the key features of our computing model. Simple CAD stations (Xilinx and Altera systems) will be provided to visitors to develop their own simple logic. Logic examples already done will be provided for people interested only in the implementation inside the chip, not in the logic development. The goal is to show them how easy and powerful the use of these tools is.

**FTK Workshop day**: a set of seminars and lectures will be provided to university students on trigger for HEP experiments and FPGA applications outside HEP. This will be also the occasion to announce the Summer school week plan for the year. Few students will be allowed to spend a week during summer in one of the partner laboratory, in particular at CERN.

Finally **Trainings and FTK Workshops** will be activities devoted to our collaboration.

Each institution will offer some trainings to the community:

**UniPisa:** "The AM system". As the opening event of the network, a set of seminars will be given on (a) global architecture and data rate problems, (b) specific logic and existing boards analysis, (c) AM chip status and future evolution, (d) existing tests, laboratory tools and test stands, (e) knowledge of the collaboration (f) career opportunities and importance of managerial skills inside the FTK project. This is also a nice occasion to meet all together at the very beginning (kickoff workshop followed by a more detailed kickoff training).

**PRIELE: "**PRIELE project overview ". PRIELE trainings are based on its experience. It is specialized on (1) intelligent sensor wireless networks and innovative products for condition based maintenance in industrial and maritime environments; (b) embedded devices for data collection, analysis and data acquisition software with Novelty detection algorithms; (c) signal analysis algorithms for embedded devices, self learning algorithms, power autonomous systems with micro generators and organic photovoltaic; (d) optical sensors connected to wireless networks and implementation of new transmission and communication protocols.

**CAEN** trainings: "Silicon Photomultiplier read out ", **"**past experience at LHC" and "overview of EU projects at CAEN".

**CNRS: "**Experience on silicon detectors: evolution from LHC to SLHC" with visit to the lab and learning to work in clean rooms

**CERN:** "Technology: (a) CERN practical experience for the development of high density electronics boards, (b) kow-how for quality assurance practices in board manufacturing", with visit to the TE-MPE-EM infrastructures.

**AUTH,** based on the experience of the electronics division, will offer these trainings: (a) a training on FPGA technology and its applications with topics such as "Embedded System Design Using FPGA Technology", "VHDL Verification Techniques" and "Design Exploiting FPGA Resources". The training will include laboratory sessions using the existing equipment of the electronics division, such as training FPGA boards and design suites; (b) a training on "Machine Vision Implementations for Lab-On-Chip applications". The electronics division plans also to present the FTK project in an International Workshop organized by the group in Thessaloniki on Modern Circuits and Systems Technologies.

We will introduce an exercise with AMs in the yearly winter school ISOTDAQ (International School on Trigger and DAQ), to diffuse the technology to young researchers in our field

# B.6 Ethics

The Beneficiaries accept to uphold the highest standards of scientific integrity and ethical conduct during the implementation of the grant agreement.

# PART C:

## Overall indicative project deliverables

| | Recruitments | | | | | | Secondments | | | | | | | | | Total |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Experienced researchers (<10) | | | Experienced researchers (>10) | | | Early stage researchers | | | Experienced researchers (<10) | | | Experienced researchers (>10) | | | |
| | Months | Researchers | % Fixed amount contract (1) | Months | Researchers | % Fixed amount contract (1) | Months | Researchers | % Fixed amount contract (1) | Months | Researchers | % Fixed amount contract (1) | Months | Researchers | % Fixed amount contract (1) | Months |
| UniPisa | 38 | 2 | 0% | 0 | 0 | 0% | 2 | 1 | 0% | 8 | 2 | 0% | 0 | 0 | 0% | 48 |
| CAEN | 0 | 0 | 0% | 0 | 0 | 0% | 6 | 1 | 0% | 17 | 3 | 33% | 28 | 4 | 100% | 51 |
| CERN | 12 | 1 | 0% | 0 | 0 | 0% | 2 | 1 | 0% | 0 | 0 | 0% | 6 | 1 | 100% | 20 |
| AUTH | 24 | 1 | 0% | 0 | 0 | 0% | 0 | 0 | 0% | 6 | 3 | 0% | 0 | 0 | 0% | 30 |
| PRIELE | 0 | 0 | 0% | 0 | 0 | 0% | 0 | 0 | 0% | 8 | 2 | 0% | 6 | 2 | 100% | 14 |
| CNRS | 0 | 0 | 0% | 12 | 1 | 0% | 0 | 0 | 0% | 0 | 0 | 0% | 0 | 0 | 0% | 12 |
| Total | 74 | 4 | 0% | 12 | 1 | 0% | 10 | 3 | 0% | 39 | 10 | 10% | 40 | 7 | 100% | 175 |

# PART D:

## Overall maximum EU contribution

| | Living allowance(1) | Mobility allowance(2) | Contribution to training expenses of eligible researchers and research/transfer of knowledge programme expenses (3) | Management activities (including audit certification) (4) | Contribution to overheads (5) | Other types of eligible expenses / specific conditions (6) | Total |
|---|---|---|---|---|---|---|---|
| Year 1 | 288,488.17 | 45,981.55 | 108,000.00 | 54,470.00 | 49,693.97 | 0.00 | 546,633.69 |
| Year 2 | 294,776.49 | 48,658.60 | 117,000.00 | 56,830.00 | 51,726.51 | 0.00 | 568,991.60 |
| Year 3 | 178,523.58 | 31,382.48 | 64,800.00 | 33,800.00 | 30,850.61 | 0.00 | 339,356.67 |
| Year 4 | 73,880.63 | 14,018.38 | 25,200.00 | 13,900.94 | 12,699.99 | 0.00 | 139,699.94 |
| Total | 835,668.87 | 140,041.01 | 315,000.00 | 159,000.94 | 144,971.08 | 0.00 | 1,594,681.90 |

# Appendix 1 Gantt chart of recruitments and secondments per researcher

| [Hosting institution] [Recruiting institution] [Country] [Comm. sector Y/N] | [Sending institution] [Country] [Comm. sector Y/N] | Active in WP | Type | Total PM | Year 1 | | | | | | | | | | | | Year 2 | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 1 13 | 2 14 | 3 15 | 4 16 | 5 17 | 6 18 | 7 19 | 8 20 | 9 21 | 10 22 | 11 23 | 12 24 |
| [PRIELE], [Greece], [Y] | [UniPisa], [Italy], [N] | 1 | MER1 | 2 | | | | | | | 1 | 2 | | | | | | | | | | | | | | | | |
| [CAEN], [Italy], [Y] | [UniPisa], [Italy], [N] | 2 | MER1 | 16 | | | | | | | | | | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | | | | |
| [PRIELE], [Greece], [Y] | [UniPisa], [Italy], [N] | 1 | MER2 | 4 | | | | | | | | 1 | 2 | | | | | | | | | | | | | 3 | 4 |
| [PRIELE], [Greece], [Y] | [AUTH], [Greece], [N] | 1 | ER3 | 6 | | | | | 1 | 2 | | | | 3 | 4 | | | | | | | | | 5 | 6 | | | |
| [PRIELE], [Greece], [Y] | [AUTH], [Greece], [N] | 1 | ER4 | 2 | | | | | | | | | | | 3 | 4 | | | | | | | | | | | | |
| [CAEN], [Italy], [Y] | [AUTH], [Greece], [N] | 2 | ER4 | 4 | | | | 1 | 2 | | | | | | | | | | | 5 | 6 | | | | | | | |
| [UniPisa], [Italy], [N] | [PRIELE], [Greece],[Y] | 1 | ER5 | 2 | | | | | 1 | 2 | | | | | | | | | | | | | | | | | | |
| [AUTH], [Greece], [N] | [PRIELE], [Greece],[Y] | 1 | ER5 | 2 | | | | | | | | 3 | 4 | | | | | | | | | | | | | | | |
| [UniPisa], [Italy], [N] | [PRIELE], [Greece],[Y] | 1 | ER6 | 6 | | | 1 | 2 | | | | | | | | | | | | | | | | | | | | |
| [AUTH], [Greece], [N] | [PRIELE], [Greece],[Y] | 1 | ER6 | 2 | | | | | | | | | | | | | | | | | | | | | | 3 | 4 | |
| [AUTH], [Greece], [N] | [PRIELE], [Greece],[Y] | 1 | ER7 | 2 | | | | | | | | | | | | | | | | | | | | | | | | |
| [UniPisa], [Italy], [N] | [PRIELE], [Greece],[Y] | 1 | ESR8 | 2 | | | | | | | | | | | | | | 1 | 2 | | | | | | | | | |
| [CERN], [Switzerl.], [N] | [PRIELE], [Greece],[Y] | 3 | ESR8 | 2 | | | | | | | | | | | | | | | | | | 3 | 4 | | | | | |
| [AUTH], [Greece], [N] | | 1,3,4 | ER9 | 24 | | | | | | | | | | | | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |
| [CERN], [Switzerl.], [N] | | 1,3 | ER10 | 12 | | | | | | | | | | | | | | | | | | | | | | | | |
| [CAEN], [Italy], [Y] | [AUTH], [Greece], [N] | 2 | MER11 | 4 | | | | 1 | 2 | | | | | | | | | | | | | | | | | | | |
| [CAEN], [Italy], [Y] | [AUTH], [Greece], [N] | 2, 4 | MER12 | 4 | | | | | | | | | | | | | | | 1 | 2 | | | | | | | | |
| [CAEN], [Italy], [Y] | [AUTH], [Greece], [N] | 2, 4 | ESR13 | 6 | | | | | | | | | | | | | | | 1 | 2 | 3 | | | | | | | |
| [CAEN], [Italy], [Y] | [AUTH], [Greece], [N] | 2 | ER19 | 5 | | | | 1 | 2 | | | | | | | | | | 3 | 4 | 5 | | | | | | | |
| [CAEN], [Italy], [Y] | [CNRS], [France], [N] | 2 | ER14 | 8 | | | | | | | 1 | 2 | | | | 3 | 4 | | | | | | | 5 | 6 | | | |
| [CERN], [Switzerl.], [N] | [CAEN], [Italy], [Y] | 3 | MER14 | 6 | | | | | | | | | | | | | | | | | | 1 | 2 | | | | | |
| [UniPisa], [Italy], [N] | | 4 | ER15 | 20 | | | | | | | | | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| [UniPisa], [Italy], [N] | | 5 | ER16 | 18 | | | | | | | | | | | | | | | | | | | | | | | | |
| [CAEN], [Italy], [Y] | [CNRS], [France], [N] | 6 | MER17 | 4 | | | | | | | | 1 | 2 | | | | | | | | | | | | | | | |
| [CNRS], [France], [N] | | 6,2 | MER18 | 12 | | | | | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | | | | | | | |

| [Hosting institution] [Recruiting institution] [Country] [Comm. sector Y/N] | [Sending institution] [Country] [Comm. sector Y/N] | Active in WP | Type | Total PM | Year 3 | | | | | | | | | | | | Year 4 | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | 1 25 | 2 26 | 3 27 | 4 28 | 5 29 | 6 30 | 7 31 | 8 32 | 9 33 | 10 34 | 11 35 | 12 36 | 1 37 | 2 38 | 3 39 | 4 40 | 5 41 | 6 42 | 7 43 | 8 44 | 9 45 | 10 46 | 11 47 | 12 48 |
| [PRIELE], [Greece], [Y] | [UniPisa], [Italy], [N] | 1 | MER1 | 2 | | | | | | | | | | | | | | | | | | | | | | | | |
| [CAEN], [Italy], [Y] | [UniPisa], [Italy], [N] | 2 | MER1 | 16 | | | | | 14 | 15 | 16 | 17 | 18 | | | | | | | | | | | | | | | |
| [PRIELE], [Greece], [Y] | [UniPisa], [Italy], [N] | 1 | MER2 | 4 | | | | | | | | | | | | | | | | | | | | | | | | |
| [PRIELE], [Greece], [Y] | [AUTH], [Greece], [N] | 1 | ER3 | 6 | | | | | | | | | | | | | | | | | | | | | | | | |
| [PRIELE], [Greece], [Y] | [AUTH], [Greece], [N] | 1 | ER4 | 2 | | | | | | | | | | | | | | | | | | | | | | | | |
| [CAEN], [Italy], [Y] | [AUTH], [Greece], [N] | 2 | ER4 | 4 | | | | | | | | | | | | | | | | | | | | | | | | |
| [UniPisa], [Italy], [N] | [PRIELE], [Greece],[Y] | 1 | ER5 | 2 | | | | | | | | | | | | | | | | | | | | | | | | |
| [AUTH], [Greece], [N] | [PRIELE], [Greece],[Y] | 1 | ER5 | 2 | | | | | | | | | | | | | | | | | | | | | | | | |
| [UniPisa], [Italy], [N] | [PRIELE], [Greece],[Y] | 1 | ER6 | 6 | | 5 | 6 | | 7 | 8 | | | | | | | | | | | | | | | | | | |
| [AUTH], [Greece], [N] | [PRIELE], [Greece],[Y] | 1 | ER6 | 2 | | | | | | | | | | | | | | | | | | | | | | | | |
| [AUTH], [Greece], [N] | [PRIELE], [Greece],[Y] | 1 | ER7 | 2 | | | | | | | 1 | 2 | | | | | | | | | | | | | | | | |
| [UniPisa], [Italy], [N] | [PRIELE], [Greece],[Y] | 1 | ESR8 | 2 | | | | | | | | | | | | | | | | | | | | | | | | |
| [CERN], [Switzerl.], [N] | [PRIELE], [Greece],[Y] | 3 | ESR8 | 2 | | | | | | | | | | | | | | | | | | | | | | | | |
| [AUTH], [Greece], [N] | | 1,3,4 | ER9 | 24 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | | | | | | | | | | | | |
| [CERN], [Switzerl.], [N] | | 1,3 | ER10 | 12 | | | | | | | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | | | | | |
| [CAEN], [Italy], [Y] | [AUTH], [Greece], [N] | 2 | MER11 | 4 | | | | | | | | | | | | | | | 3 | 4 | | | | | | | | |
| [CAEN], [Italy], [Y] | [AUTH], [Greece], [N] | 2, 4 | MER12 | 4 | | | | | | | | | | | | | | | | | 3 | 4 | | | | | | |
| [CAEN], [Italy], [Y] | [AUTH], [Greece], [N] | 2, 4 | ESR13 | 6 | | | | | | | | | | | | | | 4 | 5 | 6 | | | | | | | | |
| [CAEN], [Italy], [Y] | [AUTH], [Greece], [N] | 2 | ER19 | 5 | | | | | | | | | | | | | | | | | | | | | | | | |
| [CAEN], [Italy], [Y] | [CNRS], [France], [N] | 2 | ER14 | 8 | | | | | | | | | | | | 7 | 8 | | | | | | | | | | | |
| [CERN], [Switzerl.], [N] | [CAEN], [Italy], [Y] | 3 | MER14 | 6 | | | | | | | | | 3 | 4 | | | | | | | | | 5 | 6 | | | | |
| [UniPisa], [Italy], [N] | | 4 | ER15 | 20 | 16 | 17 | 18 | 19 | 20 | | | | | | | | | | | | | | | | | | | |
| [UniPisa], [Italy], [N] | | 5 | ER16 | 18 | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | | | | | |
| [CAEN], [Italy], [Y] | [CNRS], [France], [N] | 6 | MER17 | 4 | | | | | | | 3 | 4 | | | | | | | | | | | | | | | | |
| [CNRS], [France], [N] | | 6,2 | MER18 | 12 | | | | | | | | | | | | | | | | | | | | | | | | |

| | Person.months | % |
|---|---|---|
| **Total nr of secondments** | 89 | 51% |
| Inter-sectorial secondments | 89 | 51% |
| Intra-national secondments | 30 | 17% |
| **Total nr of recruitments** | 86 | 49% |
| **Total nr of secondments + recruitments** | 175 | 100% |

# Appendix 2: Extract from the 2012 PEOPLE Work Programme

## Structure of the cost categories applicable for IAPP (adapted from Table 3.1 and 3.3 of the WP)

This information does not substitute the relevant information of the 2012 People Work Programme, which should be consulted for further details.

| **1**<br>**Monthly living allowance** | **2**<br>**Monthly mobility allowance** | **3**<br>**Contribution to the training expenses of eligible researchers and research/transfer of knowledge programme expenses** | **4**<br>**Management activities (including audit certification if applicable)** | **5**<br>**Contribution to overheads** | **5**<br>**Other types of eligible expenses / specific conditions** |
|---|---|---|---|---|---|
| Flat rate of :<br><br>38 000 Euro/year for ESRs<br>58 500 Euro/year for ERs and<br>87 500 Euro/year for MERs<br><br>Rate for individual countries is obtained by applying the correction coefficients listed in Table 3.2 of the WP. | Flat rate allowance to cover expenses linked to the personal household, relocation and travel expenses of the researcher and her/his family in the host country: reference rate of EUR 700 for researchers without a family and EUR 1000 for researchers with a family.<br><br>Rate for individual countries is obtained by applying the correction coefficients listed in Table 3.2 of the WP. | Flat rate of EUR 1800 per researcher-month managed by the host organisations to contribute for expenses related to the participation of researchers to training activities; expenses related to research costs; execution of the training/partnership project and contribution to the expenses related to the co-ordination between participants. | Maximum of 10% of the total EU contribution. | 10% of direct costs except for subcontractors and the costs of the resources made available by third parties which are not used in the premises of the beneficiary. | **Applicable for participating SMEs only**:<br>Small equipment expenses up to a maximum of 10% of the total contribution to the SME participant, if: duly justified for the project, on the basis of real costs and after prior agreement by the REA. |

**EU27 and Associated Countries correction coefficients (adapted from Table 3.2 of the WP)**

For other countries (such as ICPC and third countries), please consult the WP.

| | |
|---|---|
| Austria | 106.2 |
| Belgium | 100.0 |
| Bulgaria | 62.7 |
| Cyprus | 83.7 |
| Czech Republic | 84.2 |
| Denmark | 134.1 |
| Estonia | 75.6 |
| Finland | 119.4 |

| | |
|---|---|
| France | 116.1 |
| Germany | 94.8 |
| Greece | 94.8 |
| Hungary | 79.2 |
| Ireland | 109.1 |
| Italy | 106.6 |
| Latvia | 74.3 |
| Lithuania | 72.5 |

| | |
|---|---|
| Luxembourg | 100 |
| Malta | 82.2 |
| Netherlands | 104.1 |
| Poland | 77.1 |
| Portugal | 85.0 |
| Romania | 69.5 |
| Slovak Rep. | 80.0 |
| Slovenia | 89.6 |

| | |
|---|---|
| Spain | 97.7 |
| Sweden | 118.6 |
| UK | 134.4 |

| | |
|---|---|
| Albania | 66.7 |
| Bosnia & Herz. | 68.1 |
| Croatia | 81.8 |
| FYROM | 60.6 |
| Iceland | 79.9 |
| Israel | 96.4 |
| Liechtenstein | 109.9 |
| Moldova | 60.5 |

| | |
|---|---|
| Montenegro | 64.6 |
| Norway | 130.7 |
| Serbia | 74.0 |
| Switzerland | 109.9 |
| The Faroes | 134.1 |
| Turkey | 97.7 |