Europe's top priority should be the exploitation of the full potential of the LHC, including the high-luminosity upgrade of the machine and detectors with a view to collecting ten times more data than in the initial design, by around 2030

https://indico.cern.ch/getFile.py/access?resId=0&materialId=0&confId=217656

The challenge to upgrade LHC experiments

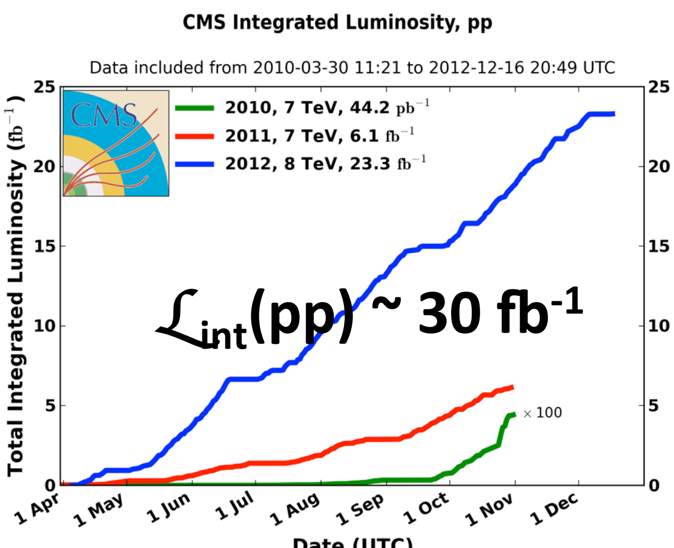
Nadia Pastrone

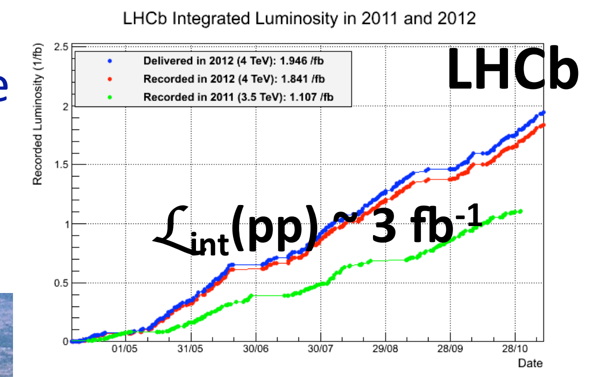
INFN Torino

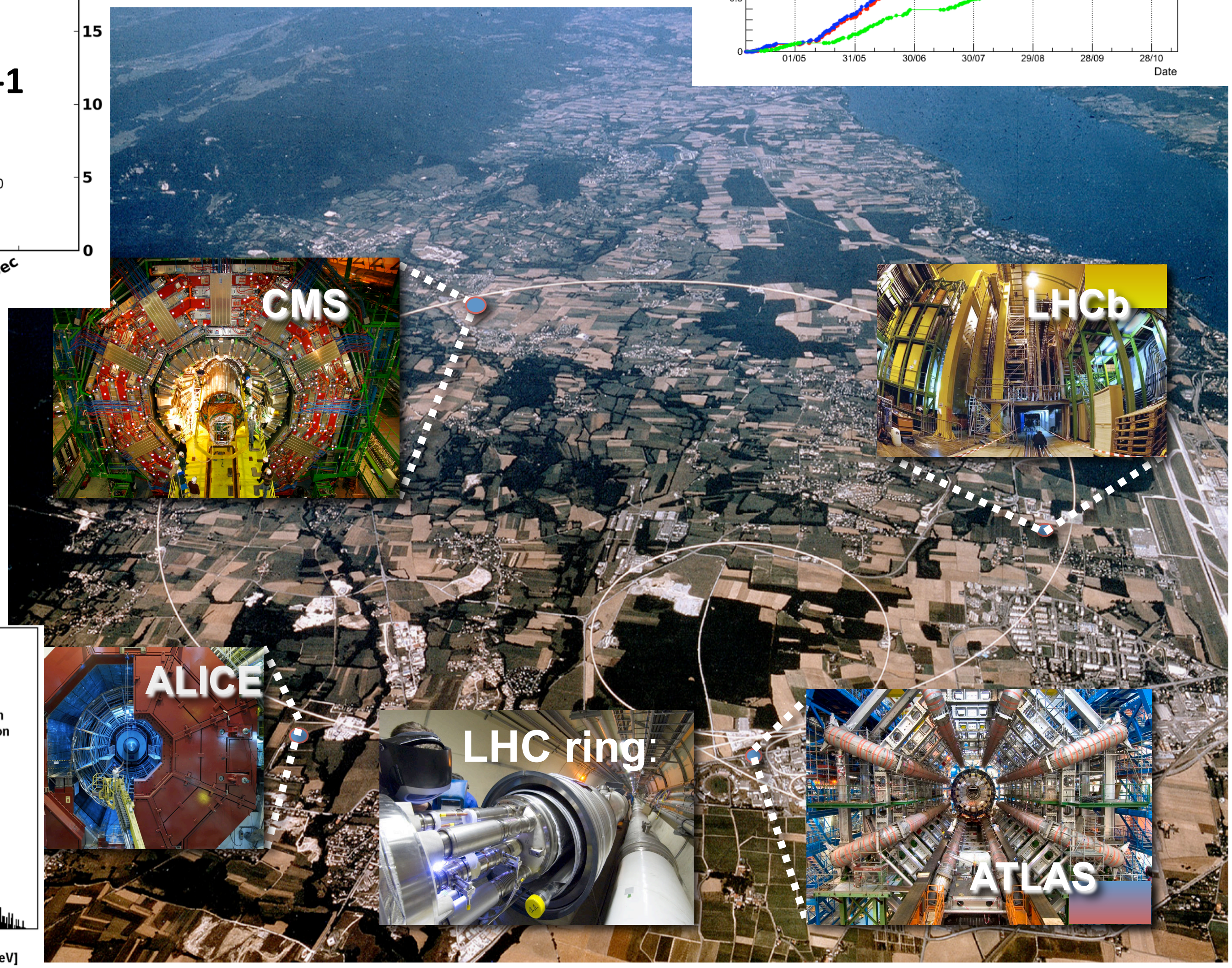
Cagliari – 3 aprile 2013

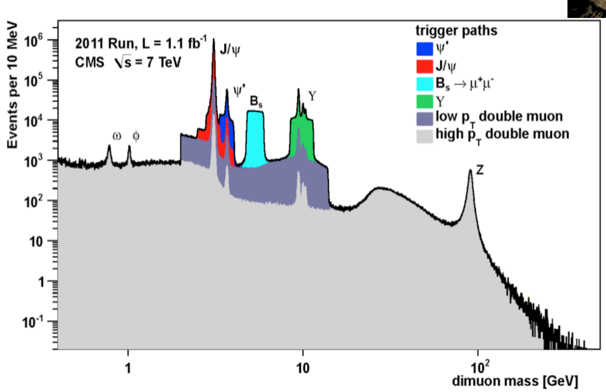
Run 1 @ LHC

- ✓ **Great results** *(A. Nisati)*
- ✓ Outstanding performance
- ✓ Problems overcome
- ✓ **Ready for upgrade**

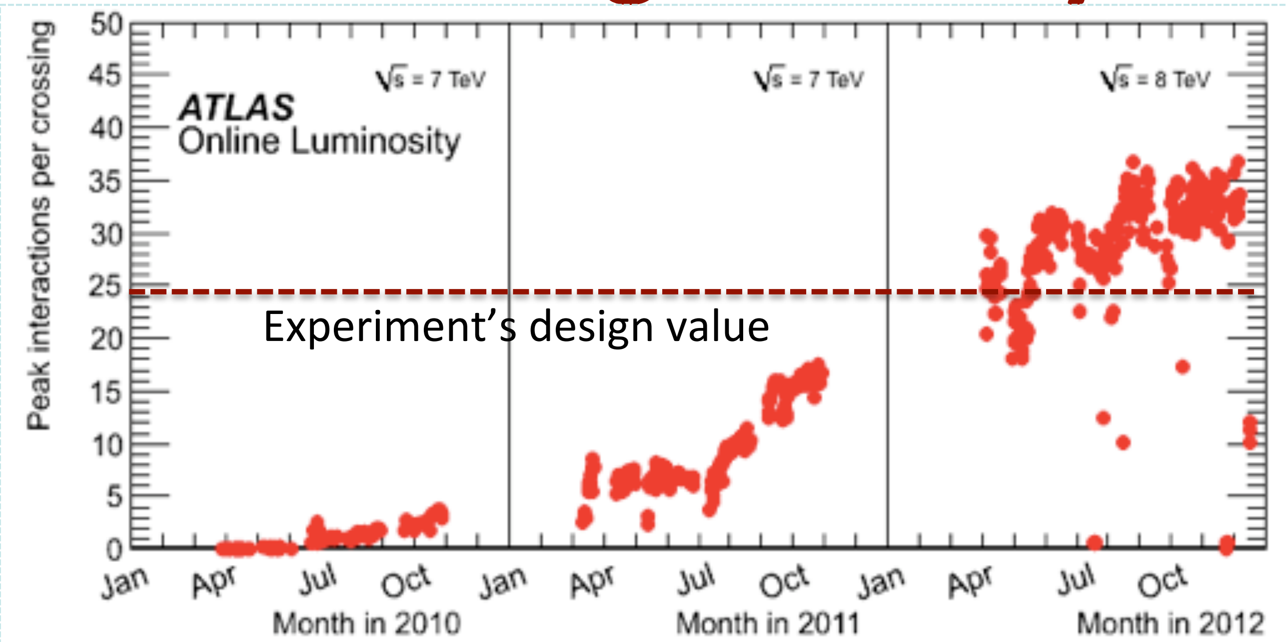




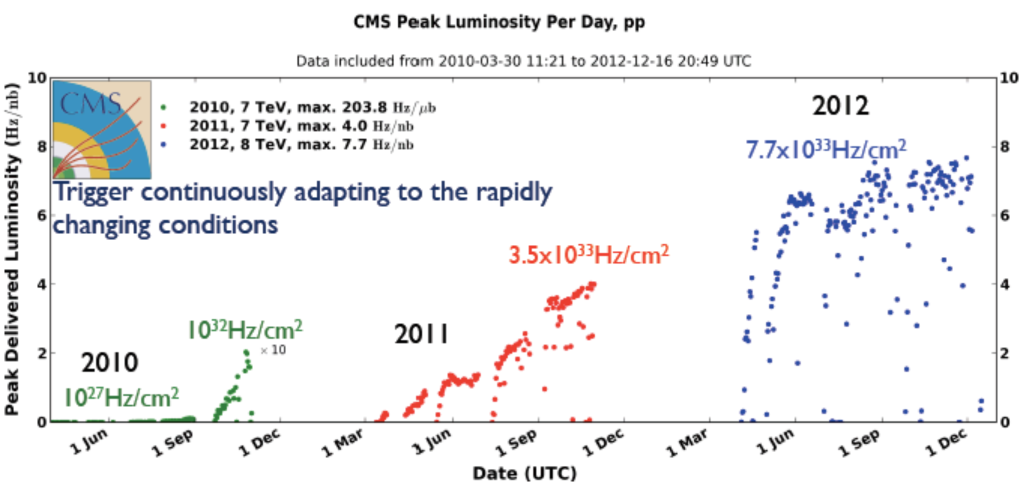




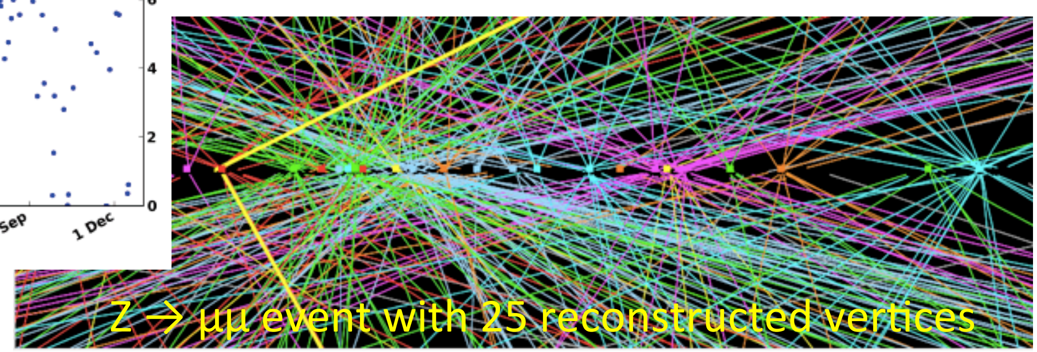
The challenge already started in 2012



50 ns bunch crossing
<PU> ~ 21 @ 2012



Design value: 25 pile-up events at luminosity 10^{34}cm^{-2} s^{-1} and 25 ns bunch spacing



Projected performance to LS3

Total $\mathcal{L}_{int}$(pp) before LS3:

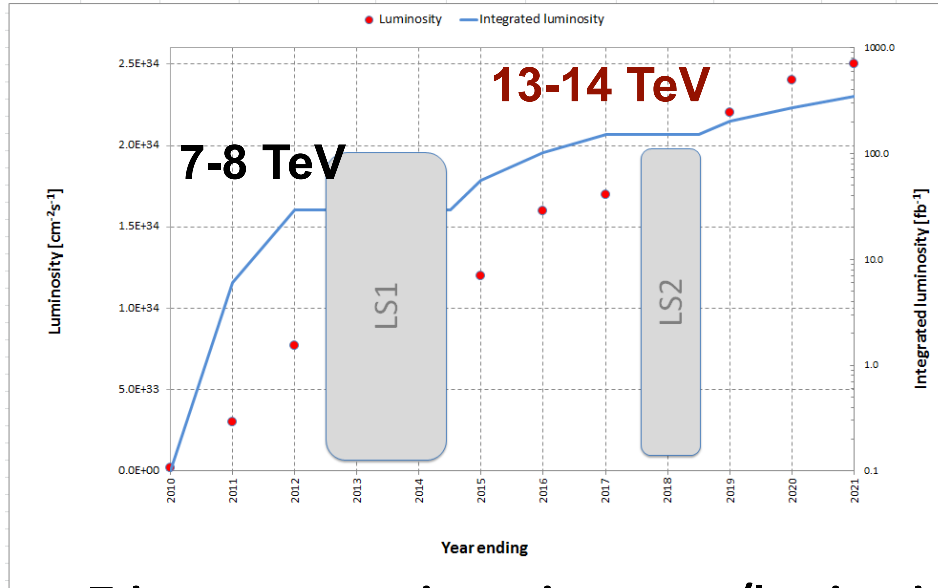
300 – 500 fb^{-1}

$\mathcal{L}_{max}$(pp) ~ 2.5 10^{34} Hz/cm^2

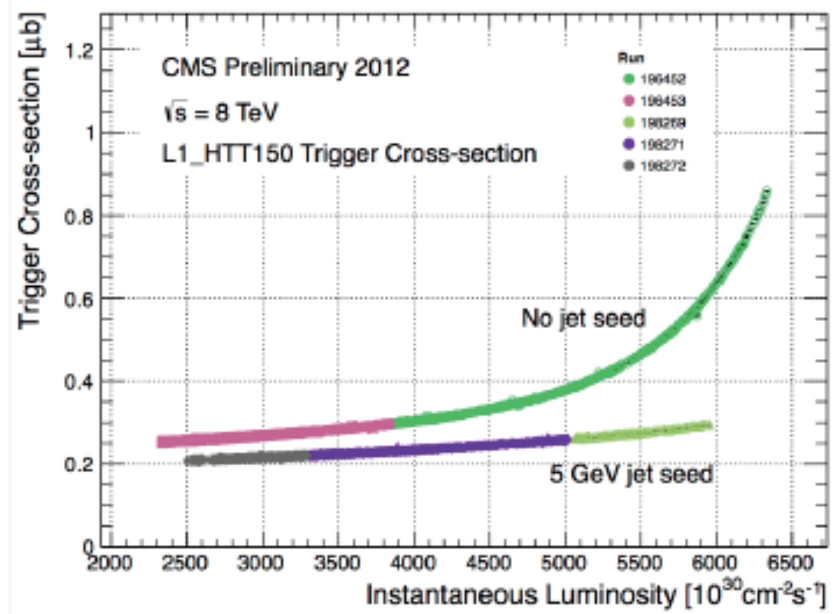
GOAL after LS3:

Total $\mathcal{L}_{int}$(pp) **3000 fb^{-1}**

$\mathcal{L}_{level}$(pp) ~ 5 10^{34} Hz/cm^2



Trigger crosssection=trigger rate/luminosity



$\mathcal{L}$ (therefore <PU>) increase affects L1 trigger efficiency

→ **TRIGGER UPGRADE**

Needed:

HIGH GRANULARITY DETECTORS

with rad-hard components

Parameters used to design upgrade

LHC up to 2021

		safer value
Peak Luminosity expected	$2 * 10^{34}$	$3 * 10^{34}$
Integrated Luminosity expected	$300\ fb^{-1}$	$400\ fb^{-1}$
μ = mean number of interactions per crossing (25nsec)	55 *	80
Safety factor to be used in the dose rate and integrated dose calculations	2?	2?

HL-LHC after 2022

		safer value
Peak Luminosity expected	$5 * 10^{34}$	$7 * 10^{34}$
Integrated Luminosity expected	$2500\ fb^{-1}$	$3000\ fb^{-1}$
Int. Luminosity per year expected	$250\ fb^{-1}$	$300\ fb^{-1}$
μ = mean number of interactions per crossing (25 nsec)	140 *	200
Safety factor to be used in the dose rate and integrated dose calculations	2?	2?

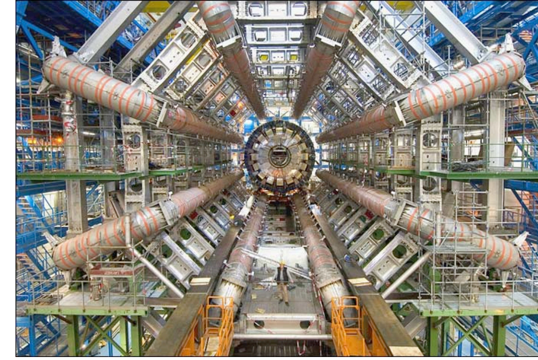
Plan integrated dose figures based on this

μ values going with the peak luminosity (25ns beam crossing)

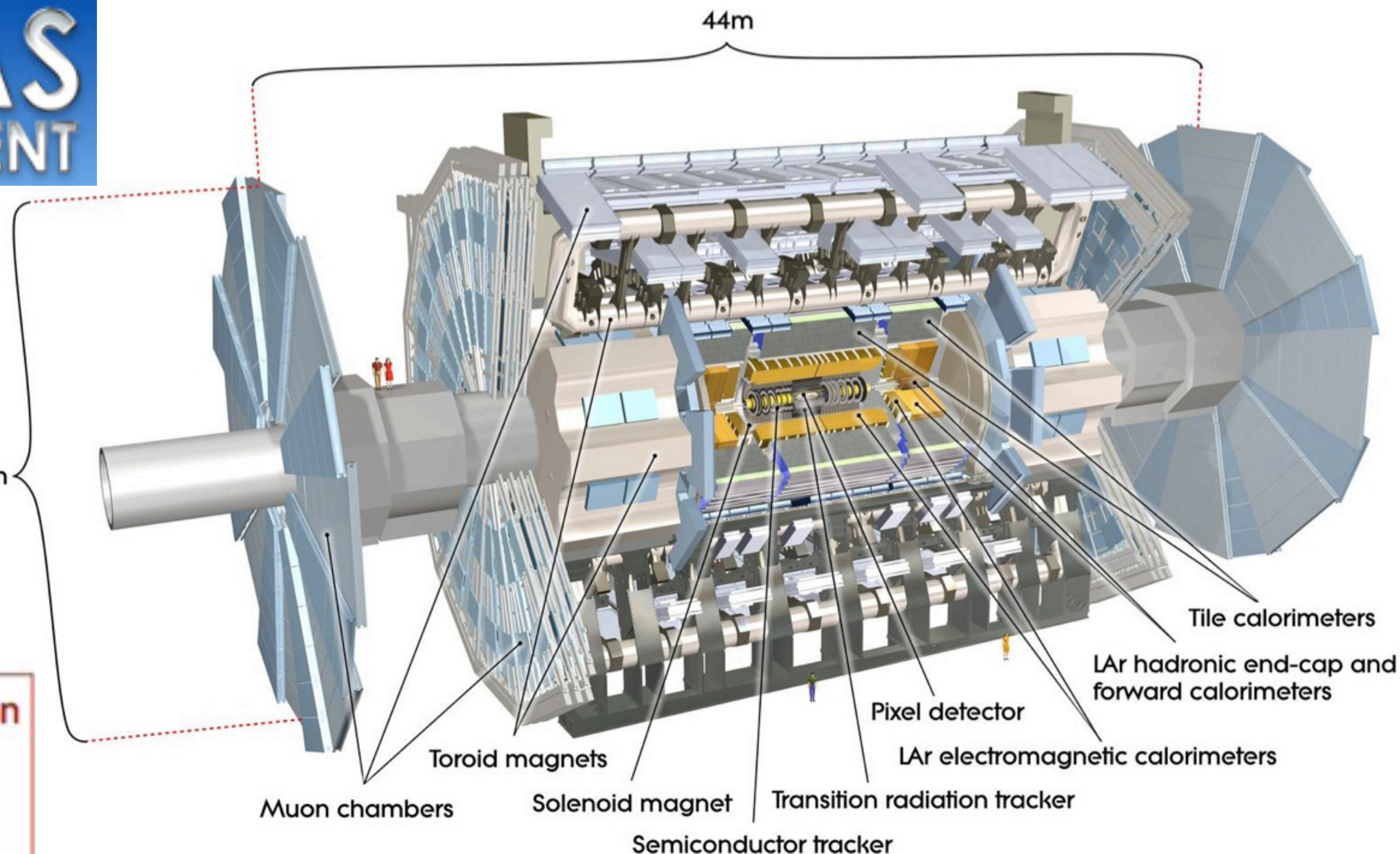
the radiation hardness of components which can be reliably tested for post-irradiation performance (eg ASICs, silicon sensors, diamond, ...) apply this safety factor to the dose calculations in setting the radiation survival specification

Multi-purpose, high resolution and hermetic detector

Magnets:	Central Solenoid + 3 Toroids
Tracking:	Silicon, Transition Radiation Tracker
Calorimeter:	EM (LAr), Had Cal
Muon:	Trigger + Precision chambers



ATLAS EXPERIMENT



Object Reconstruction

- leptons (e, μ, τ)
- photons
- jets
- b-jets
- Etmiss

Prepare for: Phase 0,I | Phase I,II | Phase II

"Phase-0" upgrade: consolidation
$\sqrt{s}$ = 13~14 TeV, 25ns bunch spacing
$L_{inst} \simeq 1 \times 10^{34}$ $cm^{-2}s^{-1}$ ($\mu \simeq 27.5$)
$\int L_{inst} \simeq 50$ fb^{-1}

"Phase-I" upgrades:
ultimate luminosity
$L_{inst} \simeq 2\text{-}3 \times 10^{34}$ $cm^{-2}s^{-1}$ ($\mu \simeq 55\text{-}81$)
$\int L_{inst} \gtrsim 350$ fb^{-1}

"Phase-II" upgrades:
$L_{inst} \simeq 5 \times 10^{34}$ $cm^{-2}s^{-1}$ ($\mu \simeq 140$) w. leveling
$\simeq 6\text{-}7 \times 10^{34}$ $cm^{-2}s^{-1}$ ($\mu \simeq 192$) no level.
$\int L_{inst} \simeq 3000$ fb^{-1}

ATLAS has devised a 3 stage upgrade program to optimize the physics reach at each Phase

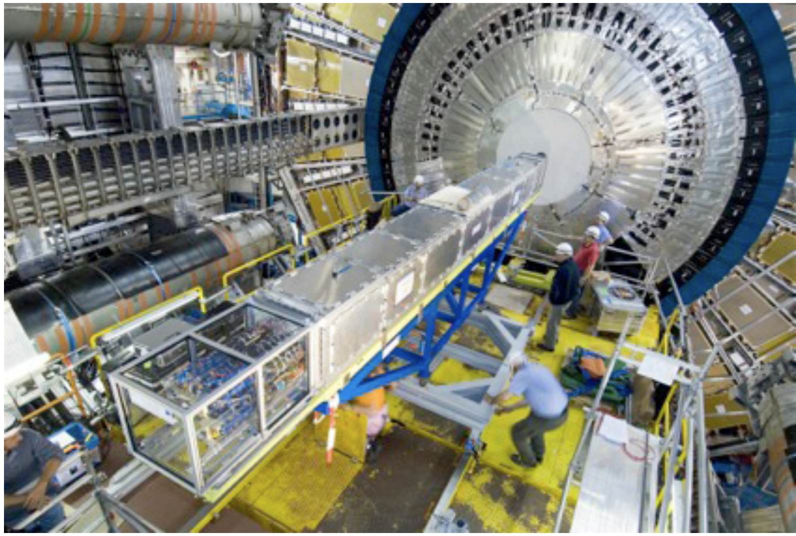
- New Insertable pixel b-layer (IBL)
- New Al beam pipe
- New pixel services
- New evaporative cooling plant
- Consolidation of detector elements (e.g. calorimeter power supplies)
- Add specific neutron shielding
- Finish installation of EE muon chambers staged in 2003
- Upgrade magnet cryogenics

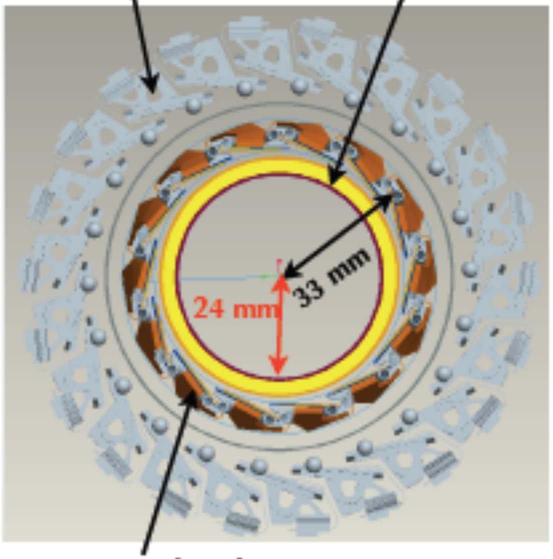
- New Small Wheel (nSW) for the forward muon Spectrometer
- High Precision Calorimeter Trigger at Level-1
- Fast TracKing (FTK) for the Level-2 trigger
- Topological Level-1 trigger processors
- New forward diffractive physics detectors (AFP)

- All new Tracking Detector
- Calorimeter electronics upgrades
- Upgrade part of the muon system
- Possible Level-1 track trigger
- Possible changes to the forward calorimeters

ATLAS @ LS1

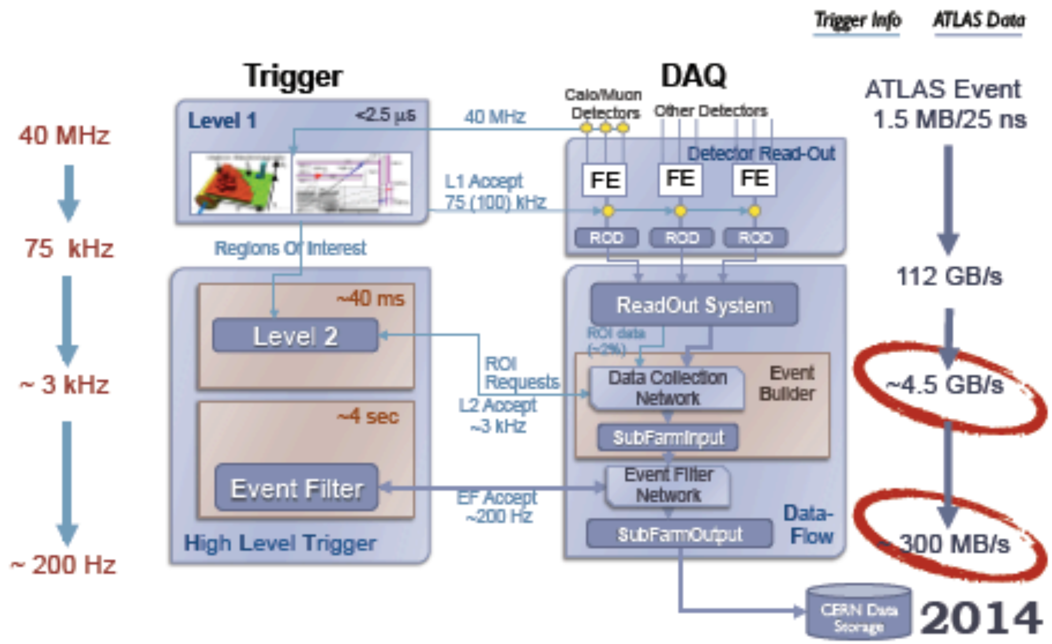
- Pixel extraction
- New Be beampine
- New Inner B Layer insertion (inner radius: 3.2 cm)





- new CO_2 cooling plant
- new FE and BE electronics
- On each stave:
- - 12 double-chip modules (planar pixel sensors)
- - 8 single-chip modules (3D pixels)
- FE-I4 Pixel Chip (26880 channels) 19 x 20 mm2 130 nm
- CMOS process, based on an array of 80 by 336 pixels
- New services being installed to fix problems and
- improve R/O bandwidth
- New Diamond Beam Monitor (DBM) also to be installed

ATLAS TDAQ + new FTK



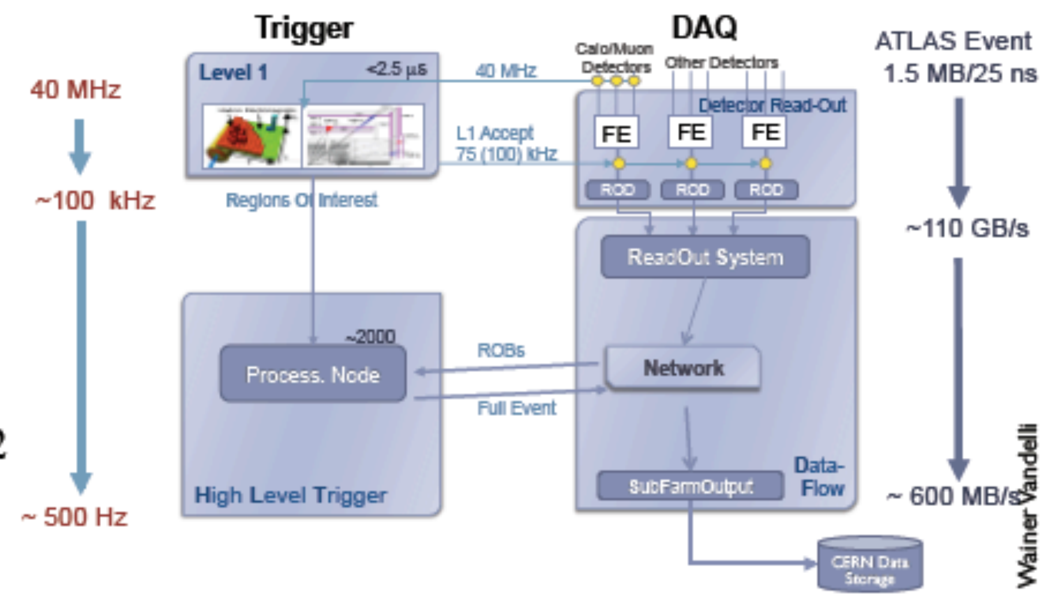
Today already in excess
of design values :

~ 6.5 GB/s

~ 700 MB/s

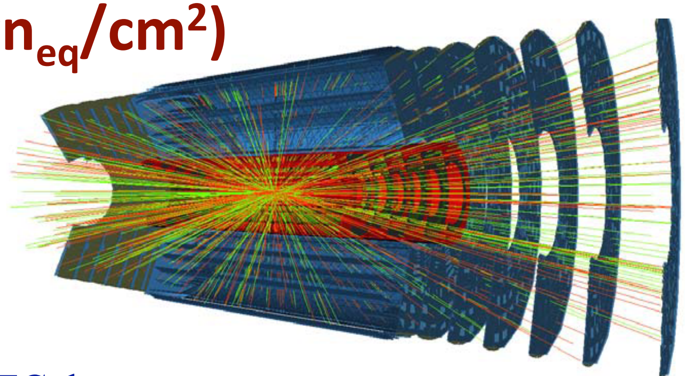
New router

- Simplified architecture
- Single homogeneous farm
- Simpler configuration
- Automatic balance of processing power, less connections to the ROS PCs
- Caching of fragments already collected @L2
Additional flexibility for HLT strategies



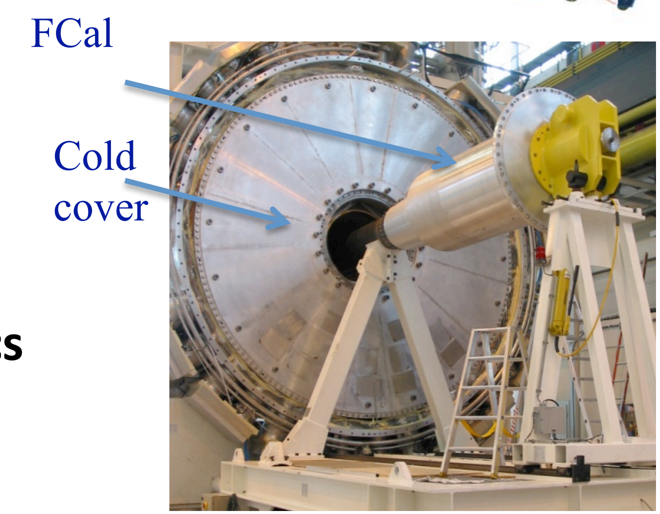
ATLAS @ LS3

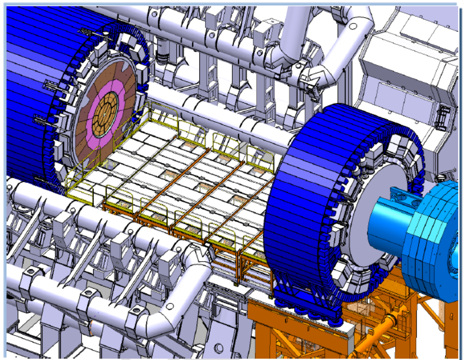
Integrated radiation levels (up to 2-3×$10^{16} n_{eq}/cm^2$) plan to cope with $\mu \approx 200$



Implications of this include:

- New Inner Detector (strips and pixels)
- TDAQ upgrade
- L1 Track Trigger
- New LAr front-end and back-end electronics
- Possible upgrades of HEC and FCal
- New Tiles front-end and back-end electronics
- Muon Barrel and Large Wheel trigger electronics
- Possible upgrades of TGCs in Inner Big Wheels
- Forward detector upgrades
- TAS and shielding upgrade
- Various infrastructure upgrades
- Common activities (installation, safety, …)
- Software and Computing



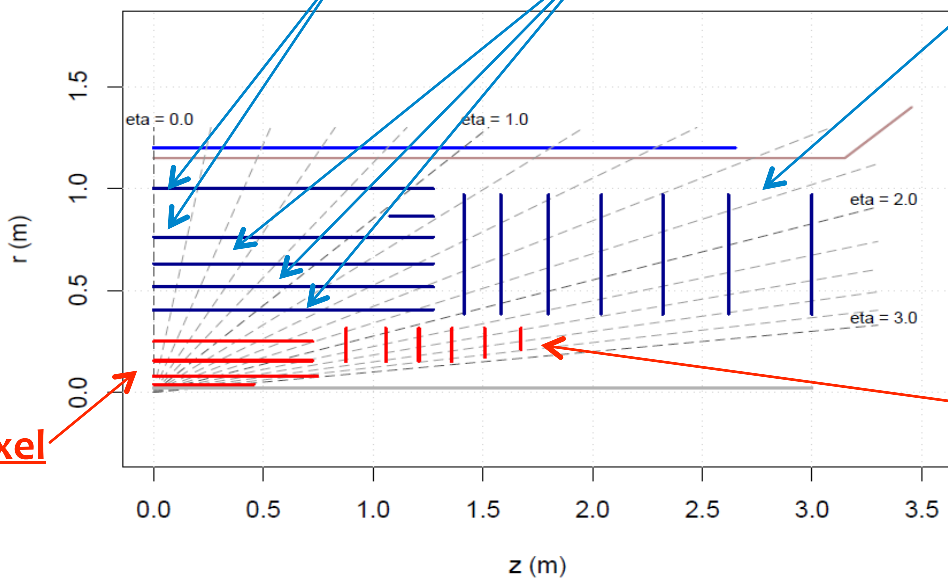


New All-silicon Inner Tracker

Long Barrel Strips

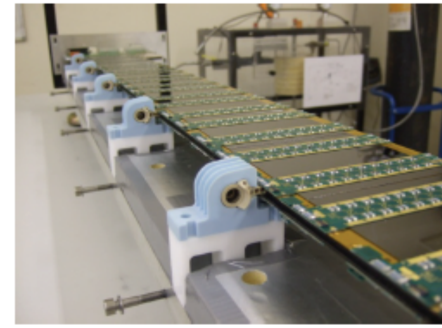
Short Barrel Strips

Forward Strips

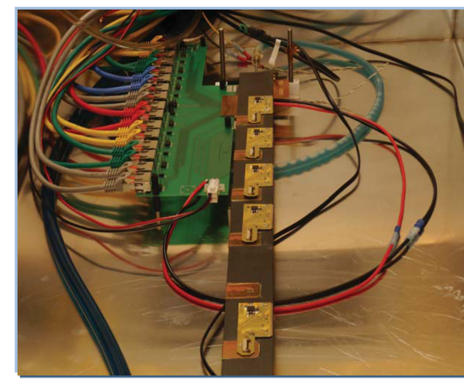


Barrel pixel

Forward pixel

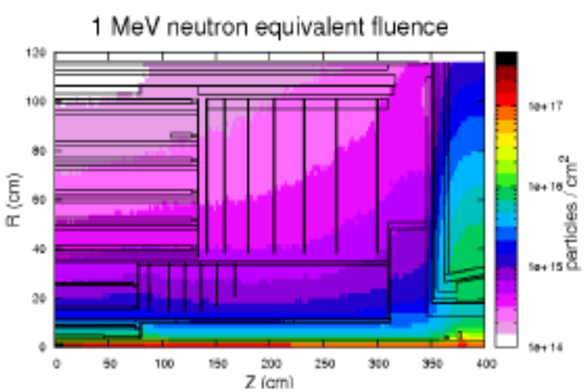


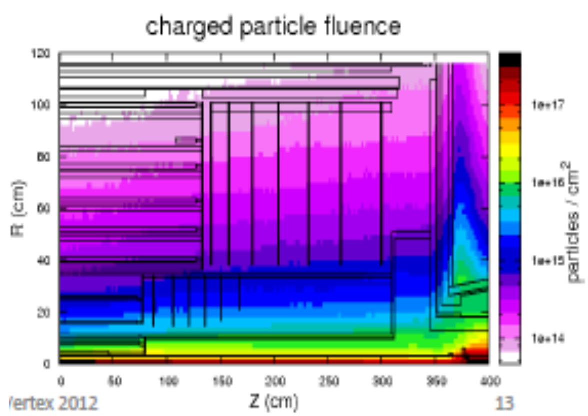
Microstrip Stave Prototype



Outer Pixel Stave Prototype

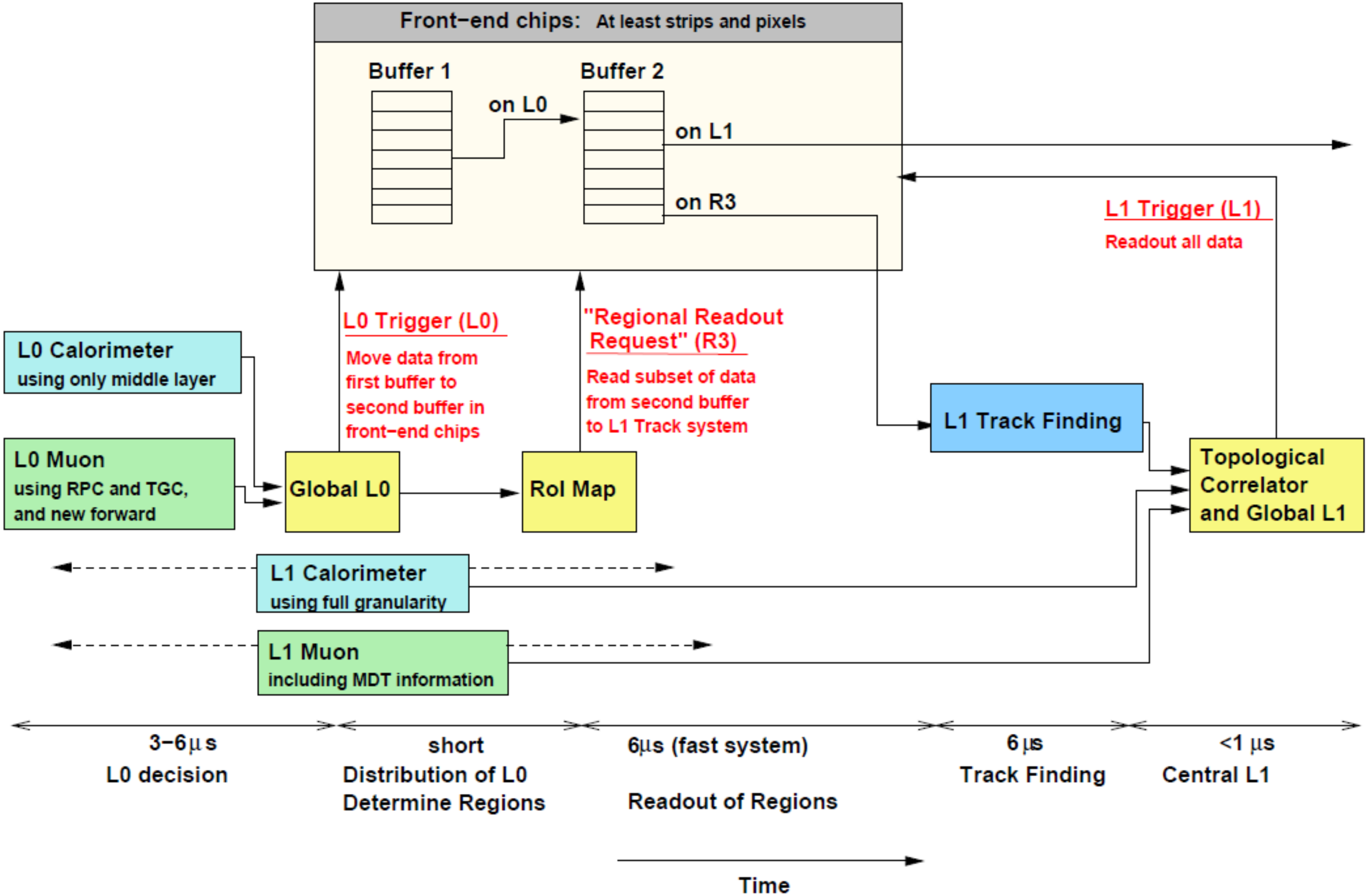
Baseline layout of the new ATLAS inner tracker for HL-LHC
Aim to have at least 14 silicon hits everywhere (robust tracking)

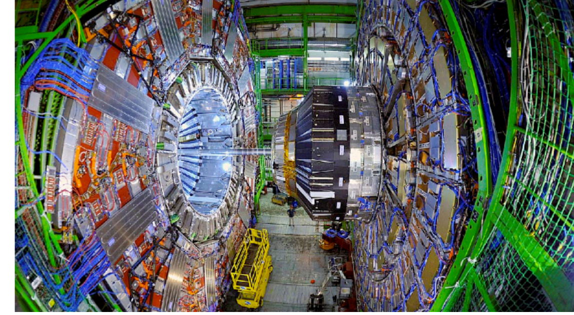


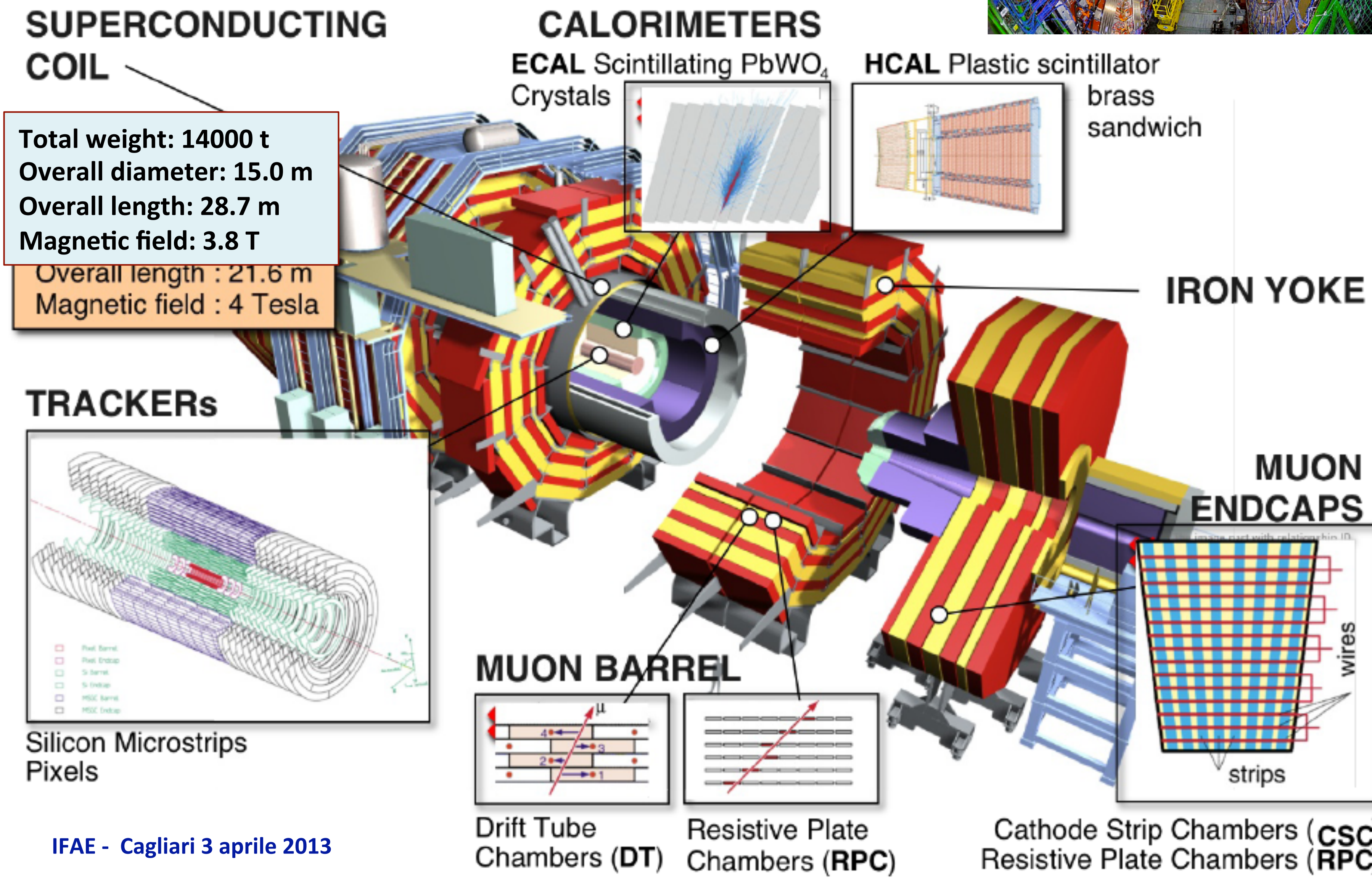


14 TeV collisions; integrated luminosity = 3000fb^{-1}

ATLAS: Split TDAQ L1 Scheme

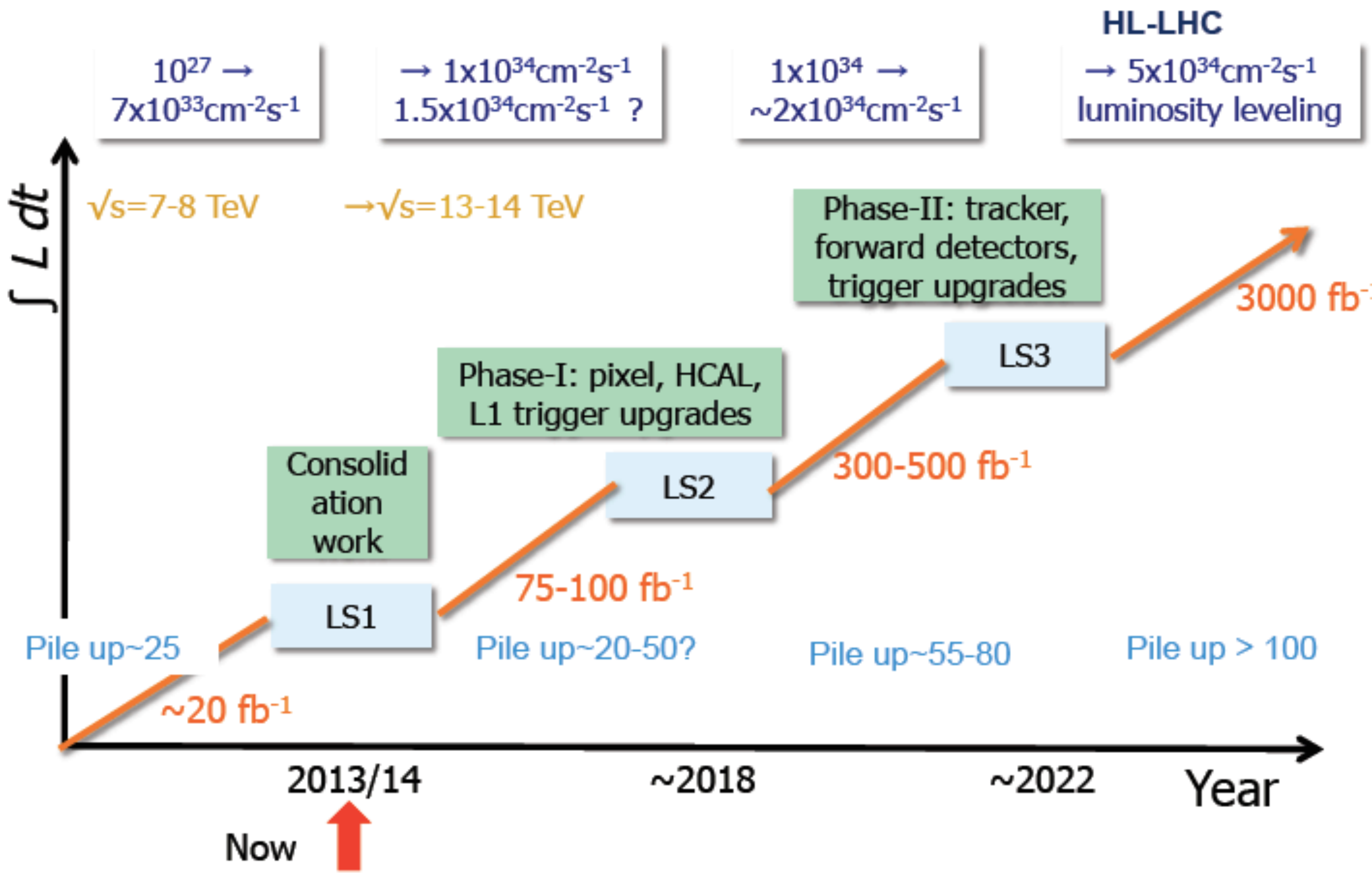




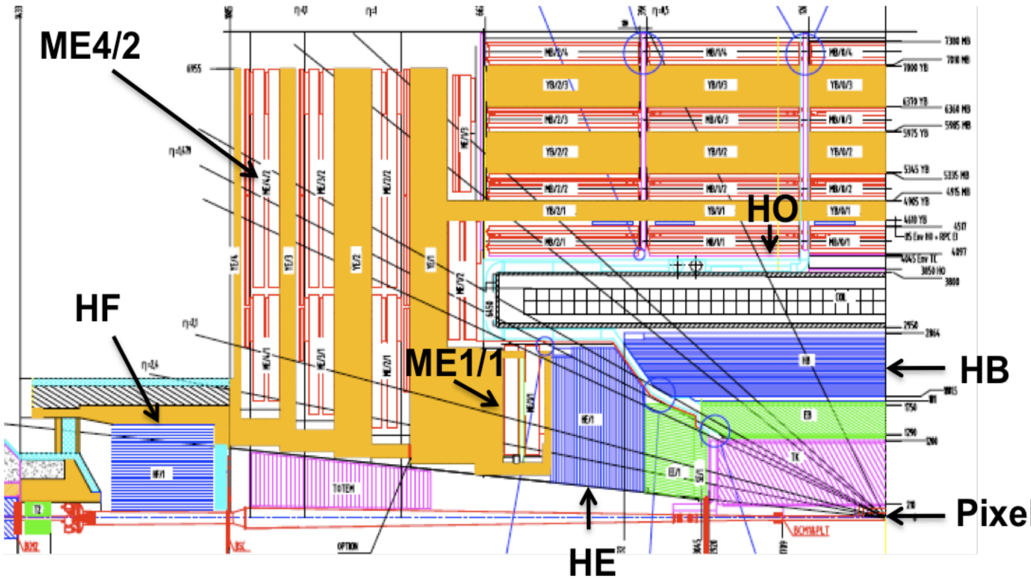


SUPERCONDUCTING COIL
CALORIMETERS
ECAL Scintillating $PbWO_4$ Crystals
HCAL Plastic scintillator brass sandwich
Total weight: 14000 t
Overall diameter: 15.0 m
Overall length: 28.7 m
Magnetic field: 3.8 T
Overall length : 21.6 m
Magnetic field : 4 Tesla
IRON YOKE
TRACKERs
Silicon Microstrips
Pixels
MUON BARREL
MUON ENDCAPS
wires
strips
Drift Tube Chambers (DT)
Resistive Plate Chambers (RPC)
Cathode Strip Chambers (CSC)
Resistive Plate Chambers (RPC)

CMS upgrade plan



CMS upgrade



LS1 Projects: in production
- Completes muon coverage (ME4)
- Improve muon operation (ME1), DT electronics
- Replace HCAL photo-detectors in Forward (new PMTs) and Outer (HPD→SiPM)
- DAQ1 → DAQ2

LS1 LS2 LS3

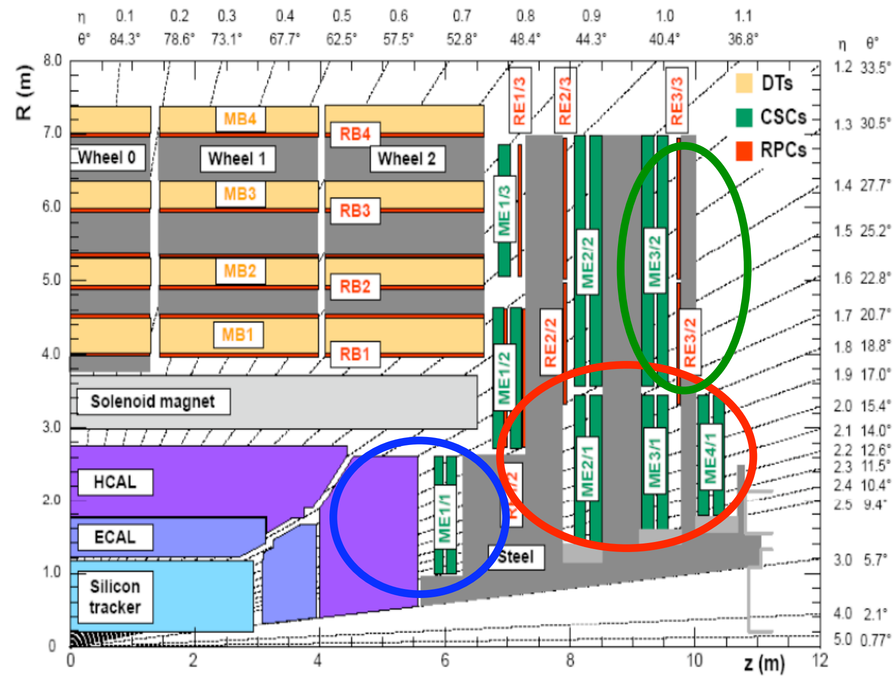
Phase 1 Upgrades (TDRs)
- New Pixels, HCAL electronics and L1-Trigger
- GEM under cost review
- Preparatory work during LS1
  - New beam pipe
  - Install test slices
    - *Pixel (cooling), HCAL, L1-trigger*
  - Install ECAL optical splitters
    - *L1-trigger upgrade, transition to operations*

Phase 2: Now being defined
- Tracker Replacement, Track Trigger
- Forward : Calorimetry and Muons and tracking
- Further Trigger upgrade
- Further DAQ upgrade
- Shielding/beampipe for higher aperture

CMS Muon Upgrade

LS1

- No new detectors in the barrel
- **DT barrel:** replace electronics and a substantial migration of electronics to USC
- **New CSC/RPC** stations in YE-4/2
- CSC ME-1/1: replace electronics (including FE) to maintain trigger and avoid deadtime



LS2

- **New system** at 1.6<|η|<2.1 to improve L1 and HLT muon momentum resolution to reduce trigger rate and ensure high trigger efficiency in high PU environment

GEM-based detector in stations 1

LS3

- R&D on new super-high eta detectors: GEM/GRPC for stations further away ➔ hooks to interconnect muons with inner tracking trigger

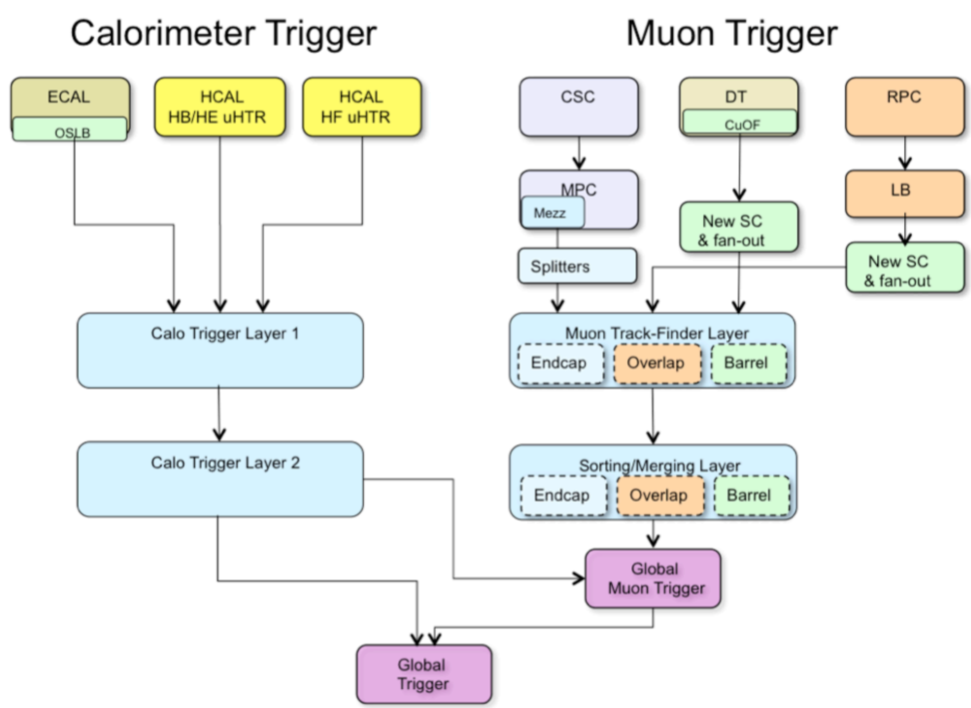
- **DT**: new minicrates

Trigger Upgrade: Plan

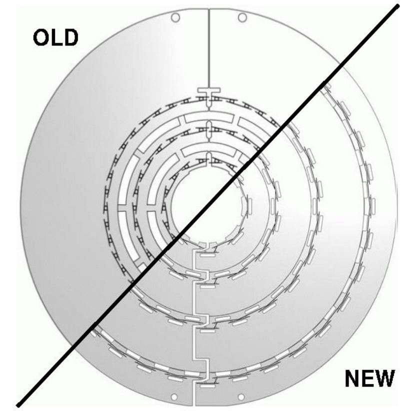
Upgrade the Calo, Muon and Global Triggers

- architecture highly configurable, based mainly on 3 boards (with large FPGA, high bandwidth optics, memory for LUTs)
- parallel commissioning of new trigger while operating present trigger
- goal to provide improvements for 2015, commission full functionality for 2016

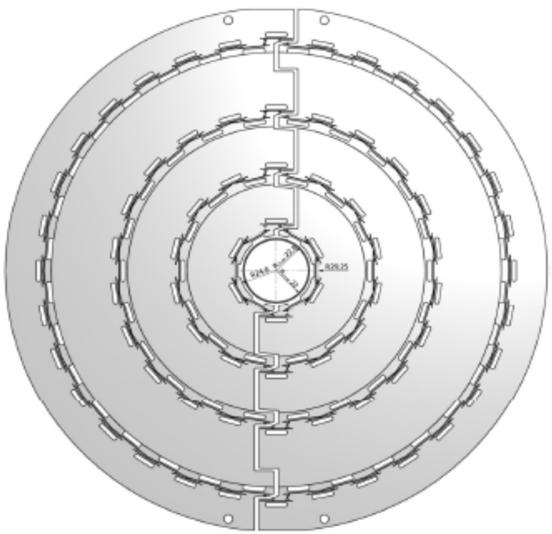
use standard μTCA boards with large FPGAs for new algorithms

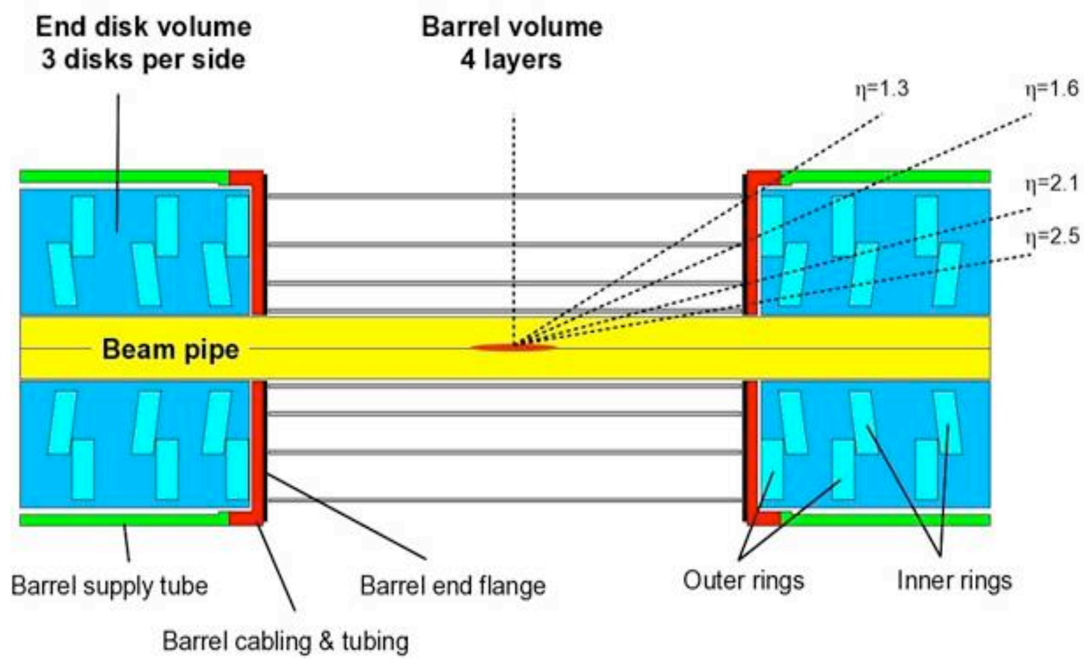


New Pixel: installation 2016



- Extra layer in barrel and end-cap
- Efficient seeding + robust tracking in increasing track density
- L4↑ reduce gap to TIB, L1↓ reduce impact of MS on dxy/dz resolution





Full Tracker and Pixel upgrade in LS3

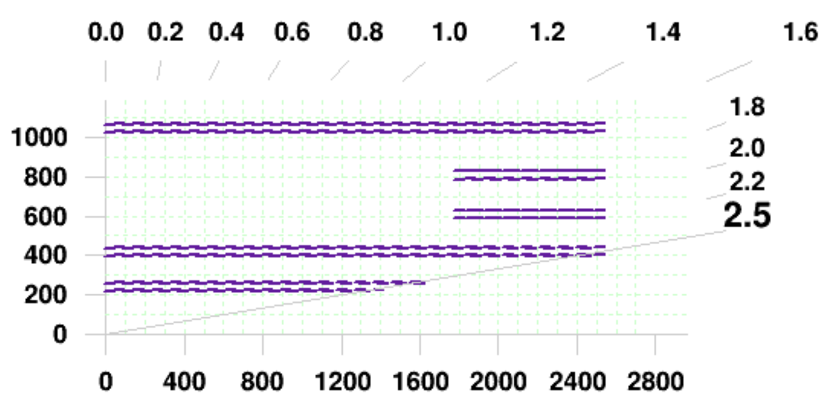
Large project, vast R&D program covering all detector aspects

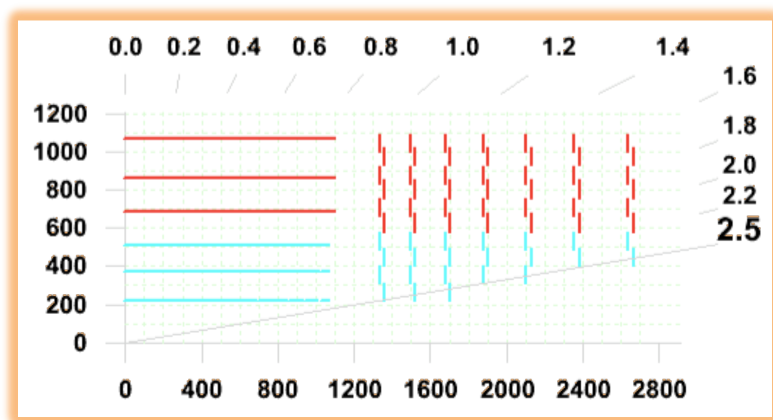
Includes requirement of tracking in Level-1 trigger

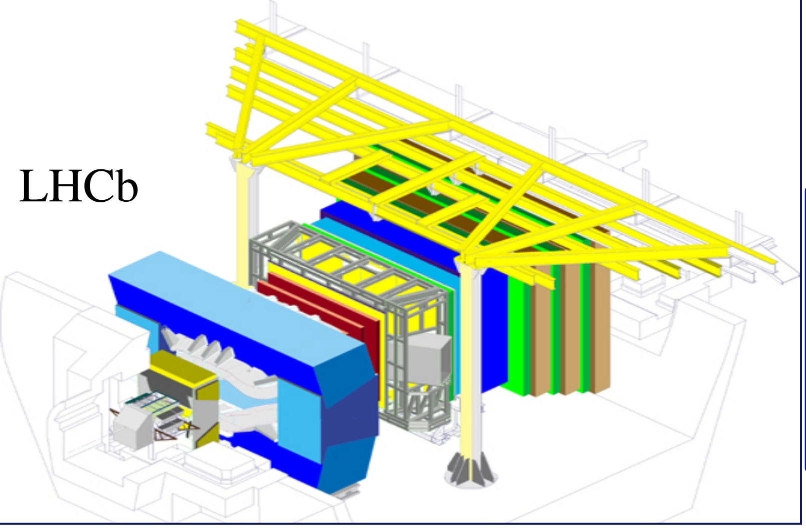
Different Layouts and Technologies under consideration

- TK Layout decision around spring 2014
- CMS HL Upgrade Technical Proposal planned end of 2014
- Tracker Technical Design Reports in ~ 2016

- Phase 2 Tracker R&D and Track Trigger activities : Appendix CMS Upgrade TP for Phase I
  http://cds.cern.ch/record/1355706?ln=it
- Phase 2 Pixel R&D activities: Appendix in Pixel Upgrade TDR for Phase I
  http://cds.cern.ch/record/1355706?ln=it







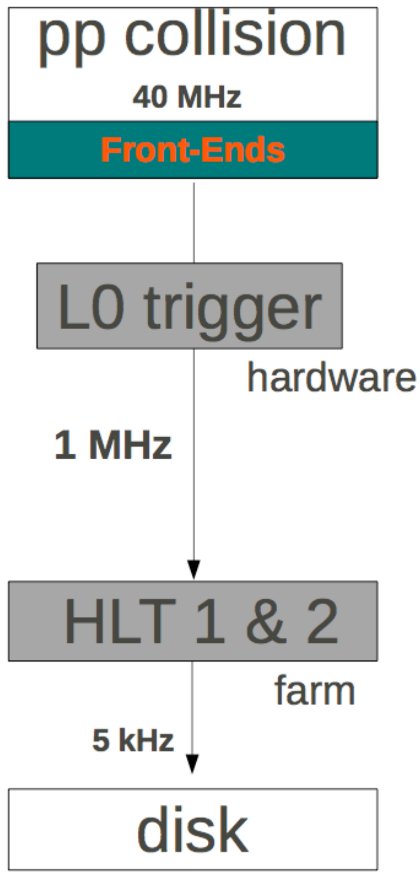
LHCb Upgrade @ LS2

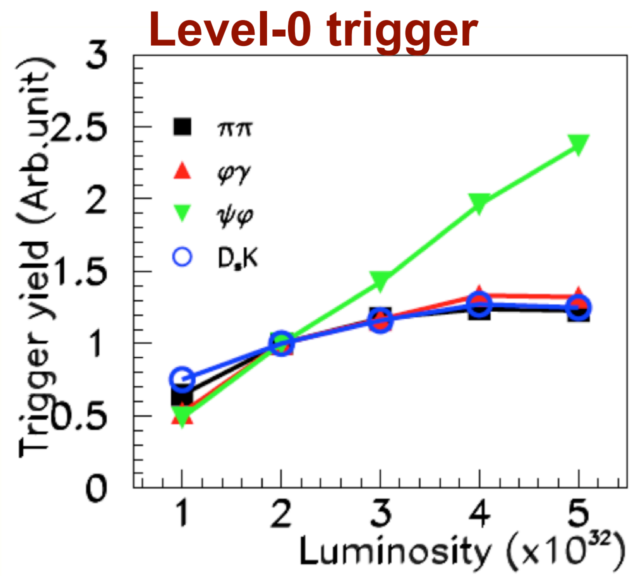
operated successfully at $\mathcal{L} = 4 \times 10^{32}$ cm^2 s^{-1}
50 ns spacing and average multiplicity $\mu > 1.5$
Collected $\mathcal{L}_{int}$ = 3 fb^{-1} (2011+2012)
➔ additional 5 fb^{-1} expected by 2018

- Upgrade:
  - Measurements to validate CKM description at sub-10% level, aiming at a precision comparable to the theory
  - **Running at $\mathcal{L}$=1-2×10^{33} cm^2 s^{-1}**, with **25 ns spacing** and **μ = 4**
  - **To collect $\mathcal{L}_{int}$= 50 - 100 fb^{-1} in 10 years of data-taking**
  - Installation foreseen by LS2

LHCb trigger

1 MHz
A technological limit at the time of construction





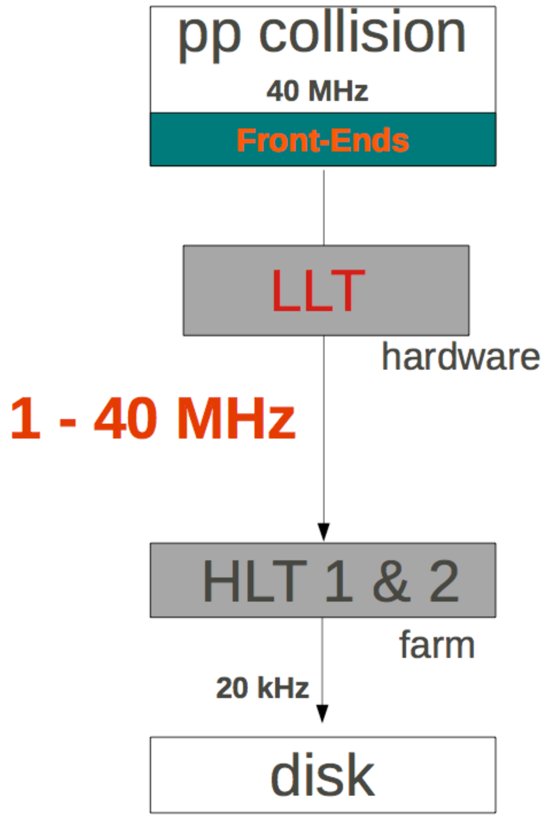
Any increase in luminosity must be currently accompanied by an increase in the hadronic thresholds due to bandwidth HLT limit of 1 MHz

L0 selection based on E_T and p_T cuts: about 50% efficiency for hadronic channels

LHCb new 40 MHz readout

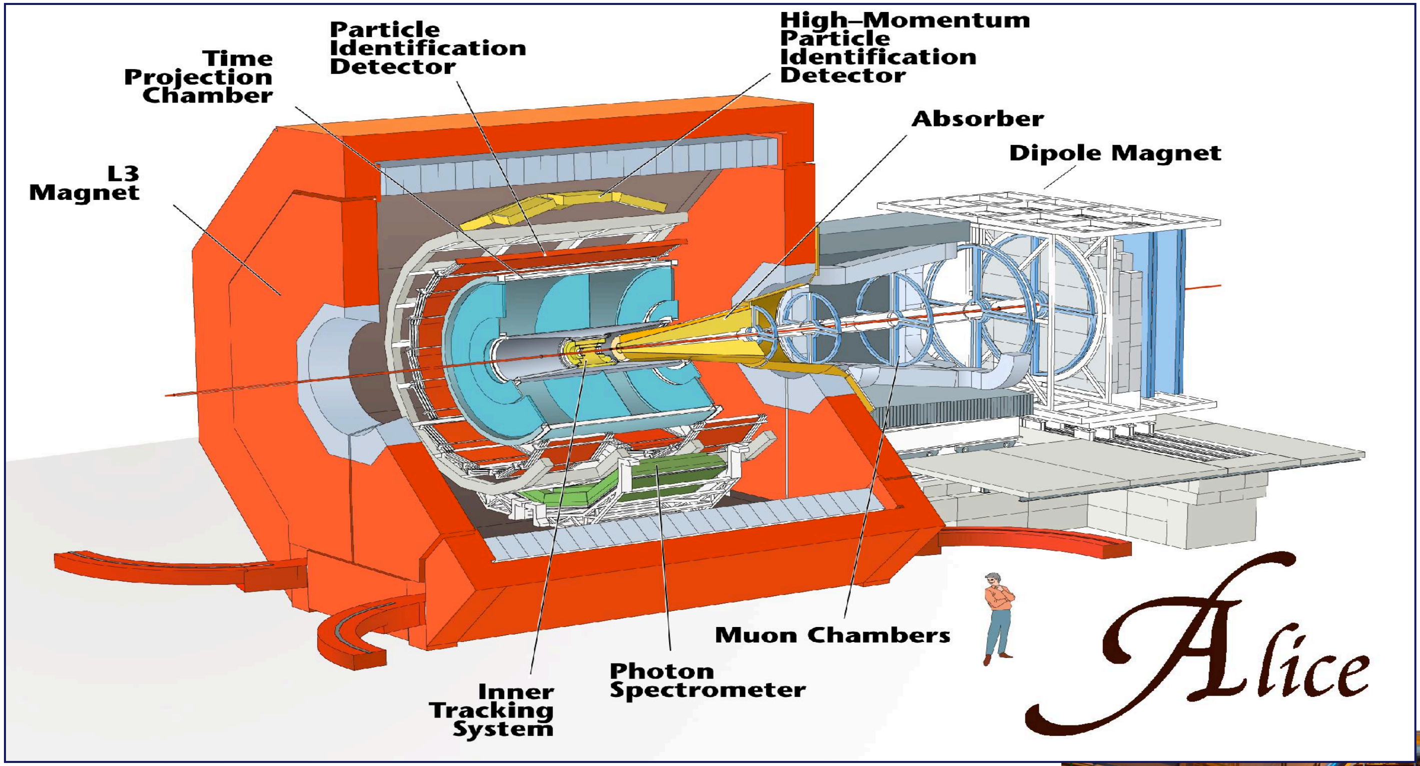
40 MHz readout implies:

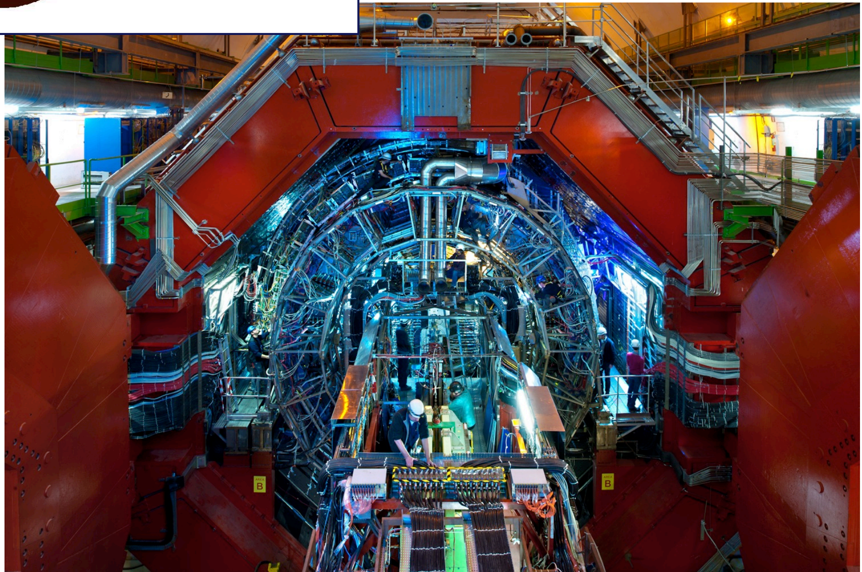
- Replacement of the front-end electronics
- A new architecture for DAQ
- New Silicon detectors (VELO, IT and TT)
- RICH photon detector replacement and geometry optimization
- Tracking stations after magnet to be redesigned (occupancy rising up to 40%)
- M1 stations of the muon system, the preshower (PS) and scintillator pad detector (SPD) are crucial for the L0 trigger



Read-out the detector synchronously with the bunch-crossing
Gradually replace the LLT hardware trigger by a fully software-based HLT trigger for high-flexibility and efficiency

ALICE upgrade @ LS2





ALICE upgrade startegy

- most physics signals are rare, but untriggerable
  - increase rate capabilities for minimum bias heavy-ion collision
    - upgrade of TPC and ITS, all readout electronics, etc.
  - target: inspection of 50 kHz of minimum bias Pb+Pb
    - factor 100 increase in statistics (for untriggered probes)
  - collect > 10 nb^{-1} of integrated luminosity
    - upgrade in LS2, implies running few years after LS3
- ALICE is unique in low-p_T/low-mass measurements and particle identification
  - further enhance capabilities, in particular with upgraded ITS
    - closer to beam, less material, better resolution

ALICE ITS upgrade

factor 3 better secondary vertex resolution:

- inner layer as close as possible (R = 2.2 cm)
- less material budget
  - thin sensors
  - thinner beam pipe (ΔR = 800 μm)

fast readout

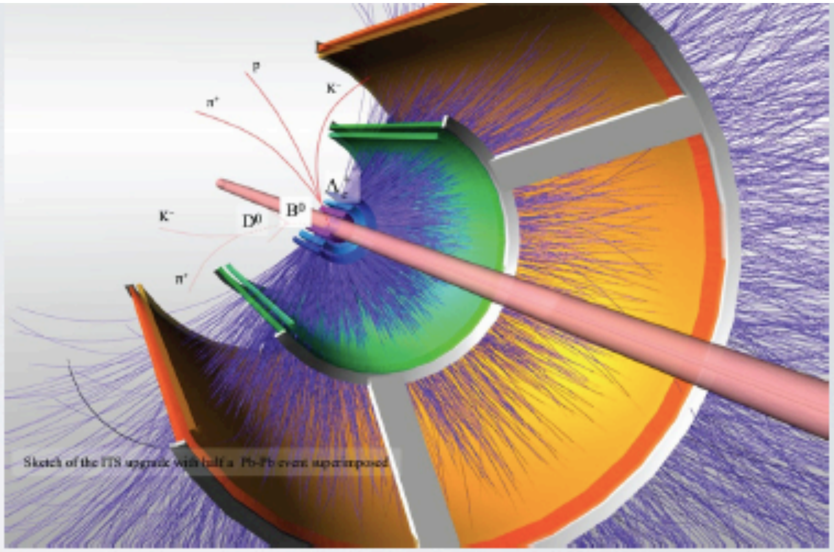
- allow 50 kHz rate in Pb+Pb

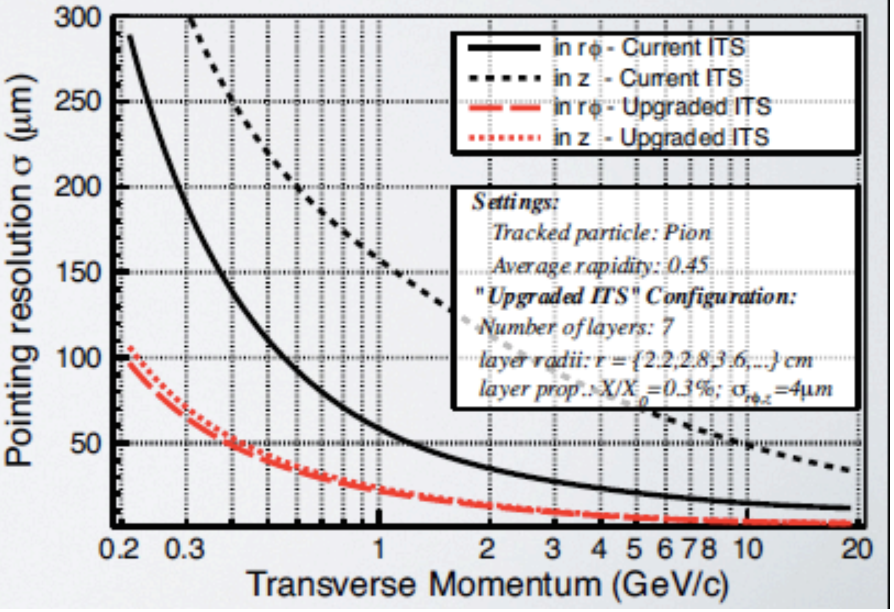
two technologies investigated

- hybrid pixels
- monolithic active pixels

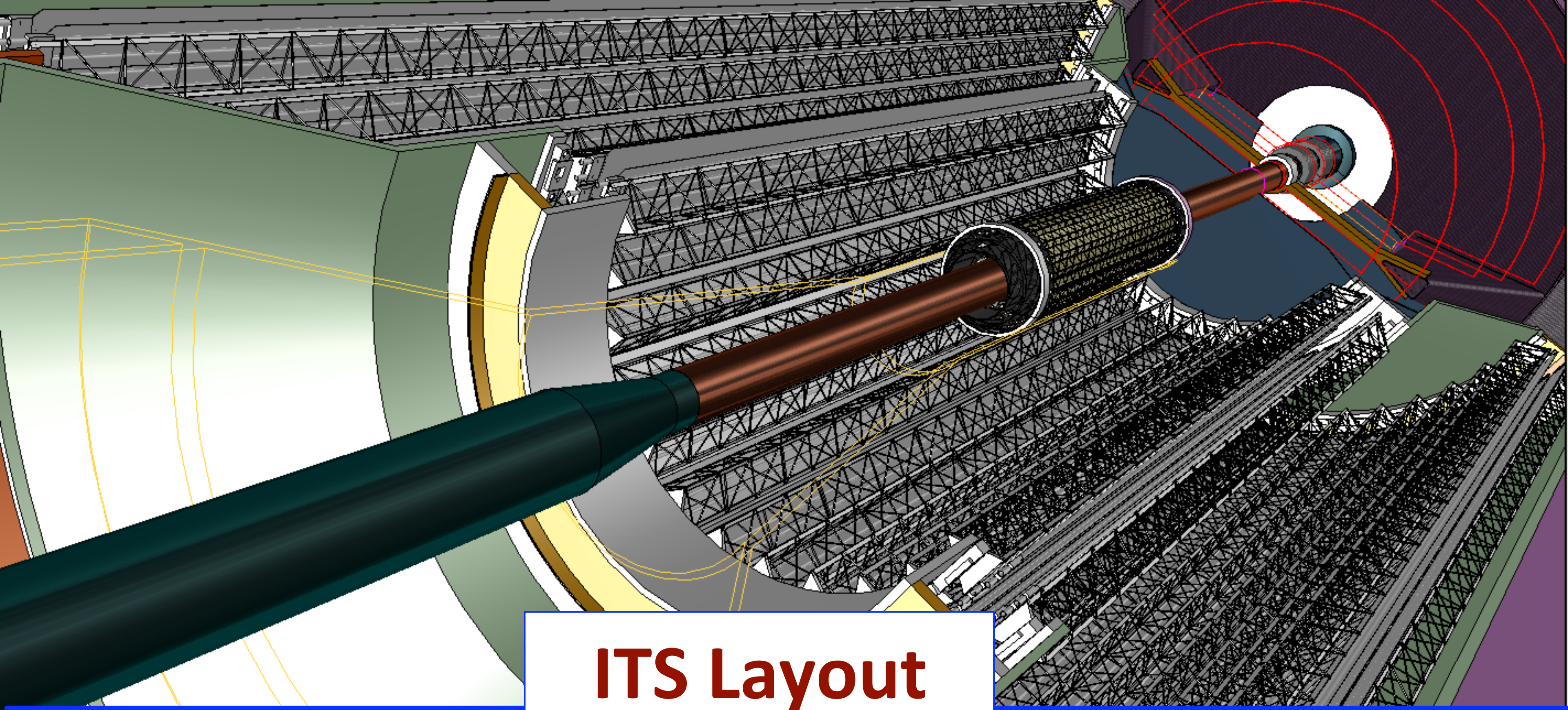
to be used as all-pixel (7 layers) or pixel(3)+strip(4)

- possibly new Si-strip sensors





talk by R. Lemmon, this session,
poster by G. Contin (ID 601)



ITS Layout

Inner Barrel (IB): 3 layers pixels

Radial position (mm): 22,28,36

Length in z (mm): 270

Nr. of modules: 12, 16, 20

Nr. of chips/module: 9

Nr. of chips/layer: 108, 144, 180

Material thickness: ~ 0.3% X_0

Throughput: < 200 Mbit / sec•cm^2

Outer Barrel (OB): 4 layers pixels

Radial position (mm): 200, 220, 410, 430

Length in z (mm): 843, 1475

Nr. of modules: 48, 52, 96, 102

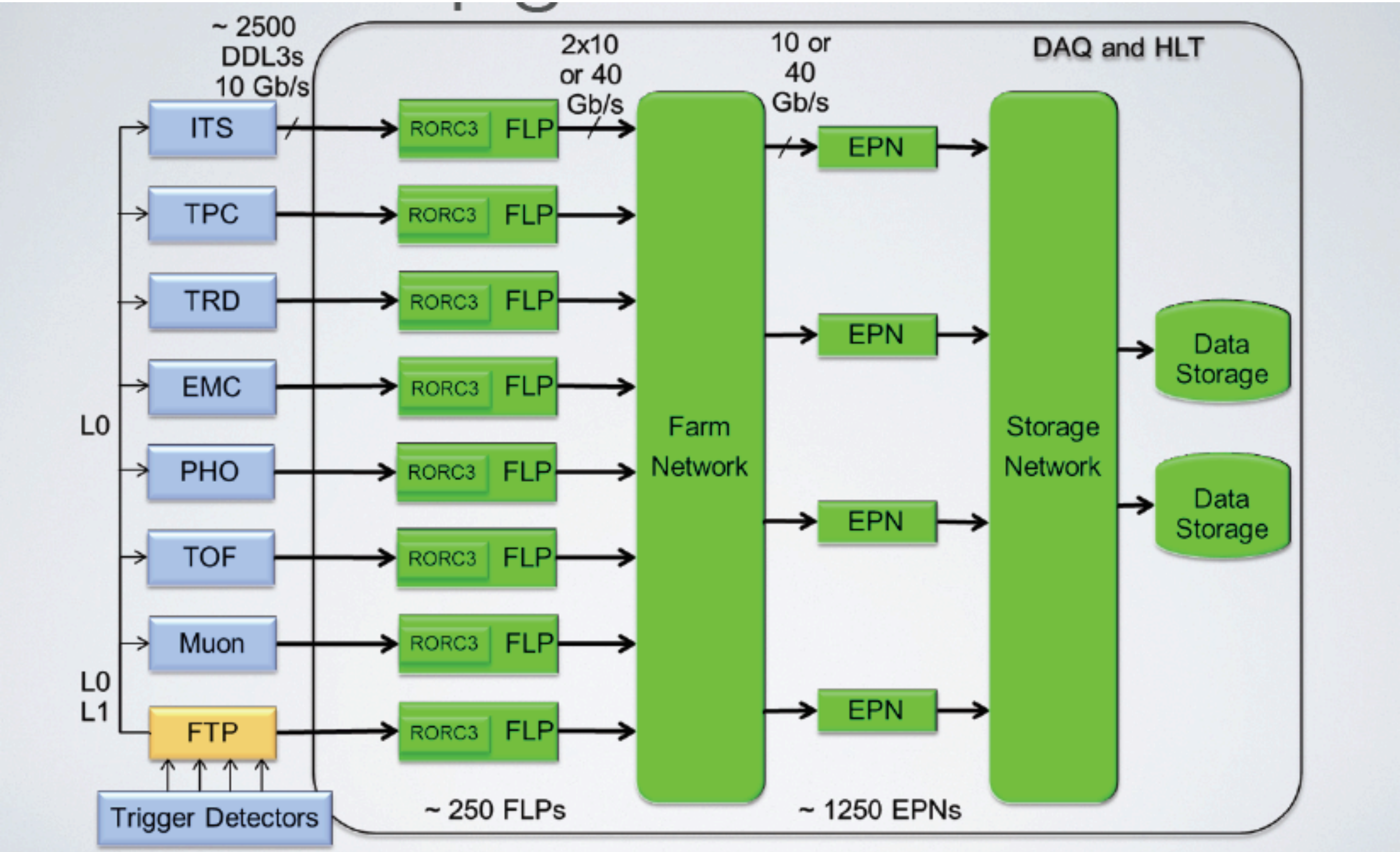
Nr. of chips/module: 56, 56, 98, 98

Nr. of chips/layer: 2688, 2912, 9408, 9996

Material thickness: ~ 0.8% X_0

Throughput: < 6 Mbit / sec•cm^2

ALICE online upgrade



FTP: Fast Trigger Processor FLP: First-Level Processor EPN: Event-Building and Processing Nodes

Conclusions

- ✓ LHC and experiments' obtained excellent results from Run 1: **the goal is to maintain or improve present performances**
- ✓ LHC upgrade ➔ Experiments' upgrades
- ✓ New challenges on tracking, readout electronics, forward regions and mostly trigger to exploit higher energy and $\mathcal{L}$

For reference:

ALICE:

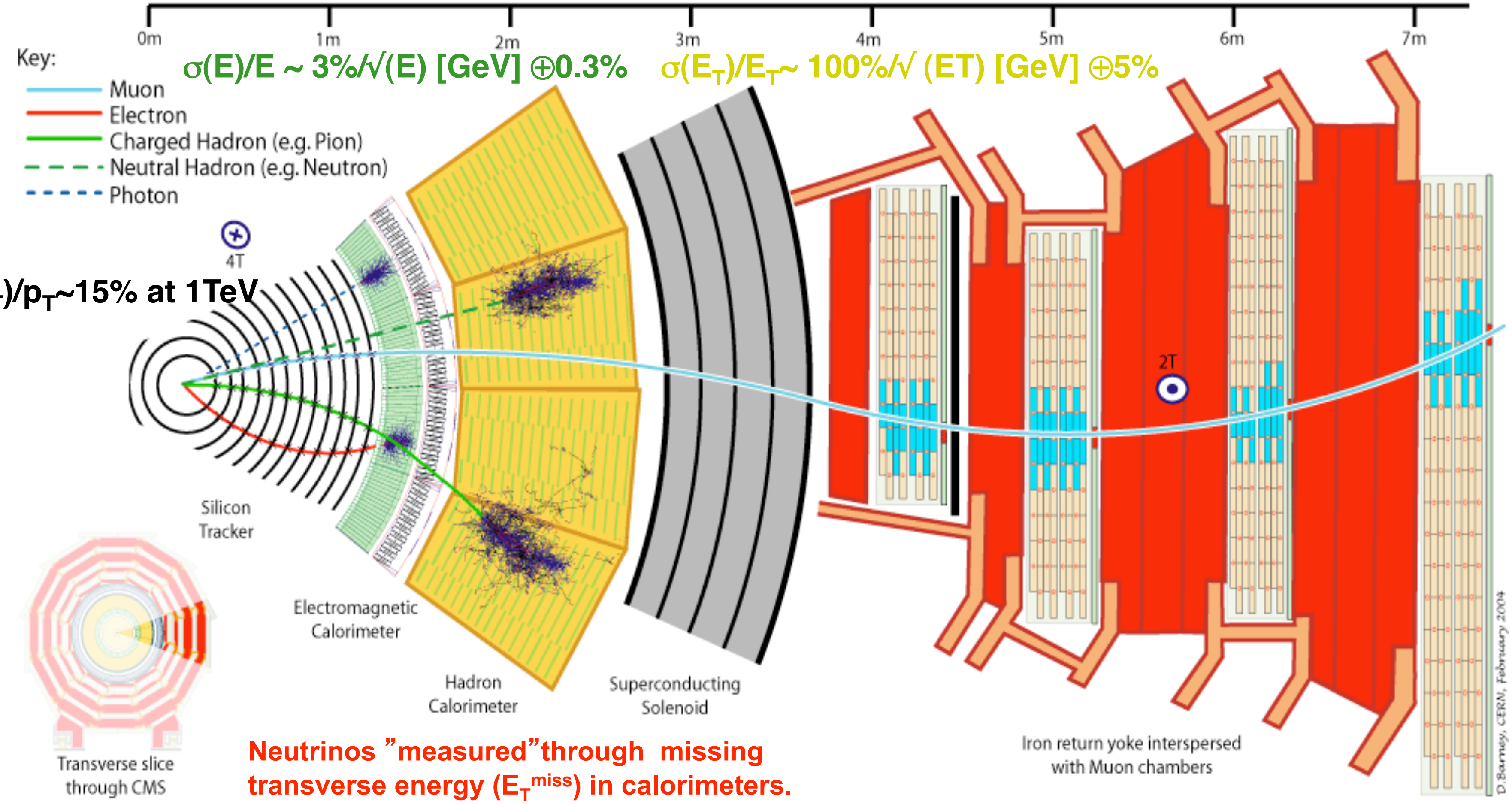
ATLAS:

CMS:

LHCb:

Back-up

A simple and elegant concept



$\sigma(E)/E \sim 3\%/\sqrt{(E)}$ [GeV] $\oplus 0.3\%$

$\sigma(E_T)/E_T \sim 100\%/\sqrt{(ET)}$ [GeV] $\oplus 5\%$

$\sigma(p_T)/p_T \sim 15\%$ at 1TeV

Neutrinos "measured" through missing transverse energy (E_T^{miss}) in calorimeters.

Fast detectors: 25-50ns bunch crossing

High granularity: 20-40 overlapping complex events

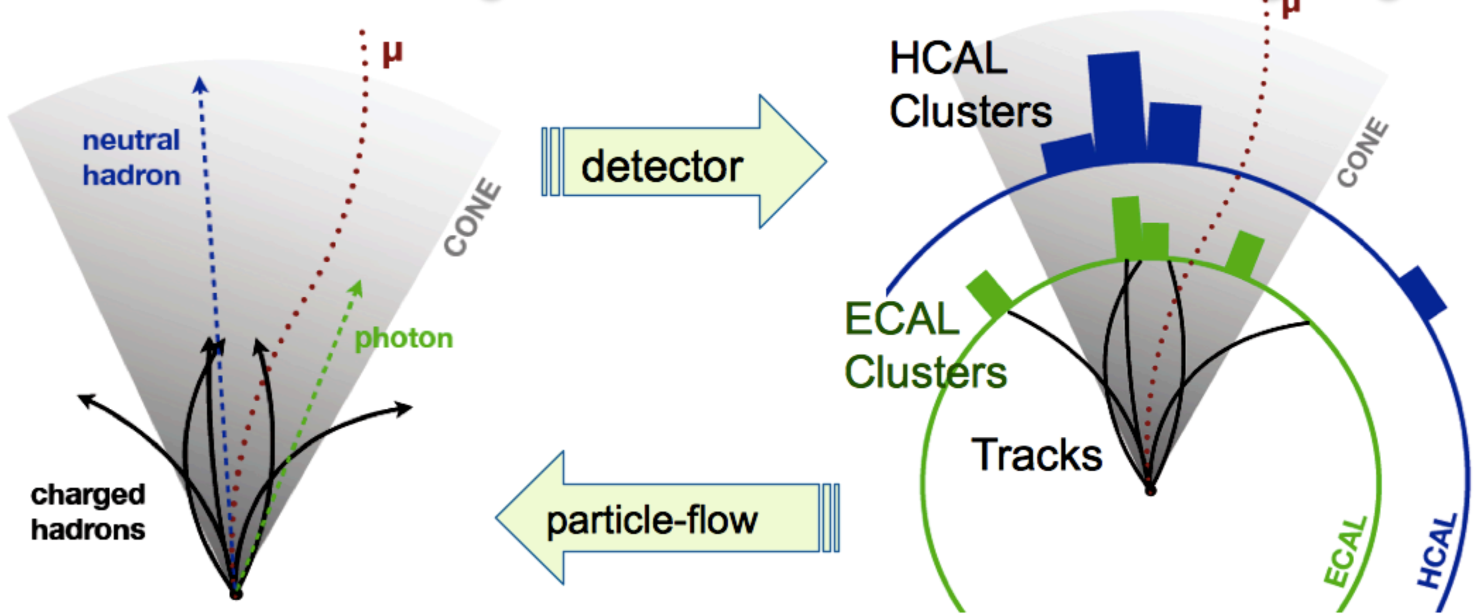
High radiation resistance: >10 years of operation

$\sigma(p_T)/p_T < 1\%$ @ 100GeV

$\sigma(p_T)/p_T < 10\%$@1 TeV

Particle Flow Reconstruction

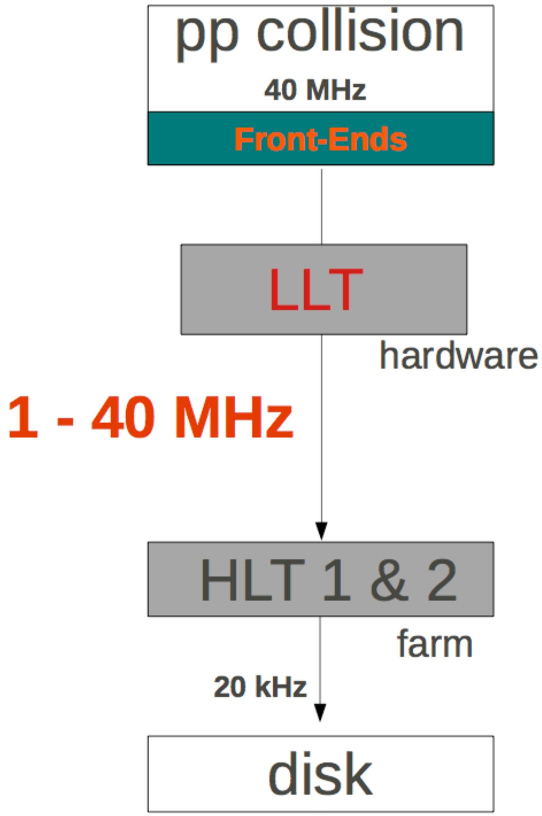
Possible for redundancy, for the excellent granularity of
Tracker and Electromagnetic Calorimeter and for the strong magnetic field

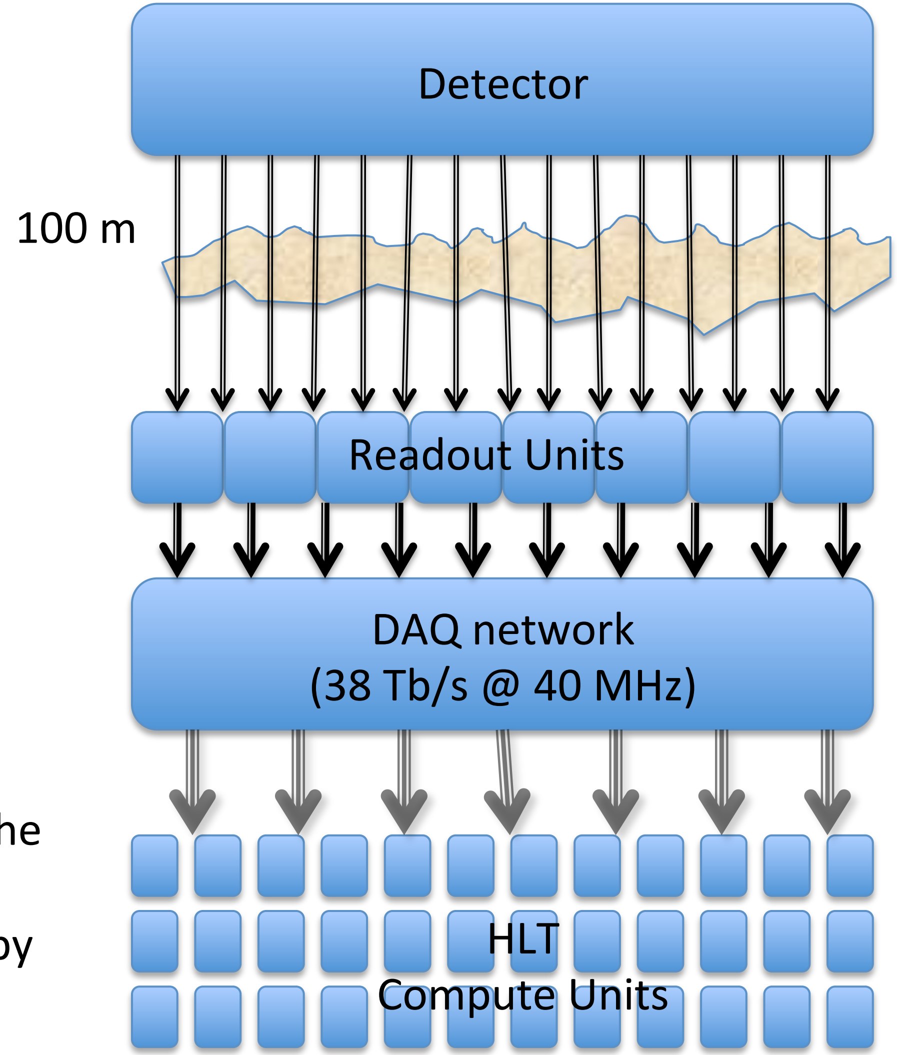


- Optimal combination of information from all subdetectors
- Returns a list of reconstructed "particles"

  ➡ **Electrons, Muons, Photons, Charged and Neutral Hadrons**
- **Used as building blocks for jets, taus, missing ET, lepton isolation**
- Allows tagging of charged particles from pile-up: minimizes impact of PU on jet reconstruction, and lepton or photon isolation

LHCb Upgrade





Read-out the detector synchronously with the bunch-crossing
Gradually replace the LLT hardware trigger by a fully software-based HLT trigger for high-flexibility and efficiency

PCIe-IB-ETH-uniform cluster