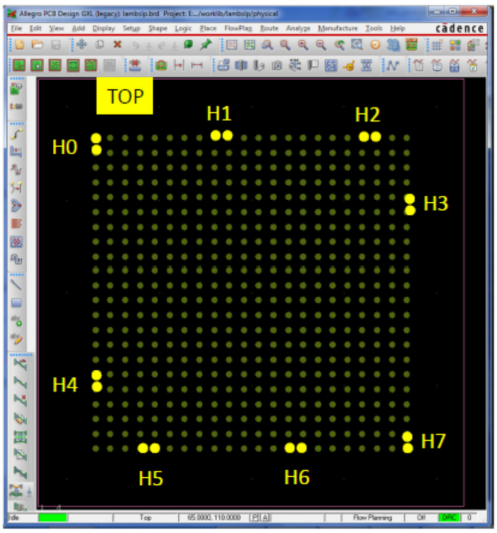
LAMBFTK

Project

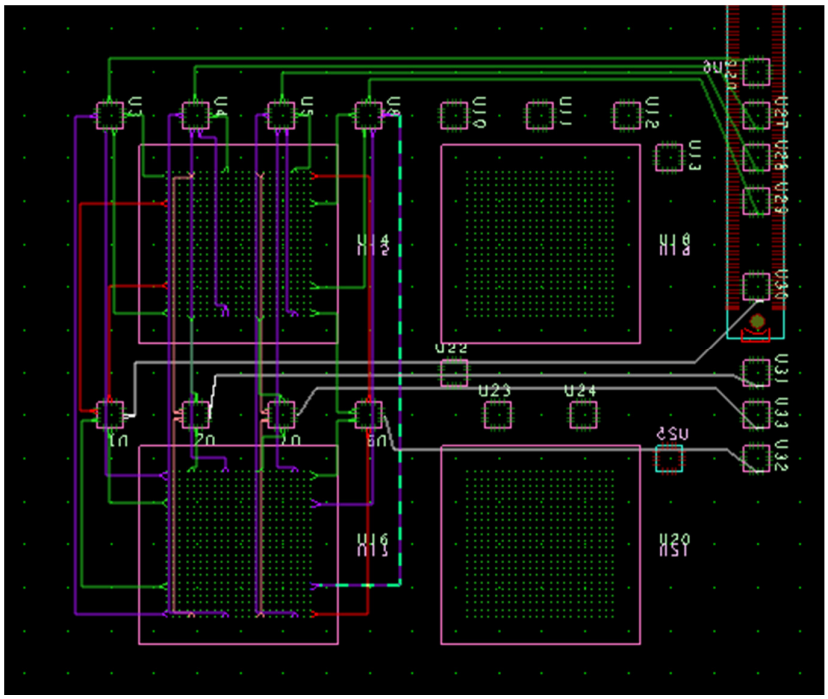
The AMchip05 has 8 input serial bus with the following pin assignment. (Example FPGA ff484 32x32 mm)



Serial Bus	Pin
H0	A1-B1
H1	A9-A10
H2	A19-A20
H3	E22-F22
H4	U1-V1
H5	AB4-AB5
H6	AB14-AB15
H7	AA22-AB22

First placement component and routing strategy

Consider the bus placement of only 1/8 of lamb, such as 4 AMchips, in the following way: we have to use until 4 routing plane for differential bus (vertical connections: violet pink, green, red) + 1 (or 2) routing layers for clock and horizontal connections. The problem is the routing of differential bus to the fan-out chips in the middle of the AMchips because we cannot use the top and bottom layer but is necessary one layer of routing dedicated .



But we can also adopt this other strategy: the horizontal connection of the buses to fan-out chips is only done with the top and bottom plane. The routing of the chip 2 is done with the horizontal mirror and then the 3 and 4 chip is the vertical mirror of the left part. In the middle of the chip is placed the clock distribution chip.