SerDes Test Features



DTESTEN	input	Digital test bus enable
DTESTOUT	output	Digital test bus output
DTESTSEL[2:0]	input	Digital test bus select
		DTESTSEL[2:0] Output
		000 -> 1'b1
		001 -> 1'b0
		010 -> TXREFCLK
		011 -> TX clock for lock
		100 -> TXLOCK pre signal
		101 -> TXCLK40
		110 -> TXCLK10
		111 -> TXLOCK
HSLPBK	input	High speed loopback
		1 -> loopback mode
		0 -> normal operating mode

Test Features:

A digital test bus is included for debugging. The bus is enabled by asserting the DTESTEN input. The DTESTSEL[3:0] bits are used to select a signal for observation on the DTESTOUT pin.

Some of the signals observed by the digital test bus are DC (such as a digital 1 or digital 0 value) or should only transition once per locking event (RXLOCK, TXLOCK).

The reference clock to the TX and RX PLLs is made observable for a PLL bypass observation. This provides a confirmation that the reference clock is the desired signal and a baseline jitter reference for the digital test bus can be set by observing this signal.

The RXCLK10, RXCLK40, TXCLK10, and TXCLK40 are divided clock signals from the RX and TX PLLs. Observing these clock signals gives some visibility to the PLL behavior without having to observe the high speed data. The digital test output is intended for a clock and signal functionality check rather than a quality check such as jitter measurement.

A baseline for jitter should rst be established by observing the reference clock over the digital test bus before analyzing the PLL jitter.

The Phy contains an internal loopback feature that can be used to route the output of either TX channel serializer to the RX as seen in fugure. If desired, external loopback is possible by implementing a load board.

HSLPBK controls which type of loopback the testchip is in. To enable internal loopback, assert HSLPBK high, HSLPBK = 1'b1. Conversely, to enable external loopback, assert HSLPBK low, HSLPBK = 1'b0. HSLPBK accomplishes this selection by multiplexing the input to the deserializer.

SerDes other Test Features

TX Testing

Testing the transmitter can be accomplished by applying a stimulus and viewing the eye diagram on the oscilloscope. If the functionality is available, it is beneficial to see time interval errors due to the transmitter additive noise. The expected time interval error (TIE) due to the serializer and TX PLL should be less than 0.01UI from 100kHz to 20MHz.

PRBS Testing

In order to evaluate the quality of the serial link PRBS testing should be done using the PRBS-7 pattern from the pattern generator. To properly transmit the PRBS test pattern across the serial link, HSLPBK should be enabled. The serial bit rate should be swept from a value near the lower end of the specied range to a value near the maximum data transmission rate to stress the link and test its robustness.

Tests not included in SerDes IP

The Silicon Creation SerDes does not include JTAG (neither 1149.1 nor 1149.6) boundary scantest.

The HSS conncetion test between AM chip on the PCB actually cannot be performed. In the IP it is not possible (and could be dangerous) to add boundary scan cells to the LVDS driver and receiver.

To implement such a test other solutions can be used:

• Use PRBS test to check the conncetions

• Putting logical '1' at the input bus of the serdes and transmitting this data without 8b/10b coding.

• Generating a '101010' sequence at low frequency (perhaps 0.1KHz) and transmitting it without 8b/10b conding.

All these solutions assumes that the serializer and deserializer on the AM chip work properly. This assumption should be correct because all chips are tested before mounting on the LAMB.

Moreover, another assumption is that the clock and high speed signal distribution on the LAMB board have to work properly.

Actually no other solutions to test chip to chip connections are available without taking some risk.

SerDes JTAG connection test Hypothesis





Fig. 7.3 Chip to Chip Interface with JTAG 1149.1 Test Features





SerDes channels scheme



There is only one PRBS Checker for all the input channels. Only one channel per time will be tested. Slow but less area and power consuming. This test will be done only during LAMB borad test. The result of the test will be read back through JTAG or Serial Link.

Serilizer and Deserializer channel scheme



Serial PRBS7 Generator



PRBS7 generator implementation using a LFSR (Linear Feedback Shift Register)

The sequence generated by an n-stage LFSR has a period of 2n – 1, it is a *maximum-length* sequence.

The polynomial for PRBS-7 is

$$PRBS7 = x^7 + x^6 + 1$$



Parallel PRBS7 Generator



A PRBS7 pattern (which is generated using an order 7 polynomial) may be sufficient to characterize a system which uses 8B/10B encoding.

Each clock cycle advances this PRBS generator by eigth positions. The current eight bits are provided as a parallel output of this circuit.

PRBS7 Checker



Before checking can begin, the