Introduction to CMOS Pixel Sensors

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OUTLINE

- Main features of CMOS pixel sensors
  - ▷ motivation ▷ principle: sensing & read-out ▷ limitations ▷ hit characteristics
- Achieved performances
  - ▷ means of evaluation ▷ beam test characterisation ▷ sources of performance degradation
- Applications
  - ▷ system integration aspects ▷ subatomic physics apparatus
- Outlook
  - ▷ 2D sensors ▷ 3D sensors
- Summary

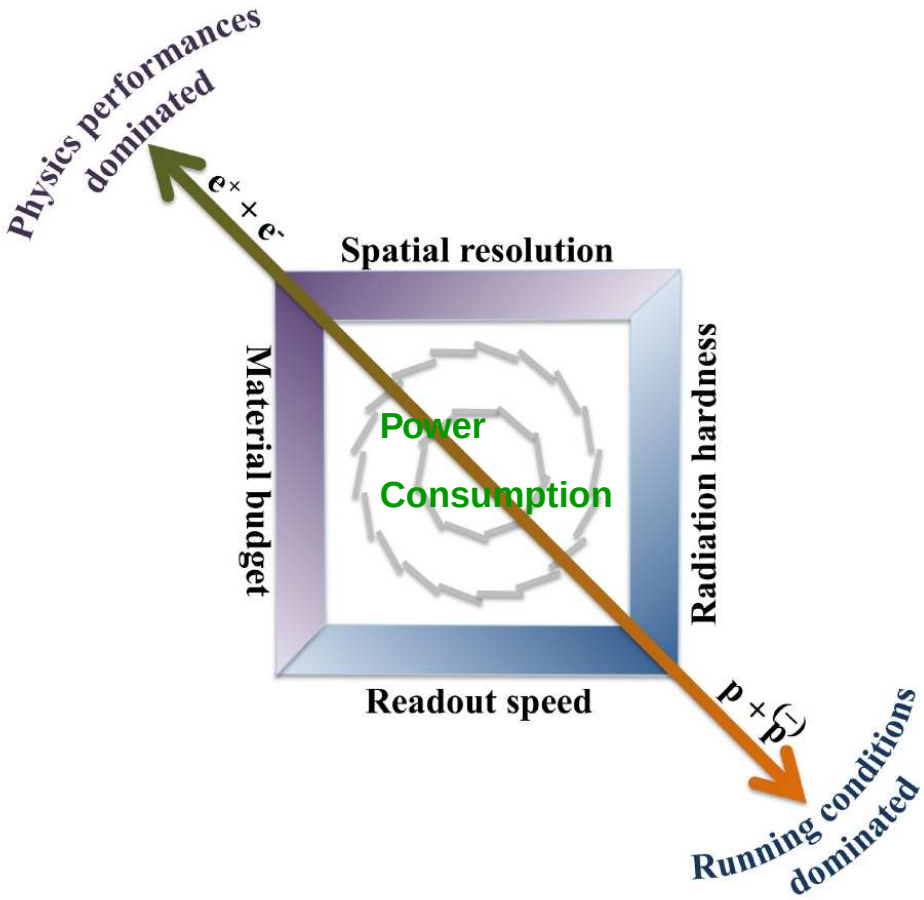
The Quadrature of the Vertex Detector

- CMOS pixel sensors offer the perspective of
  ”combining the extremes” (ultimately !)

- Several labs develop CMOS pixel sensors :
  Italy (Univ., INFN), UK (RAL), CERN,
  Germany (Heidelberg, Bonn, ...), USA,
  France (IPHC, Saclay), ...

- CMOS Pixel Sensors chosen/envisaged by growing number of subatomic physics experiments :
  - STAR at RHIC/BNL : commissionning
  - ALICE at LHC/CERN : under development
  - CBM at FAIR/GSI : under development
  - ILC : option
  - Etc.

- Variety of applications besides subatomic physics :
  dosimetry, hadrontherapy, γ & β counting, ...

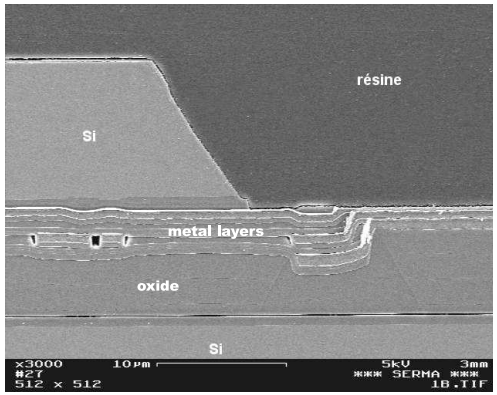


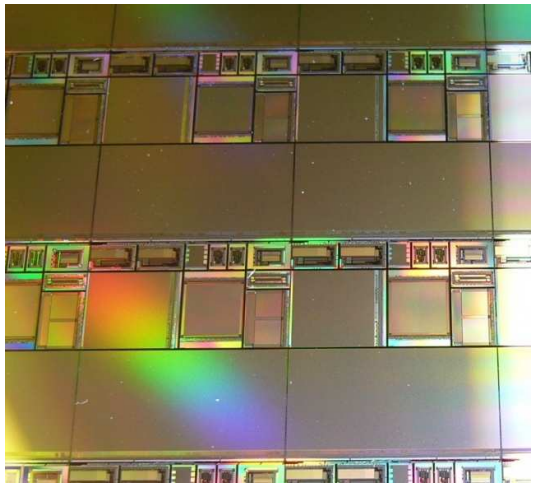
CMOS Technology

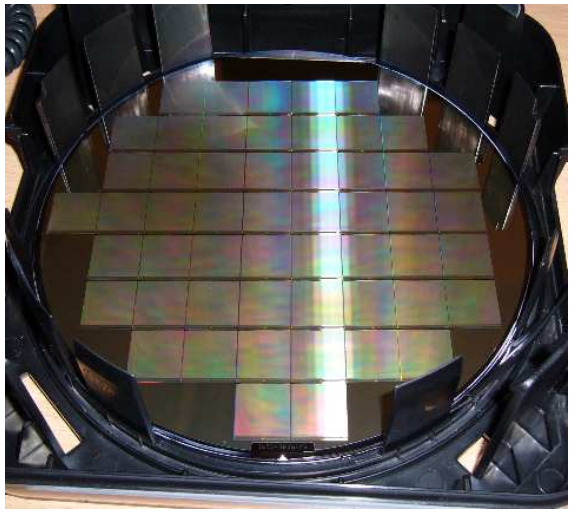
- **C.M.O.S. $\equiv$ Complementary Metal-Oxide-Semiconductor**

- **CMOS pixel sensors exploit the fabrication processes used in industry for mass production of integrated circuits :**
  - micro-processors, micro-controler, RAM, ...
  - cell phones & cameras, lap tops, cars, ...

- **CMOS fabrication mode :**
  - μcircuit lithography on a substrate
  - proceeds through reticules ($\sim$ 2x2 $\longmapsto$ 2x3 cm^2) organised in wafers (typically 8")

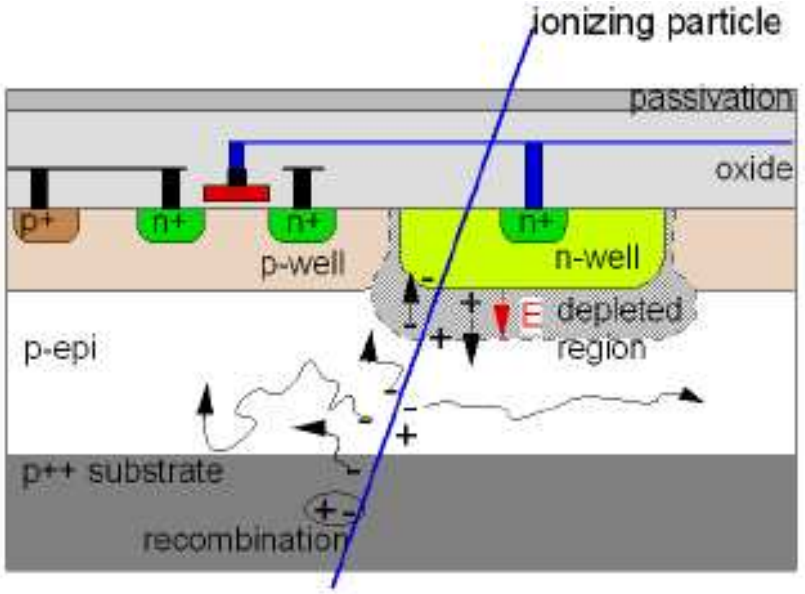






Main Features of CMOS Sensors

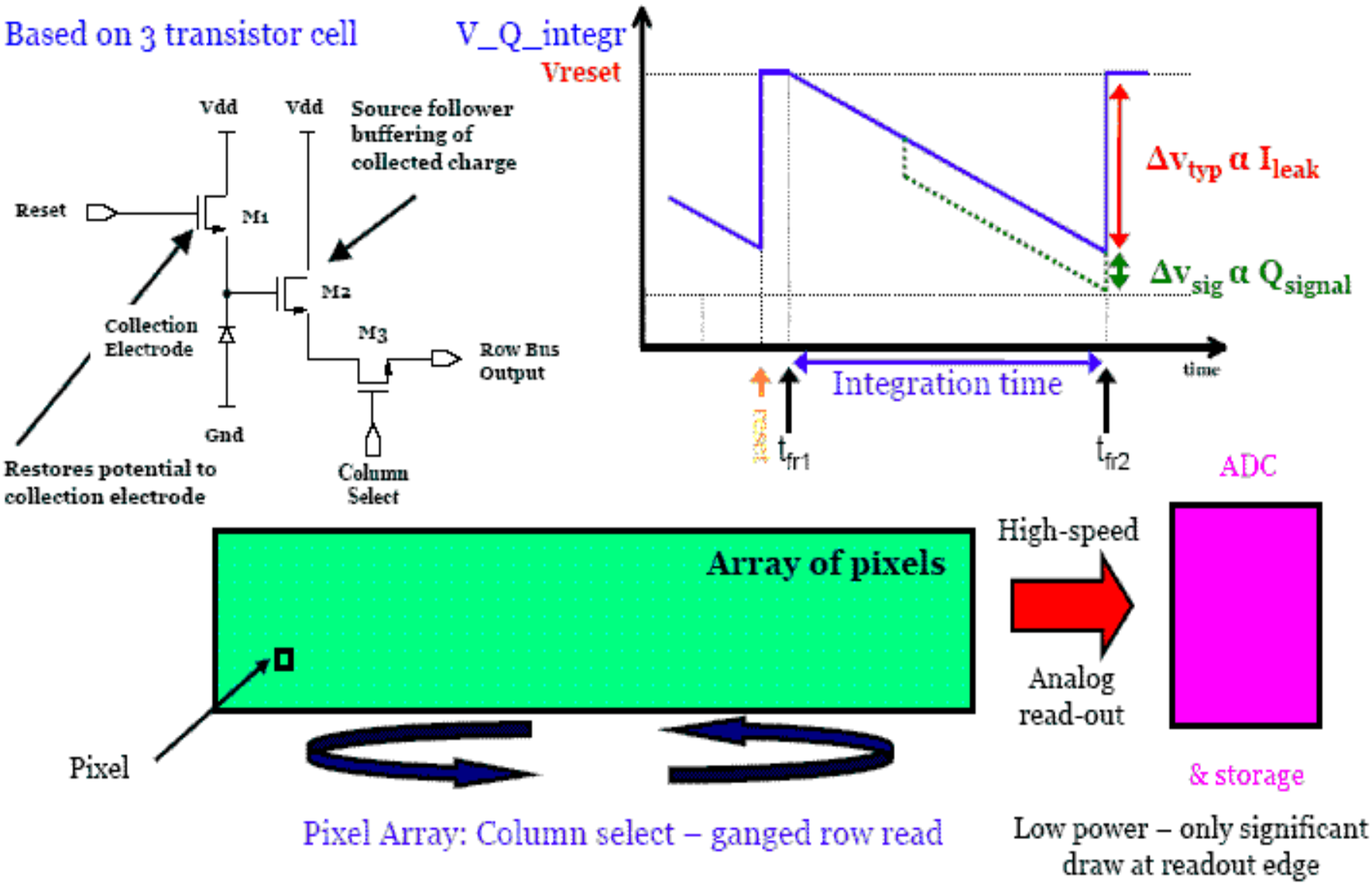
- P-type low-resistivity (O(10)$\Omega \cdot cm$) Si hosting n-type "charge collectors"
  - signal created in epitaxial layer (low doping):
    Q $\sim$ 70–80 e-h / $\mu m \mapsto$ signal $\lesssim$ 1000 e^-
  - charge sensing through n-well/p-epi junction
  - excess carriers propagate (thermally) to diode
    with help of reflection on boundaries
    with p-well and substrate (high doping)
    $\Rightarrow$ continuous signal sensing (no dead time)



- Prominent advantages of CMOS sensors :
  - ◇ **granularity :** pixels of $\lesssim 10 \times 10\ \mu m^2 \Rightarrow$ high spatial resolution (e.g. $\lesssim 1\ \mu m$ if needed)
  - ◇ **low material budget :** sensitive volume $\sim$ 10 - 20 $\mu m \Rightarrow$ total thickness $\lesssim 50\ \mu m$
  - ◇ **signal processing μcircuits integrated in the sensors** $\Rightarrow$ compacity, high data throughput, flexibility, etc.
  - ◇ **industrial mass production** $\Rightarrow$ cost, industrial reliability, fabrication duration, multi-project run frequency, technology evolution, ...
  - ◇ **operating conditions :** from $\ll 0^\circ$C to $\gtrsim$ 30-40°C

$\triangleright \triangleright \triangleright$ Thinning down to $\sim 30\ \mu m$ permitted

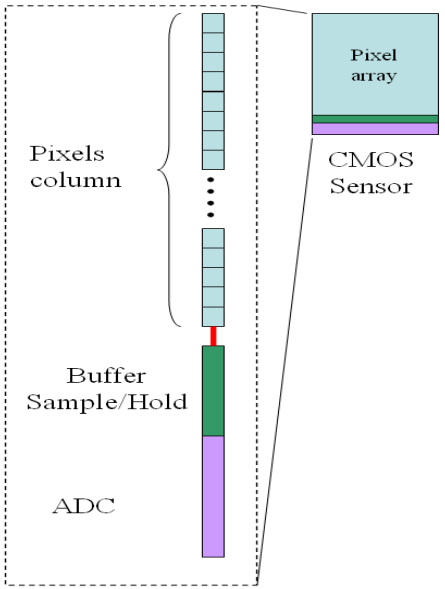
Basic Read-Out Architecture



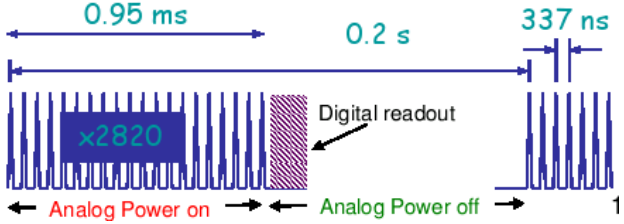
CMOS Pixel Sensors: Read-Out Architectures

- **Signal sensing and read-out are decoupled :**
  - ⁂ signal sensing (charge collection) is continuous (no dead time)
    - ⇛ signal read-out may be performed in various ways, independently of charge collection

- **Signal processing alternatives :**
  - ⁂ self-triggered : only fired pixels are (randomly) read-out ≡ hybrid pixels
  - ⁂ rolling shutter (less power consumption) : read-out of all pixels (A or D), followed by sparsification outside of sensitive area ▷▷▷▷
  - ⁂ snap-shot : requires 2 consecutive read-outs, with 1 used for average noise subtraction (rather suited to light imaging due to up to 50 % dead time)



- **Signal transfer alternatives :**
  - ⁂ continuous : permanent output to outside world
  - ⁂ intermittent : signal stored on chip until read-out sign is provided
    - ↪ event based trigger or beam time structure (ILC) ▷▷▷

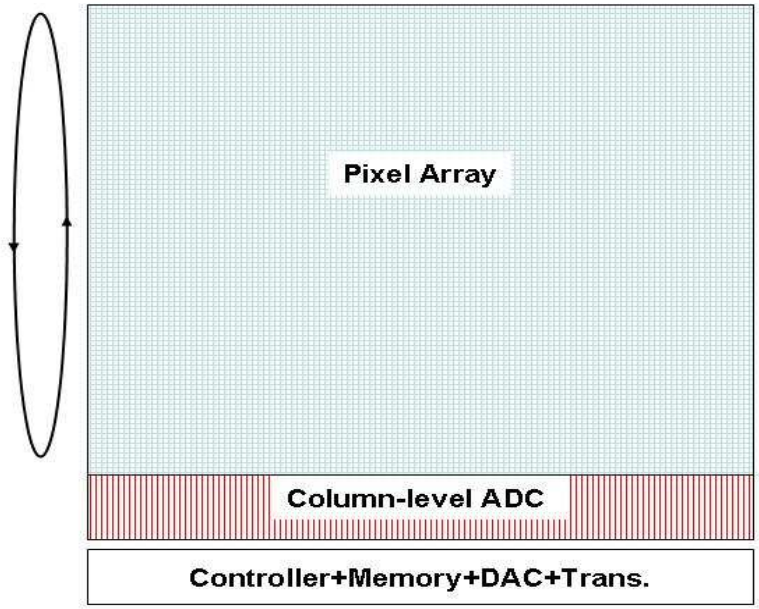


Overview of Rolling Shutter Architecture

- **Sensor organisation :**
  - ⁕ Signal sensing and analog processing in pixel array
  - ⁕ Mixed and Digital circuitry integrated in chip periphery
  - ⁕ Read-out in rolling shutter mode

    (pixels grouped in columns read-out in //)

  ⇛ trend : increase functionnalities inside pixels



- **Main consequences :**
  - ⁕ **Read-out speed :**

    ≡ integration time

    ≡ nb of pixels × pixel read-out time (O(100 ns))
  - ⁕ **Power consumption :**

    limited inside the pixel array to the row(s) being read out
  - ⁕ **Material budget :**

    peripheral band(s) for mixed+digital circuitry, insensitive to impinging particles

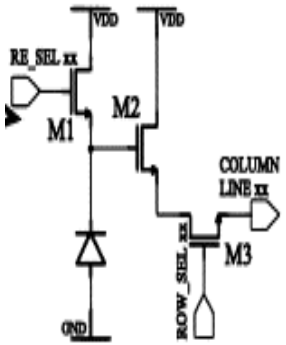
    ↪ ∼ 10 % of chip surface
  - ⁕ **Time stamp :**

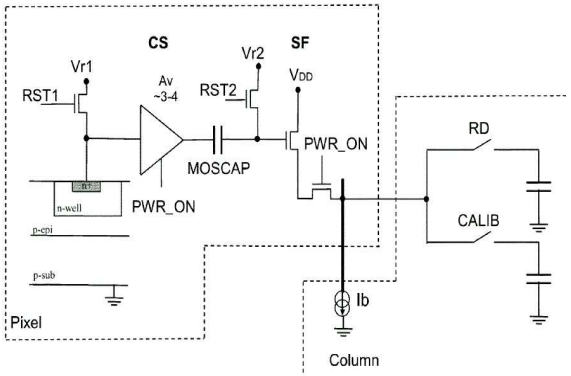
    each row encompasses a specific time intervalle ⇛ adapt (≡ exploit with) track reconstruction code

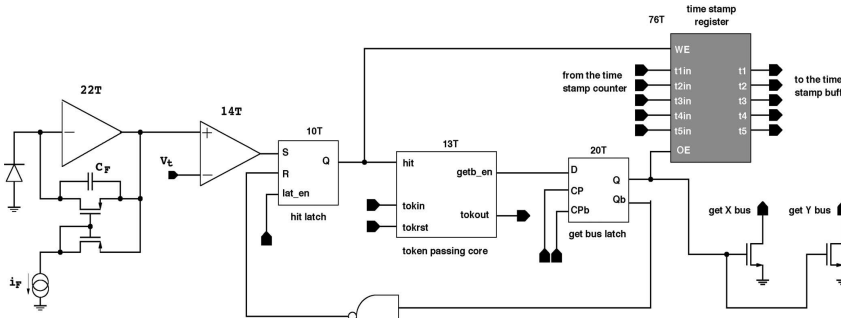
Signal Sensing & Processing Architectures

- **Main sensing and read-out micro-circuit elements :**
  - in-pixel conversion of charge into electrical signal (e.g. voltage) with average noise subtraction
  - signal discrimination (in perspective of zero-suppression)
  - discriminator output encoding (sparsification with charge encoding)
  - data transmission logic ⟶ connection with the outside world

- **In-pixel μcircuitry :**







basic read-out *pre-amp + <noise> subtraction* *pre-amp + shaper + discriminator*

Data Reduction : outside chip chip periphery inside pixel

Limitations of the Technology

- **Very thin sensitive volume**

  $\Rightarrow$ impact on signal magnitude (mV !) $\Rightarrow$ very low noise FEE required

- **Sensitive volume only partly depleted**

  $\Rightarrow$ negative impact on radiation tolerance & speed but positive on σ_{sp} (charge spread)

  $\triangleright$ **tendency :** high-resistivity epitaxial layer $\Rightarrow$ improved radiation tolerance (SNR)

- **Commercial fabrication**

  $\Rightarrow$ fabrication parametres (doping profile $\rightarrowtail$ epitaxial layer, number of metal layers, etc.)

  not optimal for charged particle detection *(optimised for commercial items)* :

  $\ast$ real potential of CMOS pixel sensors not exploited (yet !)

  $\ast$ choice of process for HEP often driven by epitaxial layer characteristics (governs signal),

  at the expense of the FEE circuitry parametres (feature size, nb of Metal Layers)

- **Use of P-MOS transistors inside pixel array restricted in most processes**

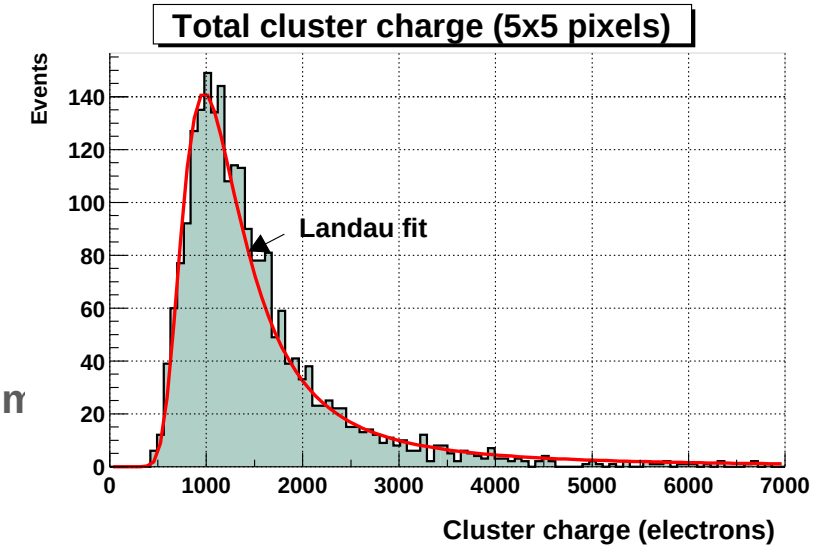
  $\Rightarrow$ limited signal processing functionnalities inside (small) pixels (most performed on sensor periphery)

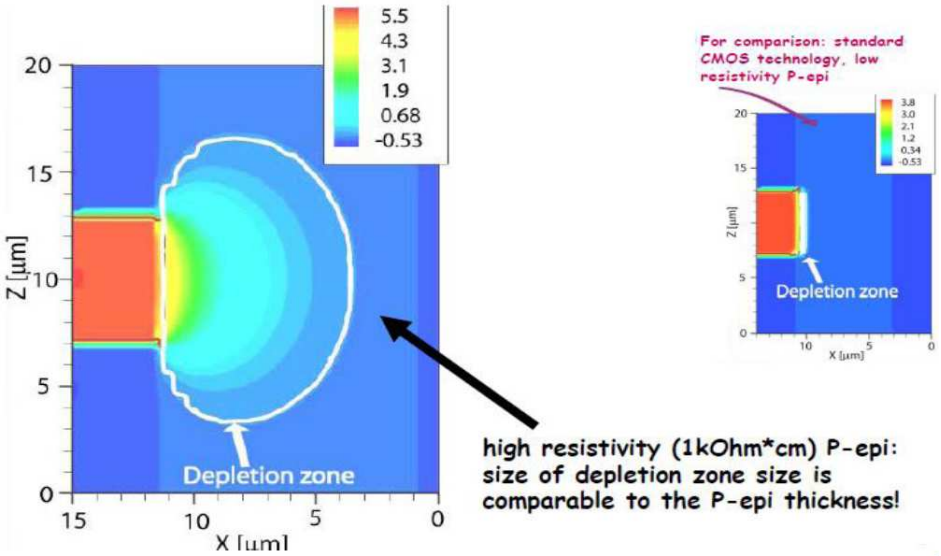
  $\triangleright$ **tendency :** buried P-well techno. $\Rightarrow$ allows use of P-MOS transistors (watch charge coll. eff. !)

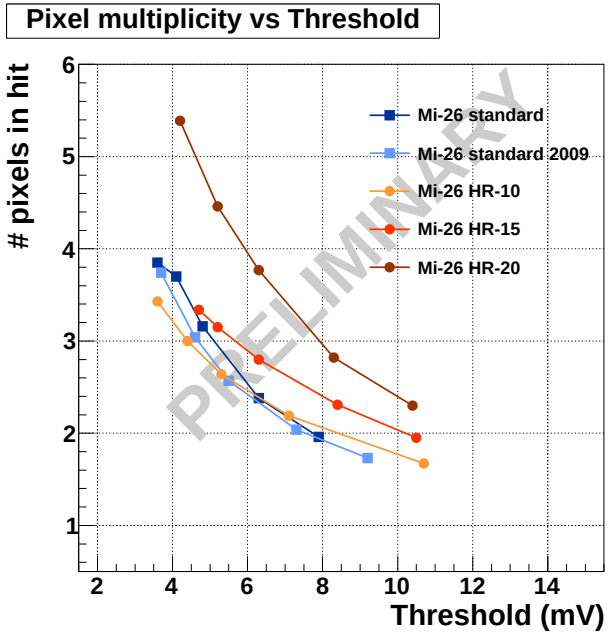
Hit Characteristics

- **Standard processes : charges diffuse thermally**
  - $\lesssim 10^3$ e^- shared among $\sim$ 10-15 pixels per cluster
  - typically $\lesssim$ 200/300 e^- (MPV) in seed pixel

- **High-resistivity epitaxy (O(k$\Omega \cdot cm$) : larger charge sensing volun**
  - less diffusion $\Rightarrow$ less pixels/cluster (typically $\lesssim$ 4)
  - larger charge collected/pixel (e.g. $\sim$ 500 e^-) $\Rightarrow$ higher SNR







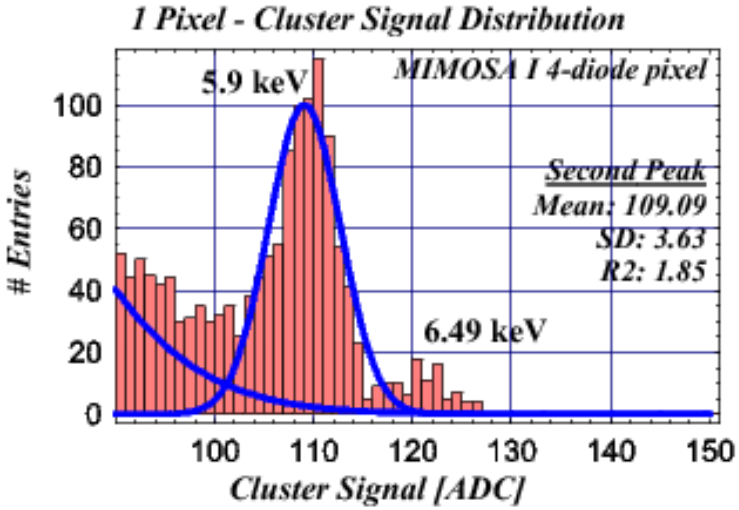
Calibration of Charge-to-Voltage Conversion Factor

- **Goal :** establish a well defined correspondence between the measured sensor output voltages and the amplitude of the charge collected by each diode

- Mean : use radioactive sources emitting particles with adapted and well defined energy

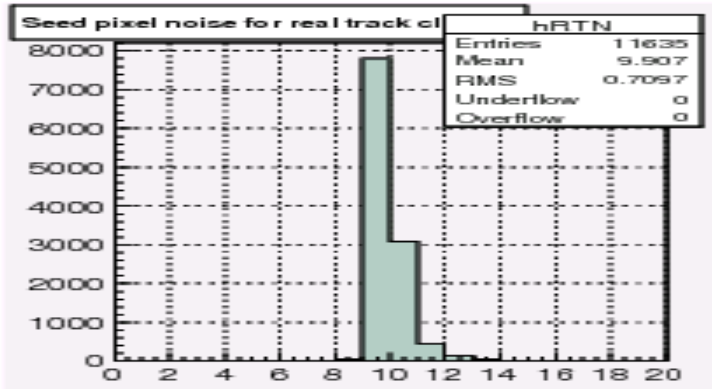
- **Ex: ^{55}Fe source**
  - emits X-Rays with 5.9 keV ($\sim$ 90%) or 6.49 keV ($\sim$ 10%)
  - X-Rays interact with Si atoms through photo-electric effect
    $\Rightarrow$ the ejected p.e. carries $\sim$ 100% of the X-Ray energy (e^- binding energy ...)
  - the p.e. creates eh pairs at the expense of $\sim$ 3.6 eV per pair
    $\Rightarrow$ 5900/3.6 $\simeq$ 1640 eh pairs (6490/3.6 $\simeq$ 1800 eh)

- **Calibration with ^{55}Fe X-Rays**
  - a small fraction of X-Rays impinge sensor near sensing diode
    $\Rightarrow$ nearly all e^- created get collected by nearby sensing diode
  - the charge distribution observed on the ADC scale exhibits 2 peaks

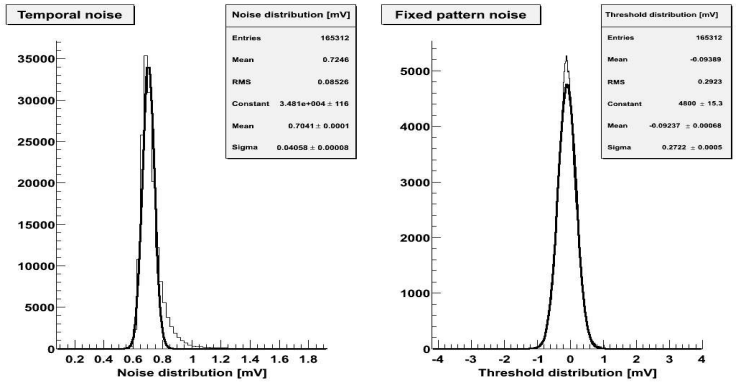


Sensor Noise: Sources, Reduction Strategies

- **Main Sources :**
  - in pixel : sensing diode capacitance ▷▷▷
  - in pixel : leakage current collected by sensing diode ▷▷
  - outside pixel : signal processing micro-circuits

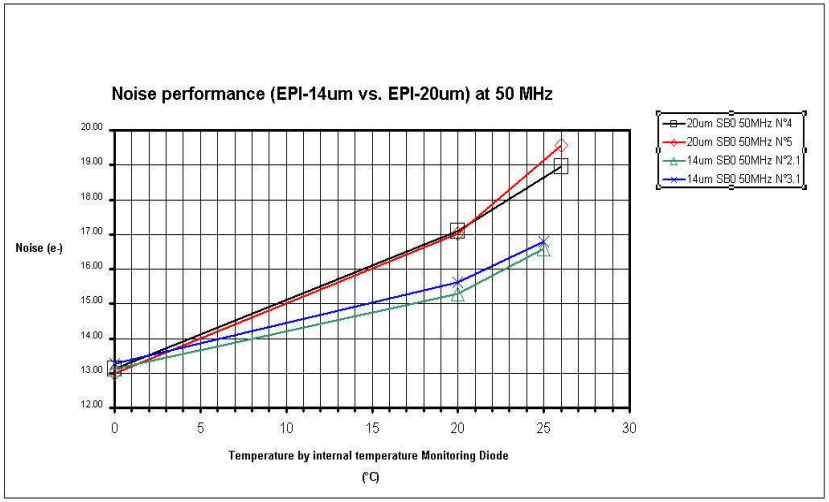


- **Tricks to minimise the noise :**
  - maximal amplification inside pixel
    - ⇛ minimises impact of the noise ▷▷▷
      of signal processing micro-circuits



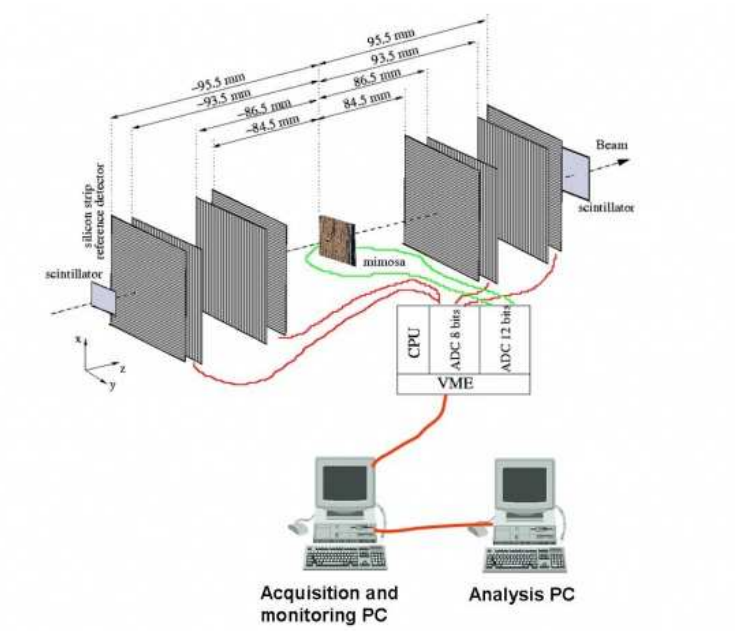
  - operate chip with short integration time
    - ⇛ minimises integrated leakage current

  - operate chip at low temperature ▷▷▷
    - ⇛ minimises thermal noise

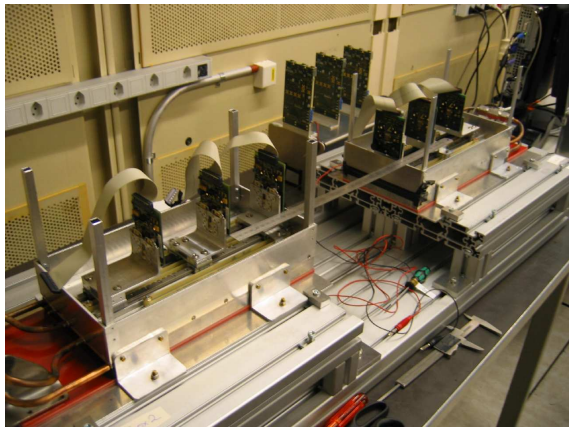


M.I.P. Detection Performance Evaluation

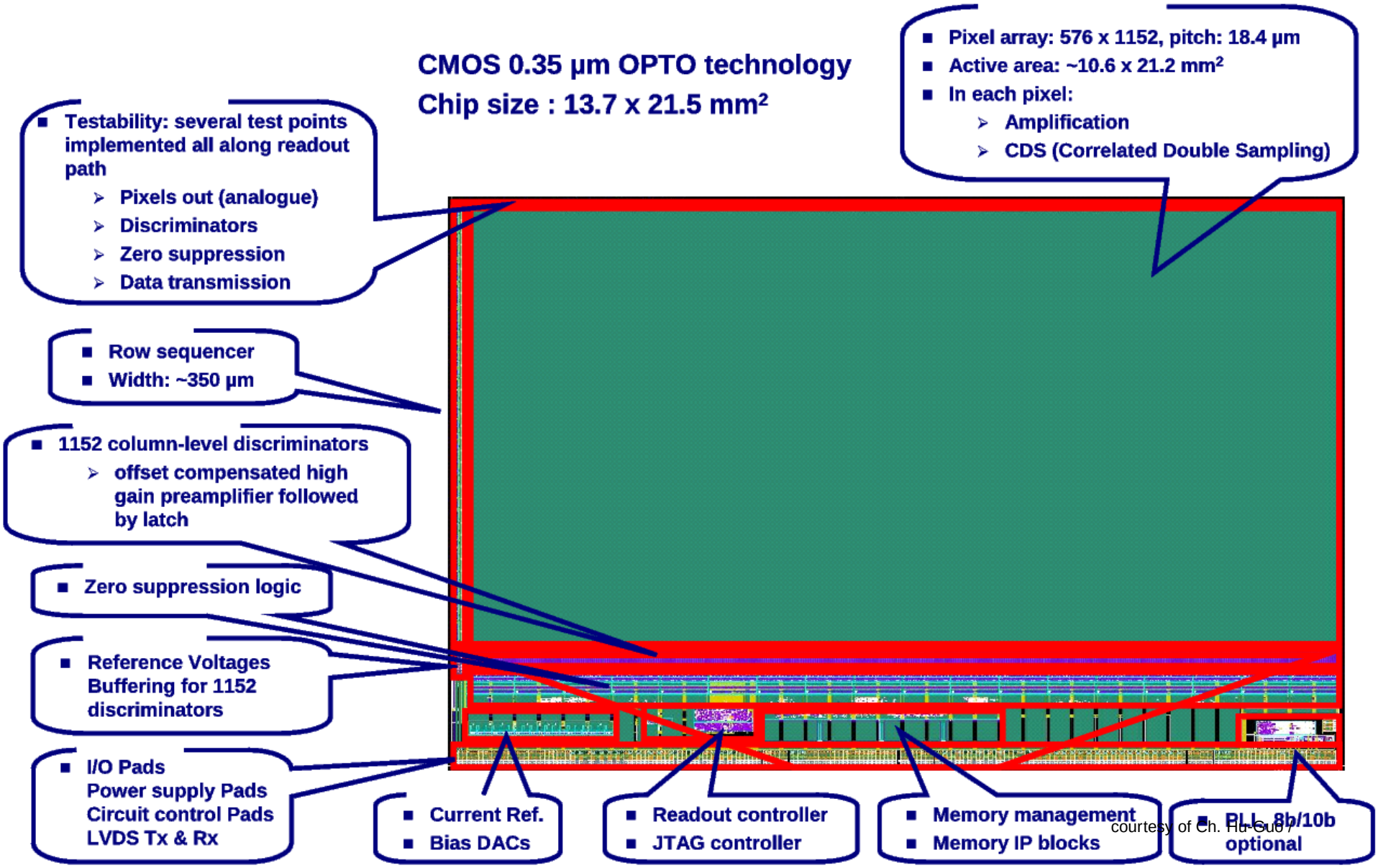
- **Laboratory :**
  - ⁕ test steering & read-out functionalities (e.g. pattern generator)
  - ⁕ evaluate charge collection efficiency & noise (^{55}Fe, light)
  - ⁕ assess charge-to-voltage conversion factor (^{55}Fe)
  - ⁕ estimate ”m.i.p.” detection efficiency with β (^{106}Ru)



- **Particle beams :**
  - ⁕ typically $\sim$ 100 GeV/c π^- at CERN-SPS *(not really m.i.p.)*
    $\Rrightarrow$ minimise multiple scattering
  - ⁕ install chip to test inside beam telescope (EUDET BT)
  - ⁕ determine :
    - ○ detection efficiency (and SNR)
    - ○ fake hit rate (and noise)
    - ○ single point resolution
    - ○ etc.

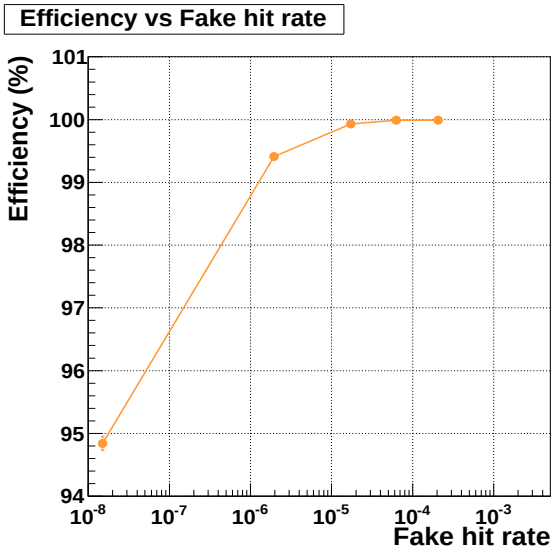


CMOS Pixel Sensors: State of the Art

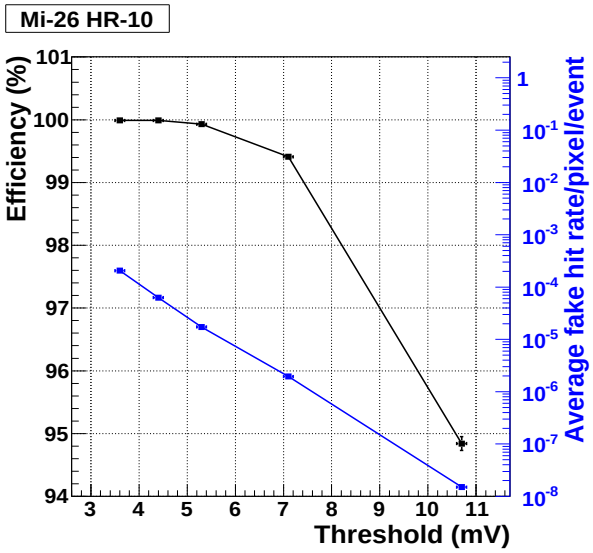


M.I.P. Detection Efficiency & Fake Hit Rate

- **Motivation :** find a sensor working point
  with high detection efficiency and marginal
  contamination from noise fluctuations (fake hits)



- **Detection efficiency**
  - fraction of tracks reconstructed in telescope
    which are also reconstructed in the sensor
  - study as function of discriminator threshold
  - a high threshold may harm detection efficiency $\Rightarrow$ Trade-off !



- **Fake hit rate**
  - fraction of noise fluctuations which pass the discriminator threshold
  - study as a function of discriminator threshold
  - a high threshold is best to keep fake rate marginal, but ...
    (typically $\lesssim 10^{-3/-4}$)

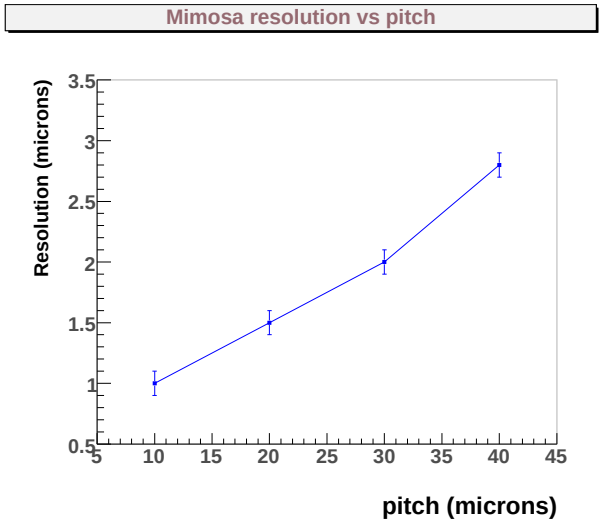
Spatial Resolution

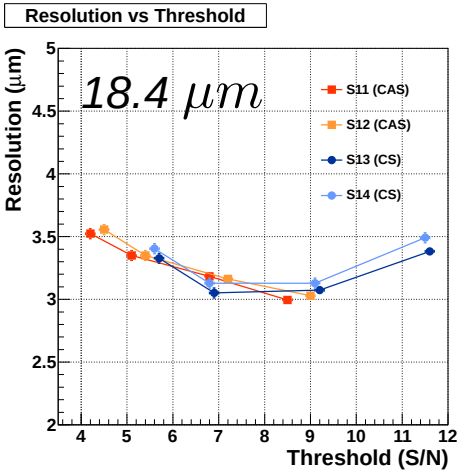
- Compare position of impact on sensor surface predicted with BT to postion of hit reconstructed with sensor under test :
  clusters reconstructed with eta-function,
  exploiting charge sharing between pixels

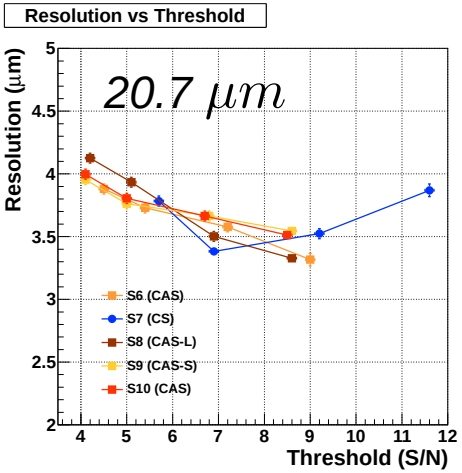
- Impact of pixel pitch (analog output) : ▷▷▷
  $\sigma_{\mathbf{sp}} \sim \mathbf{1}\ \mu\mathbf{m}$ (10 μm pitch) $\longmapsto$ $\lesssim \mathbf{3}\ \mu\mathbf{m}$ (40 μm pitch)

- Impact of charge encoding resolution :
  ▷ ex. of 20 μm pitch $\Rrightarrow$ σ_{sp}^{digi} = pitch/$\sqrt{12} \sim$ 5.7 μm

Nb of bits	**12**	3-4	1
Data	*measured*	*reprocessed*	*measured*
σ_{sp}	$\lesssim 1.5\mu m$	$\lesssim 2\mu m$	$\lesssim 3.5\mu m$







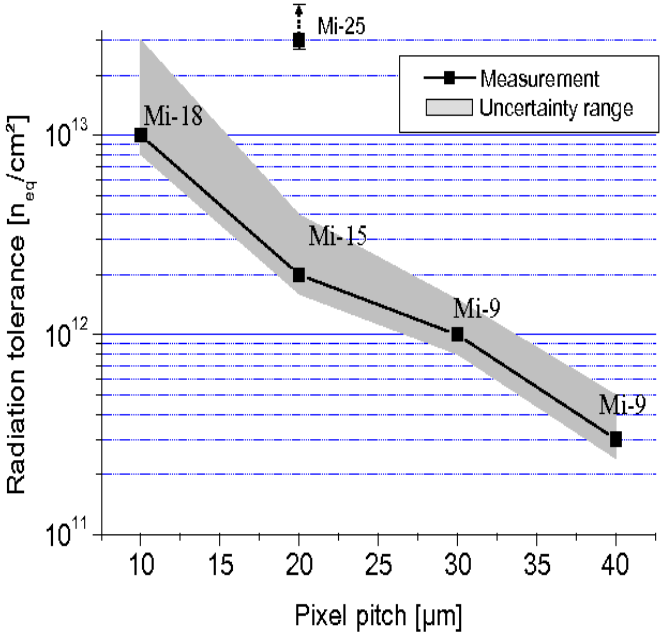
Radiation Tolerance

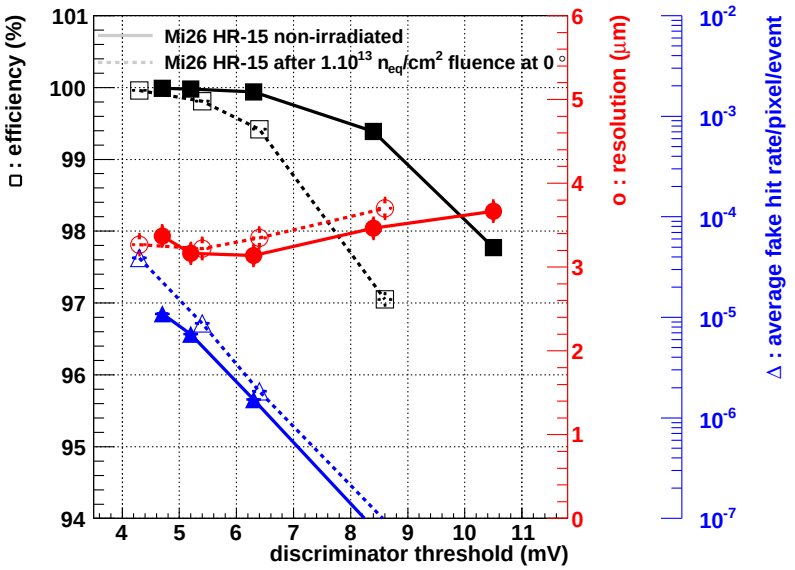
- **Introductory remarks :**
  - ⁕ still evolving (csq of CMOS industry process param. evolution)
  - ⁕ CMOS technology expected to tolerate high ionising radiation doses ($\gg$ 10 MRad), in particular with T $< 0^{\circ}$C & short t_{integ}
  - ⁕ main a priori concern : NON-ionising radiation (in absence of thick depleted sensitive volume)

- **Influence of pixel pitch :** ▷▷▷
  - ⁕ fig: all measts done with low resistivity epitaxial layer, but 1
  - ⁕ high density sensing diodes ($\equiv$ small pitch) improves non-ionising radiation tolerance

- **Influence of epitaxial layer resistivity :**
  - ⁕ ex: 400 $\Omega \cdot cm$ & O(1)V depletion voltage ▷▷▷
  - ⁕ trend : $\gtrsim 1\ k\Omega \cdot cm$ & $\gtrsim$ 10 V

$\Rightarrow$ **Tolerance to $\gtrsim 10^{14-15}$ n_{eq}/cm^2 seems achievable**





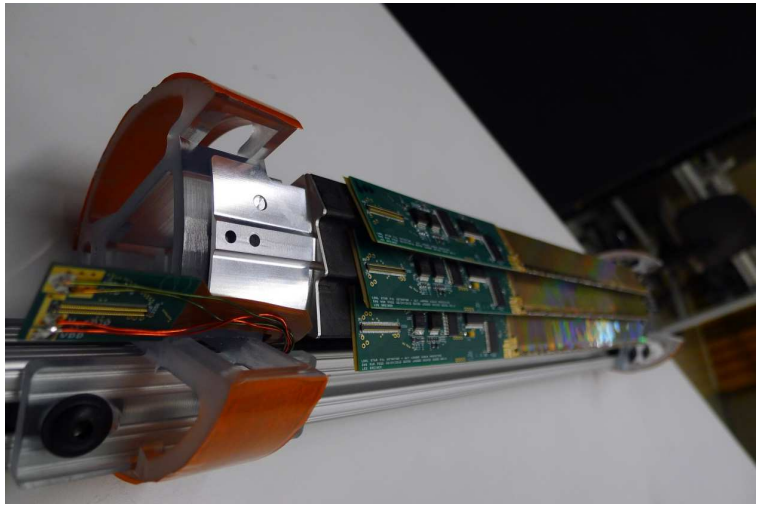
Sensor Integration in Ultra Light Devices

- **"Useful" sensor thickness $\lesssim$ 30 μm** $\Rightarrow$ *opens up new possibilities w.r.t. thicker sensors*

  $\triangleright$ *coarse thickness of sensors (e.g. STAR-PXL) is 50 μm*

- **STAR-PXL ladder** (room temperature, single-end supported)**:**

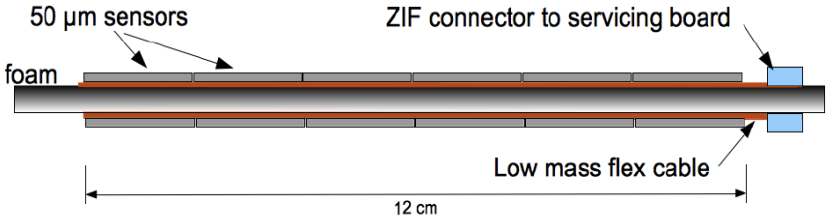
  - total material budget $\simeq$ 0.37 % X_0 :
    - 50 μm thin sensors $\simeq$ 0.05 % X_0
    - flexible cable $\simeq$ 0.07 % X_0
    - mechanical support $\simeq$ 0.2 % X_0
    - adhesive, etc. $\simeq$ 0.05 % X_0



- **Double-sided ladders with $\sim$ 0.2-0.3 % X_0 :**

  $\Rightarrow$ manifold bonus : compactness, alignment, redundancy,

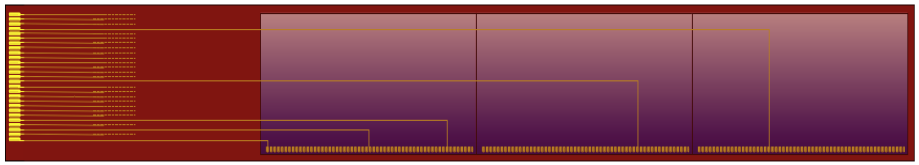
  pointing accuracy (shallow angle), fake hit rejection, etc.



- **Unsupported & flexible ladders with $\lesssim$ 0.15 % X_0**

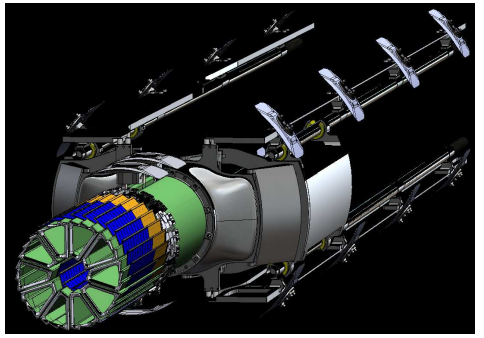
  $\Rightarrow$ 30 μm thin CMOS sensors mounted on thin cable

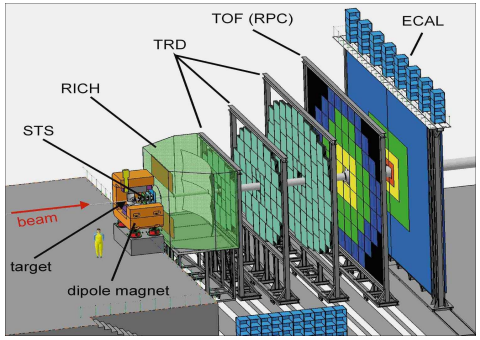
  & embedded in thin polyimide $\rightarrowtail$ suited to beam pipe ?

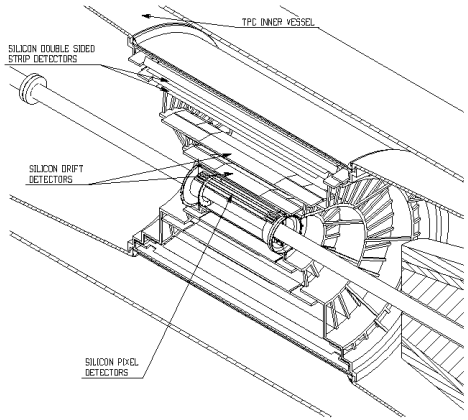


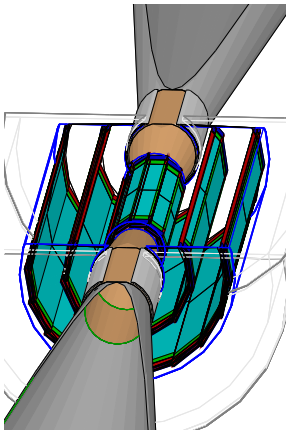
Examples of Applications in Subatomic Physics

- Beam telescopes :
  - EUDET (FP-6 / 2006-2010) : 6 planes with 1×2 cm^2 sensors
  - AIDA (FP-7 / 2011-2015) : $\geq$ 3 planes with 4×6 cm^2 sensors
- Vertex detectors :
  - STAR-PXL at RHIC : 2 layers
  - CBM-MVD at FAIR/GSI : 2-3 stations
  - ALICE-ITS at LHC : 3 inner layers
  - FIRST at GSI (p/C PMMA x-sec) : 4 stations
  - option for ILD-VTX at ILC : 3 double-layers
- Trackers (”large pitch”) :
  - BES-III at BEPC
  - ALICE-ITS at LHC : 4 outer layers (*$\lesssim$ 10 m^2 !*)
  - in general : trackers surrounding vertex detectors
- EM calorimetres : SiW calorimetre
  - generic R&D on **T**RA**C**AL



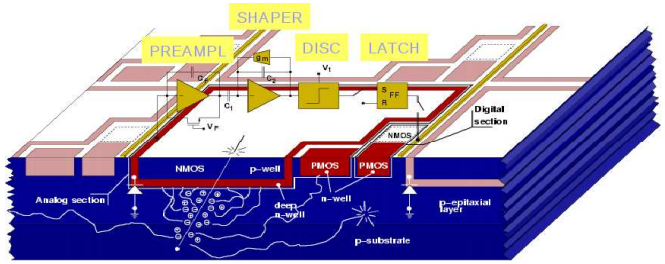


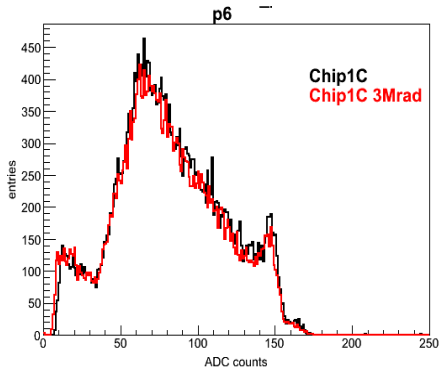


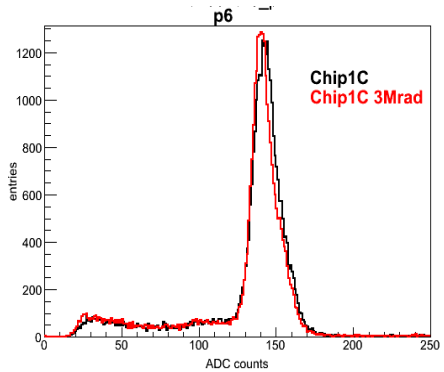


Perspectives: Fast 2D sensors

- **Evolve towards feature size $<<$ 0.35 μm :**
  - μcircuits : smaller transistors, more Metal Layers, ...
  - sensing : quadruple well, depleted sensitive volume, ...
- **Benefits :**
  - faster read-out $\Rightarrow$ improved time resolution
  - higher μcircuit density $\Rightarrow$ higher data reduction capability
  - thinner gates, depletion $\Rightarrow$ improved radiation tolerance
- **On-going R&D (examples) :**
  - *APSEL* sensor (130 nm) for future Vx Det. :
    - in-pixel pre-amp + shaping + discri. $\triangleright\triangleright\triangleright$
    - sensing through buried n-well
    - shallow n-well hosting P-MOS T
  - *TJSC* project (180 nm) for ALICE-ITS upgrade :
    - high-resistivity, 18-40 μm thick, epitaxy $\triangleright\triangleright\triangleright$
    - deep P-wells hosting P-MOS T







- **Main limitations :**
  - VDSM technologies not optimised for analog μcircuits (low V !) $\Rightarrow$ reliability
  - conflict between speed (e.g. 10 ns) and granularity (e.g. 20$\times$20 μm^2 pixels)

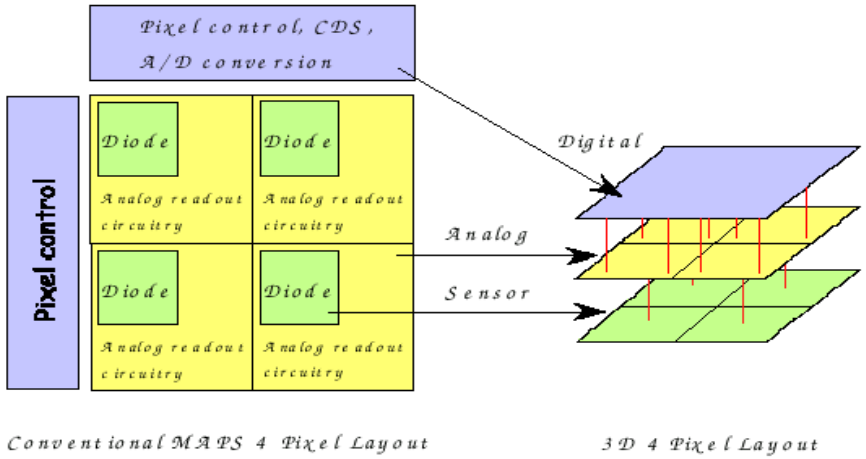
$\Rightarrow$ **Natural trend : chip stacking**

Using 3DIT to reach Ultimate CMOS Sensor Performances

- 3D Integration Technologies allow integrating high density signal processing μcircuits inside **small** pixels
  by stacking ($\sim$ 10 μm) thin tiers interconnected at pixel level

- 3DIT are expected to be particularly beneficial for (small pixel) CMOS sensors :
  - combine different fab. processes $\Rightarrow$ chose best one for each tier/functionnality
  - alleviate constraints on peripheral circuitry and on transistor type inside pixel, etc.

- Split signal collection and processing functionnalities :
  - *Tier-1: charge sensing*
  - *Tier-2: analog-mixed μcircuits*
  - *Tier-3: digital μcircuits*



- **The path to nominal exploitation of CMOS pixel potential :**
  - fully depleted 10-20 μm thick epitaxy $\Rightarrow$ $\lesssim$ 5 ns collect. time, rad. hardness $>$ Hybrid Pix. Sensors ???
  - FEE with $\leq$ 10 ns time resolution $\rightarrowtail$ solution for CLIC & HL-LHC specifications ???

- **3DIC $\equiv$ consortium coordinated by FermiLab has already produced 1st generation of chips**

SUMMARY

- **CMOS sensor technology has become mature for high performance vertexing and tracking**
  - ⁕ most relevant for specifications governed by granularity, material budget, power consumption, cost, ...
  - ⁕ excellent performance record with beam telescopes (e.g. EUDET project)
  - ⁕ 1st vertex detector experience will be gained with STAR-PXL, starting data taking in a few weeks ...
  - ⁕ new generation of sensors under development for experiments $>$ 2015 (including trackers & calo.)
    - $\hookrightarrow$ ALICE-ITS upgrade (see also talk of W. Snoeys), CBM-MVD (FAIR), ..., ILC VD (?), ...

- **Technology full potential still far from being exploited**

  (despite improvement due to high-resistivity epitaxial layer processes)

- **Evolution of industry opens the door to 2 ”natural” steps**

  towards the ”ultimate” performances of the technology :
  - ⁕ **fast 2D sensors** based on VDSM CMOS technologies may allow for $\lesssim$ O(1) μs, $\gg$ 10 MRad
  - ⁕ **3D chips** are expected to ”exhaust” the technology potential, but there is still a rather long way to go

$\Rightarrow$ **may lead to fast & rad. hard devices suited to HL-LHC & CLIC**