Update on the Analog Section and Peripheral Blocks of the FE chip for the Silicon Strip Detectors

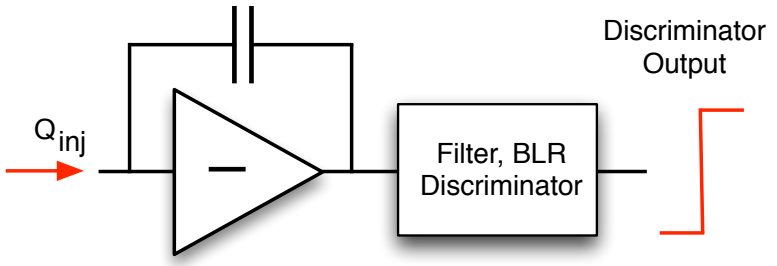
Massimo Manghisoni

November 28, 2012

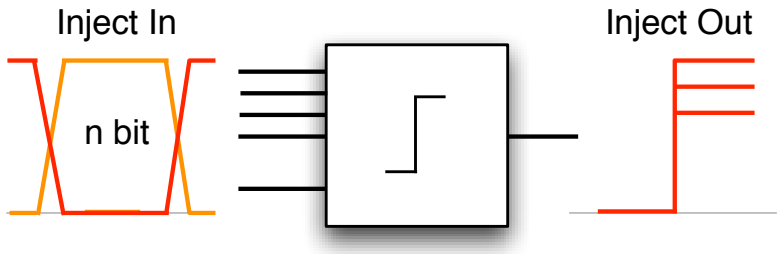
Outline

Analog Section of the readout channel

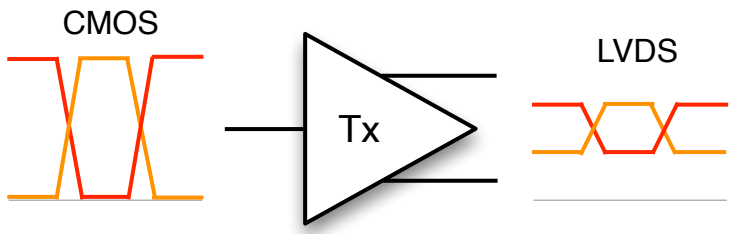
- Four-corners analysis
- Baseline restorer



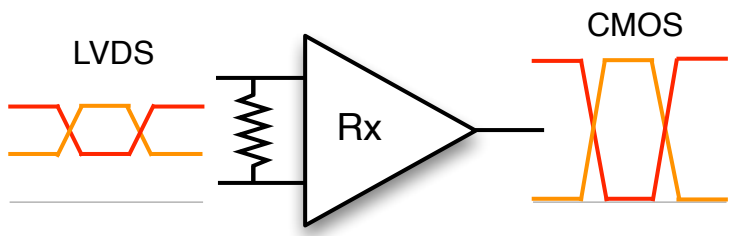
Injection Circuit injects a charge, with selectable amplitude, at the input of the front-end



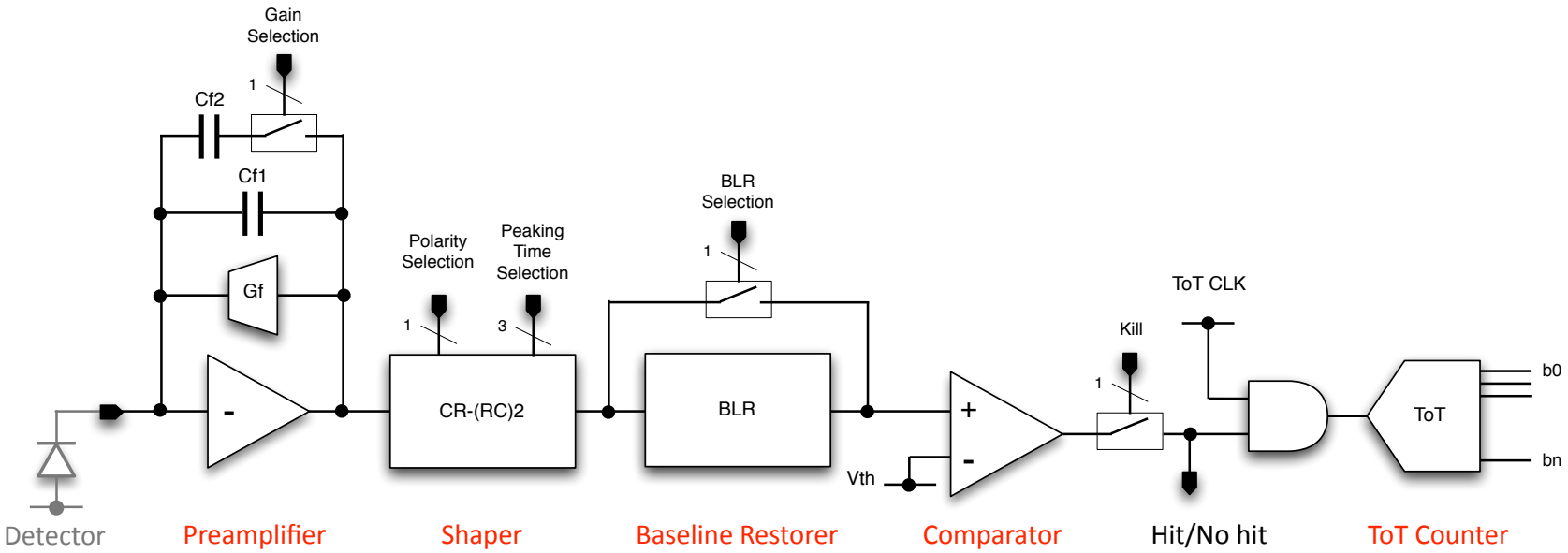
LVDS Output pad converts the CMOS signal at the input of the block in to LVDS signal to send data out of the DSSC chip



LVDS Input pad converts the LVDS signal at the input of the DSSC chip in to CMOS signal



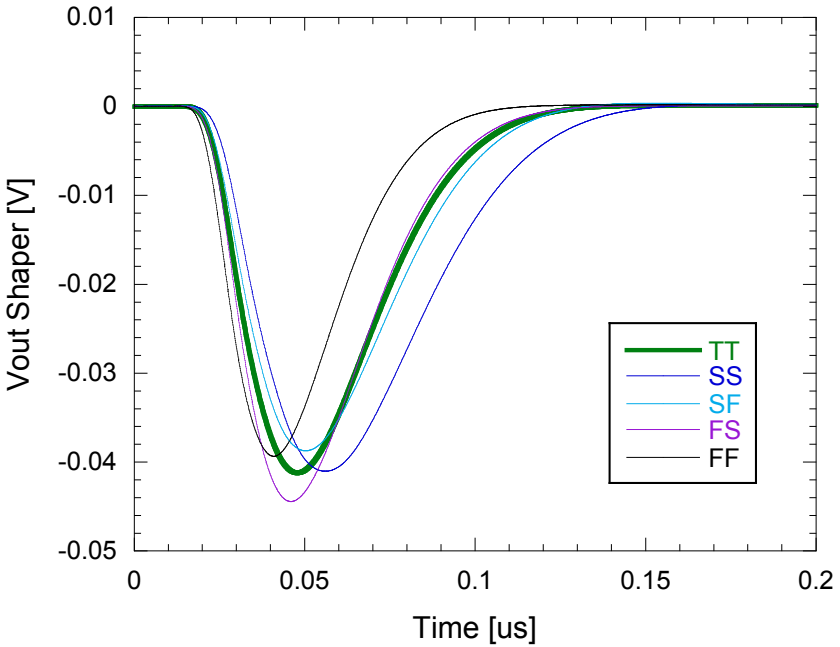
Analog channel block diagram



- Charge-sensitive preamplifier with gain selection (1 bit)
- Unipolar semi-Gaussian shaper with polarity (1 bit) and peaking time (3 bit) selection options
- Asymmetric baseline restorer to achieve baseline shift suppression, may be included or not (1 bit)
- Hit discriminator (comparator)
- 3-4 bit analog-to-digital conversion will be performed by a Time-Over-Threshold (TOT) detection

Four-corners analysis

- The analog channel was simulated with the four corner models
- The spread in gain and peaking time was reduced by modifying the bias of critical reference devices in the first and second shaper stage

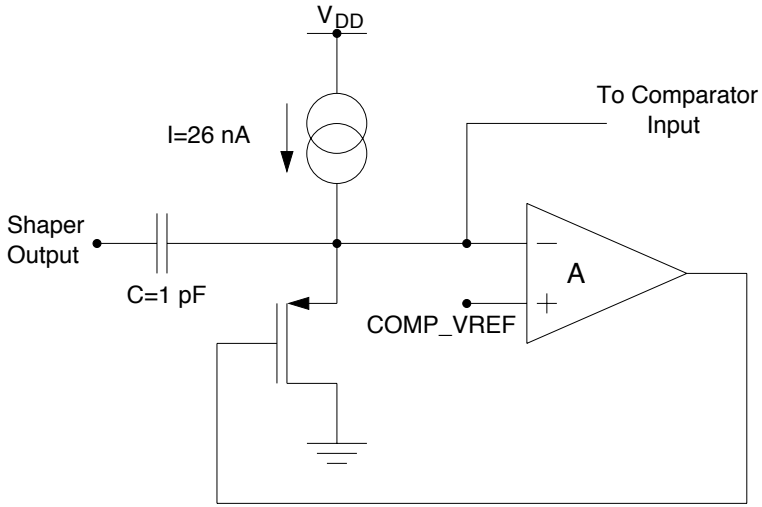


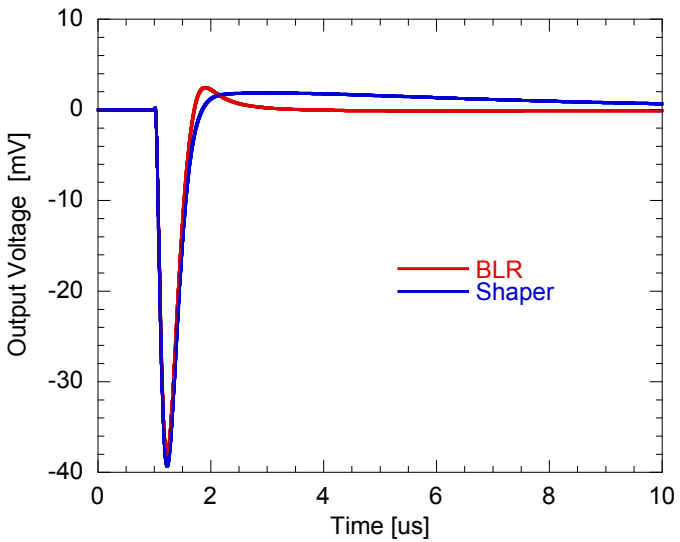
Nominal Peaking Time [ns]	Model	Signal Peaking Time [ns]	Charge Sensitivity [mV/fC]
25	TT	32	16
	FF	38	16
	FS	33	15
	SF	31	17
	SS	28	15

- Variations in peaking time: less than ± 19 % at 25 ns
- Variations in charge sensitivity: less than ± 8 % at 25 ns

Baseline Restorer (BLR)

- The unipolar pulse at the shaper output is followed by an overshoot decaying with a time constant of several microseconds
- This results in a baseline shift at the shaper output which also affects the comparator threshold
- ⇒ Asymmetric DC restorer





The PMOS acts as a switch:

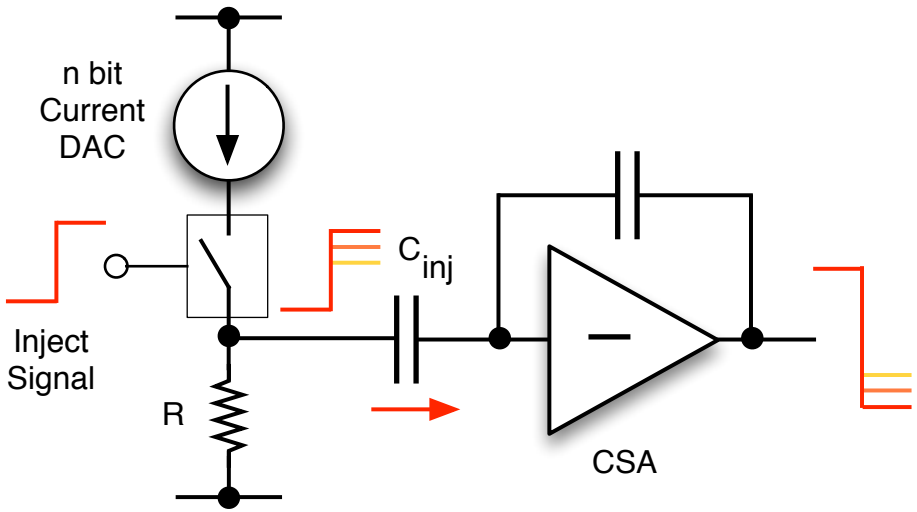
- open during the duration of the negative pulse at the shaper output ⇒ this portion of the signal is transmitted to the comparator input with no alteration
- close at the end of the pulse ⇒ ensuring a rapid return of the pulse waveform to the baseline and eliminating the long tail in the shaper output signal

The effect of using a BLR on the noise performances is presently under investigation

Injection Circuit

Generates a signal corresponding to the one delivered by the strip sensor and feeds it directly into the input of the detector readout circuit

- The injected charge is obtained by applying a voltage step to an injection capacitance integrated in the channel
- The voltage step is obtained by switching the current provided by a current steering DAC on a resistor



Dynamic range and resolution:

- Explore the full dynamic range of the signals delivered by the sensor $\Rightarrow$ 15 MIP
- 1th point lower than the required analog resolution $\Rightarrow$ 0.2 MIP

	Q_{MIN} [ke-]	Q_{MAX} [ke-]
L0	3.2	240
L1-L5	4.8	360

Requirements fulfilled with **7 bit** and Q_{MAX}=360 ke- $\Rightarrow$ Q_{LSB}**=2.81 ke-**

7-bit current steering DAC

- Unary current source architecture with 127 cells arranged in a two-dimensional array (8×16)
- Thermometric selection of current cells

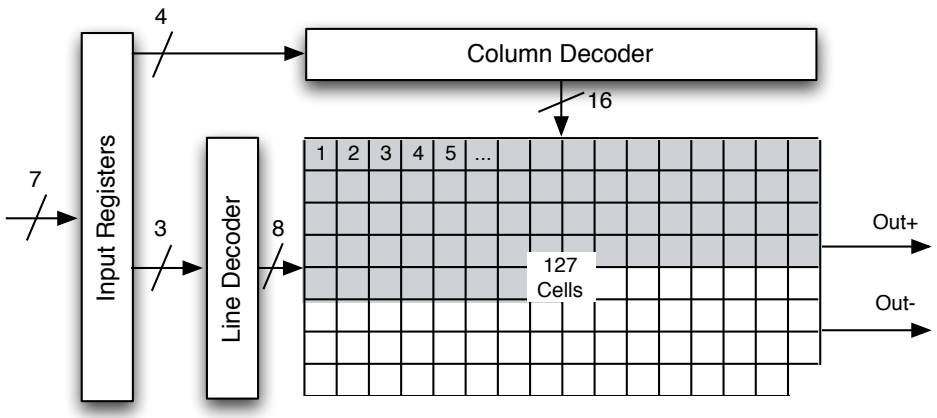


Figure: 7-bit DAC with thermometric selection of current cells.

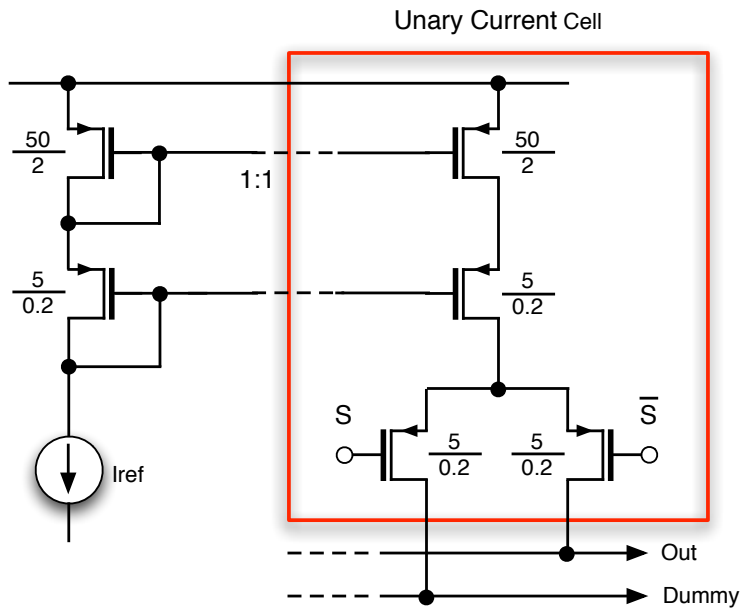
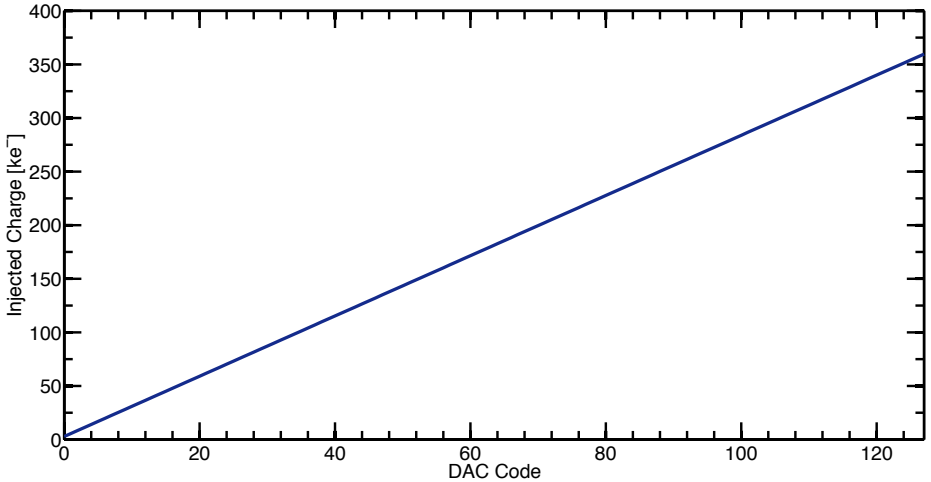
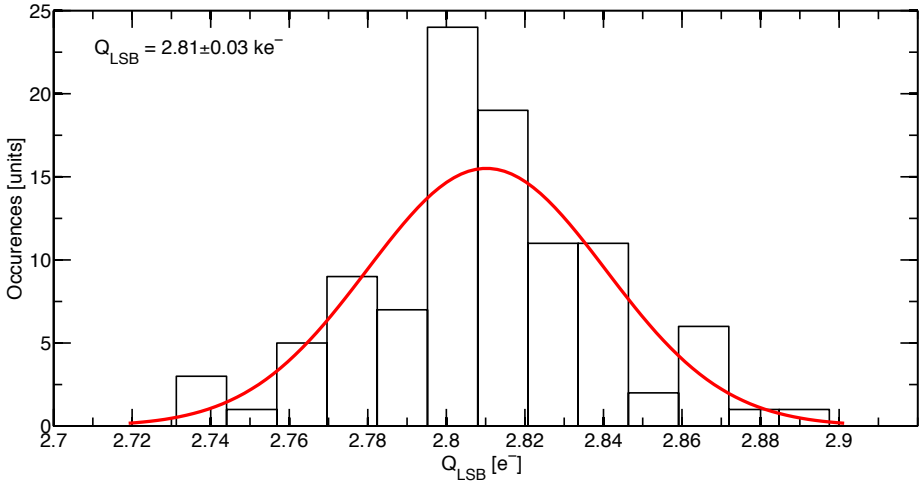
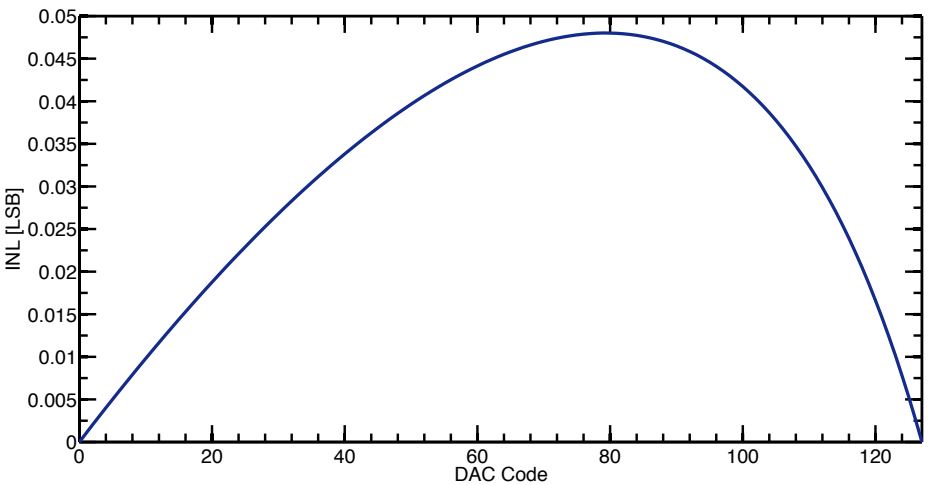


Figure: Switching scheme for the unary current source.

Injection Circuit performance





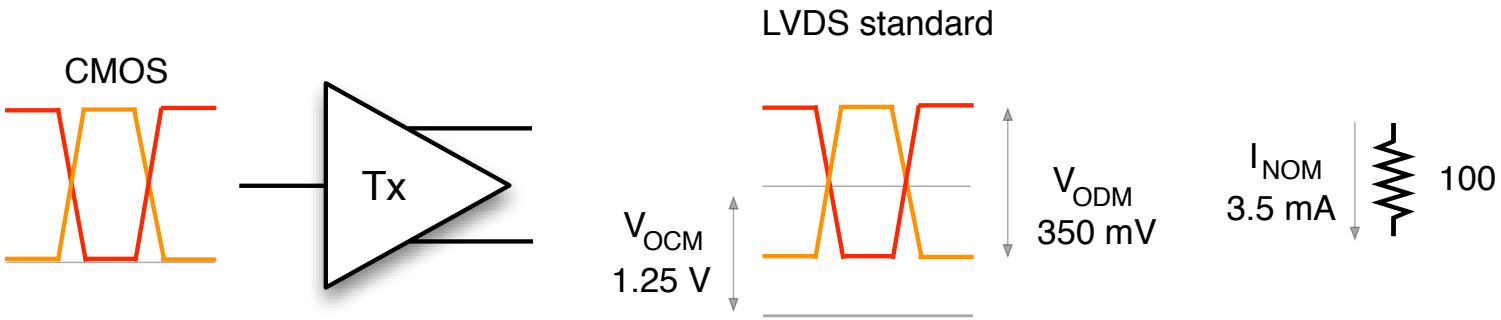


- $Q_{LSB} = 2.809\,\mathrm{ke}^-$
- $Q_{MIN} = 2.812\,\mathrm{ke}^-$
- $Q_{MAX} = 359.6\,\mathrm{ke}^-$
- $INL_{MAX} = 0.048\,Q_{LSB}$

W_0 [μm]	6	15	30
Q_{LSB} [ke^-]	2.88	2.85	2.81
σ_{LSB} [%]	5.48	2.54	1.08

Output pad: CMOS-to-LVDS converter

Converts the CMOS signal at the input in to LVDS out signal

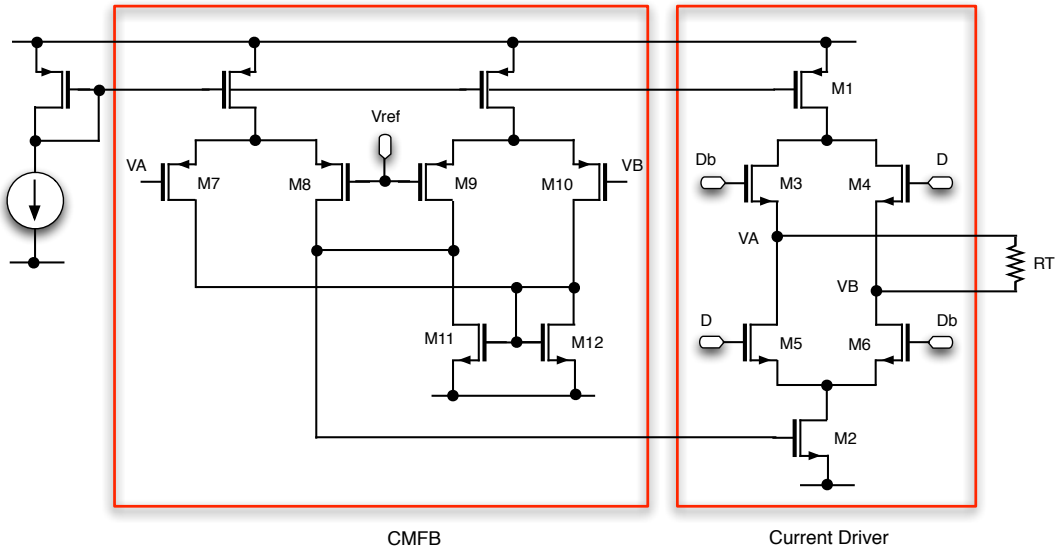


Since the Transmitter is biased at V_{DD}=1.2 V the output signal cannot meet the LVDS standard specification $\Rightarrow$ we have established our own values for the Output Common Mode Voltage V_{OCM}, the Output Differential Mode Voltage V_{ODM} and the Nominal Output Current I_{nom}

	LVDS Standard	**DSSC Chip**
V_{OCM} [V]	1.25	**0.60**
V_{ODM} [mV]	350	**200**
I_{nom} [mA]	3.5	**2.0**

The values of V_{OCM} and V_{ODM} measured on a termination resistor R_T fully meet the requirements for the signal levels at the receiver input specified by the LVDS standard: **100 mV**$\leq V_{ICM} \leq$ **2.4 V** and $|V_{IDM}| \geq$ **100 mV**.

Transmitter schematic and performace

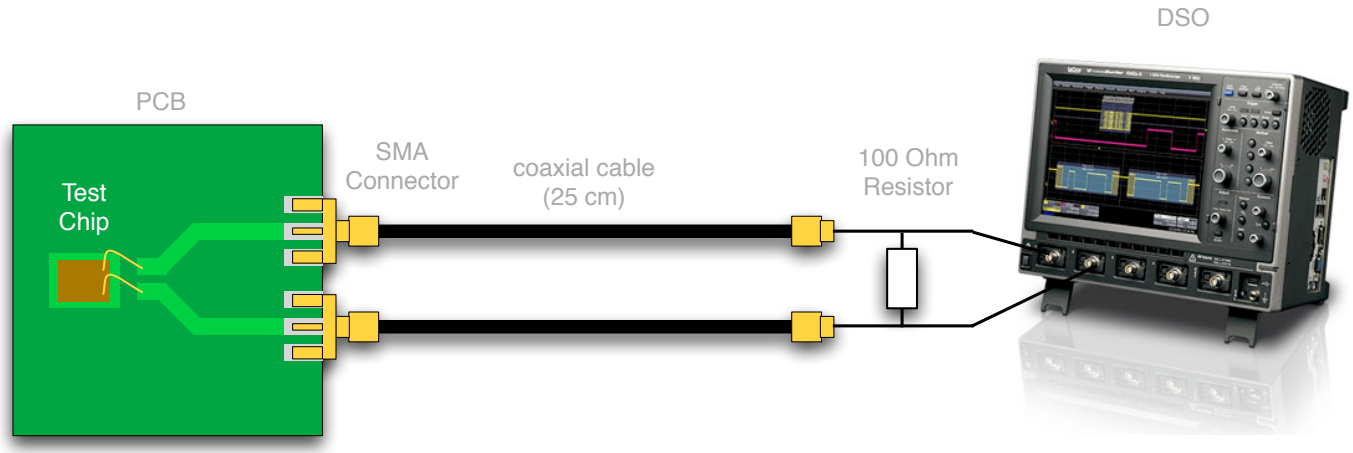


V_{DD} [V]	1.2
V_{OCM} [V]	0.6
V_{ODM} [mV]	200
I_{nom} [mA]	2.0
Power [mW]	2.4
Area [μm^2]	30×27
Data Rate	1.6 Gb/s

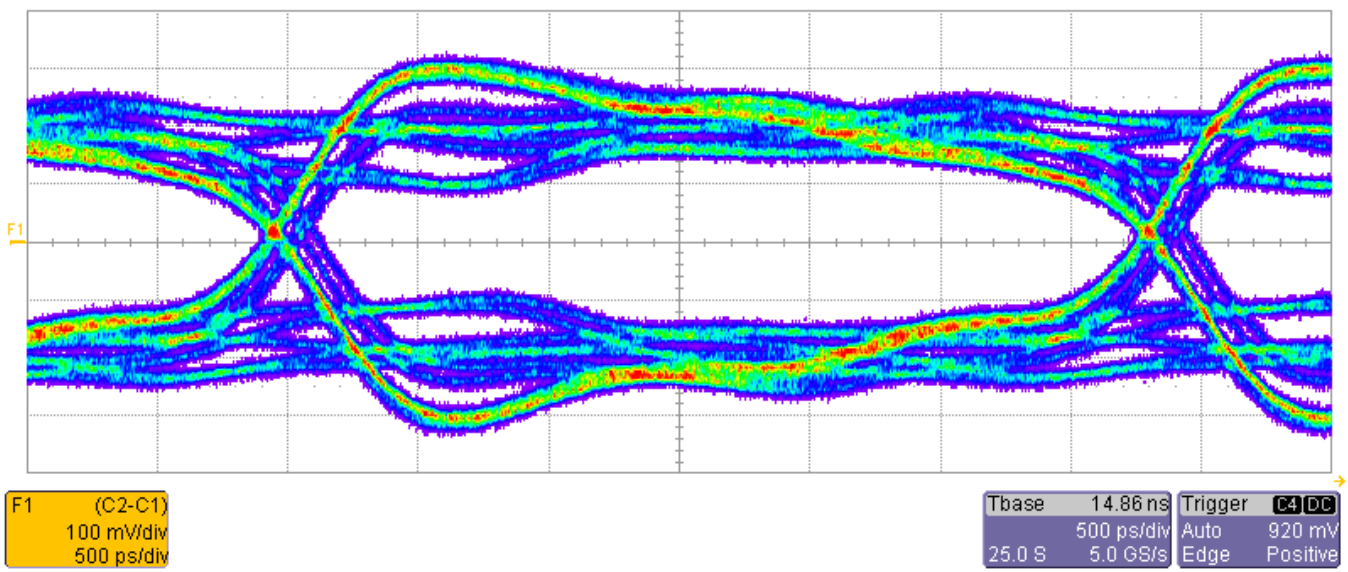
- **Current Driver** comprises a current source transistor $M1$, a current sink transistor $M2$, and four MOS current switches $M3$, $M4$, $M5$ and $M6$ in the full-bridge configuration.
- **Common-Mode FeedBack** keeps the common-mode output voltage stable over Process, supply Voltage and Temperature (PVT) variations.

Transmitter performance

Tested with a CMOS input signal at f=300 MHz with the following setup:

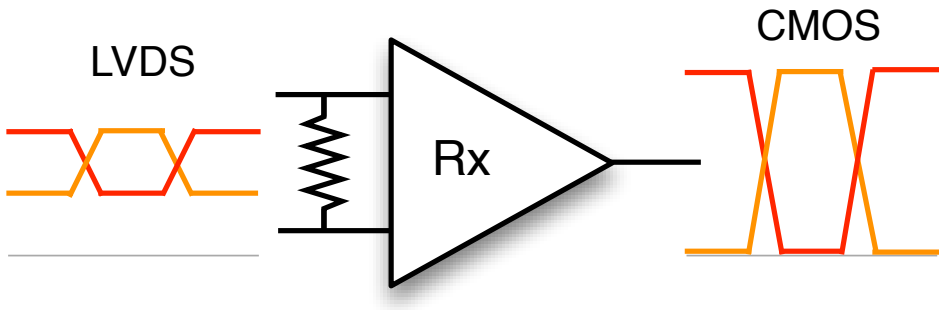


Differential signal on 100 Ω load resistance: V_{CM}=600 mV and V_{DM}=200 mV

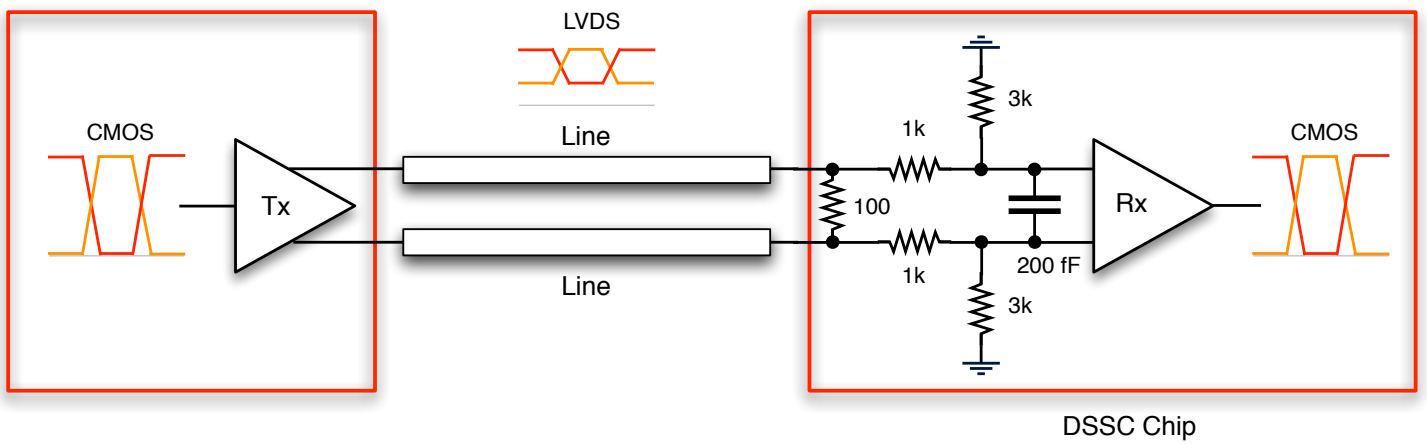


Input pad: LVDS-to-CMOS converter

Converts the LVDS signal at the input of the pad in to CMOS signal



Find a solution to reduce the V_{ICM}=1.235 V at the FPGA output.



LVDS Receiver Schematic

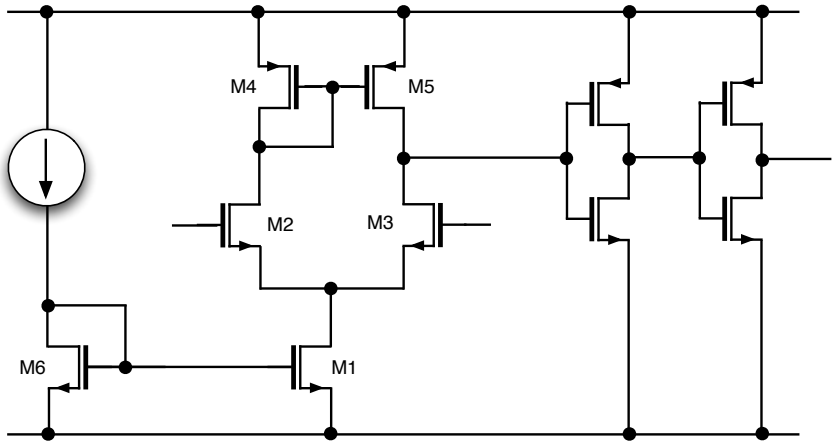
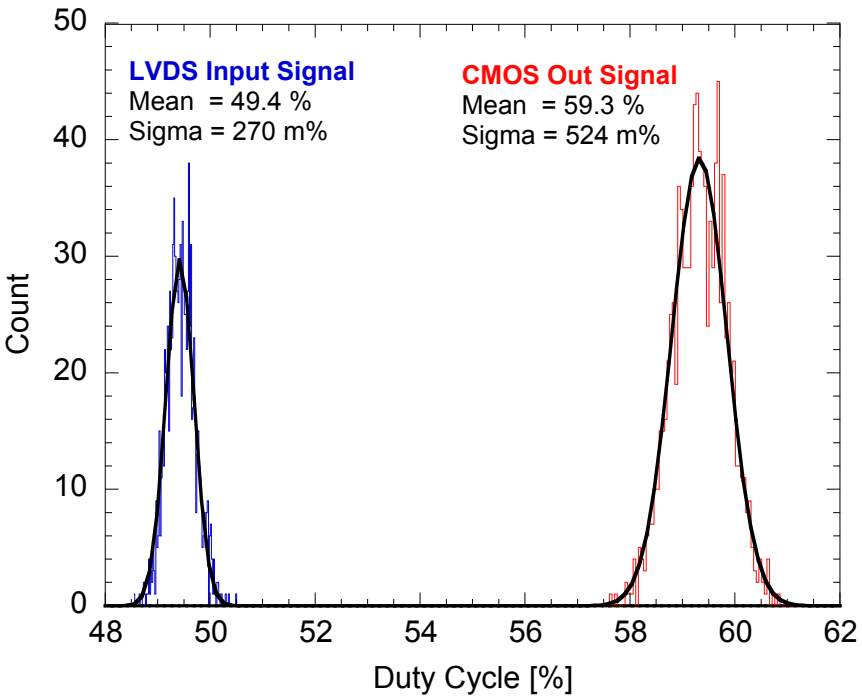


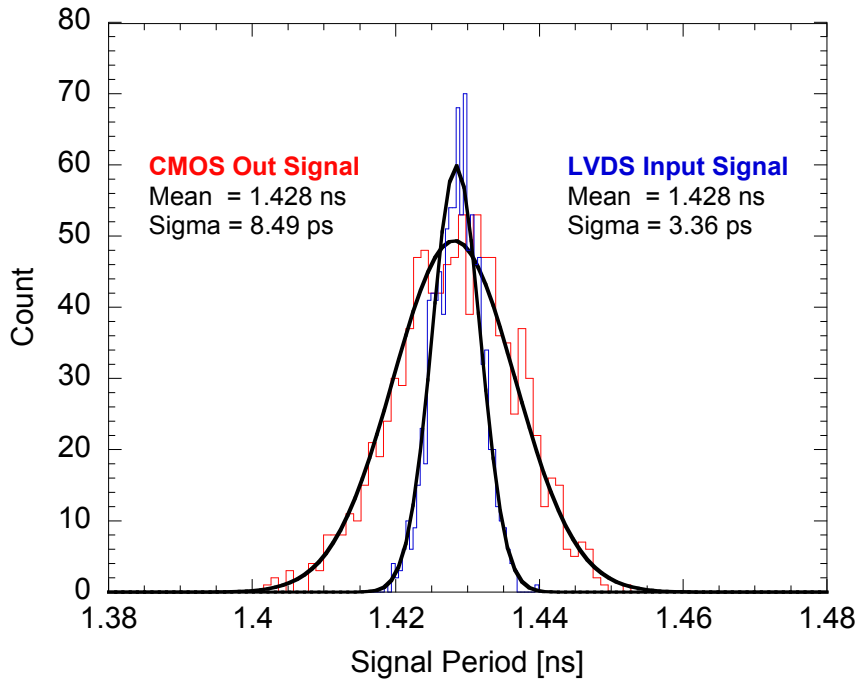
Table: Receiver main properties

V_{DD} [V]	1.2
V_{ICM} [V]	$0.5 \leq V_{ICM} \leq 1.4$
$\lvert V_{IDM} \rvert$ [mV]	≥ 200
Power [mW]	0.5
Area [μm^2]	17×17

LVDS-to-CMOS Input Pad: timing jitter

Tested with an LVDS square input signal with f=700 MHz and levels of 0.95-1.45 V (provided by a Tektronix DTG5334 with DTGM30 module)





- An unexpected duty cycle shift appears at f>300 MHz (to be understood)
- Duty-cycle jitter: 524 m% (3.74 ps at 700 MHz)
- Period jitter: 8.49 ps

Conclusions

- An improved version of the readout channel has been simulated with:
  - Optimized performance in terms of sensitivity and peaking time spread
  - Baseline restorer included
- The design of an Injection circuit for test and calibration of the front end chip is under development
- Prototypes of the I/O pads have been successfully tested