New DAQ System Strategy and its Implementation in the KLOE-2 Experiment

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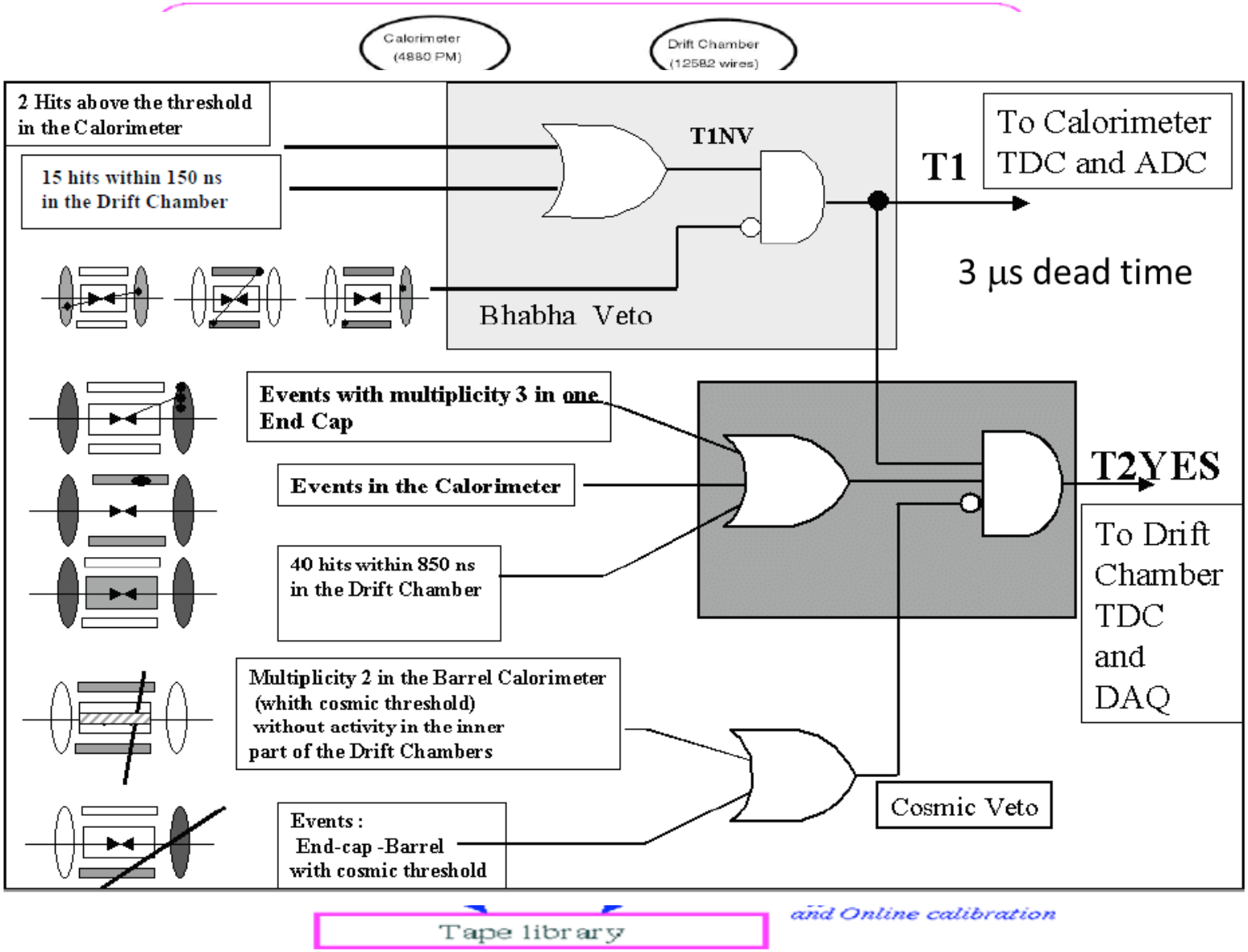
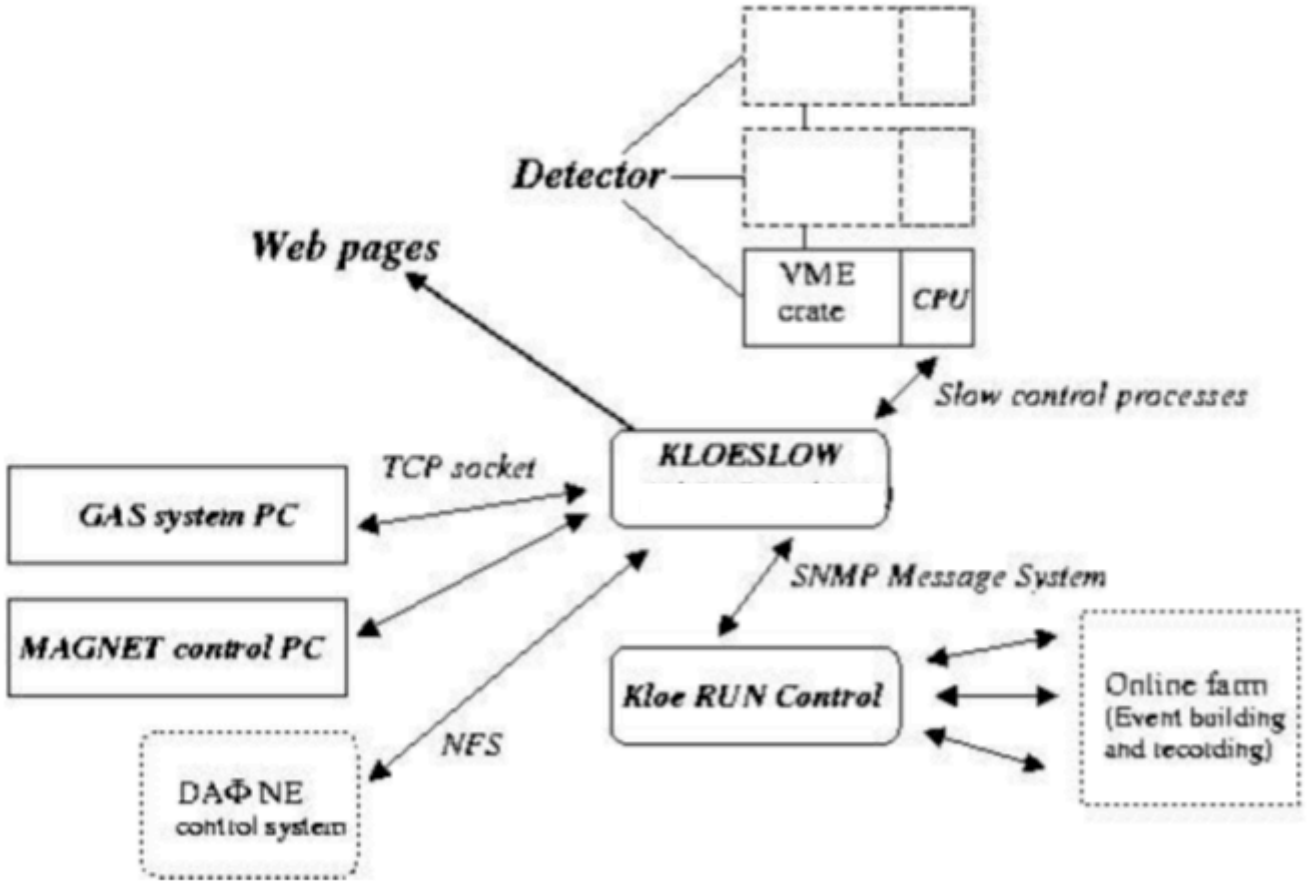
Talk layout

- KLOE original daq and daq system architecture
- KLOE upgrades
- Casting the upgrades in the original architecture

DAQ and trigger architecture



Slow control schematic and dataflow



System upgrade requirements

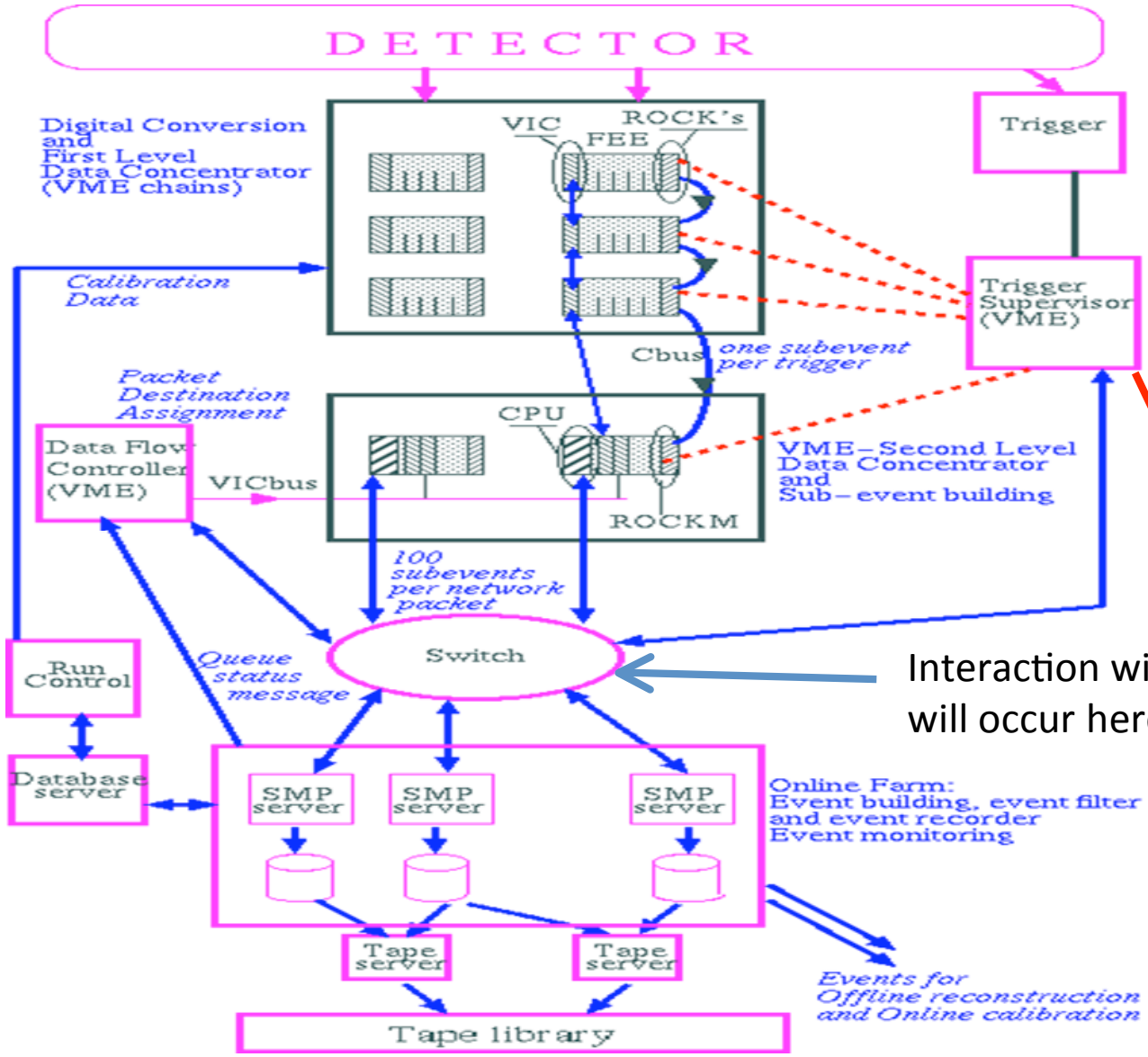
- It must efficiently collect data from the new detector.
- Old detector front-end and daq hardware must be reused.

System upgrade strategy

- The front-end L2 CPU have been changed and the switch technology as well.
- This has increased the data throughput from the original 50 Mbyte/s to 100 MB/s on disk allowing us to collect data at more than 20 KHz of sustained trigger rate on disk.

New detectors

- Qcal and Inner tracker data must be collected and they must cope with a 20 Khz trigger rate.
- At 20 KHz IT data throughput is 80 MB/s assuming no zero suppression.
- Moreover single event data collection latency should be less than the DAQ dead time.
- Front end architecture can be different but the new detector data stream must be built together with the old detector ones at the farm level.



Trigger will be delivered to new detectors as well.

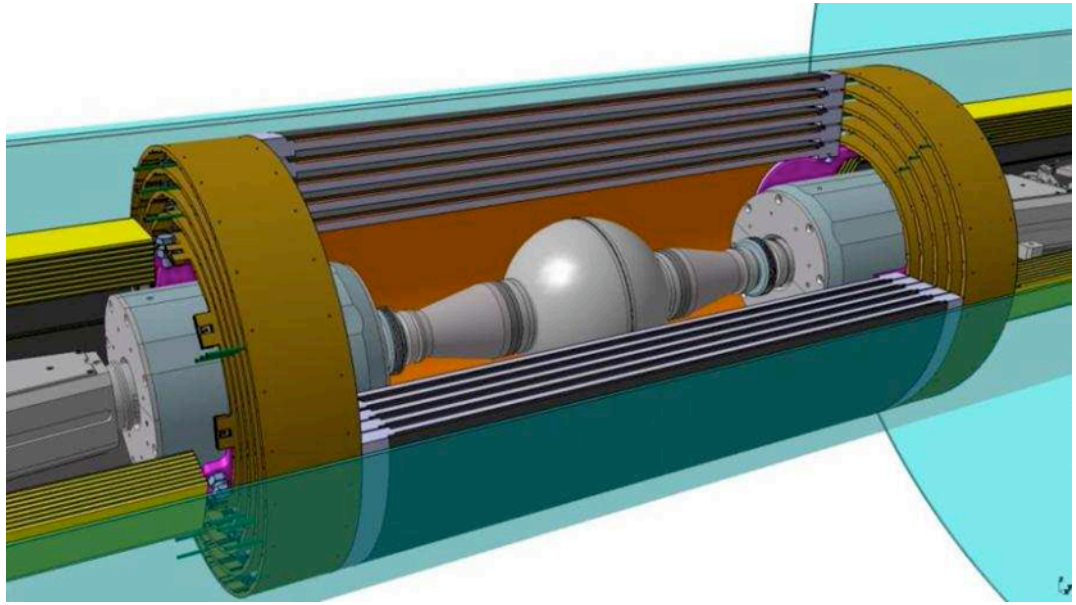
Interaction with new detectors will occur here

The Inner tracker readout

- The front end is based on the gastone chip a custom chip from KLOE collaboration. The gastone chip is a threshold discriminator 1 bit/channel info.
- All gastone chip parameters are downloaded during initialization via optical fibre links.
- During run serial links download front end data to GIB (General Interface Boards) gastone front end converted data.

Inner tracker general read out specs

Side A



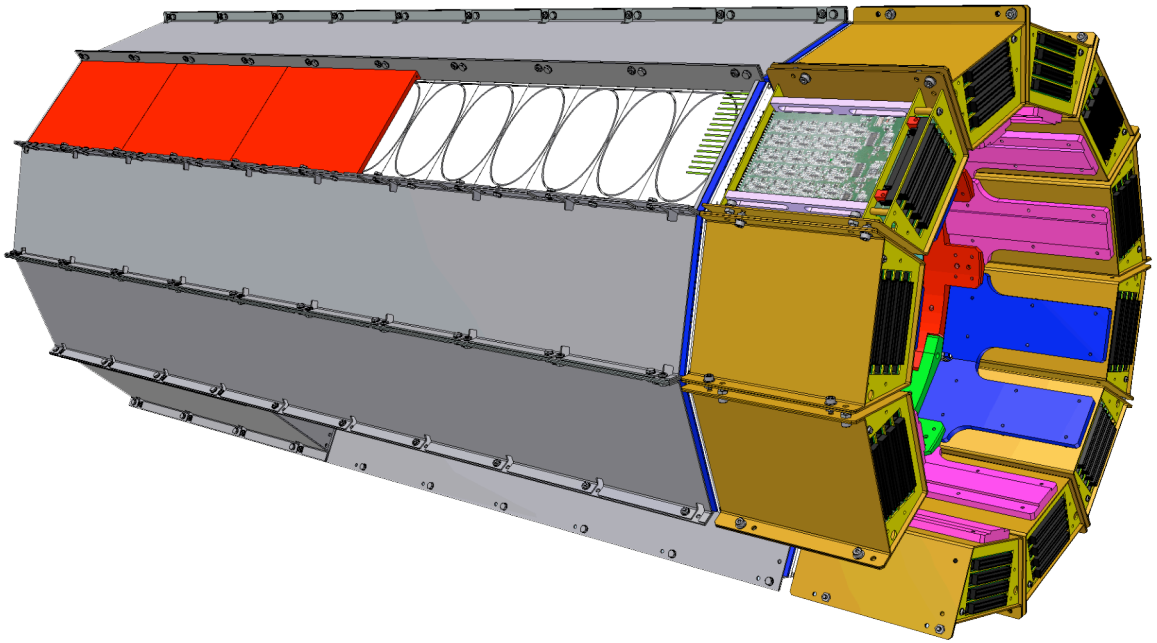
Side B

- IT detector readout consists of 30 kchannels to read 1 bit each channel.
- IT is partitioned in 2 read-out chains one per side
  consisting of 12 optical links each
- Since we exploit 2 Gbps links 1.5 μs are necessary to deliver data to optical links

The Qcal readout

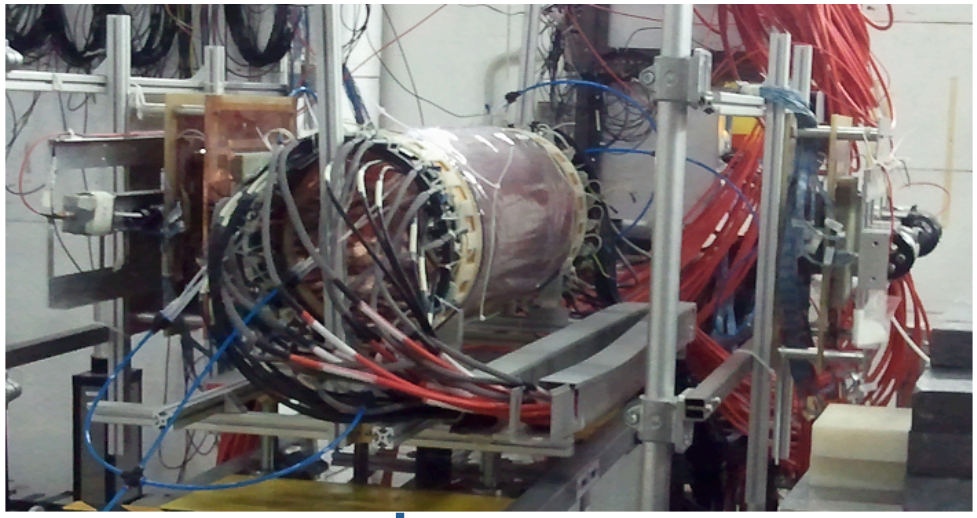
- The front end is based on KLOE custom electronics (TDC FPGA based with 1 ns resolution)
- All TDC parameters are downloaded during initialization via optical fibre links.
- During run serial links download front end data to GIB (General Interface Boards).

Qcal general read out specs

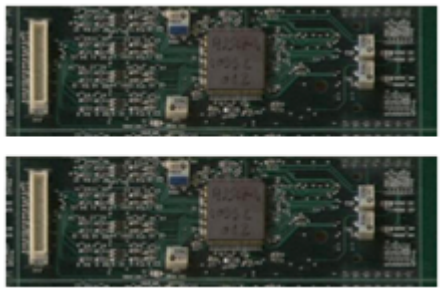


- Qcal detector readout consists of 1980 TDC channels.
- IT is partitioned in 3 read-out chains one per side consisting of 16 optical links each.
- Since we exploit 2 Gbps links 13 μs are necessary to deliver data to optical links if we run at 20 kHz data rate and without zero suppression.

IT chain read out

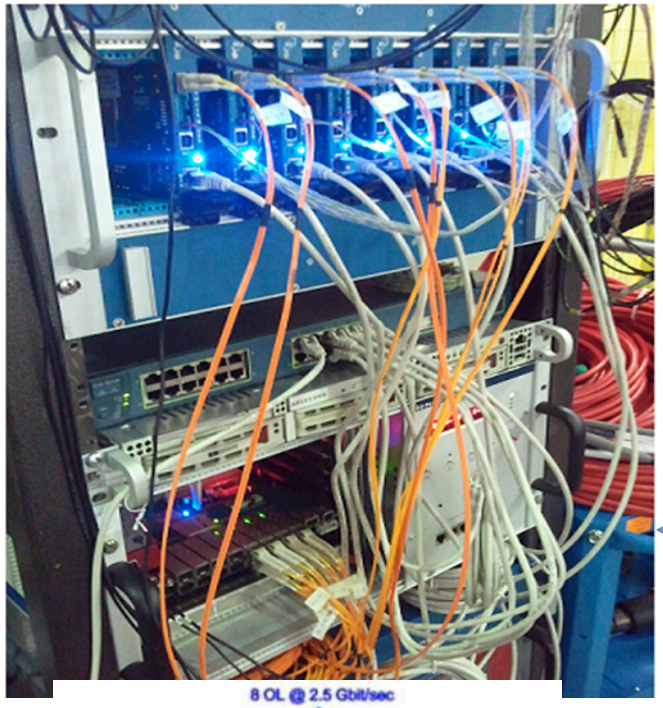


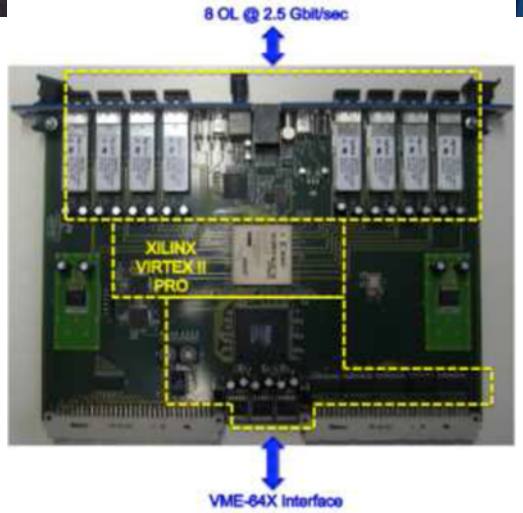
Inner tracker module



Gastone front end board

General readout



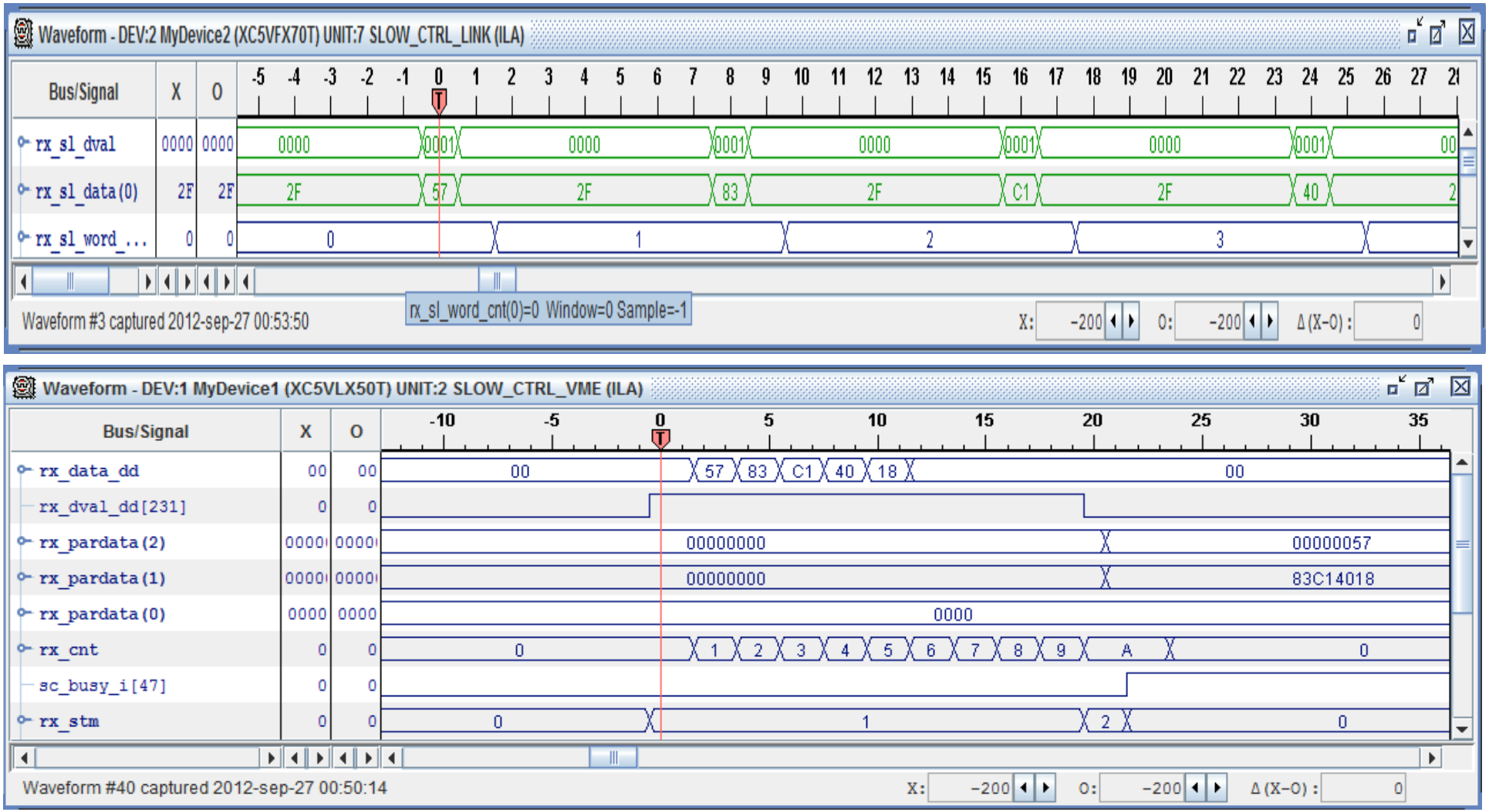


The GIB boards collect data from front end and deliver them through an optical link to a general purpose VME board. The VME board hosts up to 16 optical link 1 Gb/s each and builds a packet out of the collected data.

2 Gb/s optical links we have 16 links on the VME receiving card so we have 32 Gbps aggregate throughput on the optical links collected by a 6U VME board

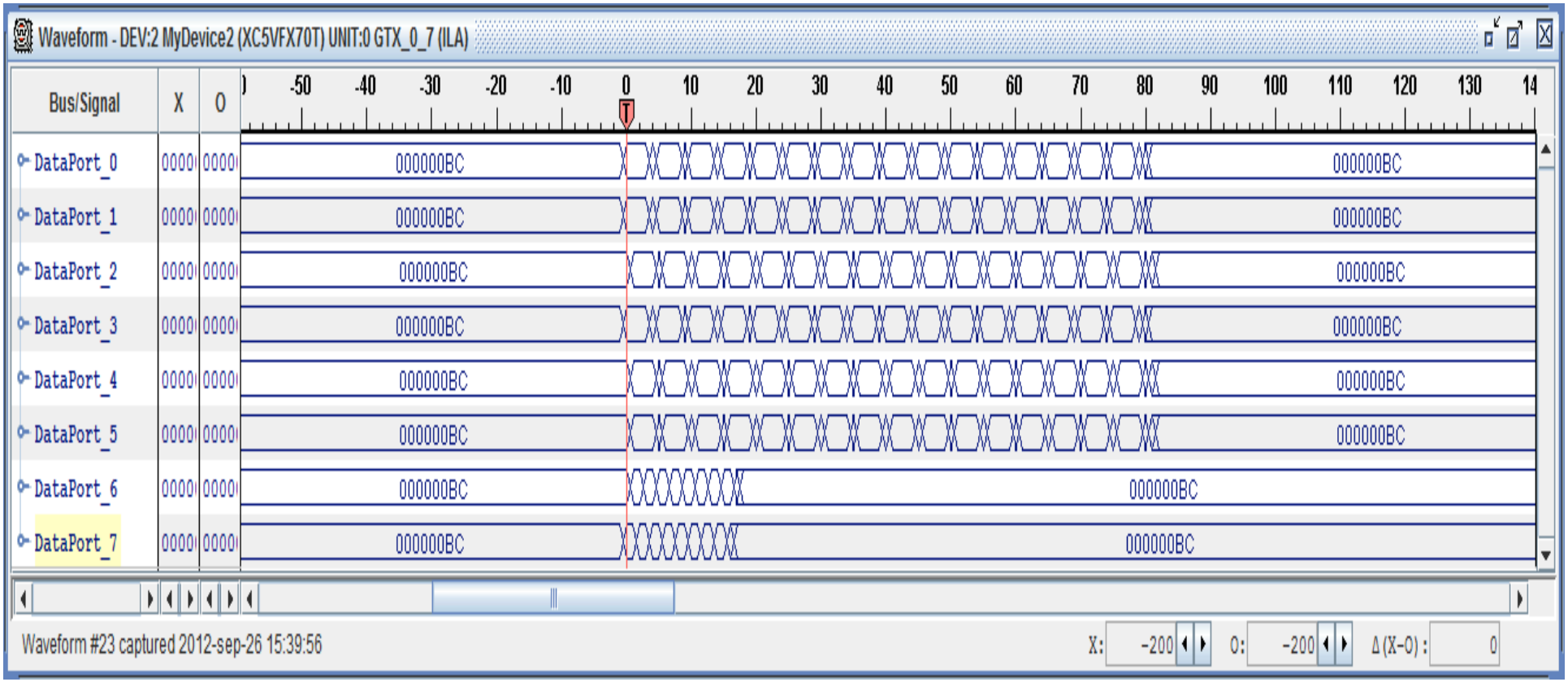
The data are collected from the VME board by a MVME6100 and Delivered to the kloe farm on line

Initialization through optical links



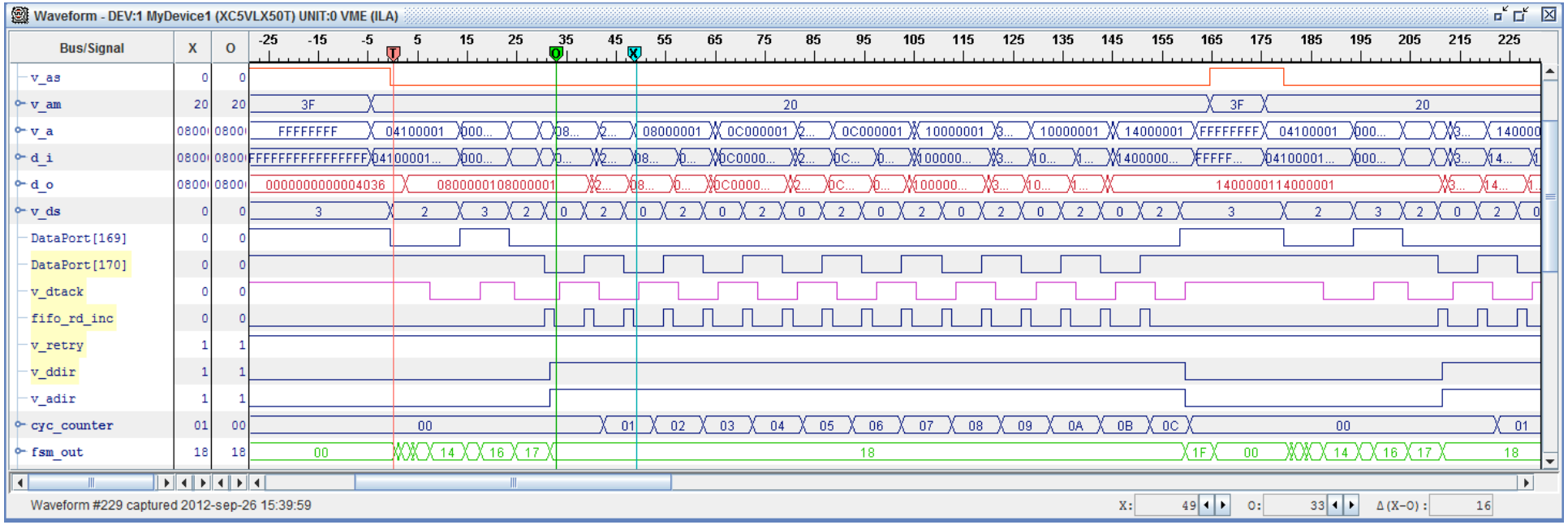
Initialization and slow control occurs through optical links.
We have used chipscope to debug and monitor the Initialization.
A snapshop of data delivery from front-end is shown in this slide

Data delivery through optical links



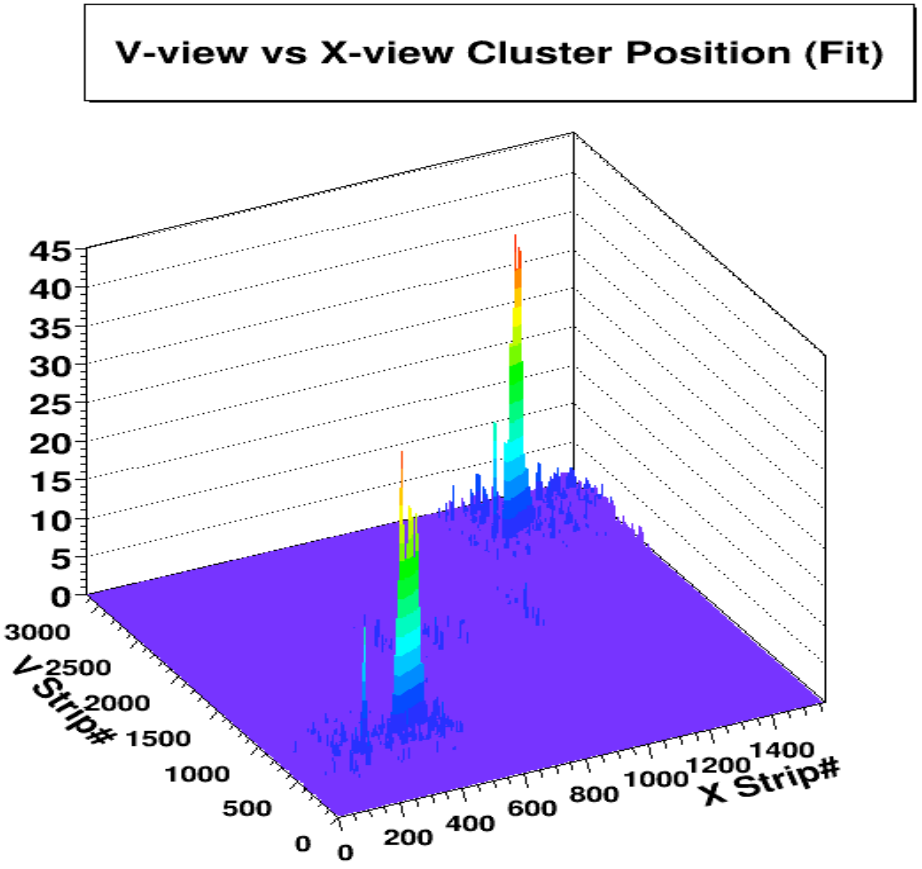
We have done an extensive use of chipscope to debug the front-end daq.
Here we show data flowing through the first 8 links to the data collection board.

VME interface



During data taking the VME interface has been monitored.
In this slide a snapshot of the data transmission over the VME bus has been shown. The VME interface supports BLT MBLT 2eVme 2eSST data cycles.
We read 8 btye @ 12.5 MHz therefore 100 Mbyte/s as top speed per single chain.

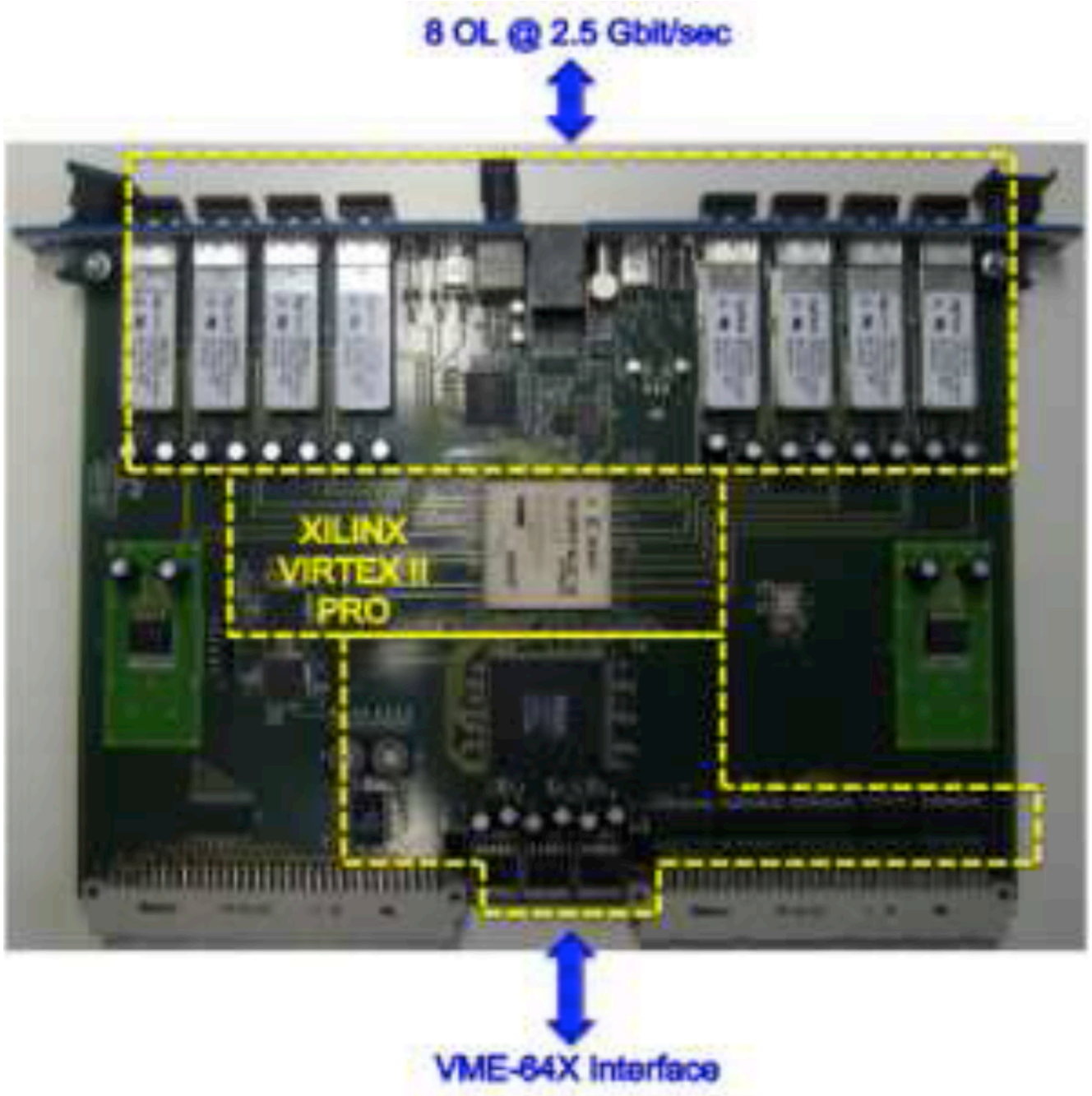
Reconstructed cluster position in comic triggered events



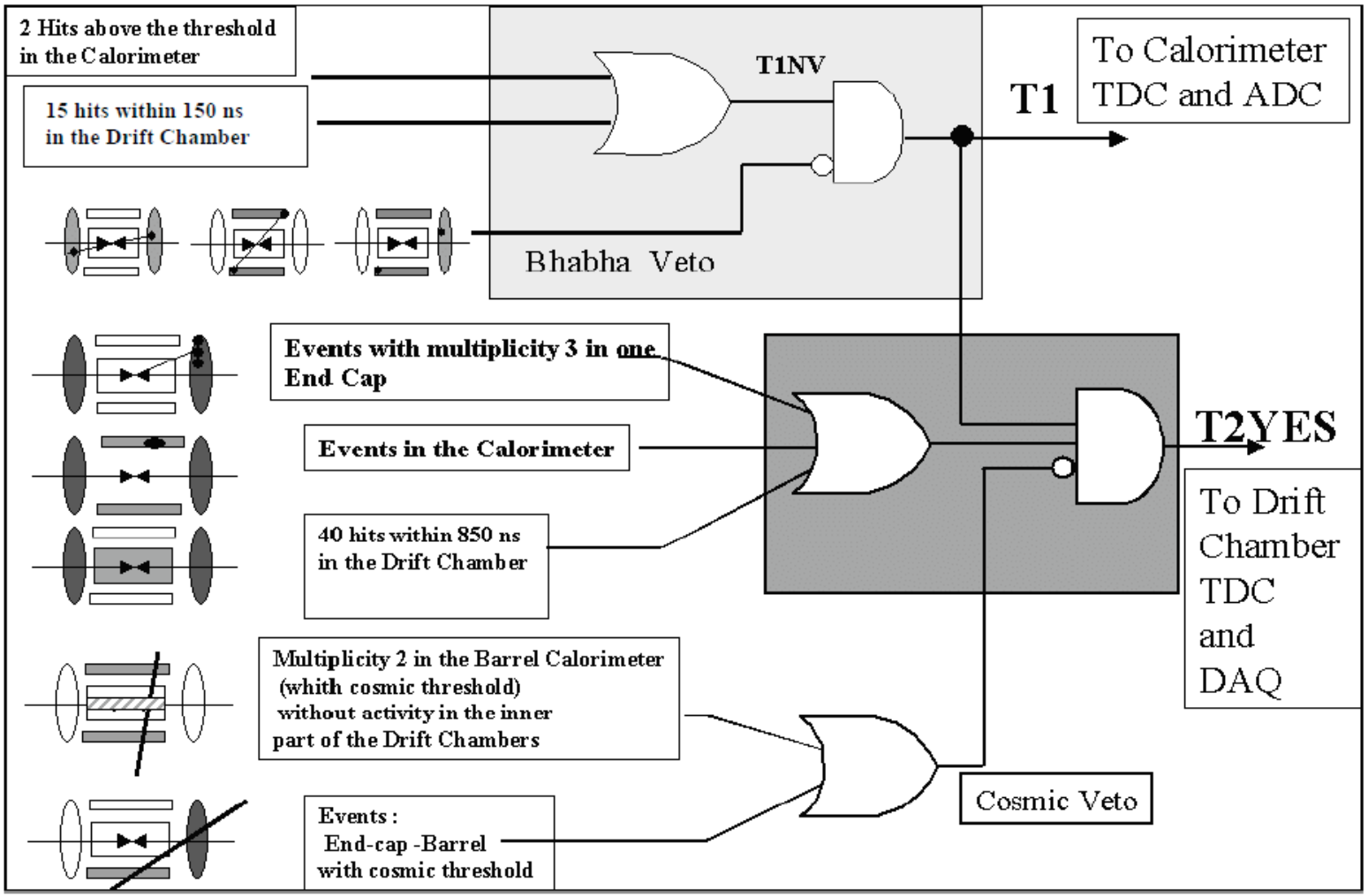
Conclusions

- The daq for the new KLOE detectors is finally ready.
- The KLOE daq system has been succesfully upgraded.
- We are now ready for a new data taking period.

Back up slides


8 OL @ 2.5 Gbit/sec
XILINX
VIRTEX II
PRO
VME-64X Interface

Trigger logic 1



Trigger logic 2