GASTONE (Gem Amplifier Shaper Tracking ON Events)

A Front-End chip for the KLOE-2 Inner Tracker Detector & its development for future applications

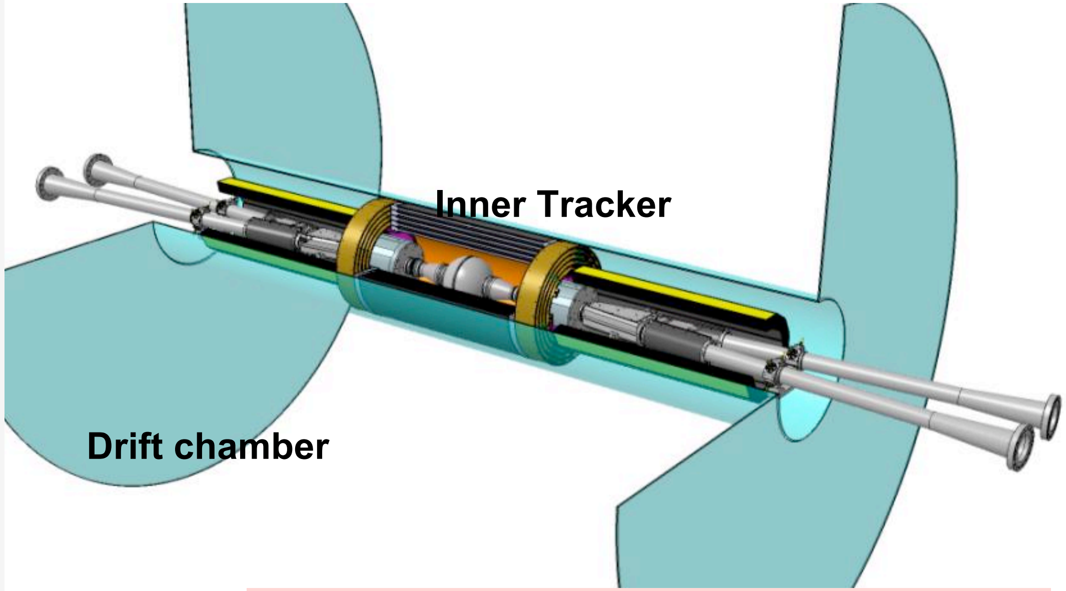
On behalf of KLOE2
Bari (SE)-LNF(SELF) Collaboration

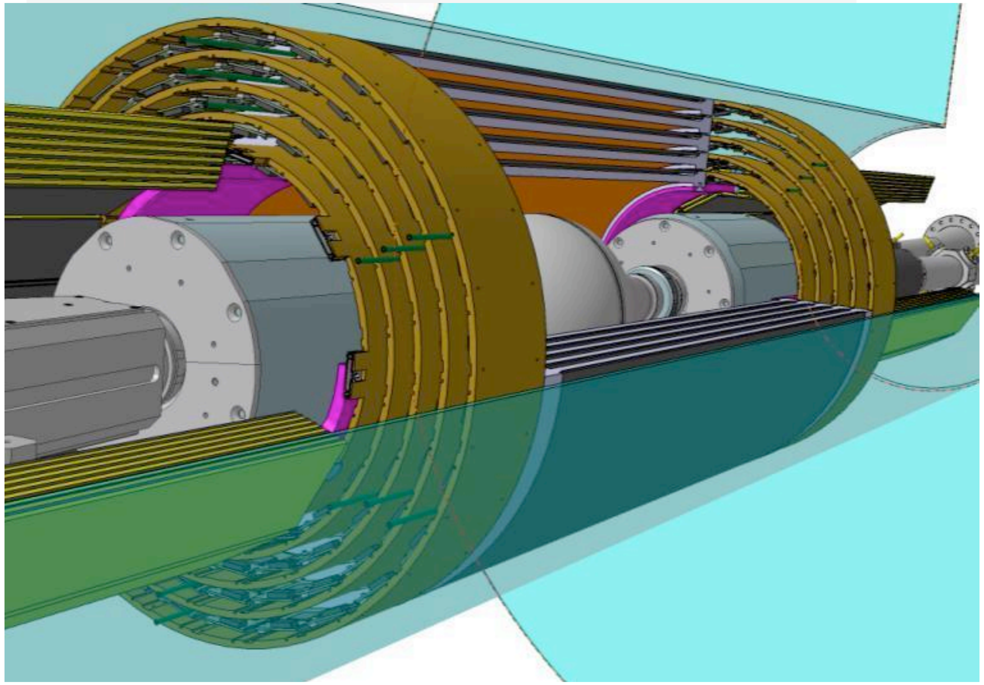
Outline

- Inner Tracker purpose and requirements
  - detector parameters
- Readout device parameters
  - readout requirements & time constraints
  - readout data frame
- Front-End Electronics
  - reasons of choice
  - GASTONE analog and digital blocks (main features)
  - A comparison of the two releases
  - Front-End Board
  - FEB testing & production
- Detector - FE integration
  - Input protection
- GASTONE analog version
- Conclusions

KLOE apparatus upgrade requirements

- Improve vertex reconstruction of K_S and η decays of a factor 3
- 2.0% X_0 total radiation length
- $\sigma_{r\varphi}$~200 σz ~500 μm spatial resolution
- 5 kHz/cm^2 rate capability
- 4 tracking layers
- from 260 to 460 mm in diameter
- 700 mm active length
- **Technology: Cylindrical-GEM**





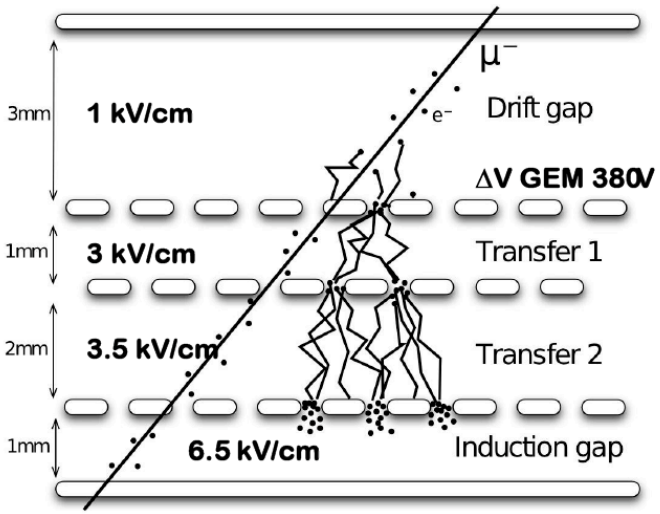
IT Proto 1.0 (constructed in 2007-2008)

- Triple-GEM with 3,2,2,2 gap thickness
- 150 mm radius (Layer 1) x 354 mm active length
- Electrodes obtained splicing 3 foils (314x354 mm^2)
- One-dimensional readout
- 650 μm pitch (only along rφ)
- Anode readout with 1538 strips-pads
- 128 ch equipped with GASTONE16

Inner Tracker Purpose and Requirements

- Tracking device (NO charge / NO time measurements)
- Low gas gain device
  - High sensitivity head amplifier (few fC)
- High density readout (pitch ~ 650μm / ~30k RO channels)
  - Low power FE
- Most internal layer strip rate < 30 kHz
  - DC base-line restorer was avoided
- Stereo strips RO
  - C_{in} spread (0 pF ÷ 150 pF)
- Very light device (kapton + support structure)
  - Detector + readout hard to integrate
- IT strip is "short" i.e. Propagation delay ~ signal rise time →
  - Strip behaves not as a transmission line → no need for line termination
  - In practice no space for termination readout on both sides of detector

Signal production: in the drift region



From table 28.5 (Properties of noble and molecular gases at 20 degrees C and 1 atm pressure), Journal of Physics G, Nuclear and Particle Physics

Ionization produced by a traversing charged particle produces electron/ion pairs. The number of primary electrons is N_P.

High energy ejected electrons can produce further ionization such that the total number of electrons N_T is greater (about a factor 3÷4) than N_P.

The electrons drift in the electric fields towards the GEM foils whilst the ions recombine at the cathode.

Typical numbers for N_T are a few tens of electrons following a Landau distribution.

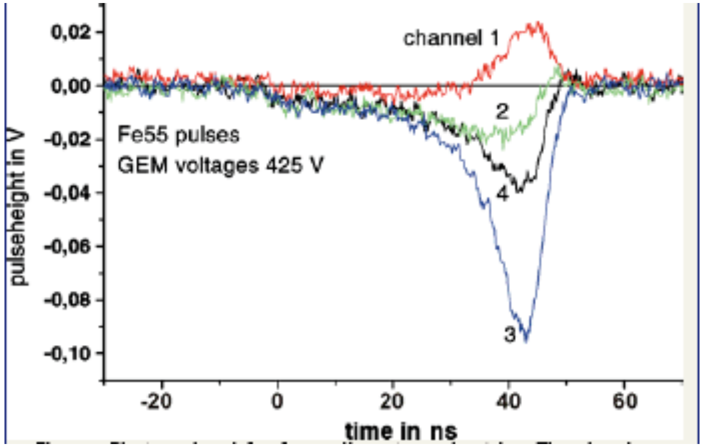
Compare that to ~220000 e⁻ produced in 300 μm of Si

Gas	N_P/cm	N_T/cm	%
Ar	25	97	70
CO_2	35	100	30
Total	28	83	

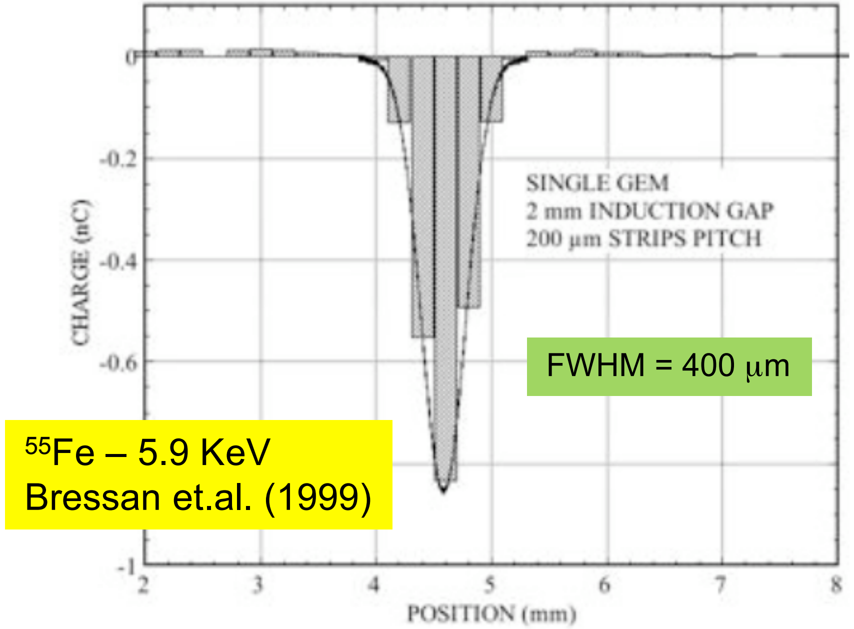
→ $N_T \cong 25\ e^- / 3\ mm$

Signal formation

- The strips outside of the main charge cloud show bipolar response due to induction process. Total charge on these strips integrates to zero.
- The width of the charge cloud collected on the anode for localized events or cluster size, depends on:
  - Detector geometry
  - Gas filling
  - Fields in the transfer regions
  - Time constants of the amplifiers



M.Ziegler, U.Straumann. Development of a triple GEM Detector for Particle Tracking. 2005 IEEE NSS Conf. Record

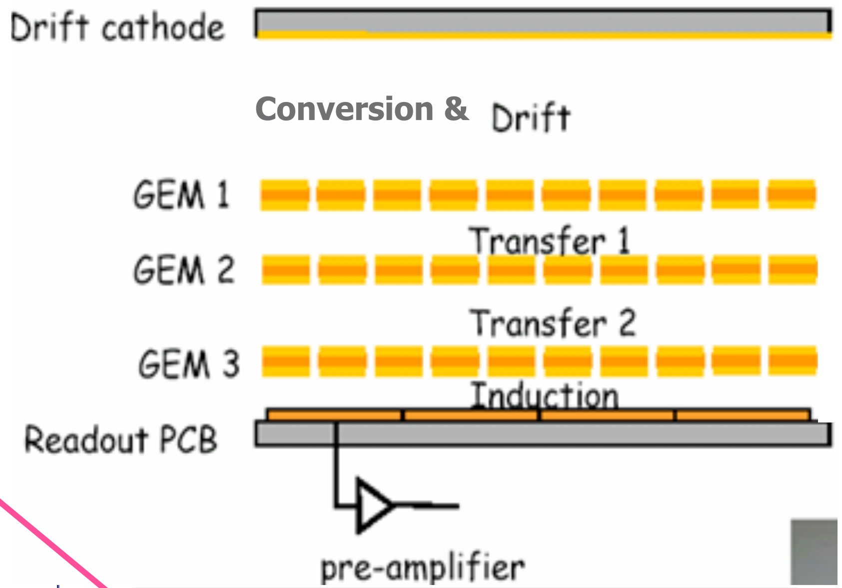


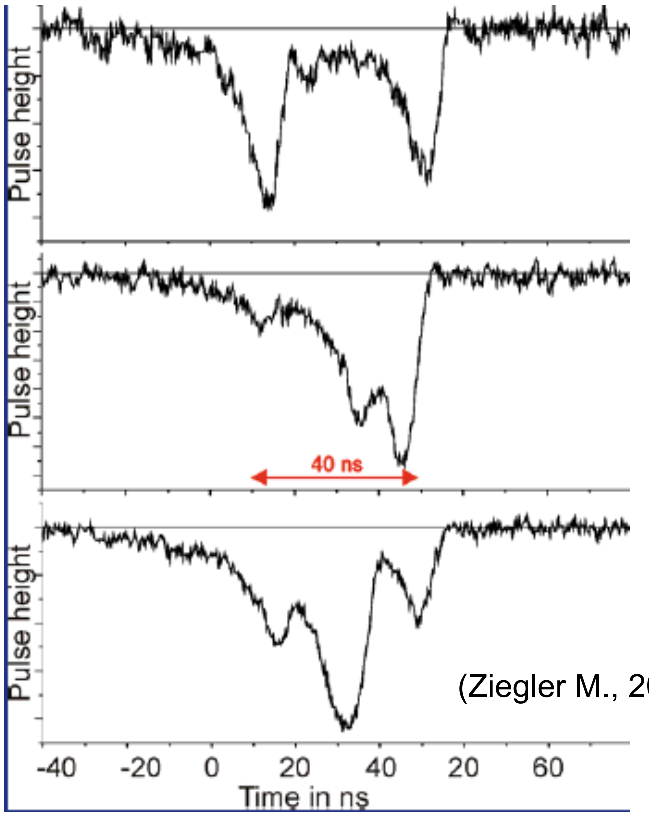
Charge cluster collected with 50 ns shaping time with readout strips 200 μm apart

Signal duration - example

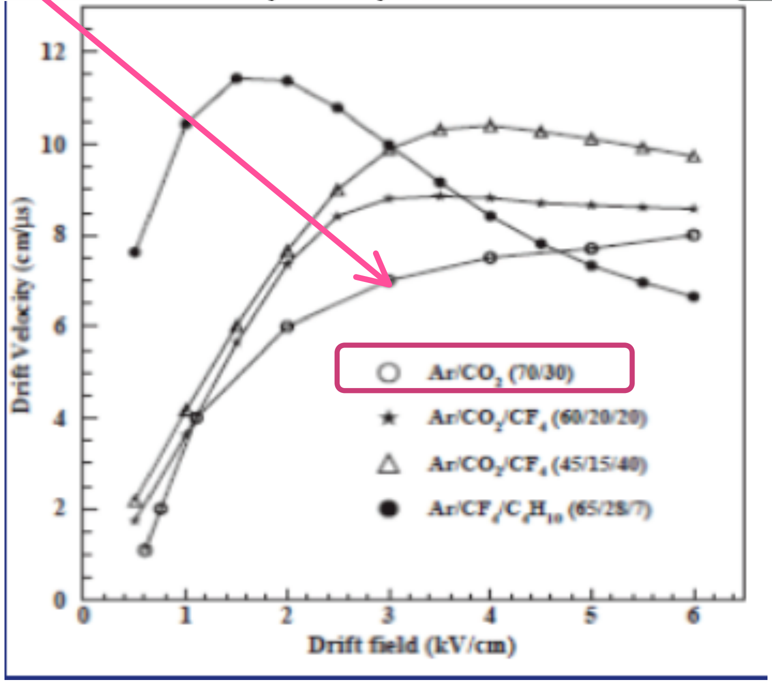
Drift velocity →
Drift region: 7 cm/μs @ 3kV/cm → 42 ns
Induction region: 13 ns

- Total collection time ~ 80 ns
- No ion tails due to screening effect of foils and clusters confinement in the holes

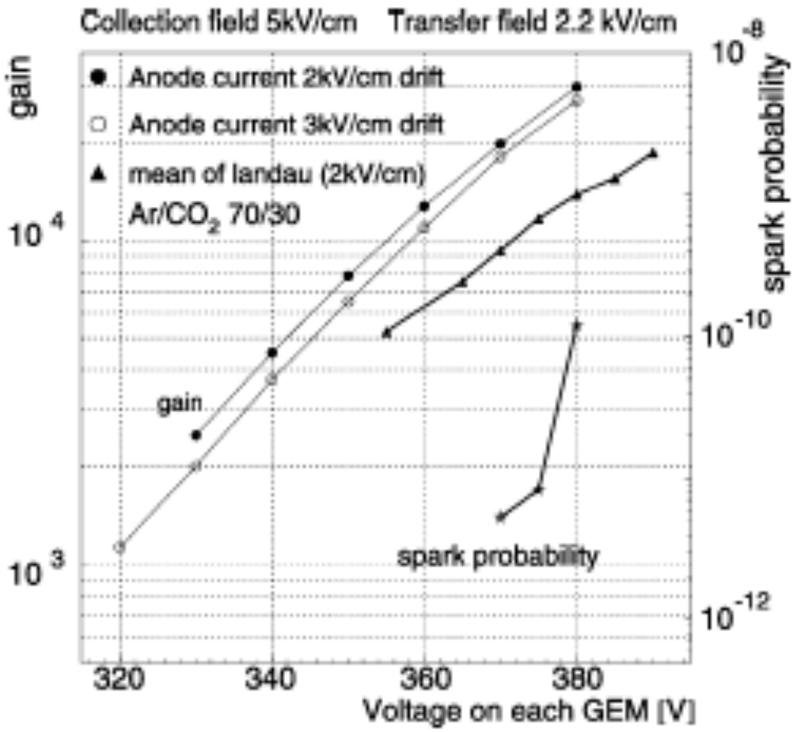




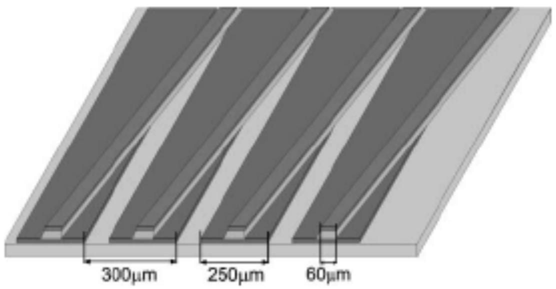
(Ziegler M., 2002)

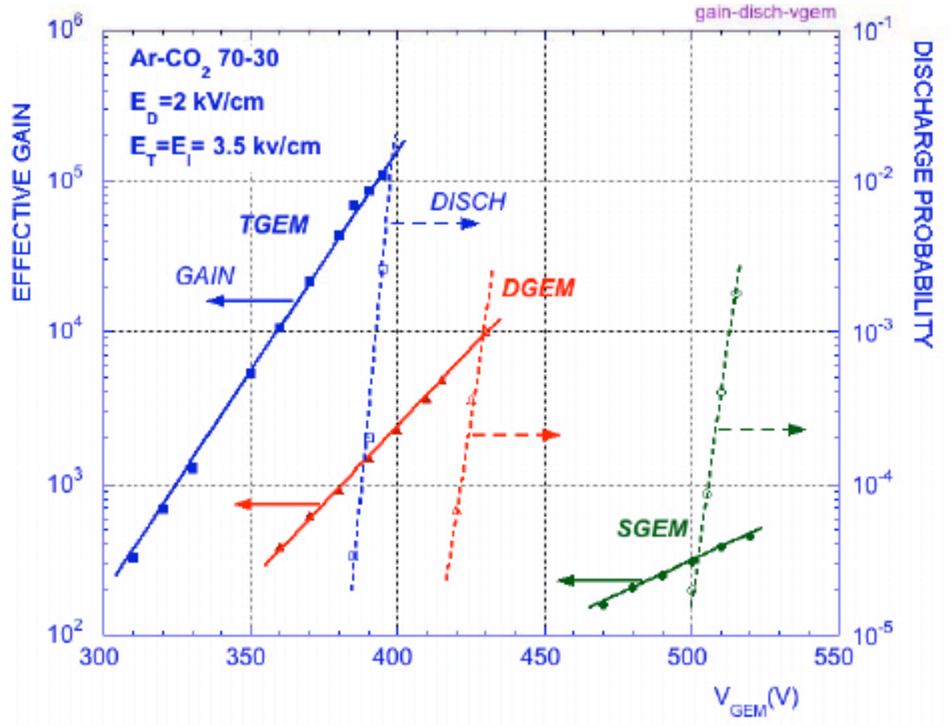


GEM Spark discharge probability



Gain and discharge probability on irradiation with **MIP**
Bi-Conical holes (80-50 μm) double mask GEM planes
Ziegler et.al. NIM A 471(2001) 260-263





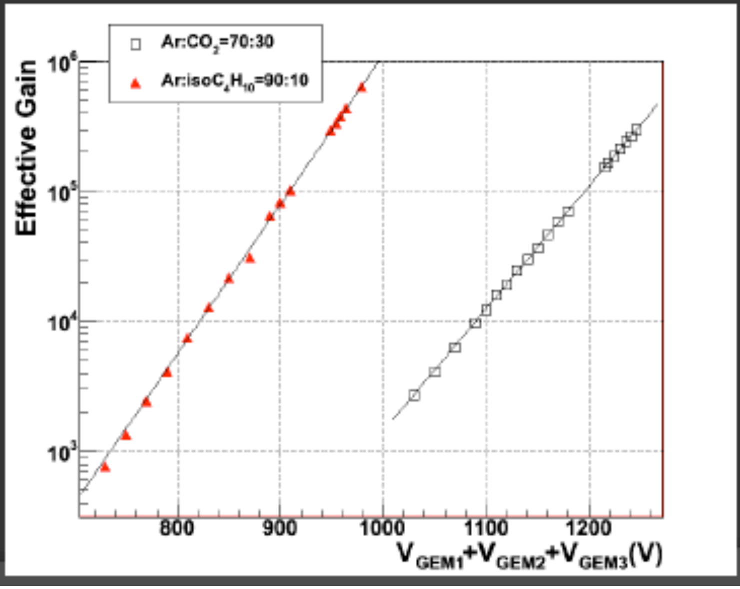
Gain and discharge probability on irradiation with **alpha** particles.
Conical holes (90-45 μm) single mask GEM planes
G. Croci – RD51 WG2 Meeting December 10° 2008

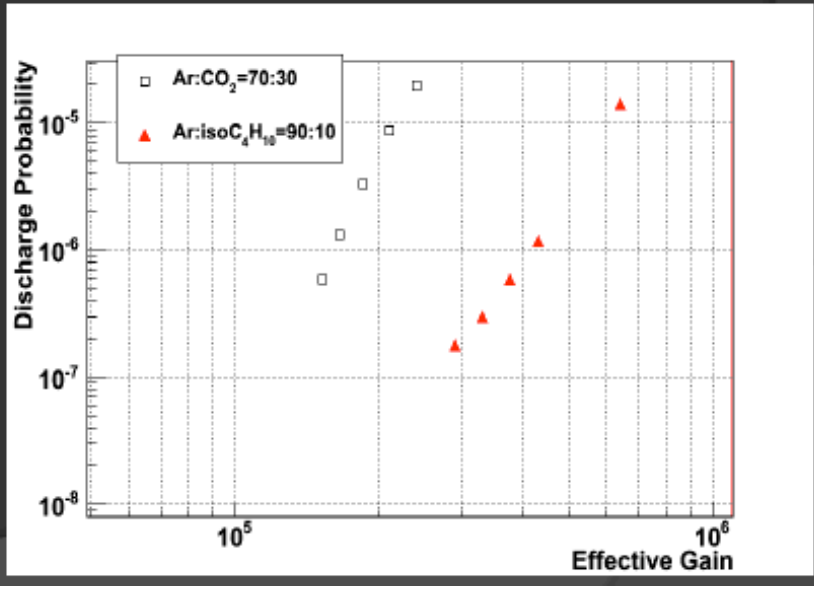
Layer2 X-rays Test

- In January L2 has been tested in current mode with 6 keV photons
- 2 gas mixtures characterized:

Conical holes (70-60 μm) single mask GEM planes

  - Ar/CO_2 (70/30) – we reached a Gain of $2x10^4$
  - $Ar/i\text{-}C_4H_{10}$ (90/10) – we reached the same Gain with higher stability (suppressed the number of discharges) at lower voltage (Vmax = 2800V instead of Vmax = 3800)
- Good gain uniformity found over the surface





From D. Domenici, *KLOE-2 General Meeting March 2012*

… the number in summary

- Ar/CO_2=70/30
- G=10^4 with
- 10 primary clusters/3 mm
- Clsize=2.5 electrons/primary_cluster
- V_{drift}= 7cm/µs → 14ns/mm → 42ns/3mm

Charge_mip = 10x2.5x1.6.10^{-19}x10^4 = 40x10^{-15} = 40 fC

Charge_mip_strip ~ 40fC/4 = 10 fC

The initial signal charge needs further amplification
The strips geometry and density are important as well
The shaping time should be calibrated on type of application

…in conclusion

The design and operational space for GEMs has many variables making life difficult for the electronics designer.

Some (but for sure not all) are listed below :

Fixed design variables

- Drift gap dimensions
- Transfer gap dimensions
- Induction gap dimensions
- GEM foil thickness
- GEM foil hole diameter and pitch
- Bias scaling of electric fields (drift, GEM foils, transfer and induction regions)
- Strip dimensions (pitch and length)

Operational Variables

- Gas components
- Gas component relative concentrations
- Gas pressure, temperature and humidity
- Bias voltage applied

Environmental Variables

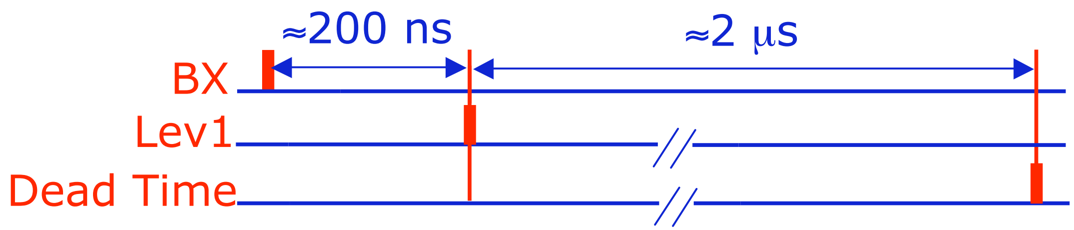
- Temperature
- Aging
- Magnetic field

Particle Variables

- Angle of incidence on detector

KLOE readout requirements

KLOE DAQ timing →



- Serial RO protocol (to reduce output channels)
  - Copper/Optical Link
- High modularity (64/128 channels)
- Switched signals only while reading data (to avoid internal X-talk) → no permanent clock running
- Asynchronous Trigger
- Asynchronous RESET
- OR output
  - Self-trigger capability for self triggering (NOT REQUIRED for IT readout)

Which kind of electronics?

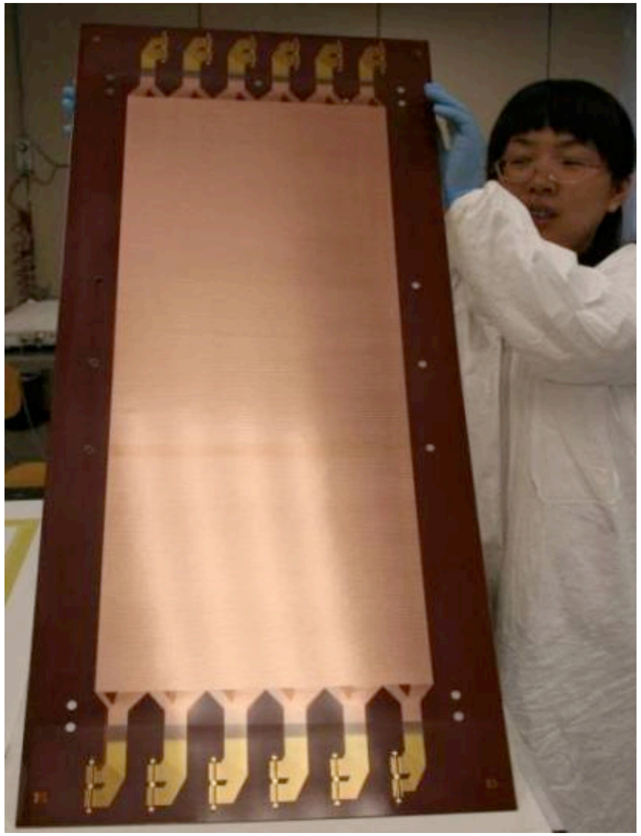
- The main constraint is due to the so big span in the capacitive load of each input channel (1pF < C_{det} < 180pF)

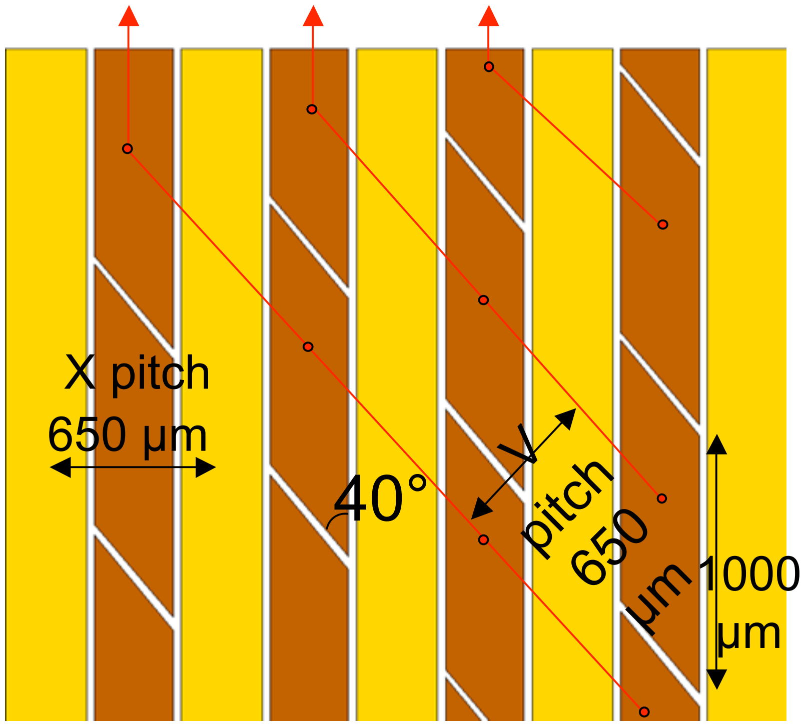
- We need to have:
  - good sensitivity for the expected charge
  - stability
  - uniformity
  - linearity

- we adopt *charge pre-amp* scheme as input stage:
  i. Low C_{det} sensitivity
  ii. Resistive dominant term in input impedance up to frequencies close to f_C
- BUT:
  i. More component s required
  ii. Greater power consumption than other considered configuration
  iii. C_{det} matching required for optimum S/N ratio → big size MOS devices
  iv. Shaping circuit required

A new topology for the anodic readout

A 2-D readout structure used for the first time (2007) to extract signal information including a diffused and separated ground plane for signal reference



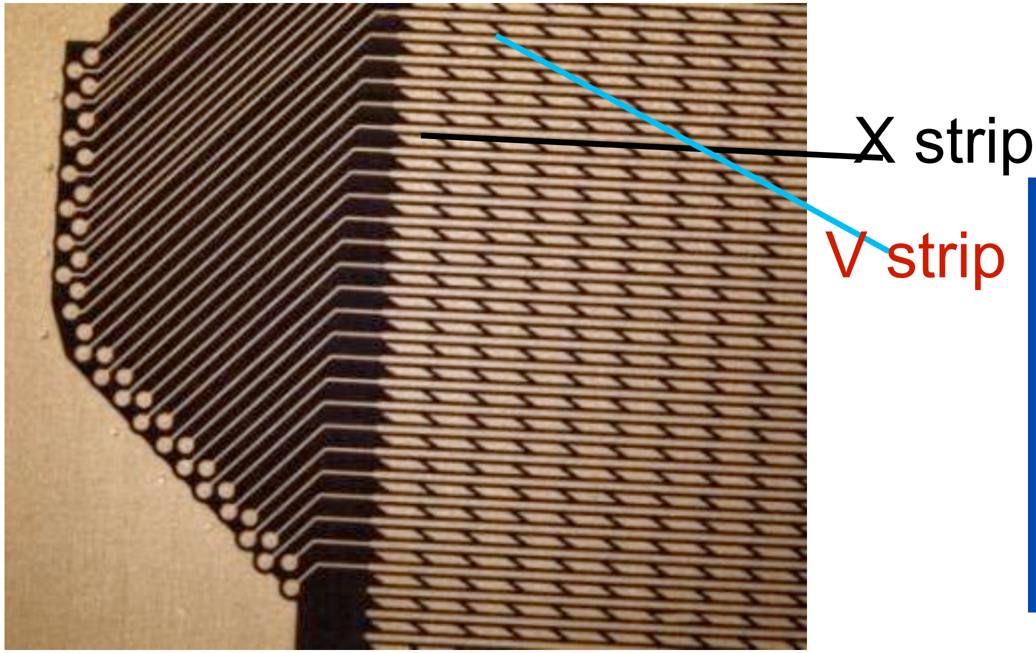


New 2-D anodic readout structure

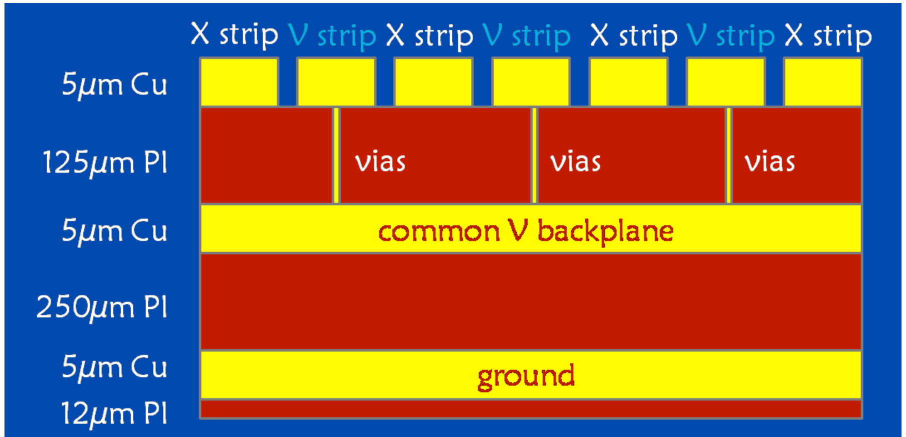
2-dimensional readout with XV strips on the same plane

X pitch 650μm → X res 190μm

V pitch 650μm → Y res 350μm



Multilayer Kapton circuit realized at CERN

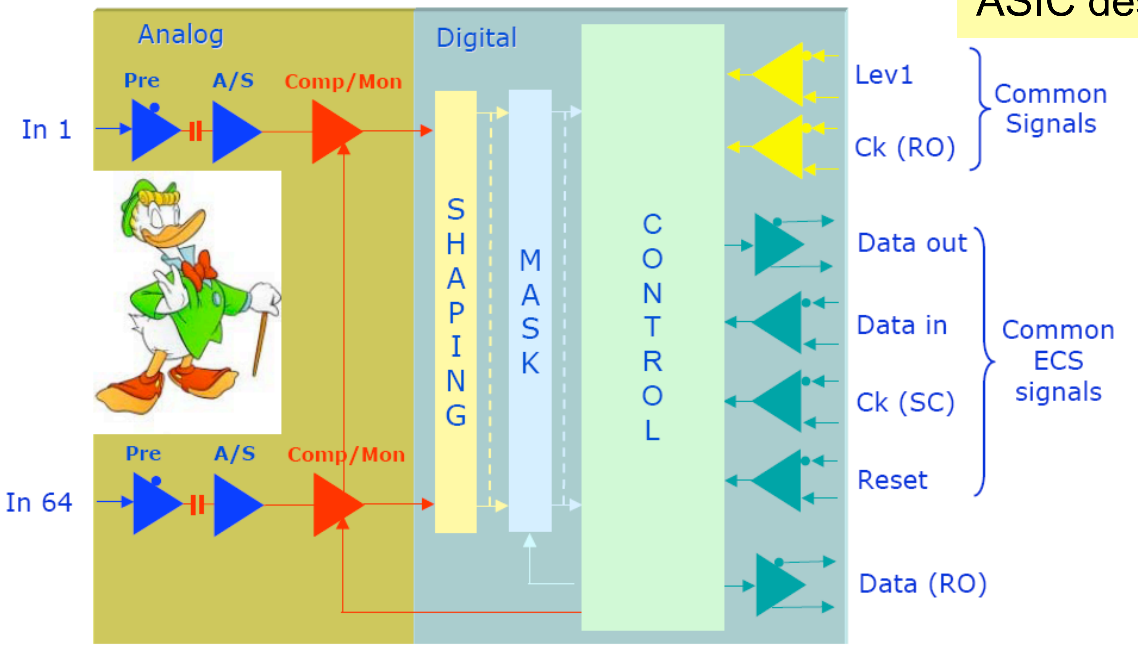


Material composition cross-section

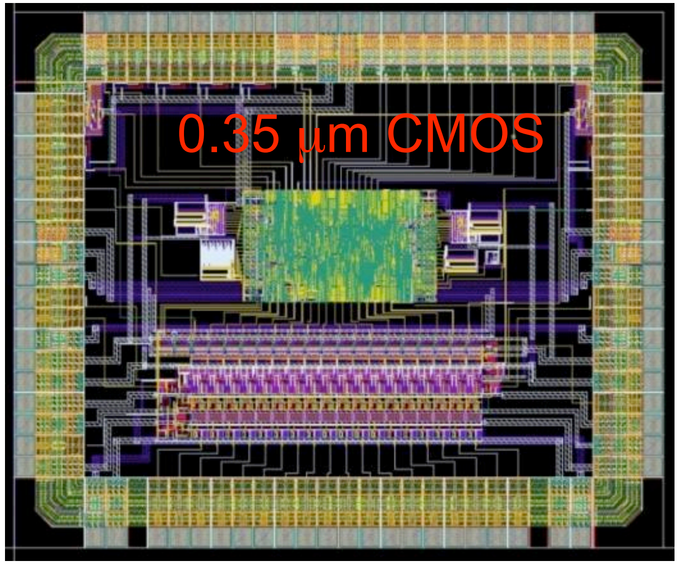
	Polyammide	**12,5 (um)**	**Coverlay**
	Adhesive	**12,5**	
1	**Copper**	**5**	**Double-Sided Copper-Clad**
	Polyimide	**50**	
2	**Copper**	**5**	
	Epoxy	**25**	**Bond ply**
	Polyimide	**25**	
	Epoxy	**25**	
	Epoxy	**25**	**Bond ply**
	Polyimide	**25**	
	Epoxy	**25**	
	Polyimide	**50**	**Double-Sided Copper-Clad**
3	**Copper**	**5**	
	Adhesive	**12,5**	**Coverlay**
	Polyammide	**12,5**	

GASTONE16
Analog Section - 3 basic blocks

Low-noise and low-power mixed analog-digital ASIC designed to satisfy IT requirements

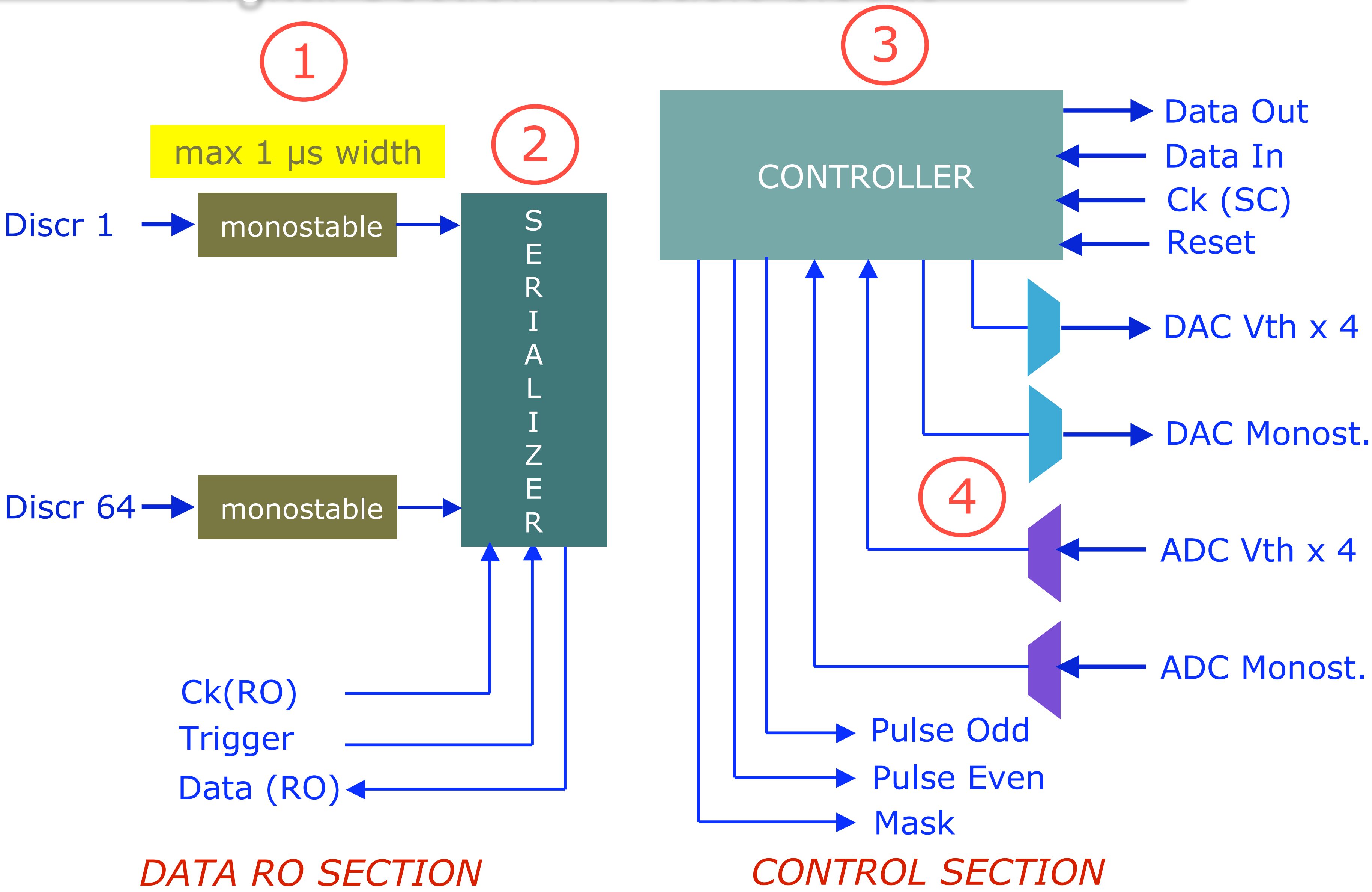


GASTONE (Gem Amplifier Shaper Tracking ON Events)



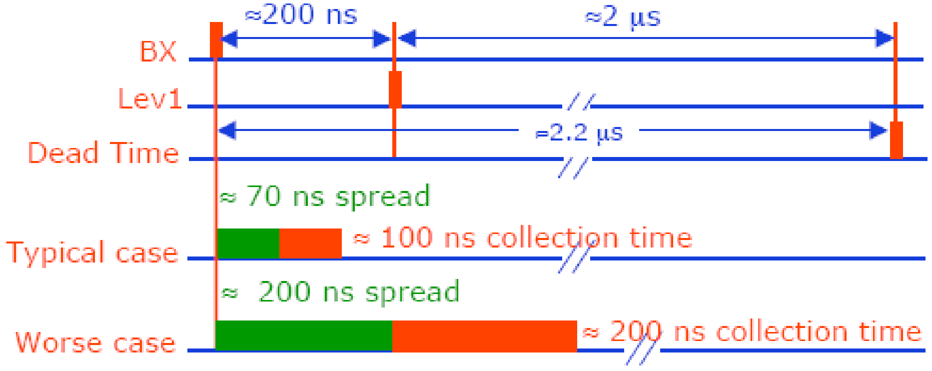
1. a charge preamplifier to integrate the input strip current into a voltage. Internal test pulsing capability (~10 fC)
2. A semi-gaussian shaper (CR-RC) circuit providing noise filtering
3. A leading-edge discriminator
4. AC-coupled

GASTONE16
Digital Section - 4 basic blocks



Readout device parameters

Signal processing



KLOE DAQ timing
"bunched" beam structure

- < 2 μs (data RO)
- 200 ns (input signal spread – worst case)
- 96 bits to be read in < 2 μs (acquisition rate 100 Mbps)

1. High modularity (64 channels)
2. Serial RO protocol (to reduce power consumption and cables
3. RO clock only after trigger arrival (to avoid internal x-talk)
4. OR output (self-trigger capability)

1 bit / channel

Header (8+2 bits)	**Trigger Counter(5bits)**	**Chip ID (9 Bits)**	**Data (64 Bit)**	**End Byte (8 zeros)**

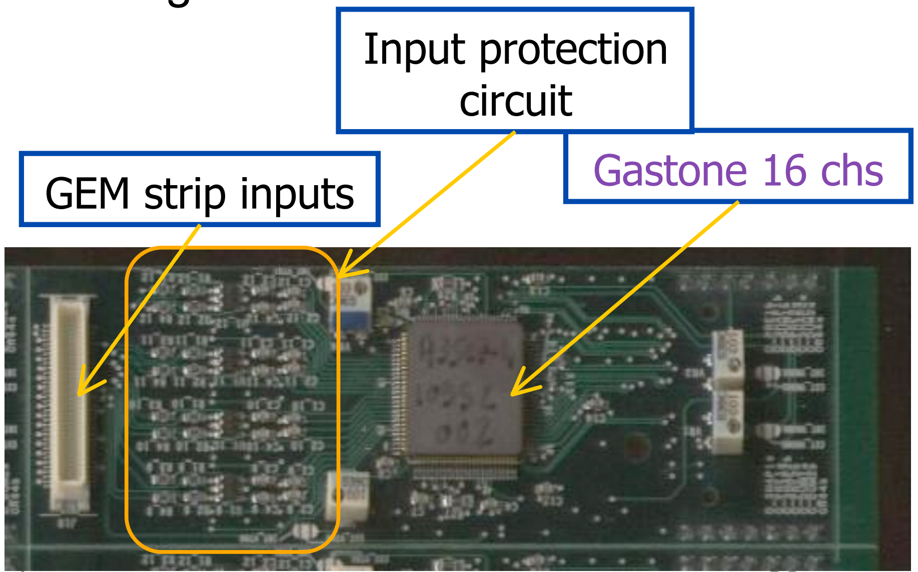
GASTONE16 Front-End Board (1'st release)

<u>Main features</u>:

- 2 chips/board (16 ch up / 16 ch down)
- One serial readout line per chip
- 10 LVDS communication lines/board
- Clock readout signal (50 MHz)
- One mask register for dead channels
- OR output for 16 channels for self-triggering
- HW ID for each chip
- 4 DAC + 4 ADC (8 bits) to set thresholds (one for 16 channel)
- 1 DAC (8 bits) + 1 ADC (8 bits) to set monostable output width
- Default threshold value (~fC) set at "power-on"

<u>'Slow Control" section implemented to</u>:

– Set threshold value (8 bit DAC)
– Set the monostable pulse width
– Enable external pulse system
– Enable internal/External pulsing system
– Read back threshold values (8 bit ADC)
– Read back the value for monostable width setting
– Enable channel readout through an internal mask register



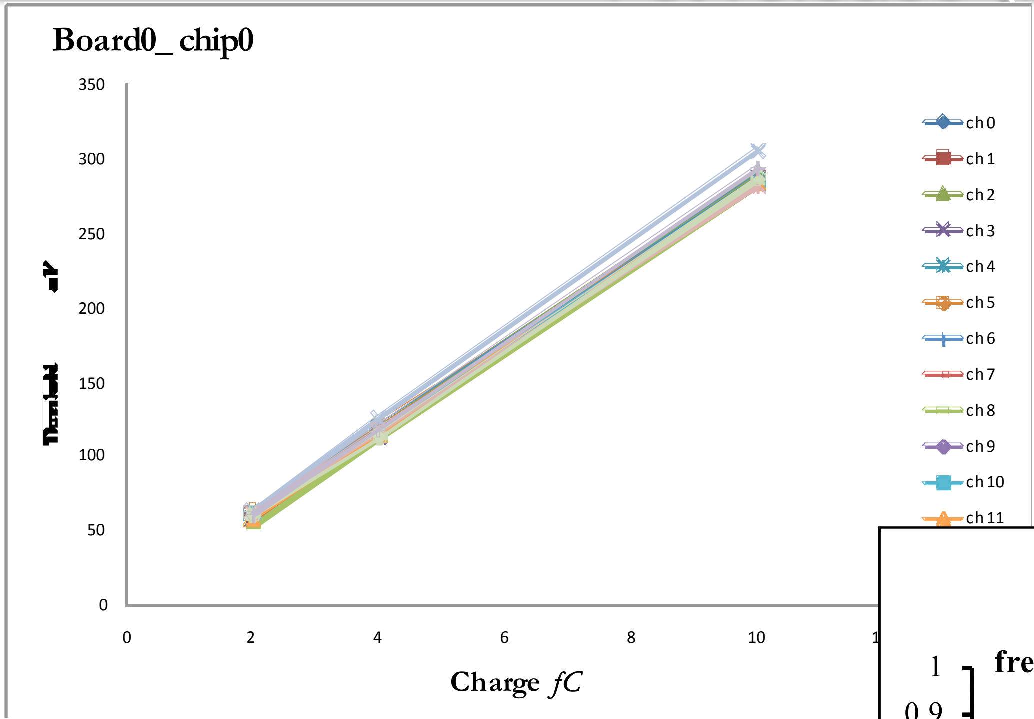
Dimensions: 30x95 mm^2

Testing procedures

Measurements:

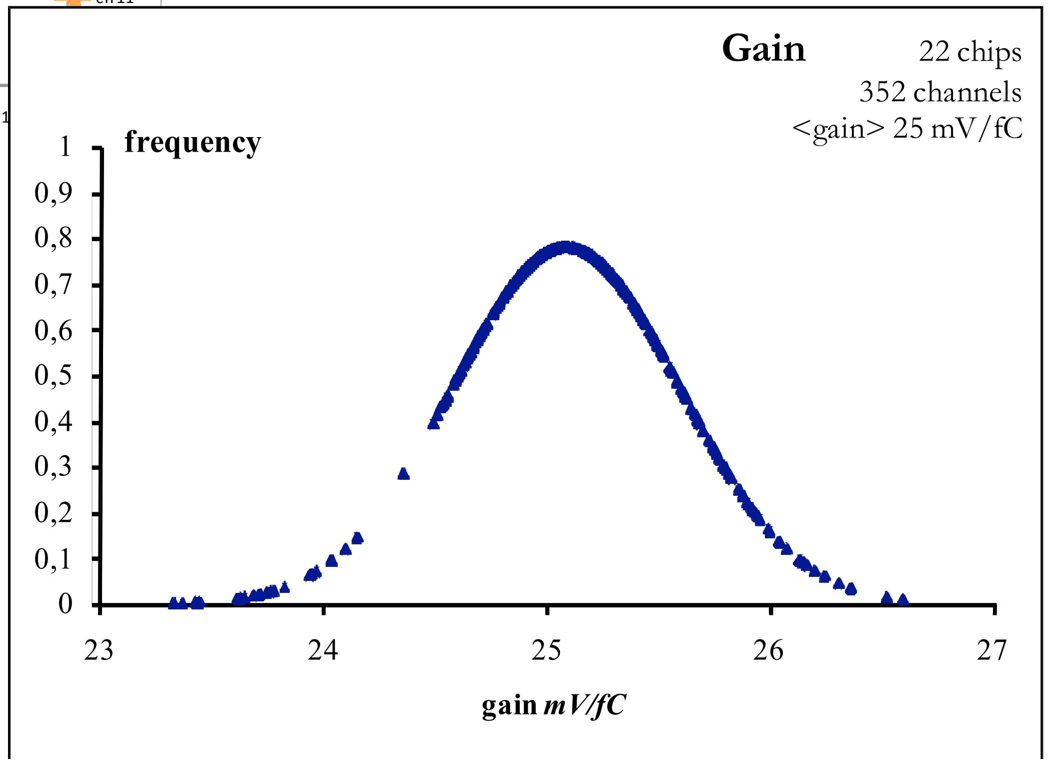
1. Charge sensitivity → Linearity
2. Uniformity among channels
3. Time-walk
4. ENC
5. Cross-talk
6. Threshold calibration curve
7. Pulse-width calibration curve (vs. Vmon voltage)
8. Functional test of digital section:
    a) SPI interface (write/read internal registers, DACs and ADCs)
    b) Data readout

Prototype testing GASTONE16 1’st release (I)

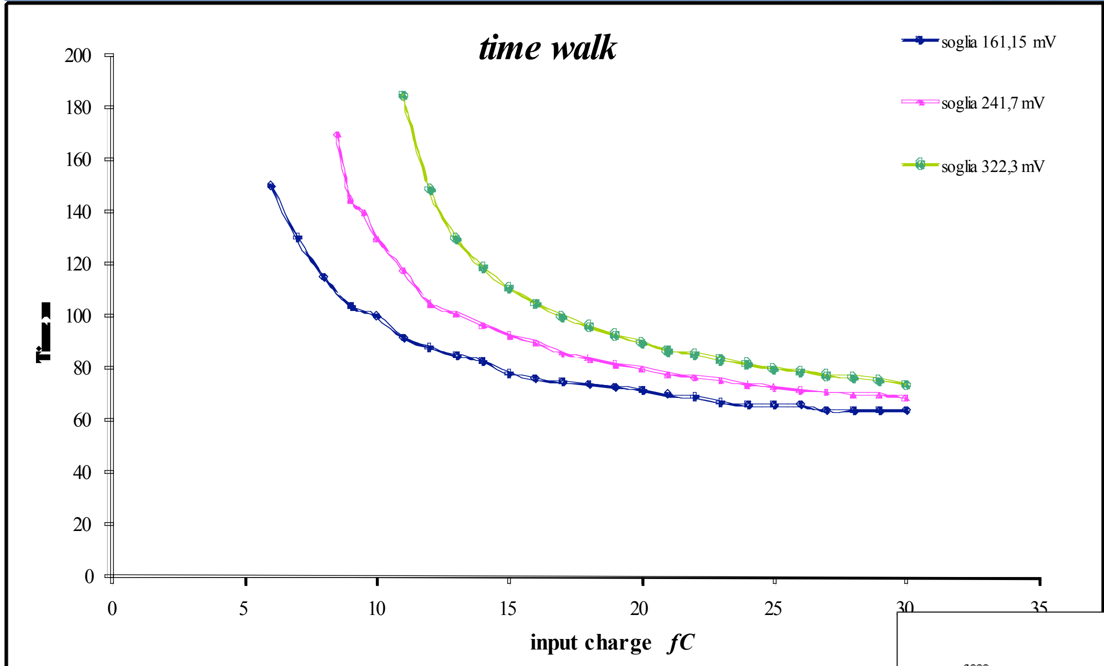


Charge sensitivity, linearity and uniformity

Gain sensitivity measurement
(average of gain slope)



Prototype testing GASTONE16
1'st release (II)

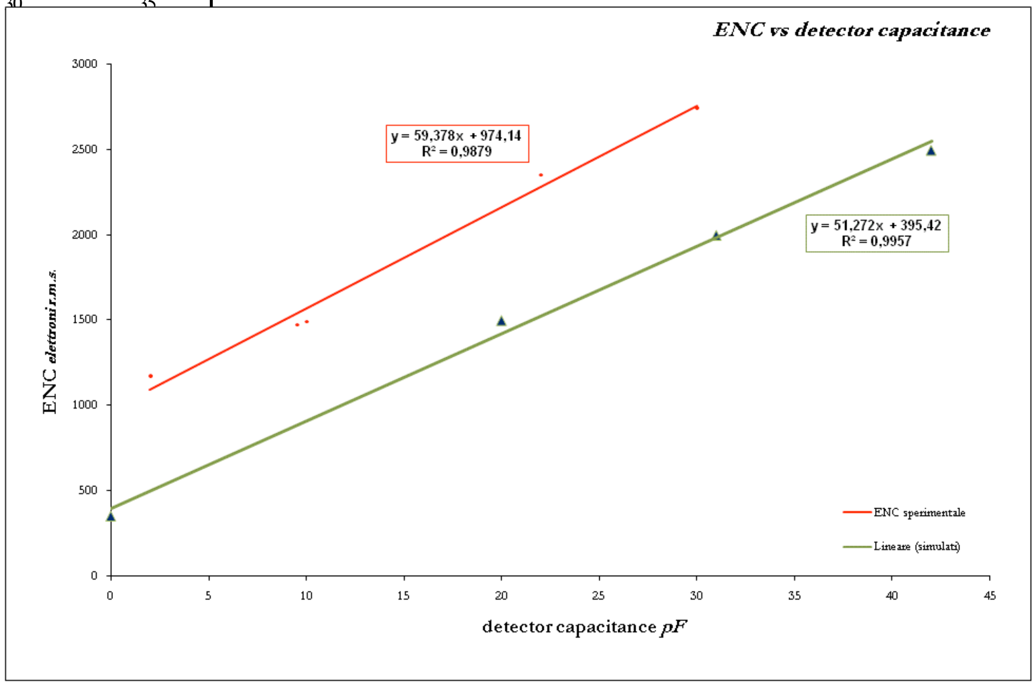


Different threshold values:
- Th1 = 6.45 fC
- Th2 = 9.67 fC
- Th3 = 12.9 fC

$$\sigma_t = \frac{ENC}{Q_S} \times t_r$$ (time jitter)

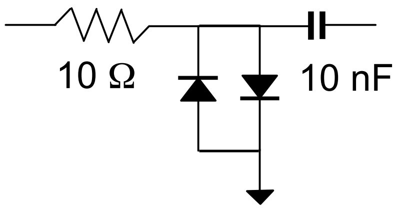
$$t_W = \frac{Q_{th}}{Q_S} \times t_r$$ (time walk)

ENC sim = 395 e⁻ + 51 e⁻ /pF
ENC meas = 974 e⁻ + 59 e⁻ /pF

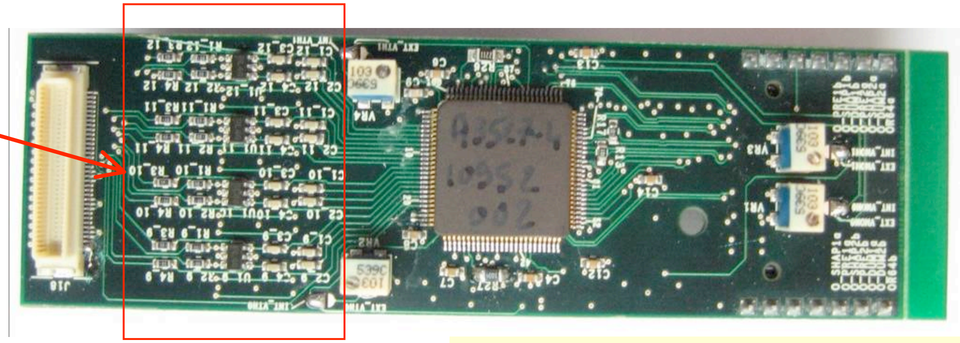


Protection network against discharge

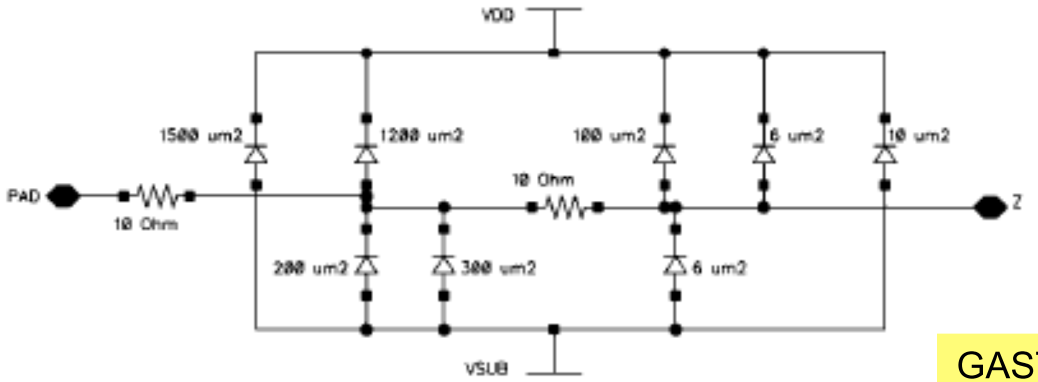
Input protection &
strip reference network



GASTONE16 1’st release (95x30 mm^2)



1. Wasting space on FEB
2. strip referred to GND → AC-coupling



GASTONE16 2’nd release contains integrated in the input pads a protection network against the (remote) discharge probability of the triple GEM (« 10‰)

1. Input protection network inside chip
2. Strip DC-coupled and referred to in-MOS (~500 mV)

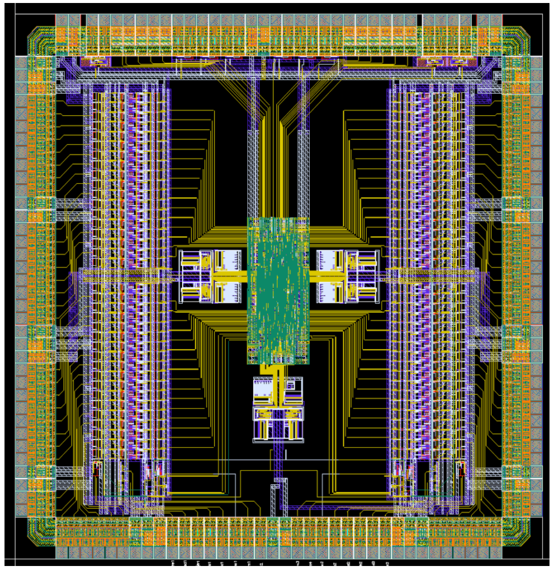
Protection Network Lab Testing

Cscarica	Vscarica	Resterna	Risultato
940 pF	460	56 (pth)	Vivo dopo 50 scariche
470 pF	850	56 (pth)	Morto dopo 3 scariche
470 pF	850	110 (pth)	Vivo dopo 60 scariche
470 pF	950	110 (pth)	Morto dopo 42 scariche
470 pF	1050	110 (pth)	Vivo dopo 30 scariche
470 pF	1050	100 (ResArr 0603)	Morto dopo 12 scariche
470 pF	1050	94 (47+47 ResArr 0603)	Morto dopo 9 scariche
470 pF	950	94 (47+47 ResArr 0603)	Morto dopo 23 scariche
470 pF	950	140 (47+47+47 ResArr 0603)	Vivo dopo 30 scariche
470 pF	950	100 (ResArr 0603)	Vivo dopo 30 scariche
690 pF	950	100 (ResArr 0603)	Morto dopo 2 scariche
690 pF	950	140 (47+47+47 ResArr 0603)	Vivo dopo 30 scariche

Provoked discharge voltage values related to the foreseen induction thicknesses…and something more (1, 2, …mm) by means an external RC network

3'rd release features summary

GASTONE parameters	
Input impedance	400 Ω
C_{det} range	0 – 150 pF
Number of channels	64
I/O	Differential and serial
Baseline restorer	No
Total Gain sensitivity	22 mV/fC (C_{det} = 0 pF)
Peaking time	80 ns÷150 ns (C_D=0 ÷100 pF)
Measured X-talk	< 1%
ENC (rms) measured on detector	800 e^- + 40 e^-/pF
Threshold sensing/setting	8 bits ADC/DAC (16 chs modularity)
Input protection circuitry	Integrated in each input channel
Internal trigger generation	For test purpose
Programming test pulse capability	Q_{inj} = 0 – 50 fC
Power consumption	7.5 mW/Ch

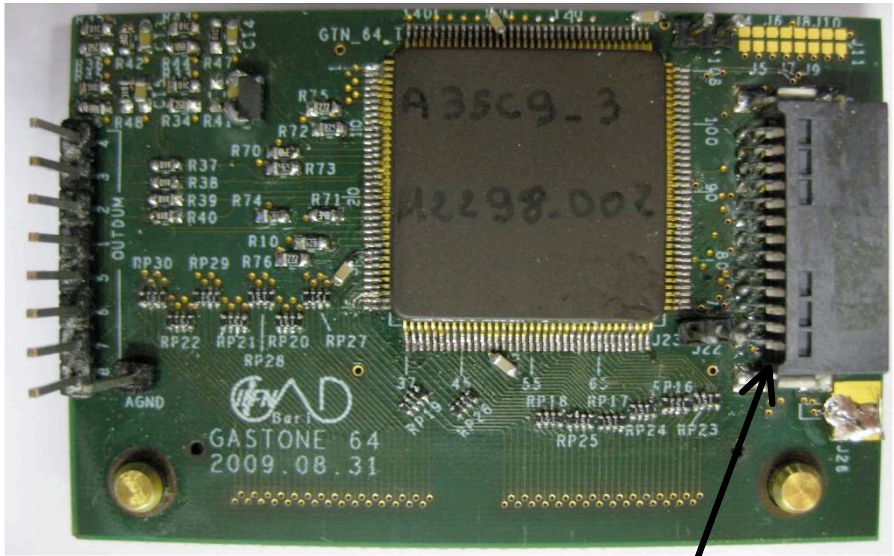


GASTONE64 layout of final release

- Noise measurements in the final setup (i.e. boards connected to the layer 0 readout strips) show a value of 800 e^- + 40 e^-/pF = 1.088 fC (150 pF) → 1.5 fC will allow good event selection.

Front-end board (120 channels)

Dimensions: 62x40 mm²



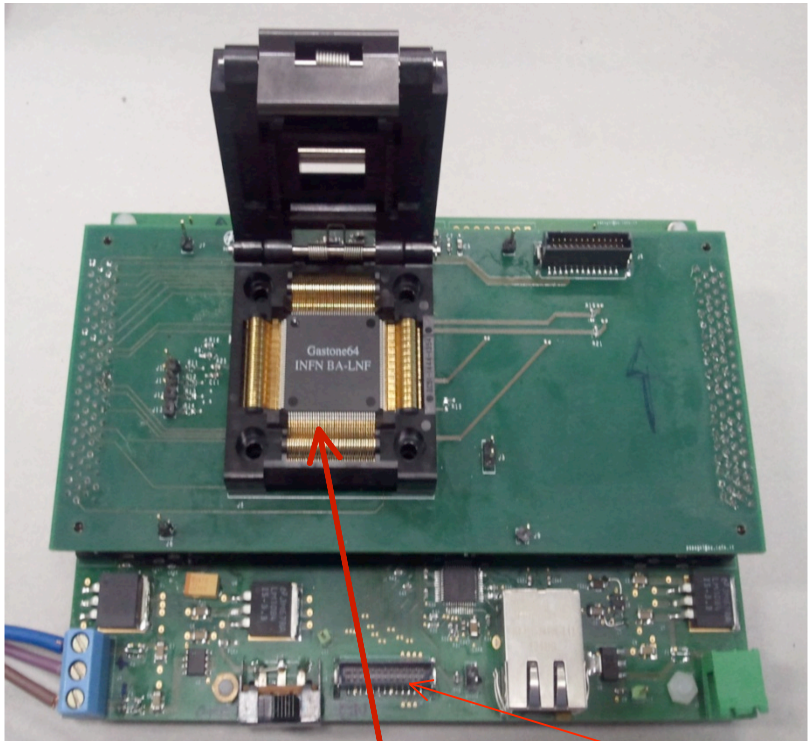
Input connector (GEM)
- **120 strips**
- **GND**

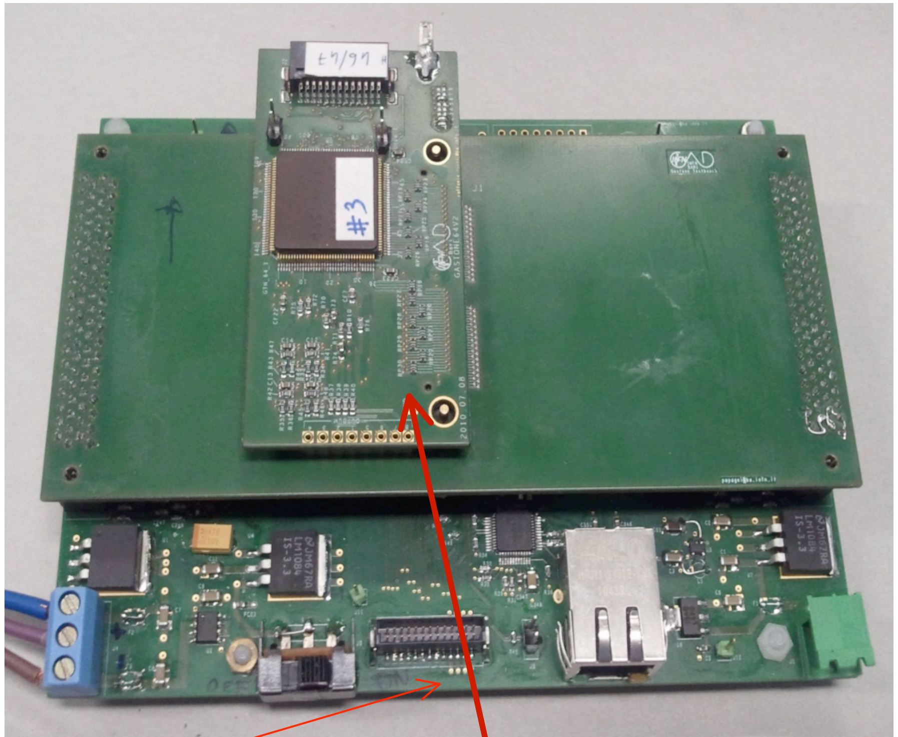
I/O connector
- **Power supplies**
- **SPI slow control bus**
- **Readout bus**

About 700 chips plus 340 VFEB including spares has been built to fully instrument the final detector

Test Bench for FE validation

- Mother Board controlled through Ethernet
- 2 “piggy back” boards for chip test only and with FE-Board

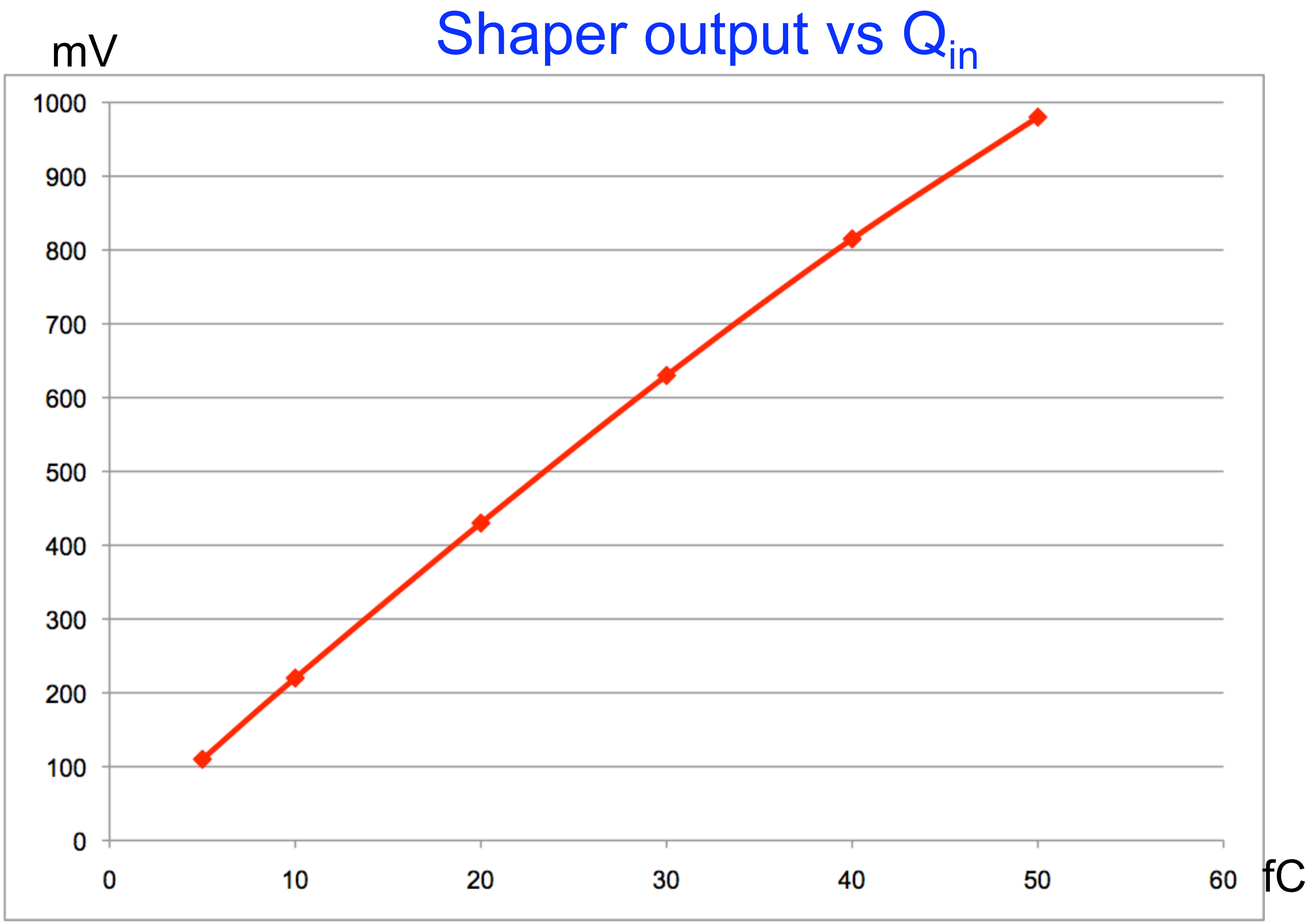




Piggy-socket board

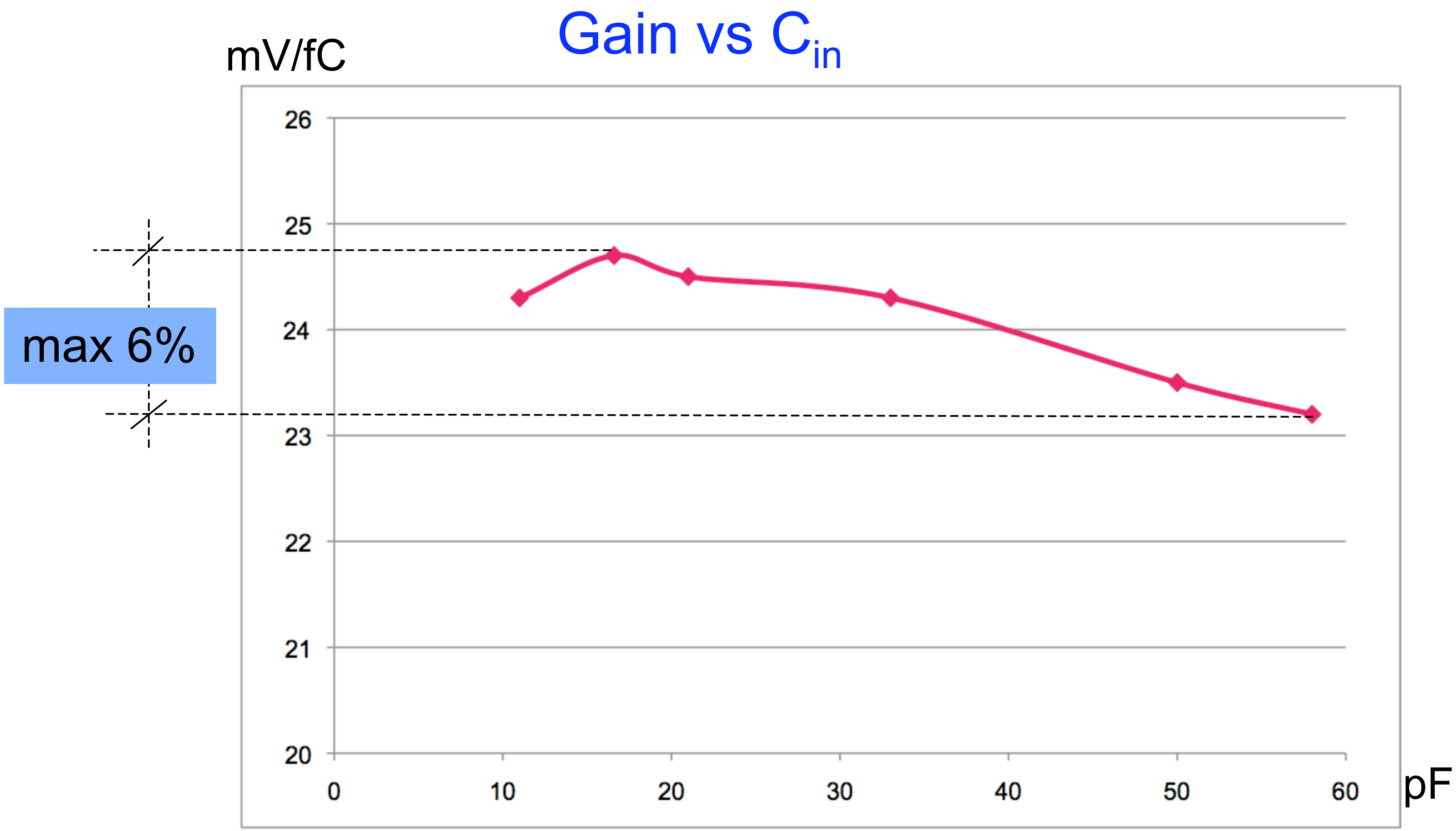
Piggy-FEB board

Analog Section – Preamp + Shaper



GASTONE64 final release

Analog Section – Preamp + Shaper

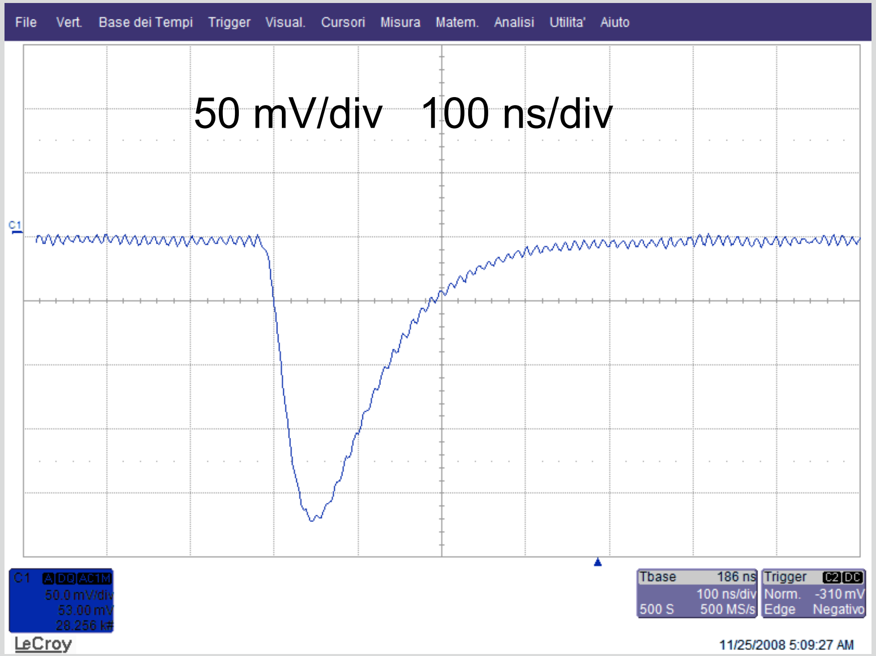


Measured xtalk ~ 1%

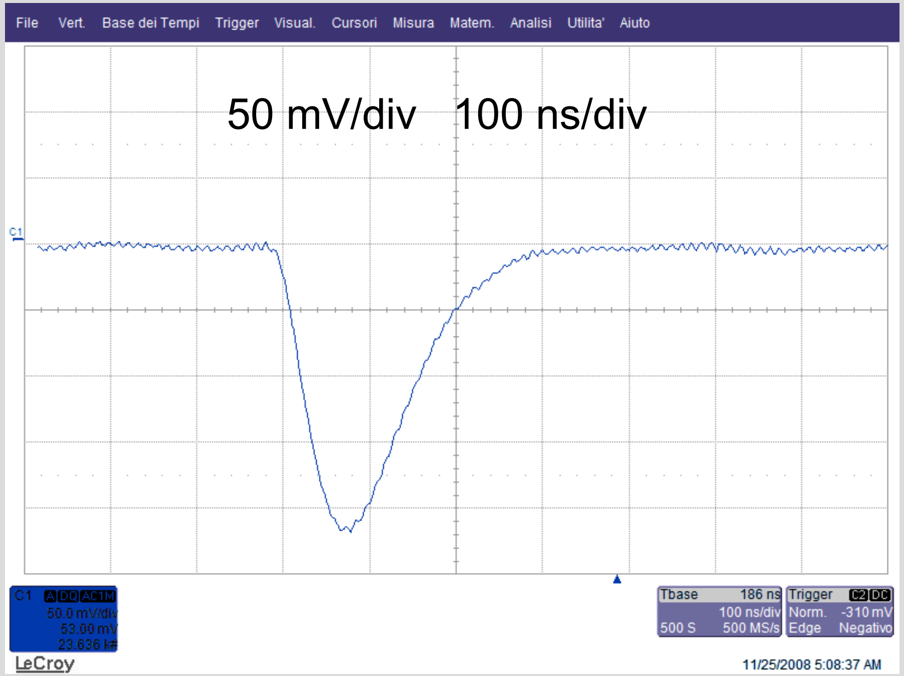
GASTONE64 final release

Analog Section – Preamp + Shaper

Shaper output (Q_{in} = 10 fC)

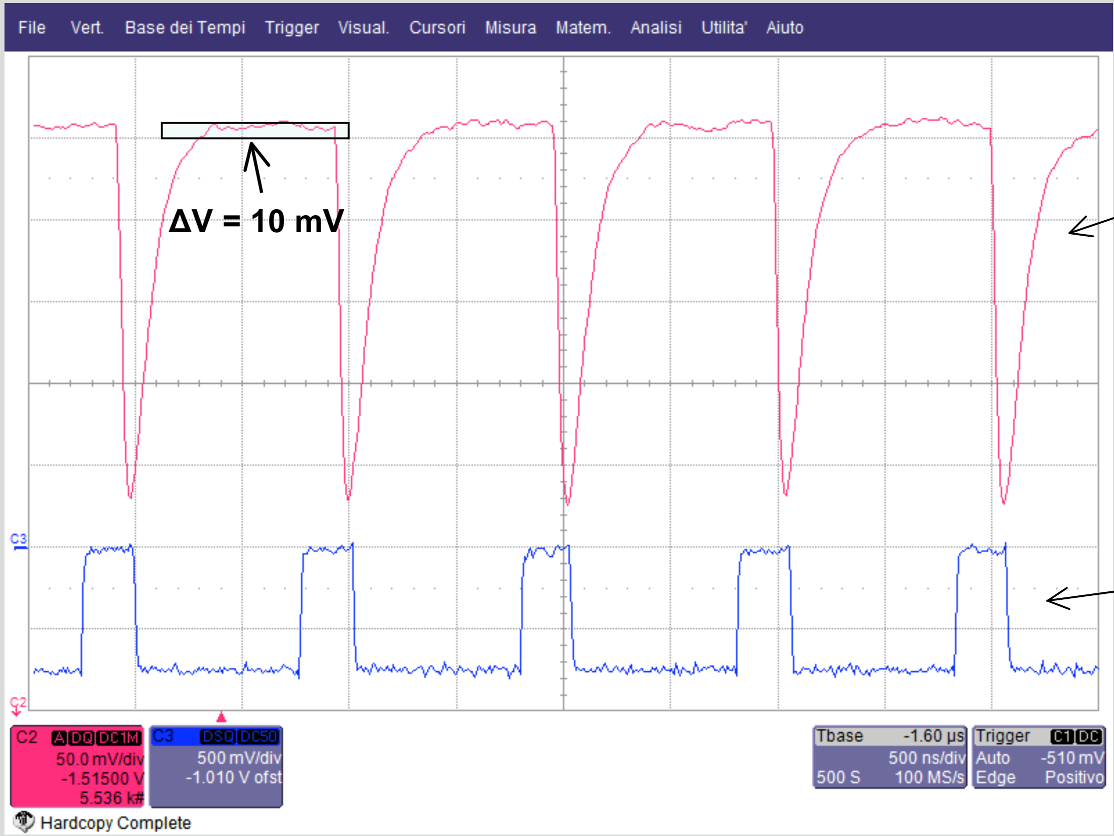


C_{in} = 10 pF



C_{in} = 50 pF

Analog Section – Max freq



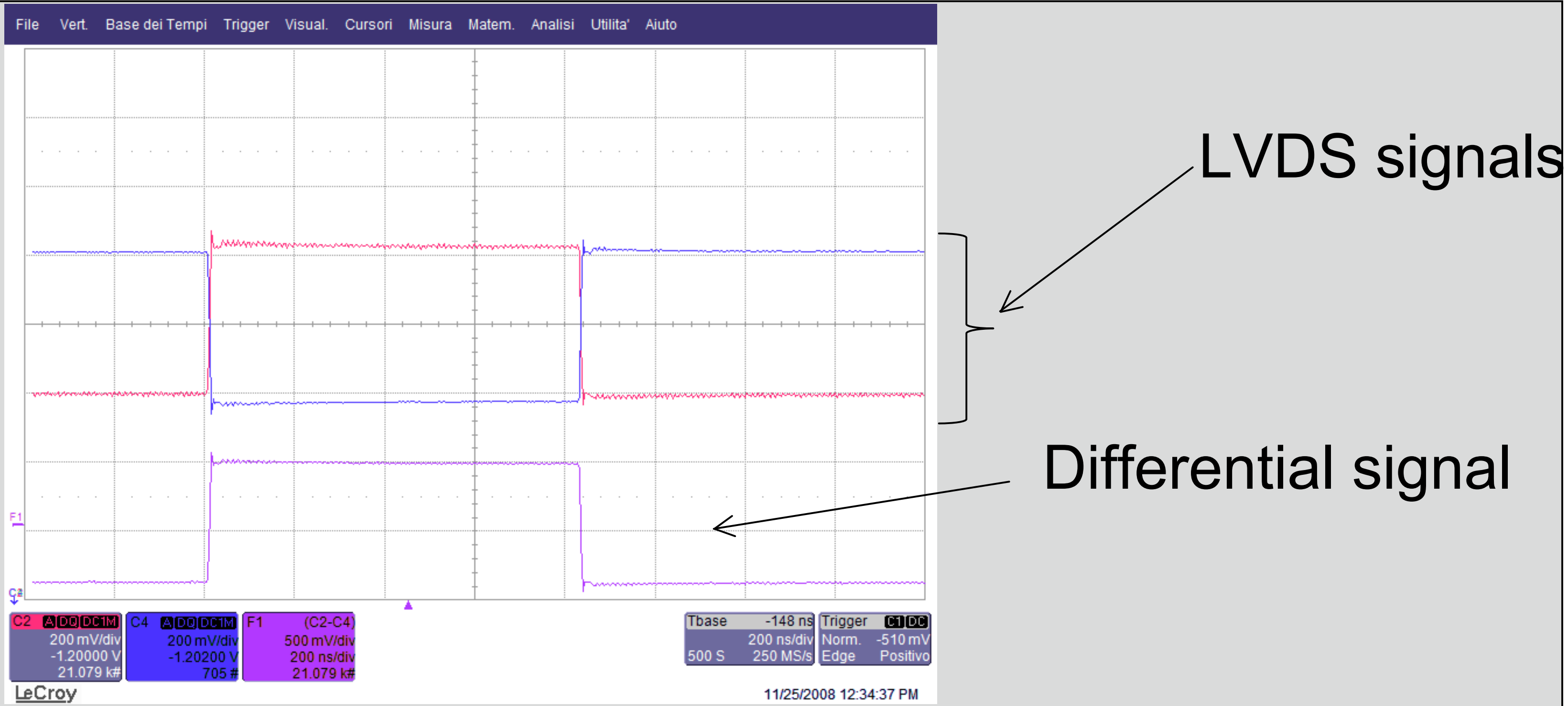
Shaper output

Q_{in} = 10 fC
V_{th} = 3 fC

Monostable output (NIM)

- f_{max} = 1 MHz
- pile-up effect: baseline shift = -10 mV → -0.5 fC

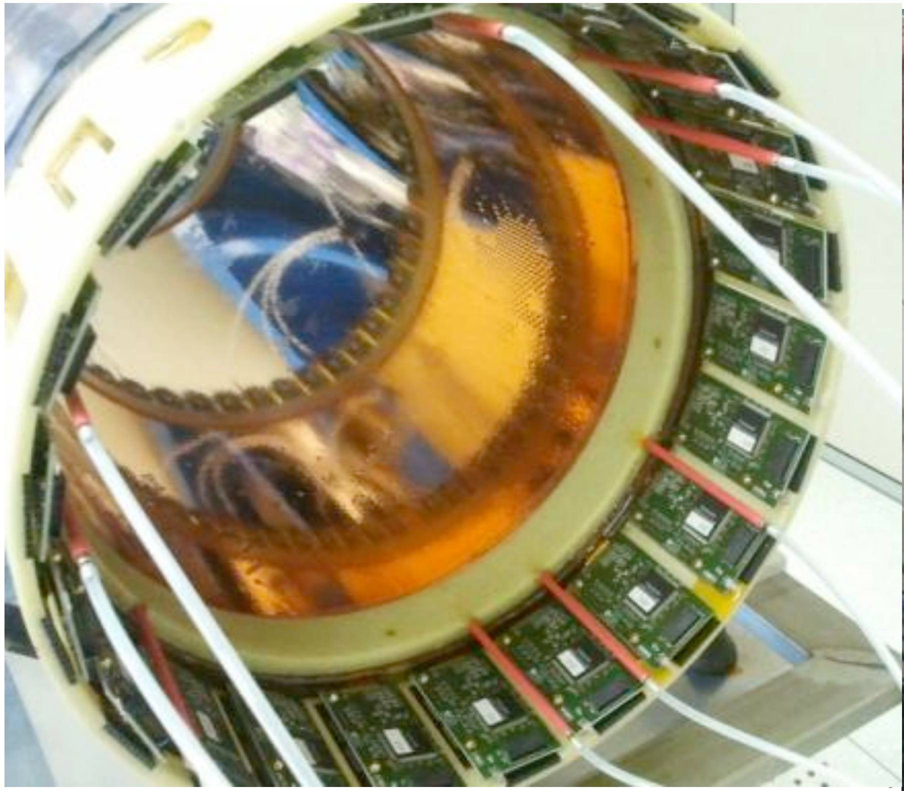
Digital Section – LVDS driver



- Common mode: 1.2 V
- Voltage swing: 400 mV
- Differential signal voltage swing: 800 mV
- Capable to drive long lines (20 m)
- Power consumption: 12 mW

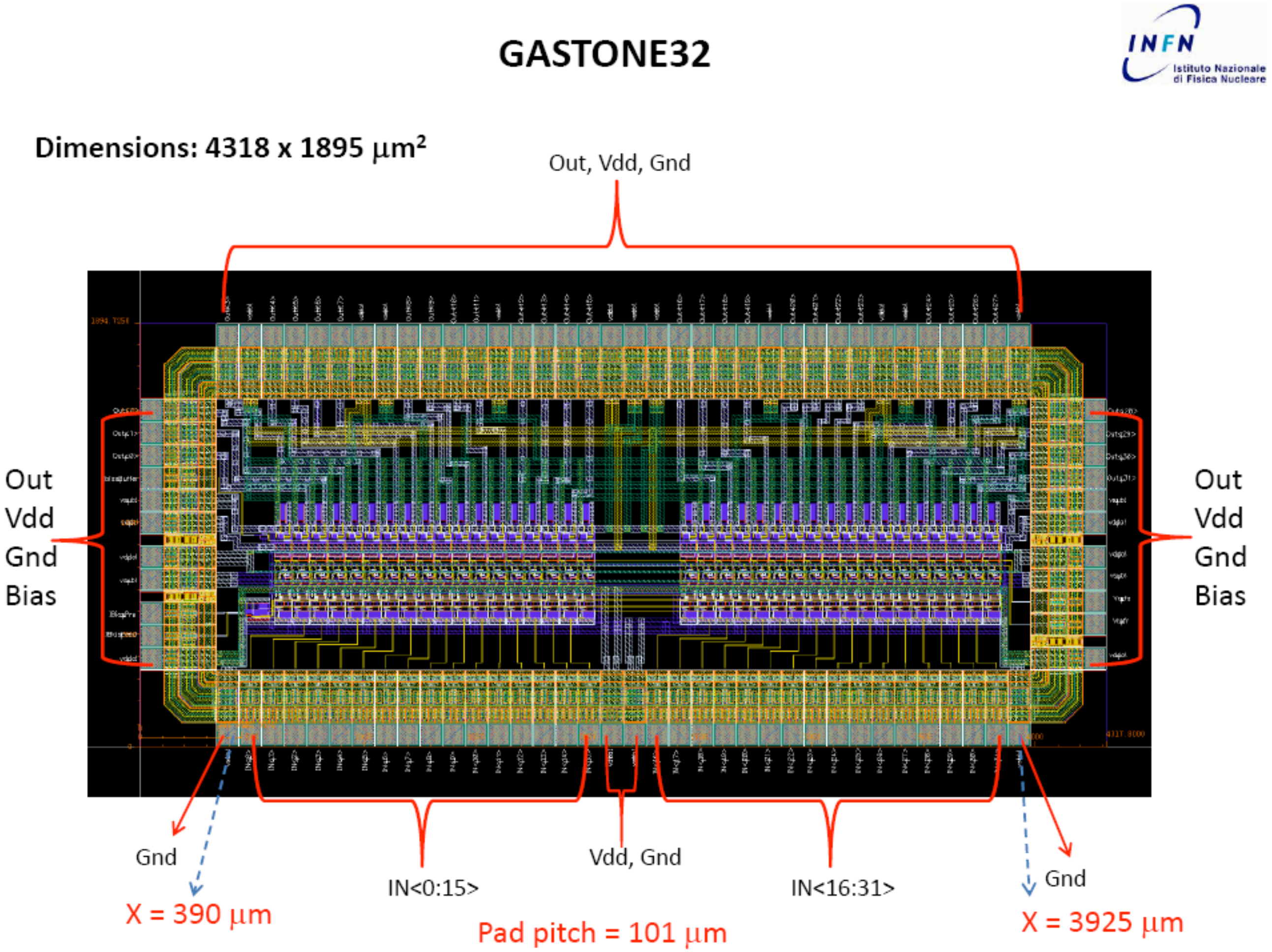
FEE Integration

- Three layers (1,2 and 3) out of four ready and working
- The fourth is waiting for raw materials coming from CERN
- The layer 4 will be ready (we hope) for the end of the year
- Afterward the sliding procedure of all layers the full detector will be ready for validation w. muon test



GASTONE32 with analog readout (the story continues)

- Developed for R&D of a detector for medical applications
- a daughter version including only analog channel has been designed
- It includes only 32 input channels and corresponding output channels
- It produces an amplified and shaped output of the detector input



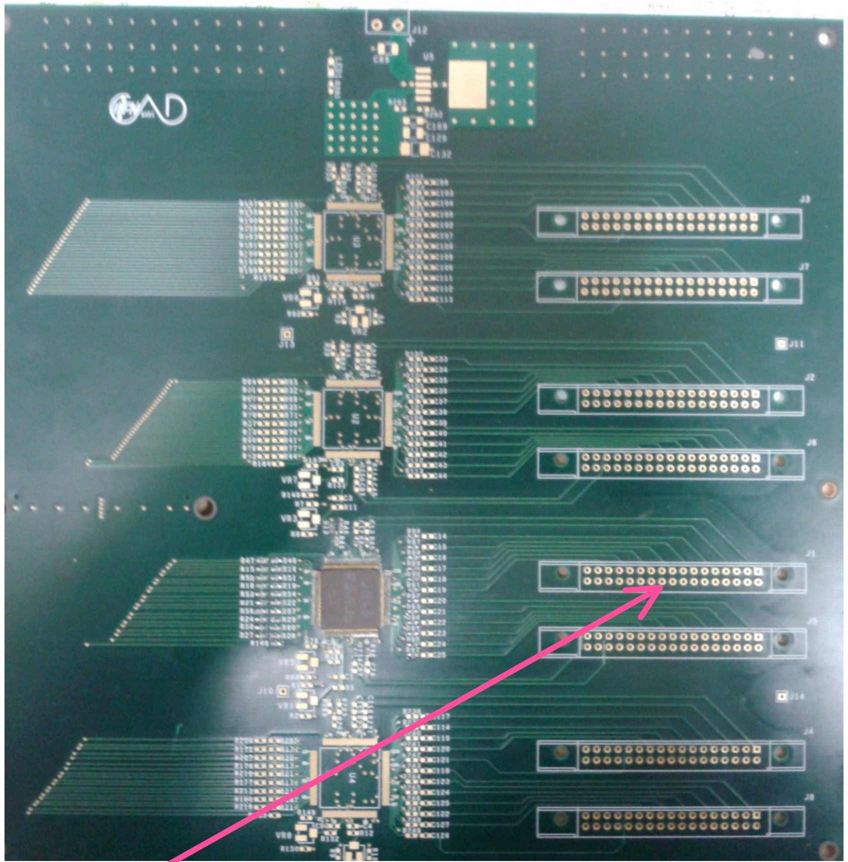
GASTONE32 Board

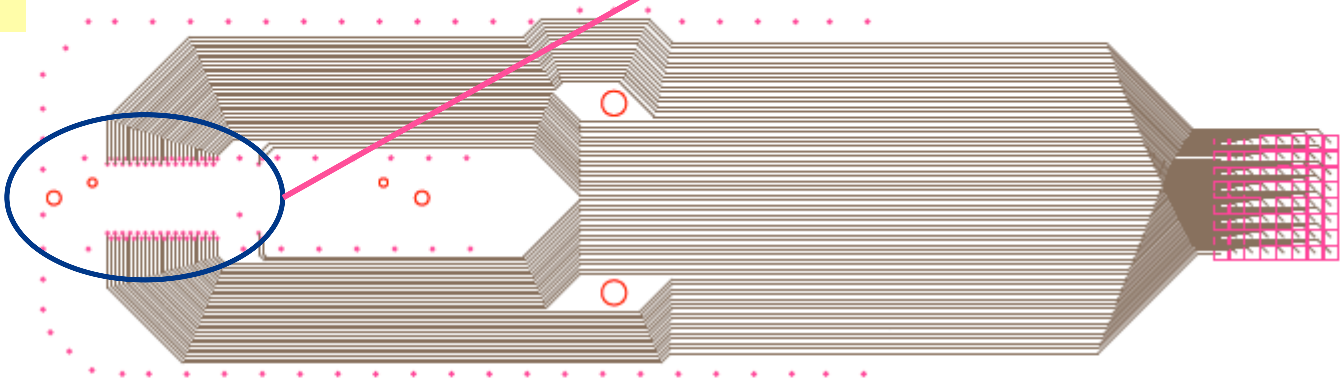
•GASTONE 32 Board ready to be mounted on a small planar 3-GEM with resistive 2x2 mm^2 pad readout; total # pad 8x8=64
total area of 16.5x16.5 mm^2 (*charge dispersion* readout method)

•A total of 128 channels are to be fully instrumented to readout a total area of 272 mm^2

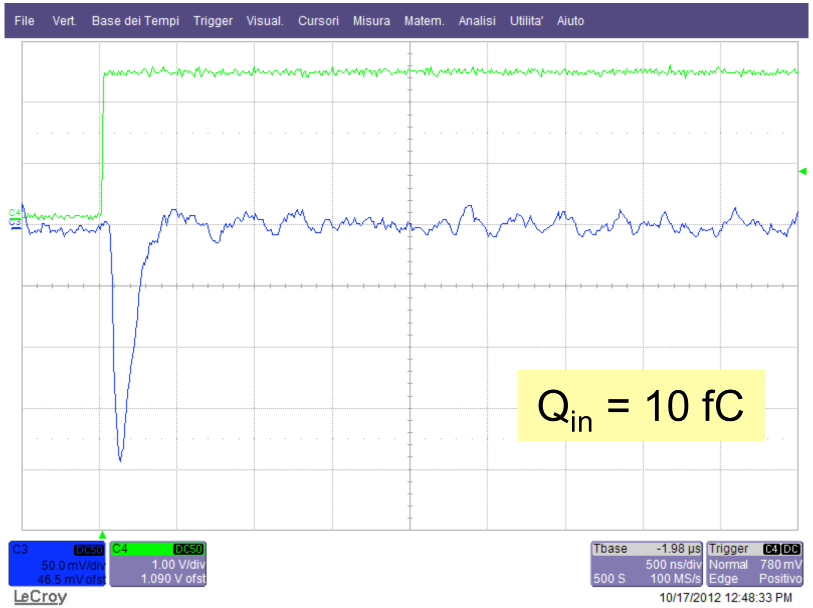
• The analog output will be read out through a "Peak Sensing" ADC for charge *center of gravity* analysis

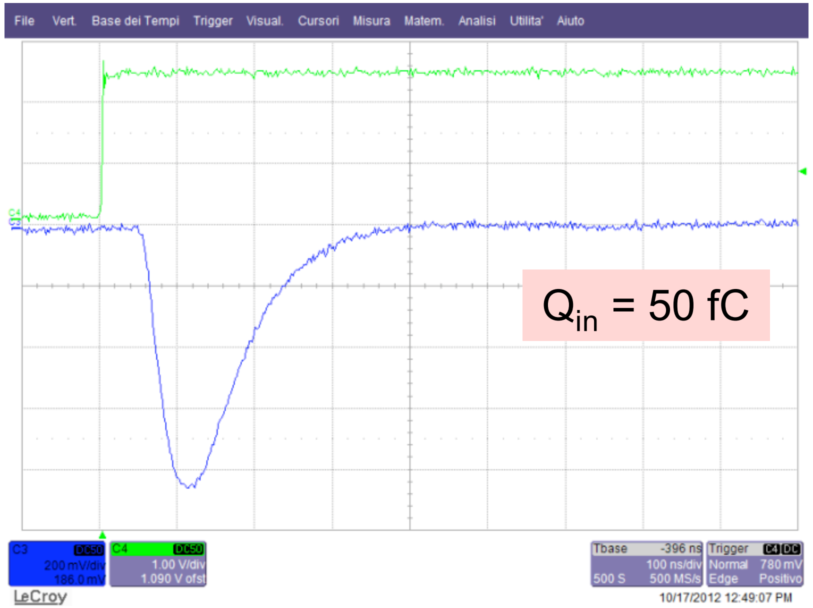
•It's a project to be further developed for what concern the readout architecture i.e.:
i.Do we need to develop an ADC per channel or for a group of channels?
ii.…and something more

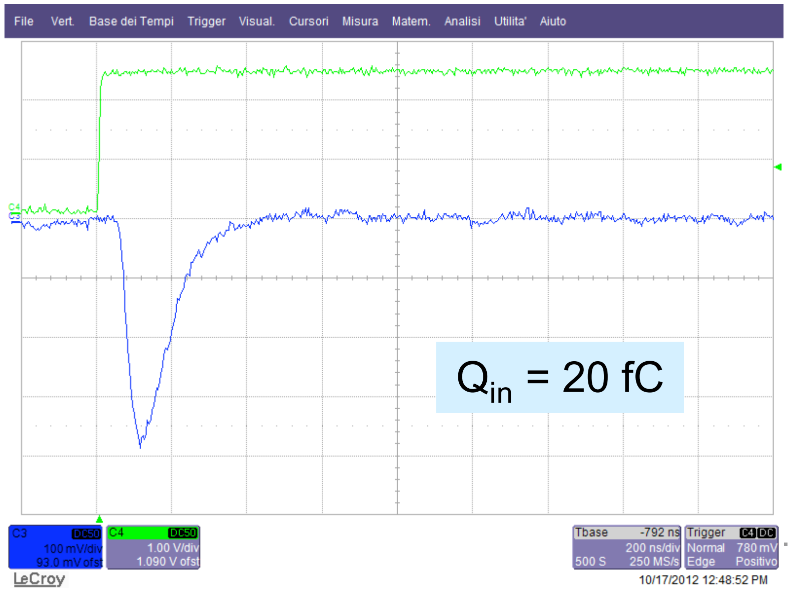


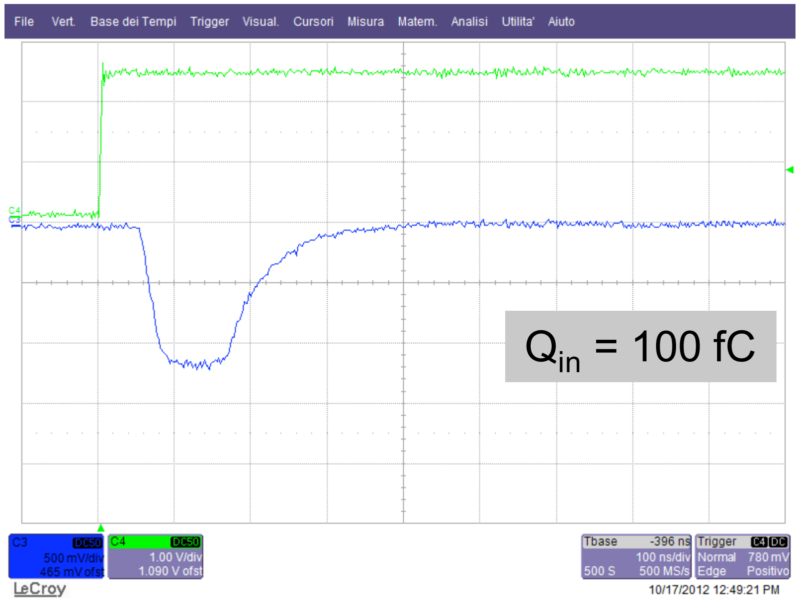


GASTONE32: some test results









New design for rad-hard applications(?)

- What about rad-hard design
- This implies the choice of well evaluated design strategy and technology
- A big effort has been produced in the past on this item thanks to LHC experiments by Bari Group
- Bari Group was participating in the past to many radiation hardness campaign on different technologies [(1)]
- In parallel it is involved in collaboration with CERN to another rad-hard project
- It is well acquainted on rad-hard technology available nowadays by European brokers

(1)

a. L. Gonnella et.al. “Total Ionizing Dose effects in 130-nm commercial CMOS technologies for HEP experiments”. NIM A 582 (2007) 750-754
b. A. Gabrielli et.al. “Design and submission of rad-tolerant circuits for future front-end electronics at S-LHC

Conclusions

- The development of GASTONE64 has proceeded hand in hand with that one of the readout plane

- The project has required a period of time of about 4 years to reach the final design passing through three releases

- GASTONE64 is a mature project ready to take real data

- GASTONE32 should be revised to satisfy new requirements (analog readout, rad-hardness, etc.) and t.w. some new anodic readout strategy (50 μm spatial resolution is feasible)

- Very advanced European VLSI technology complying the previous requirements are available to our Community

Acknowledgements

Fabio Sauli holding a 30x30 cm^2 GEM electrode.

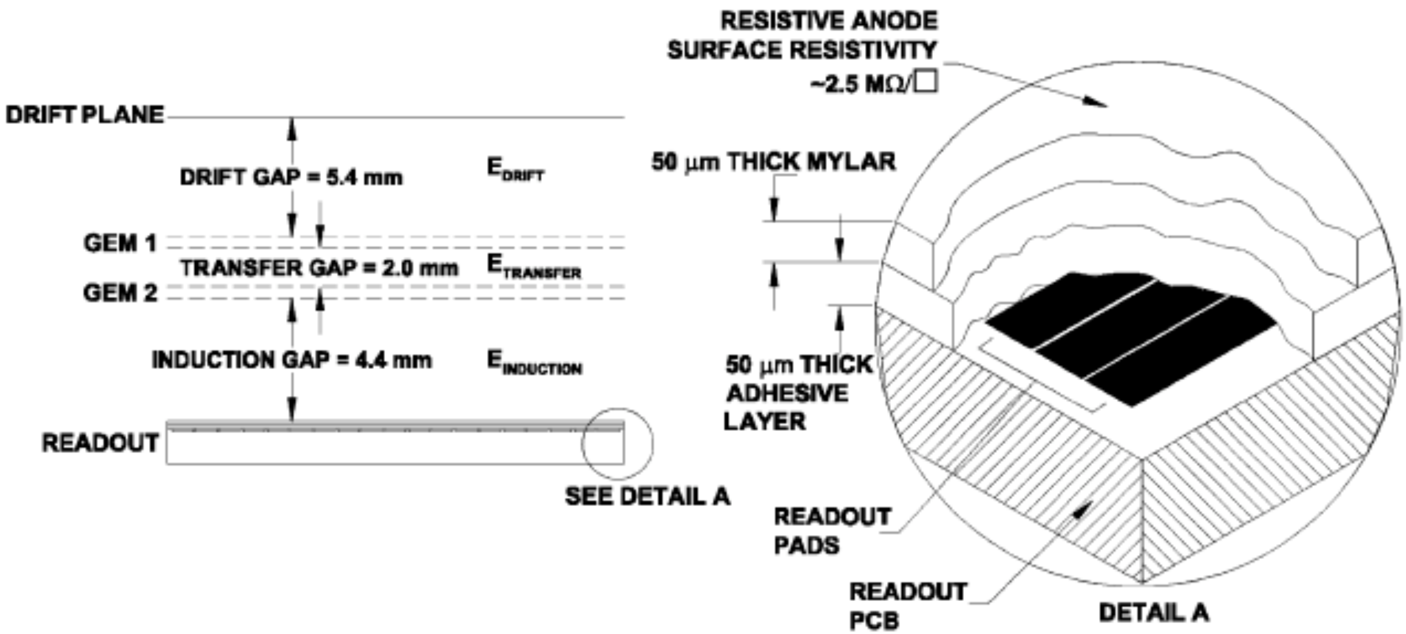
Angelo Gandi (left) and Rui de Oliveira with a large GEM foil

1. Many thanks to the inventor and the developers too
2. …and to you for your patience!

SPARE SLIDES

Spatial resolution

- How to improve spatial resolution without to increase significantly the electronic channels number?
- Analog readout with "*centre of gravity*" method
- New anodic readout by using "*charge dispersion*" method with resistive anode
- Or both?

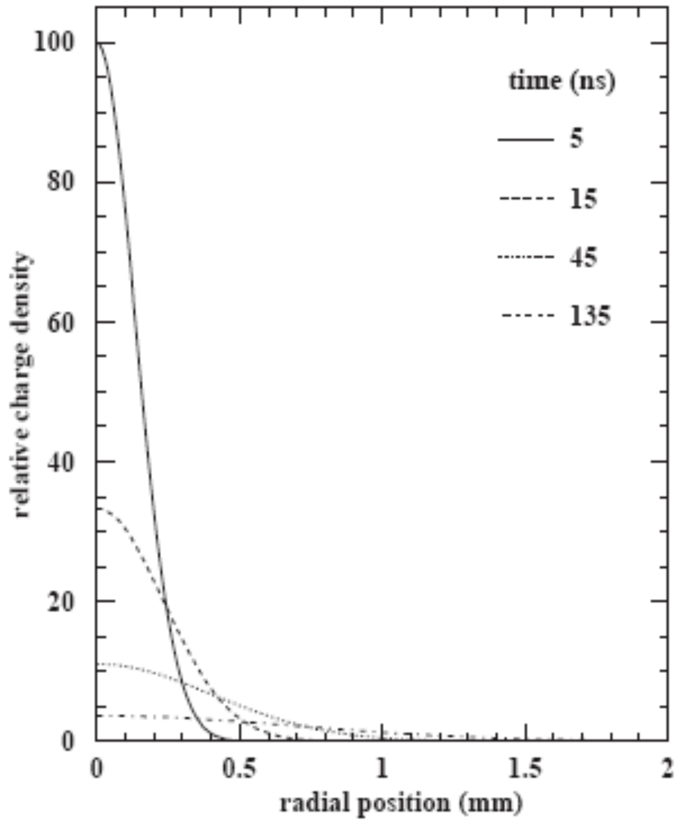


Charge dispersion method

- Starting from the so called "Telegraph equation" for a resistive surface

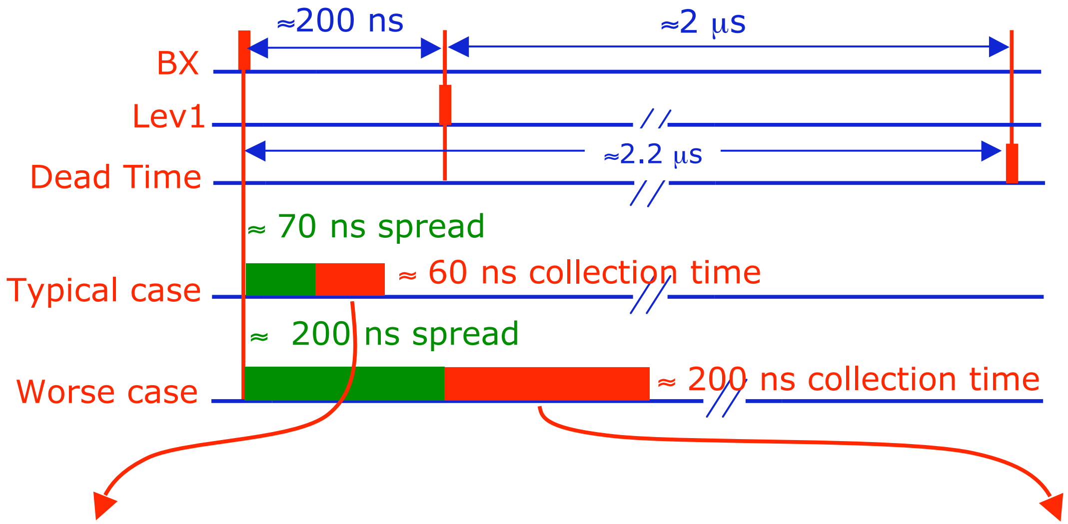
$$\frac{\partial \rho}{\partial t} = h\left[\frac{\partial^2 \rho}{\partial r^2} + \frac{1}{r}\frac{\partial \rho}{\partial r}\right]$$

- the charge density function is given by $\rho(r,t) = \frac{1}{2th}\exp(-r^2/4th).$
- It is function of time

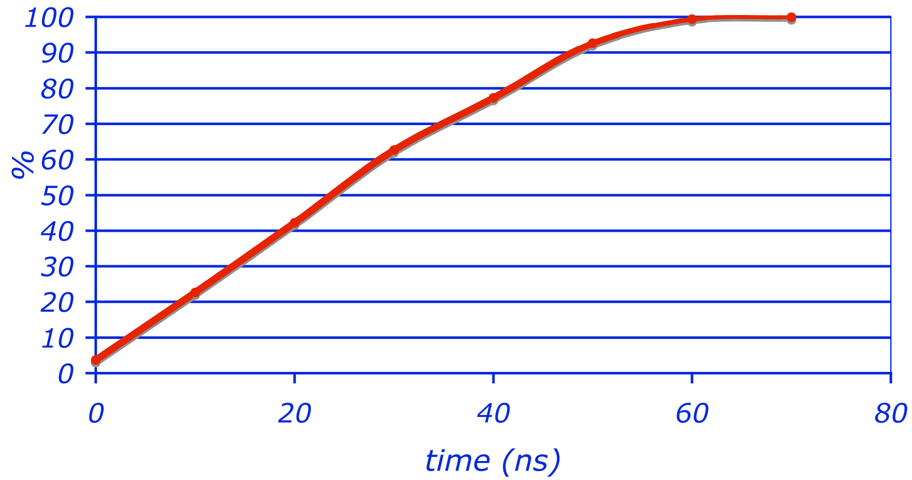


- Its shape depends on the pad geometry
- …on the location of pad readout wrt the initial charge
- …and the RC time constant of the system
- The signal on the readout strip can be computed by:
  – integrating the charge density function
  – Cluster dimensions
  – Signal rise time
  – Rise and fall time of the readout electronics

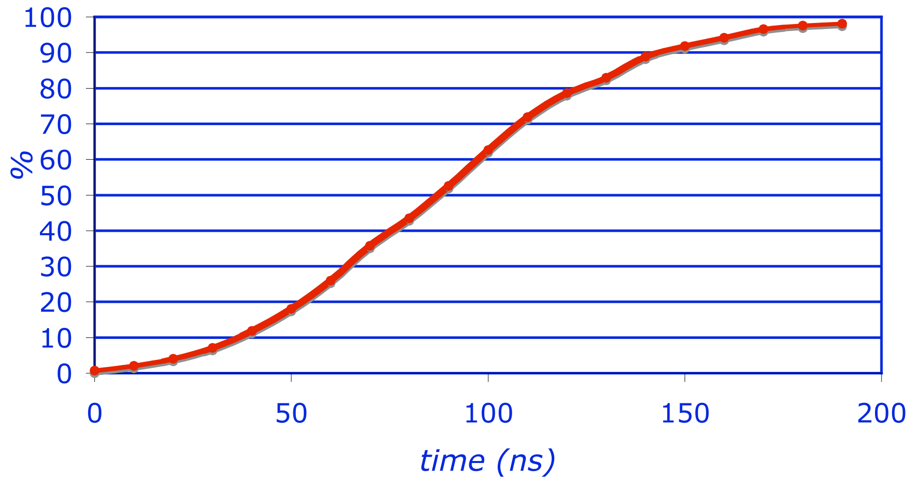
Charge collection time



Charge Collection Time (typical case)



Charge collection time (worse case)



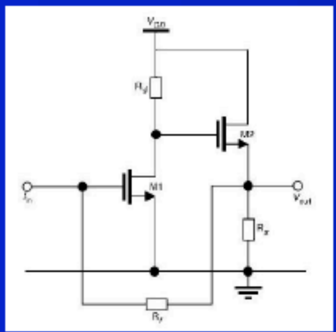
Q_{max} = 10 - 30 fC

Which kind of elctronics ?

Kloe2 IT — Current mode & charge pre

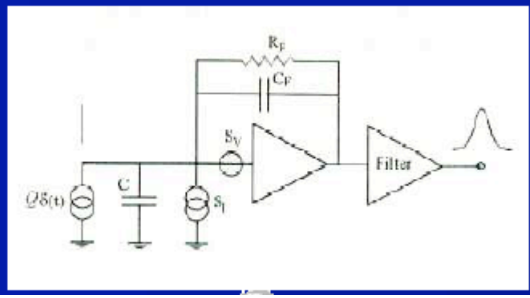
- Current Feedback
  - Require few components
  - Low PD
  - NO Shaping circuit required

  BUT
  - C_{DET} sensitivity
  - Inductive input behavior due to internal pole



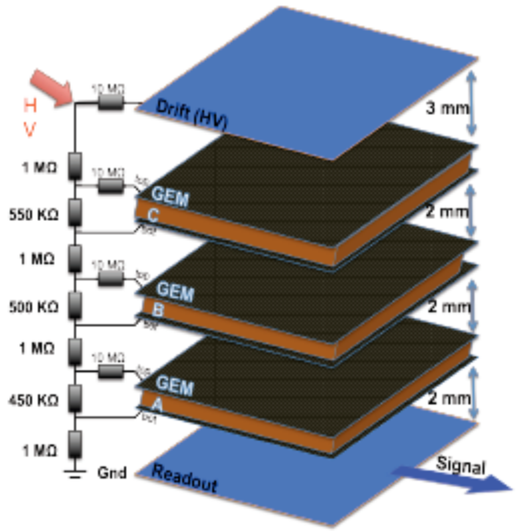
- Charge Preamplifier
  - Low C_{DET} sensitivity
  - Resistive dominant term in input impedance up to frequencies close to f_t

  BUT
  - More components required
  - Power consumption
  - C_{DET} matching required for optimum S/N ratio → big size MOS devices
  - Shaping circuit required



Estrarre dal file: Felici GM 2006 (Kloe Future)

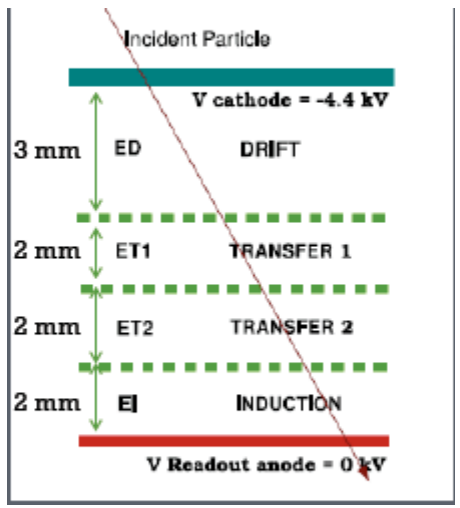
GEM biasing



Biasing each side of the GEM foils produces electric fields for electron drift and an intense electric field across the GEM foils for amplification.

Transfer electric field typically higher than Drift.
Induction electric field typically higher than transfer.
This aids focusing the electrons

Parameter	Value
ED	1.0 kV/cm
ΔVGem1	390 V
ET1	3.0 kV
ΔVGem2	380 V
ET2	3.5 kV
ΔVGem3	370 V
EI	6.5 kV



device block diagram - 3

Analog blocks

Three basic blocks

- a charge preamplifier to integrate the input strip current into a voltage
- a shaper circuit providing noise filtering and semi-gaussian shaping
- a discriminator designed in fully differential mode (together with the AC coupling it helps in reducing the channel to channel offset variations)

AC coupling

The AC coupling is possible because the (relatively) low rate/channel. Moreover it

- restricts the matching problems to the differential discriminator
- improves reliability against low frequency drifts
- improves the device PSRR in low frequency range

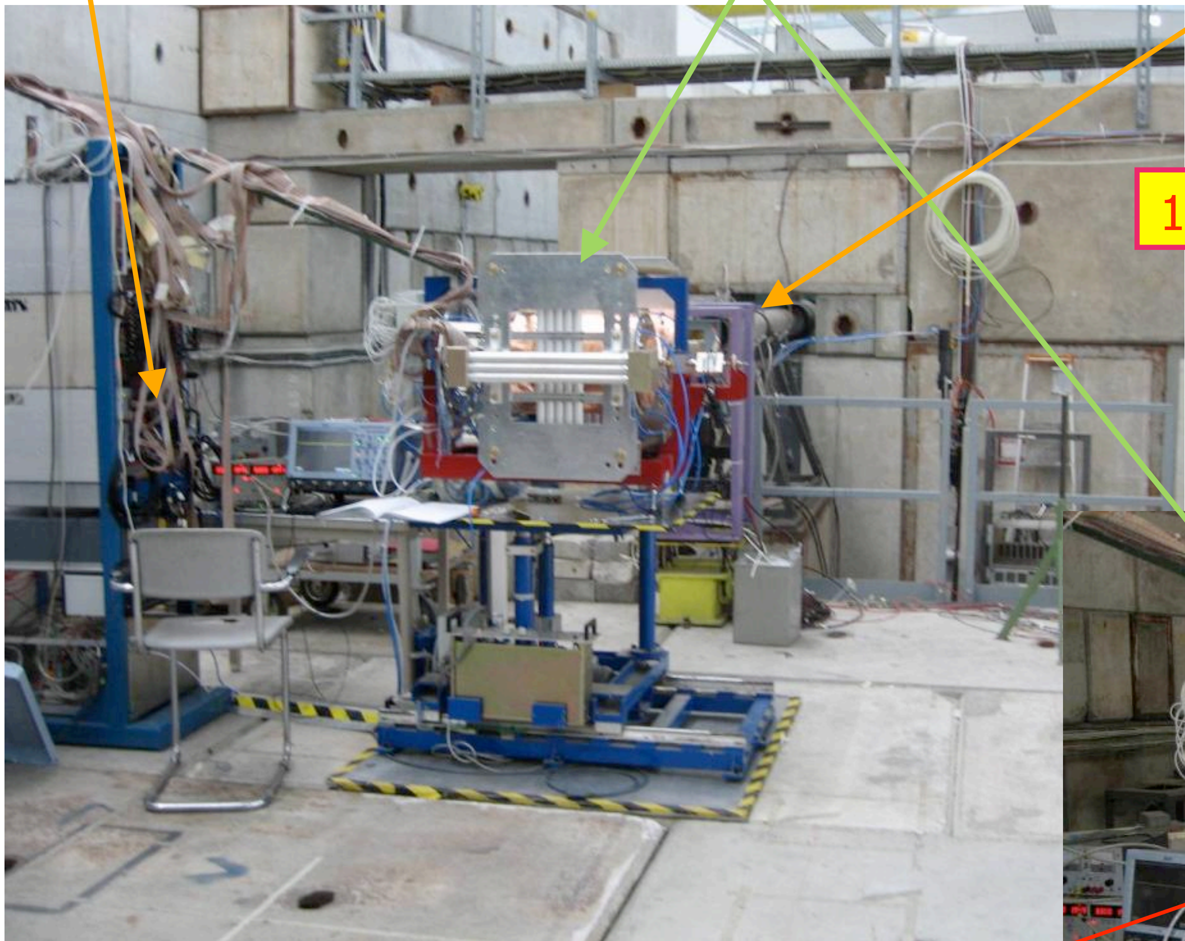
Test beam pictures

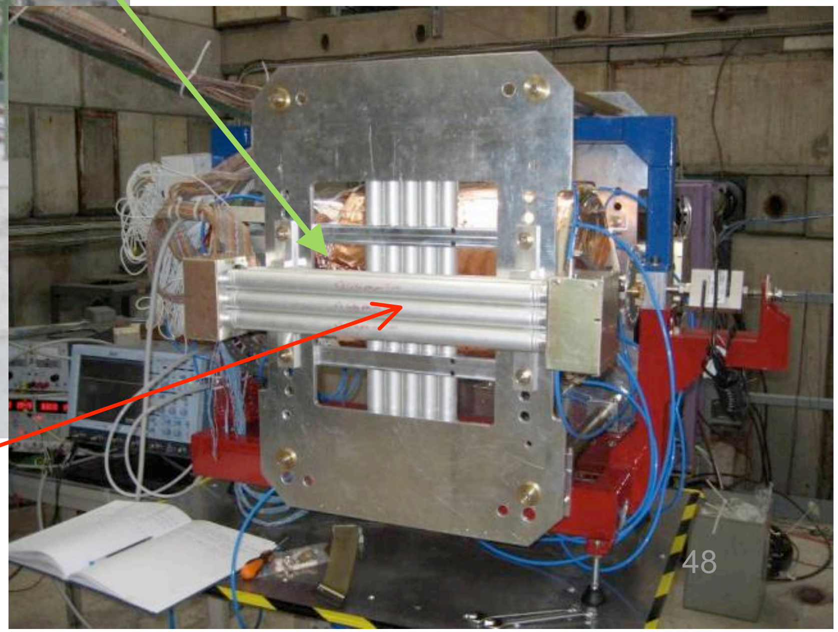
electronics rack

detectors

beam line: 10 GeV pion beam

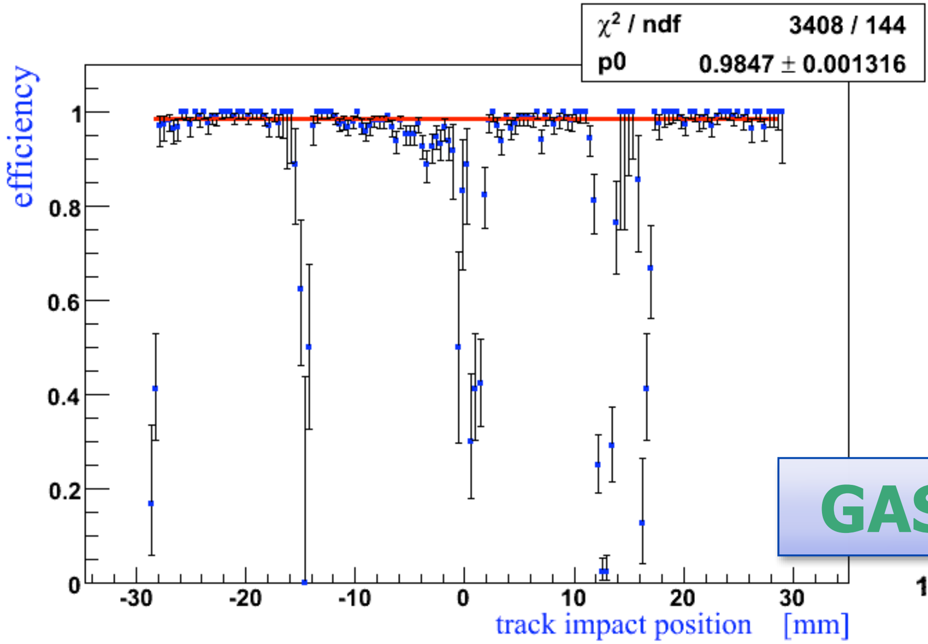
128 ch w GASTONE (0.5M evts)



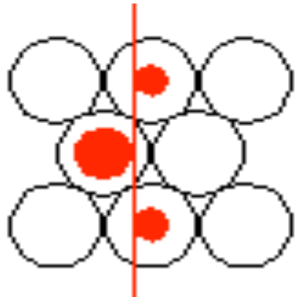


drift tubes in streamer mode for tracking

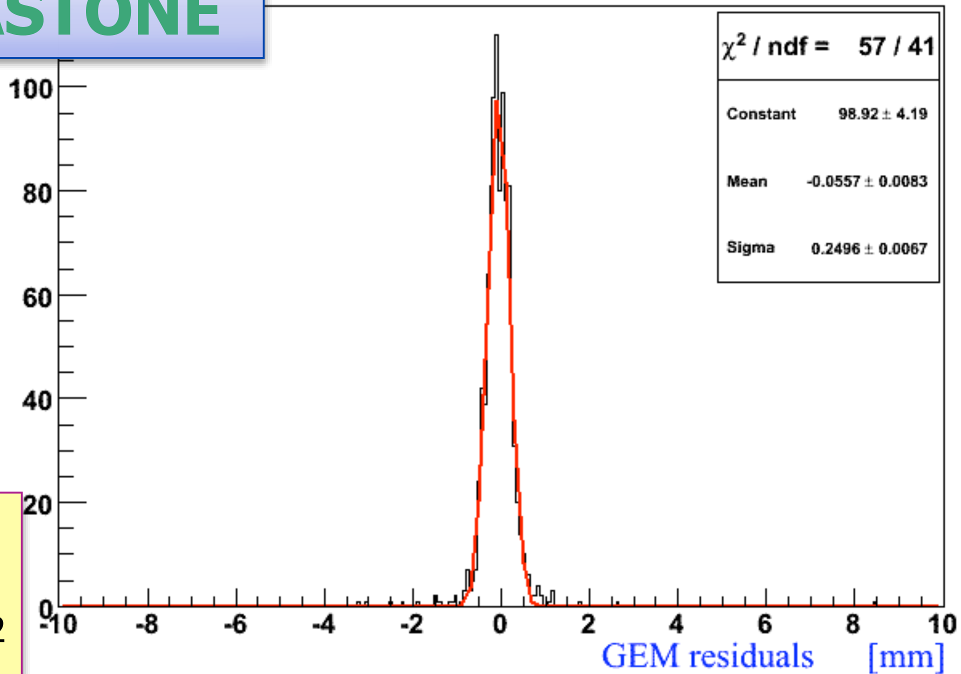
Test beam results



GEM residuals with respect to the track reconstructed by the drift tubes



GASTONE



$\sigma(\text{global})^2 = \sigma(\text{GEM})^2 + \sigma(\text{tracker})^2$

$\sigma(\text{GEM})^2 = 250\mu m^2 - 140\mu m^2 \cong 200\mu m^2$

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