Quality test of Readout Flexes PCB exploiting TDR technique

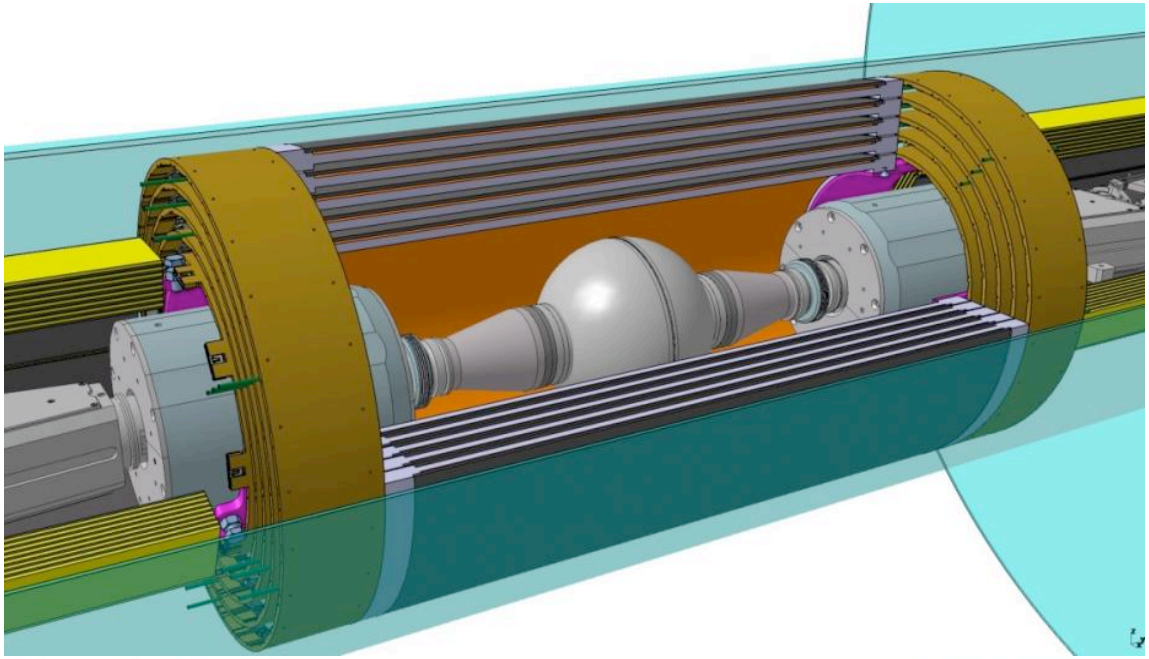
by G. Fanizzi on behalf of KLOE-2 I.T. group

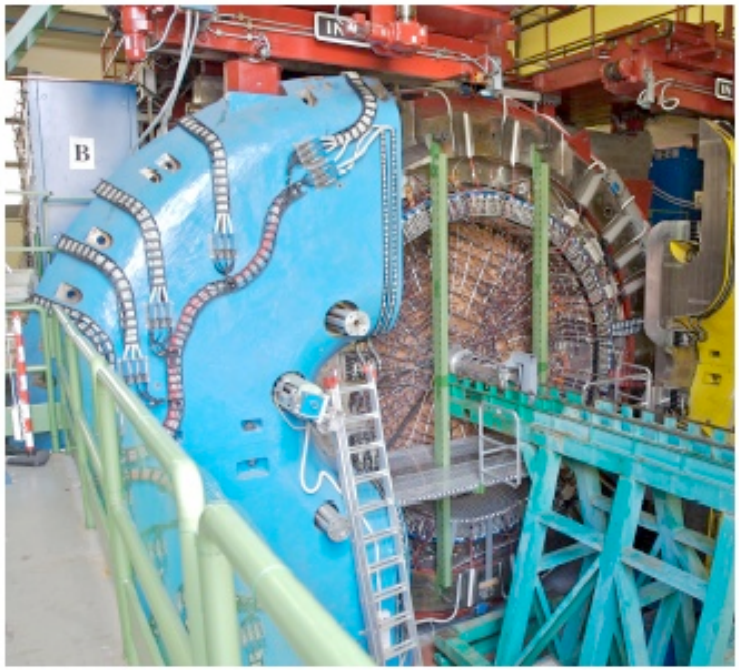
Summary

1) The KLOE-2 Inner Tracker - readout geometry
2) A quality assurance test setup
   a) Time Domain Reflectometer Method
   b) FPGA implementation and features
   c) Preliminary test
   d) Characterization: DNL and INL by SCM
3) Test results on KLOE2 IT anode
4) Conclusions

KLOE-2 Inner Tracker up-grade

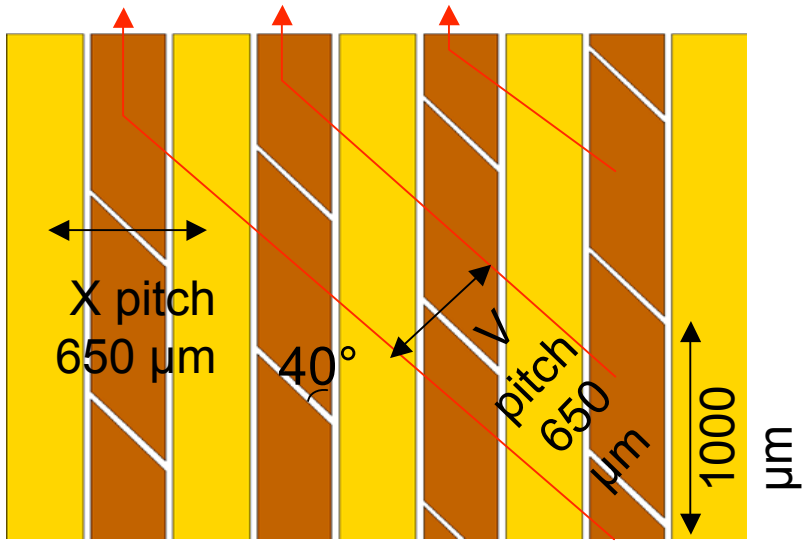
- 4 independent tracking layers for a fine vertex reconstruction of K_S and η
- 200 μm $\sigma_{r\phi}$ and 500 μm σ_z spatial resolutions with XV readout
- 700 mm active length
- from 130 to 220 mm radii
- 1.8% X_0 total radiation length in the active region
- Realized with **Cylindrical-GEM** detectors



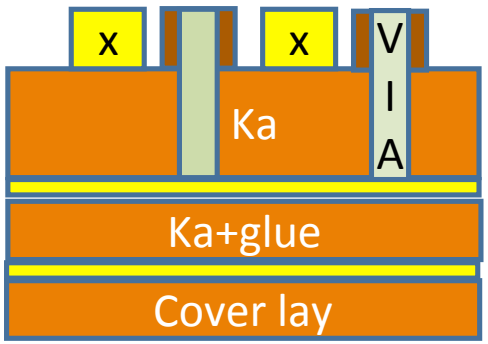


Anodic sheet for KLOE-2 I.T.

- Distinguishing **XV readout** designed for the cylindrical geometry
- X Strips on a layer for *r-φ* coordinate
- V Strips at 40° formed by Pads connected by internal vias (~220.000 VIAs!)
- Crossing of X and V gives Z coordinate

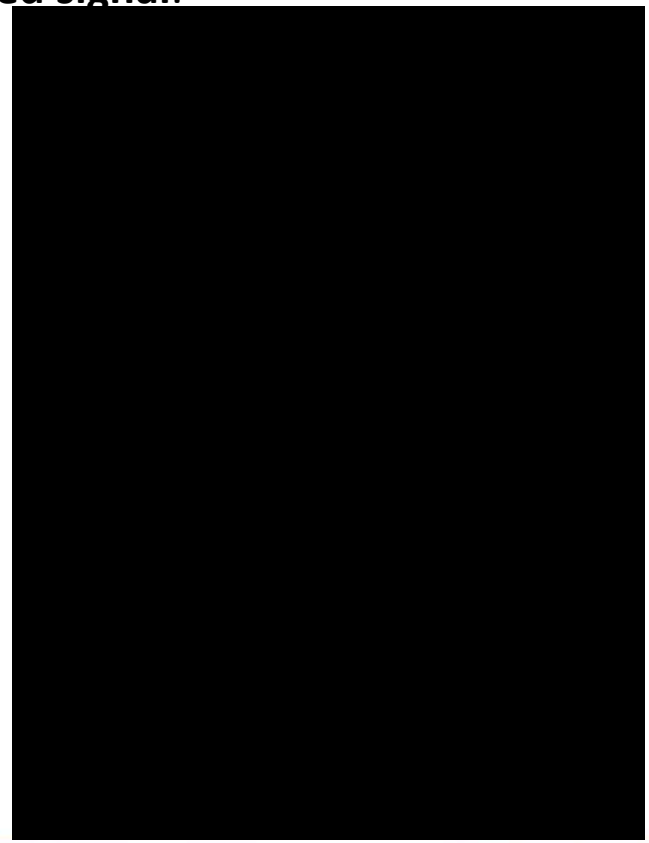


Schematic of XV strips-pads geometry top-view (above) and cross-section (below). On the left a picture of the anode plane.
Manufactured by EST-DEM CERN



Signal reflection on transmission lines

Reflectometer methods and test devices are commonly used since signal cable: the **length** of the transmission line and hence a possible damage in it is evaluated by measuring the **delay** of **reflected signal**.



Above:
scheme of connections for a Reflectometer setup

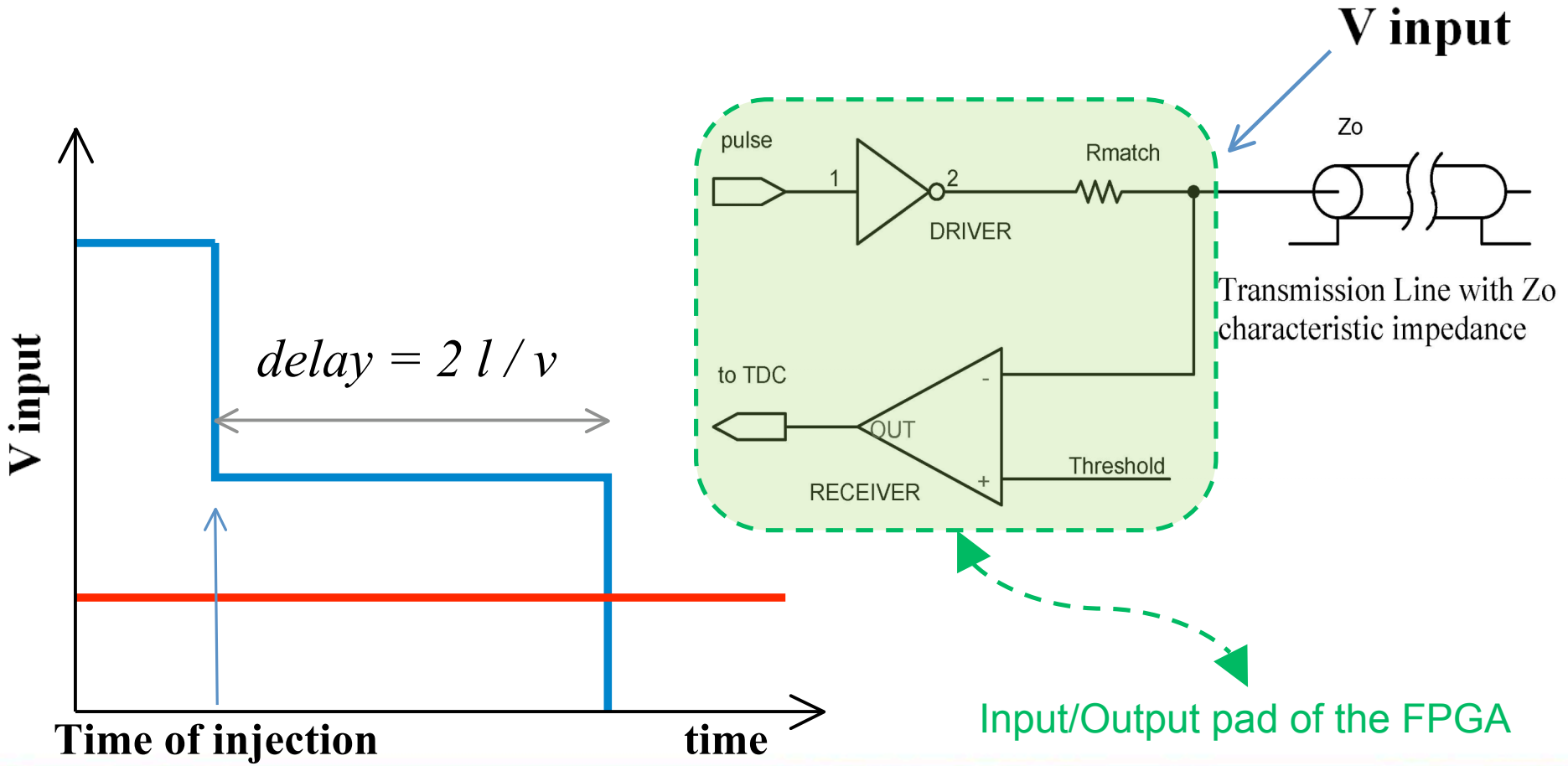
On the right:
reflections produced by resistive terminations Z_L at one end of a transmission line;
Z_0 is the characteristic impedance of the line.

Pics from HEWLETT-PACKARD Application Note 62 (1964).

TDR test exploits time measure -> TDC

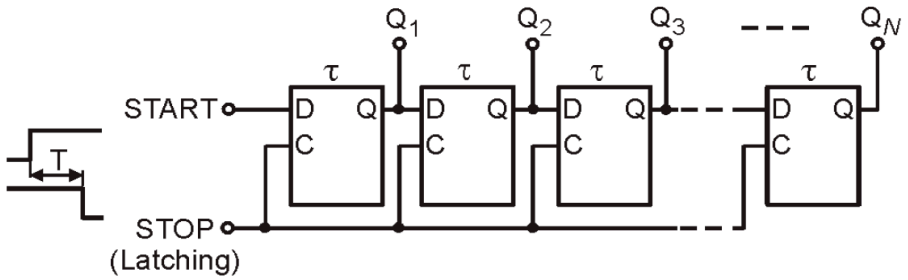
The drawing shows the foreseen run of a signal, in this case a transition from high to low state, injected into an un-terminated transmission line.

The first edge occurs when the signal is injected at the input while the second edge is observed after that the signal reflected comes back (in red a threshold level) .



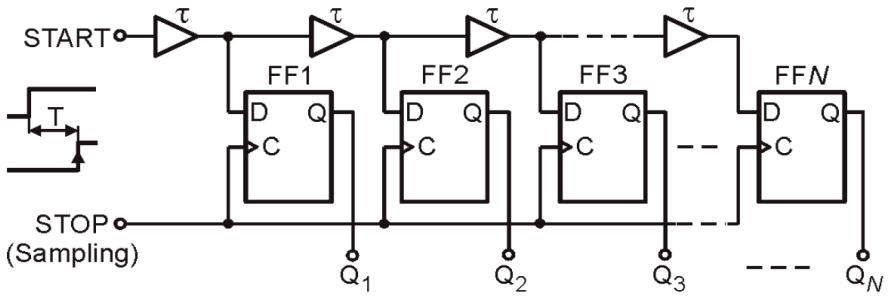
TDC by Tapped Delay Lines

Few examples of TDC by delay lines in ASIC:



HP5371A
Stephenson, 1989

➡ Resolution 200 ps

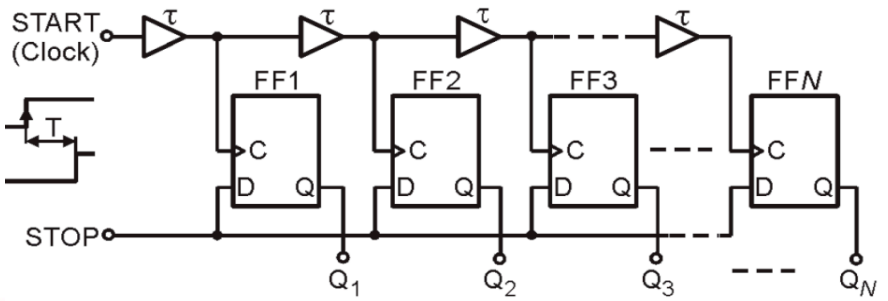


0.8 µm CMOS
Gorbics et al., 1997

➡ Resolution 46.9 ps

0.25 µm CMOS
Mota et al., 2000

➡ Resolution 24.4 ps



0.6 µm CMOS
Mantyniemi et al., 2002

➡ Resolution 29.6 ps

0.35 µm CMOS
Jansson et al., 2006

➡ Resolution 12.5 ps

Left schematics from J.Kalitz in Metrologia 41 (2004) 17–32
"Review of methods for time interval measurements with picosecond resolution"

TDC implemented in a Spartan3 FPGA CLB as delay unit

We have designed a test board to check the strips integrity by measuring the timing of reflected signals. We have implemented the digital time conversion in a FPGA (clock250MHz) by using the single CLB as delay element and register.

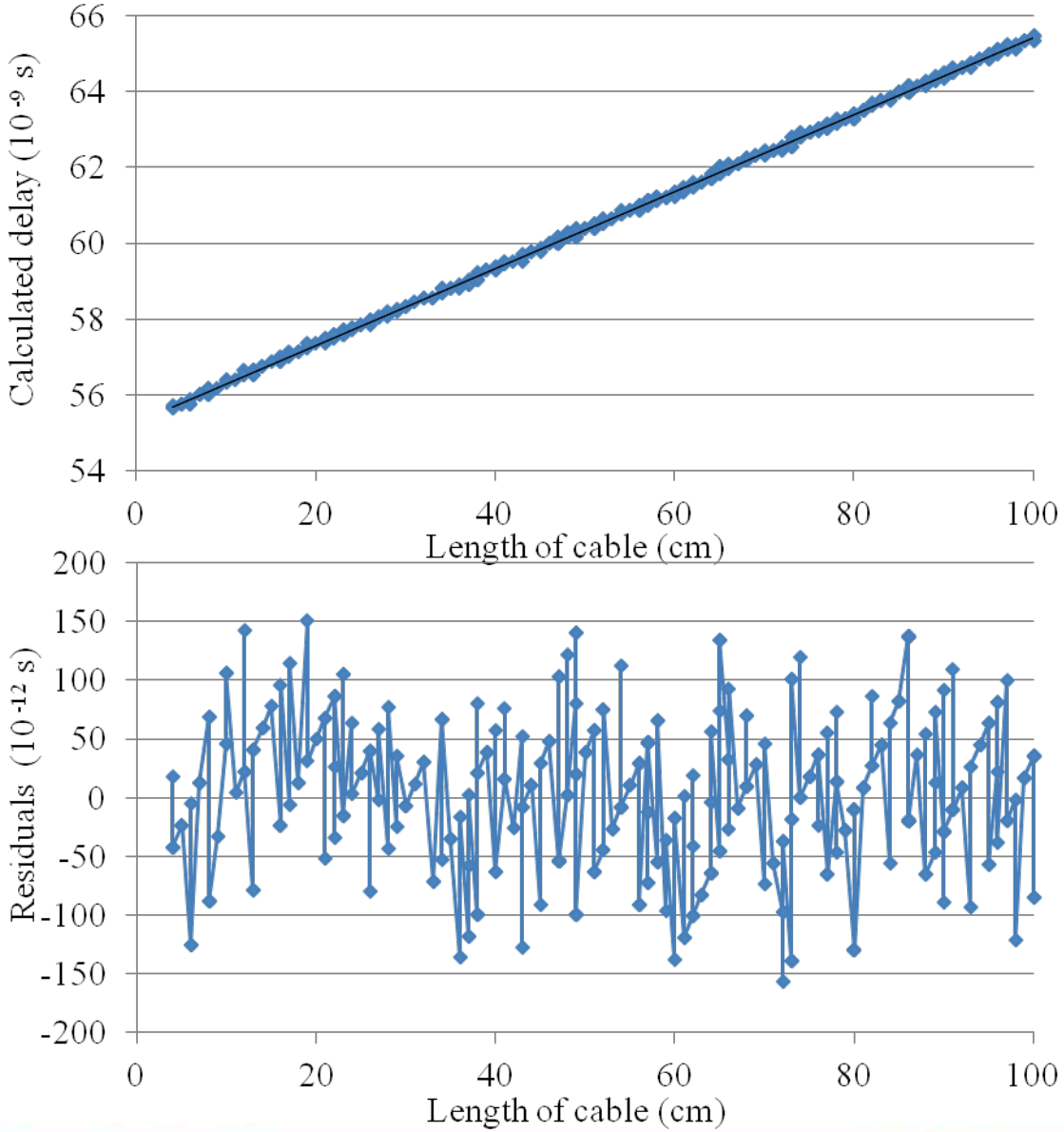
Moreover all encoding and control logic have been implemented in the same FPGA :

- A course counter with 4 ns resolution
- Fine counter by delay lines with time resolution ~100 ps

Circuit implementation based on a single FPGA (Xilinx_XC3s400):

- Simple and robust
- Off-the-shelf component
- Cost-effective

TDR prototype: a qualitative trial on a coaxial cable



A preparatory test has been performed on a coaxial cable (LEMO type C-50-2-1) cut onwards in steps of roughly 1 cm

Calculated Delay (ns) => y

Length of cable (cm) => x

$y = 0{,}102\,x + 55$

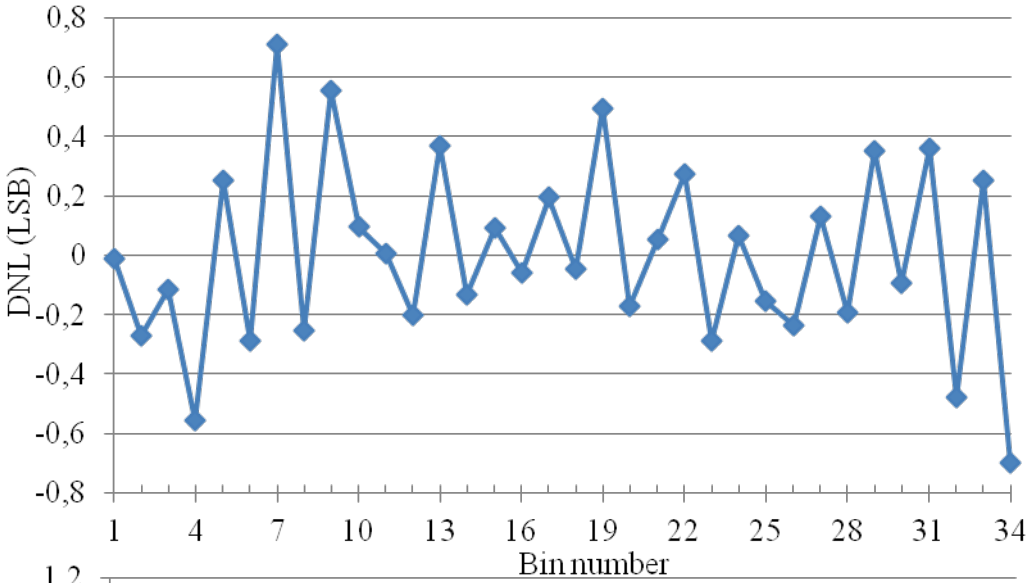
$r^2 = 0{,}9994$

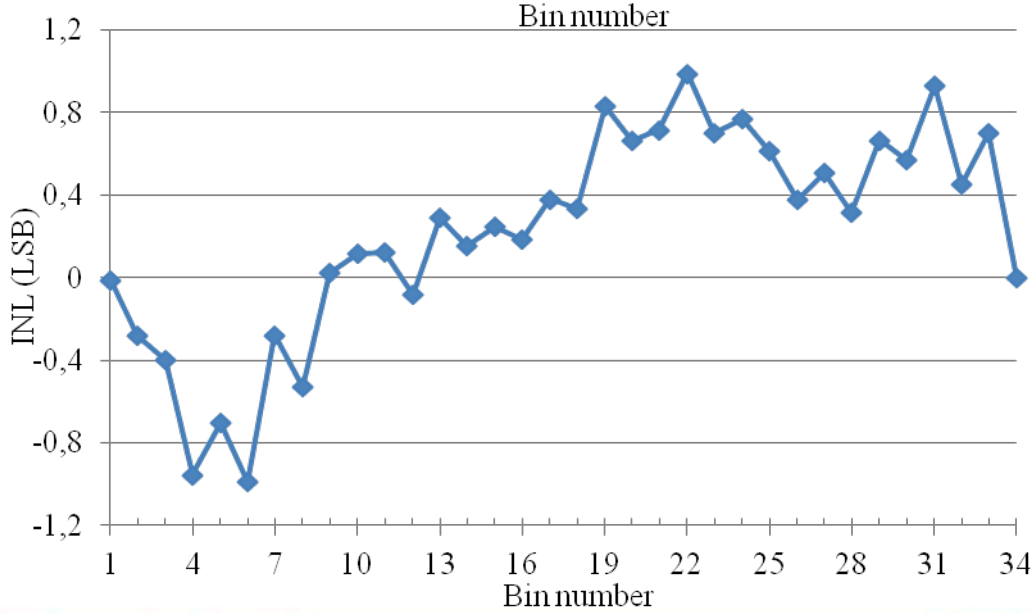
Max residual = 157 ps

RMSD = 64 ps

root-mean-square deviation
or rms of residual

TDC delay line characterization: DNL and INL by SCM





Statistical Code Method

J.Kalitz in Metrologia (2004) above-cited and various Appl. Notes by Maxim, Analog Devices.

$$DNL_i = (n_i - n_{th}) / n_{th}$$

$$INL_i = \Sigma\, DNL_i / M$$

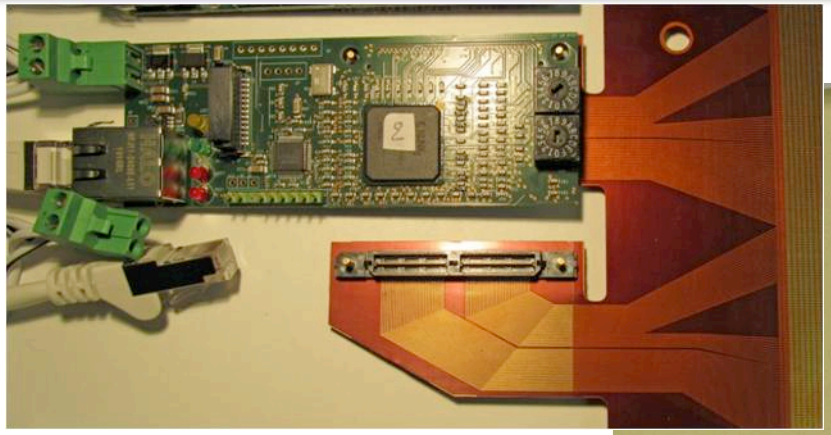
N_{tot} is the total amount of events collected;
M is the number of bins;
n_{th} is the expected number of events per bin (ideally would be equal to N_{tot} / M);
n_i is the amount of collected events per bin.

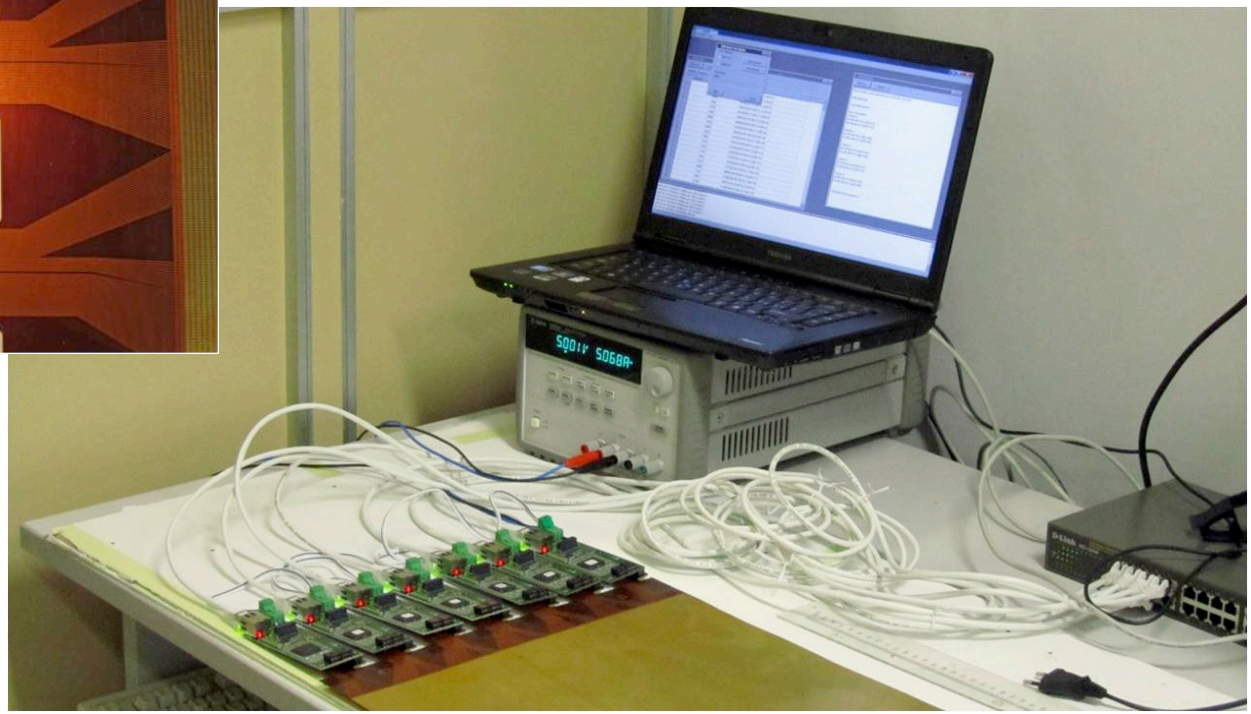
1. Data with radiative source ^{90}Sr
2. Coincidences by two Scintillators
3. DNL and INL calculated by SCM
4. DNL and INL within 1 LSB

Note 1: results validated by other sources (external pulse generator and cosmic rays).

Note 2: results from raw data without processing.

TDR: a test setup for IT Anode





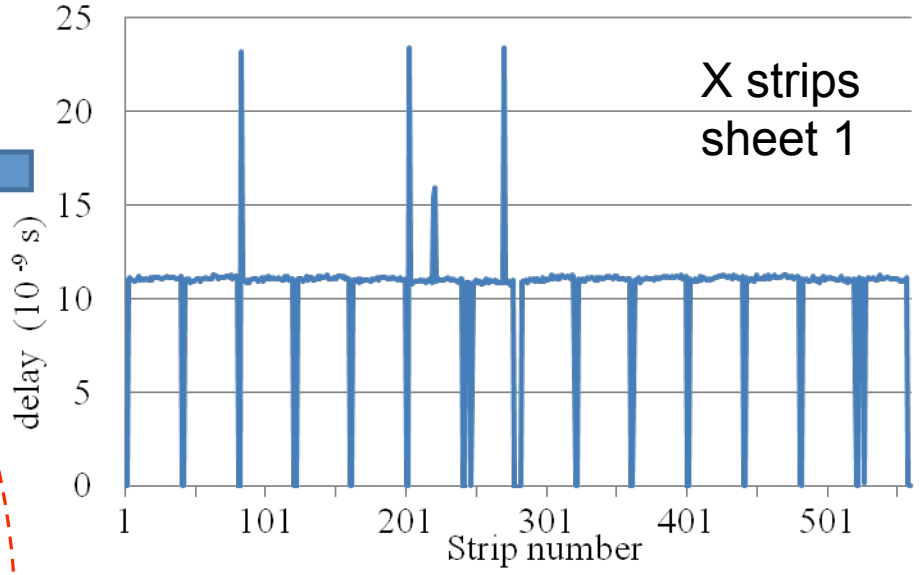
Main features:

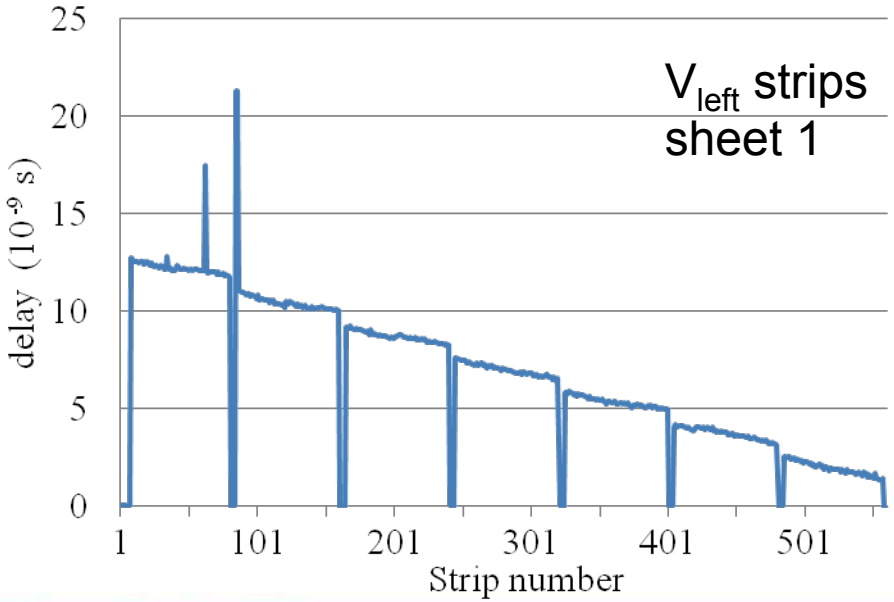
1. **Compact** + **Cost-effective**.
2. Software for **Test** quick and **automatic**.
3. Interface with an external PC by RS232 and/or **Ethernet**.
4. **One board** can check up to 120 chs (**one plug**).
5. Several boards can be fitted together in order to test an huge number of channels **Modularity**.
6. Easy programming/debugging/upgrading the device via Firmware **Versatile**.

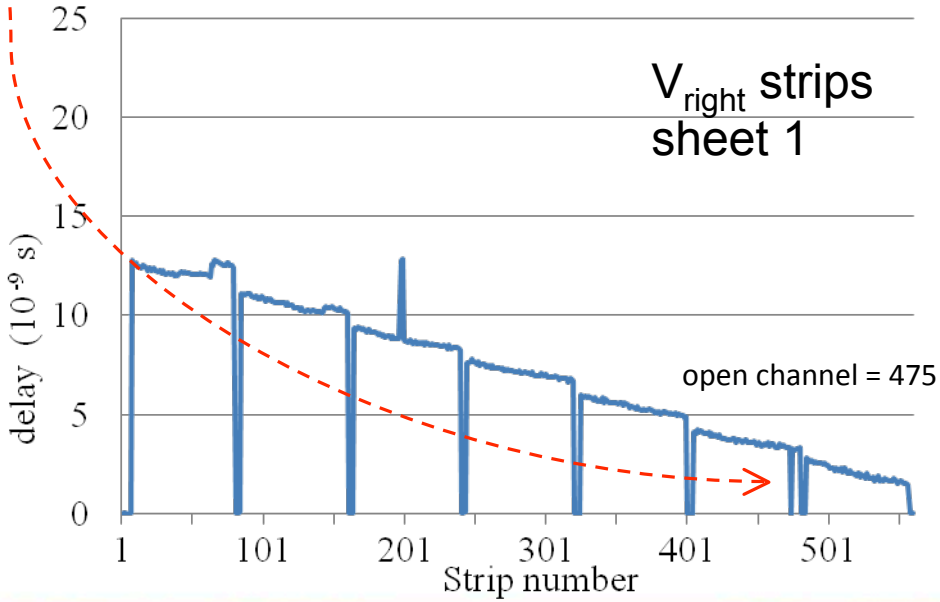
First case of study: KLOE-2 IT Layer 2 anodic sheets

Sheet num.	Short clusters	Short chs	open X	open V_{left}	open V_{right}	open Tot
1	5	11	0	0	1	1
2	15	30	0	1	0	1
3	12	24	0	0	2	2
4	6	12	0	0	0	0

Summary of defects found on four samples of the readout anode plane for the Layer 2 of the cyl.GEM IT for KLOE-2.



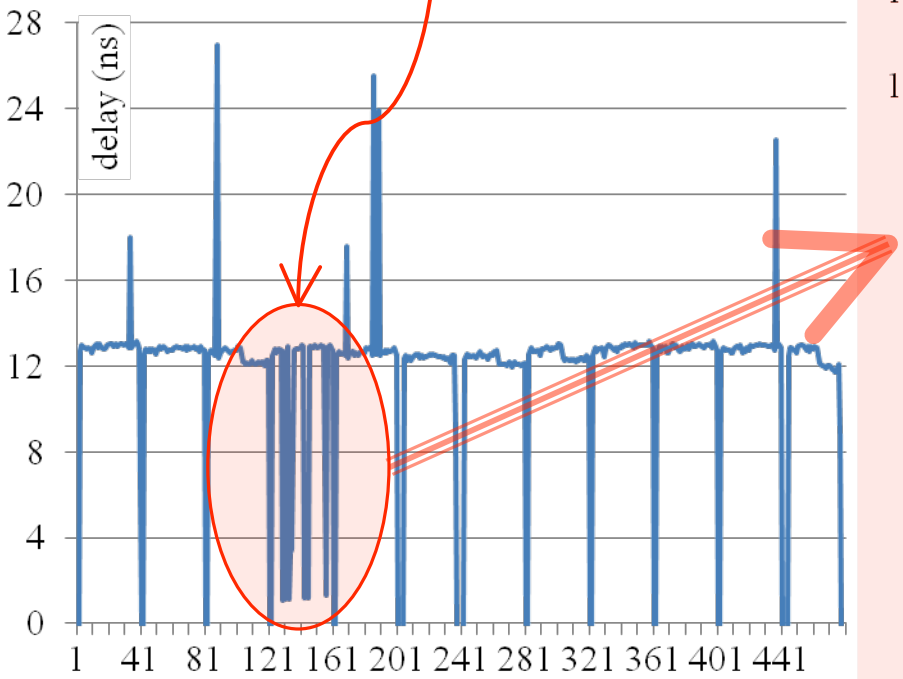




Second case of study: Sheet num.2 for Layer 1

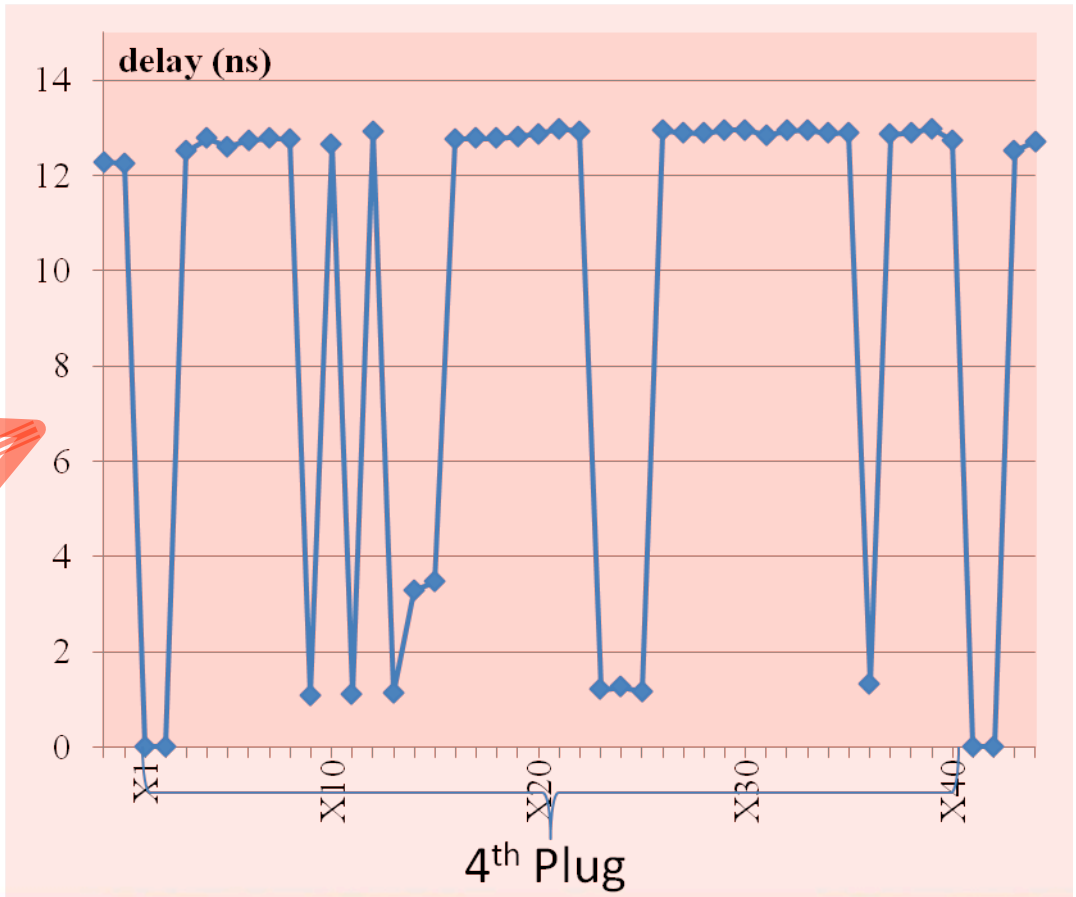
Defects found on a sample (named sheet 2) of the readout anode plane for the Layer 1

Sheet num.	Short clusters	Short chs	open X	open V_{left}	open V_{right}	open Tot
2	7	14	9	0	0	9



Below on the left the plot of calculated delay for the X strips of Layer 1 - Sheet2

Below on the right the detail of the 4th plug (test board n.3)



Summary of channels tested

On the right:
proofs of an article about this subject **in press** on NIMA

Below :
an overview of flaws found on the anodic sheets of first two layers.

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Nuclear Instruments and Methods in Physics Research A ▮ (▮▮▮▮) ▮▮▮–▮▮▮

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A Time Domain Reflectometer with 100 ps precision implemented in a cost-effective FPGA for the test of the KLOE-2 Inner Tracker readout anodes

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ABSTRACT

A Time Domain Reflectometer implemented in a single cost-effective Field Programmable Gate Array device is shown to achieve a precision around 100 ps. The Time to Digital Converter section of the device is based on a tapped delay line followed by an encoder and shows both Differential and Integral Non-Linearity below one least significant bit. The same Field Programmable Gate Array houses an 8051 8-bits microprocessor, for the control of the pulse signals generation, the acquisition and the first treatment of raw data. Principles of operation, architecture, performance and preliminary trials on the prototype are presented in this paper. As an example of possible application, the proposed circuit has been usefully used to perform the quality control of the micro-strip anodic planes of the Gas Electron Multiplier Inner Tracker of the KLOE-2 experiment.

Layer	n. plugs	Chs per plug	Tot chs per sheet	Tot chs tested in 4 sheets	Short chs	Open chs	Bad chs	percent
2	14	≈ 120	14x120=1680	1680x4=6720	77	4	81	1.2 %
1	12	≈ 120	12x120=1440	1440x4=5760	36	9	45	0.8 %

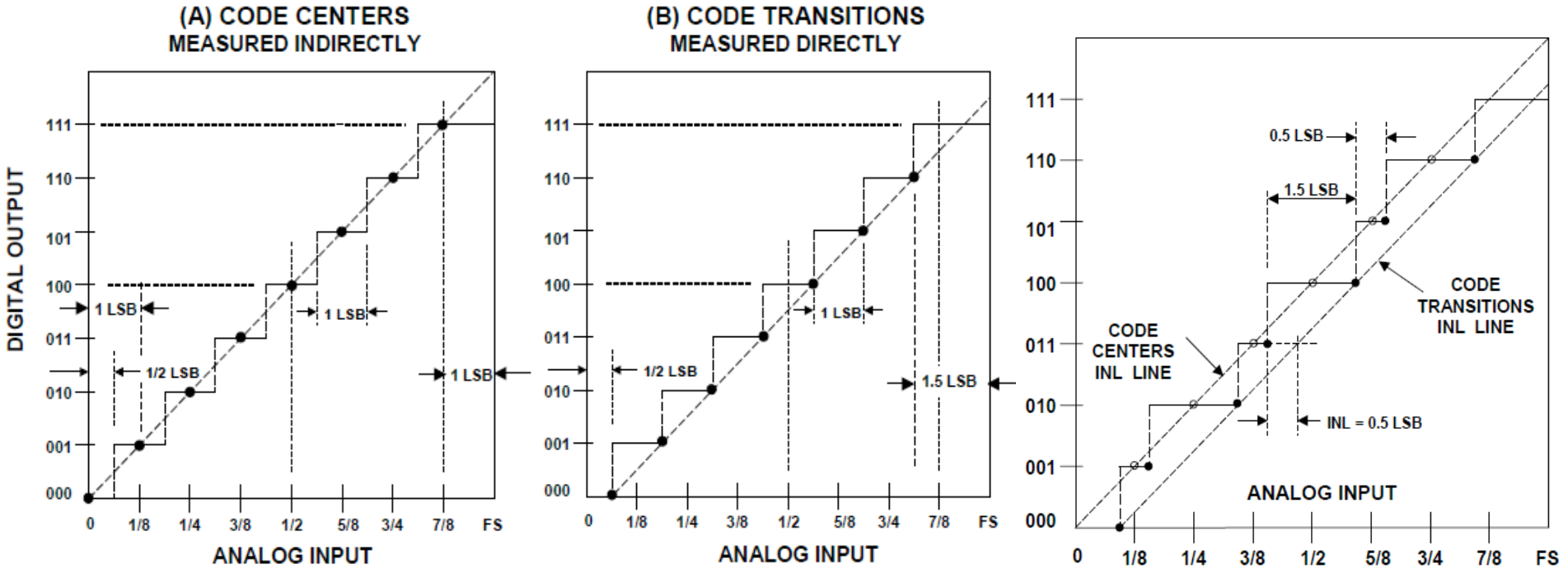
Conclusions

1. A very reliable quality assurance system for the readout plane of MPGD has been developed.
2. Test system outlines:
   a) Time Domain Reflectometer Method
   b) Easy implemented in basic FPGA (stock availability, cost-effective)
   c) Software for analysis, data log via Ethernet and Auto-calibration
   d) Modular technology (easy-fitting to different readout geometries)
   e) Resolution 100 ± 62 ps (without calibration and processing, roughly 1 cm coax cable)
   f) DNL and INL within 1 LSB
3. Test on KLOE2 IT anode planes shows benefits of the device
4. A test setup available in Bari has been used to test the readout planes of I.T. detector in KLOE-2 apparatus.

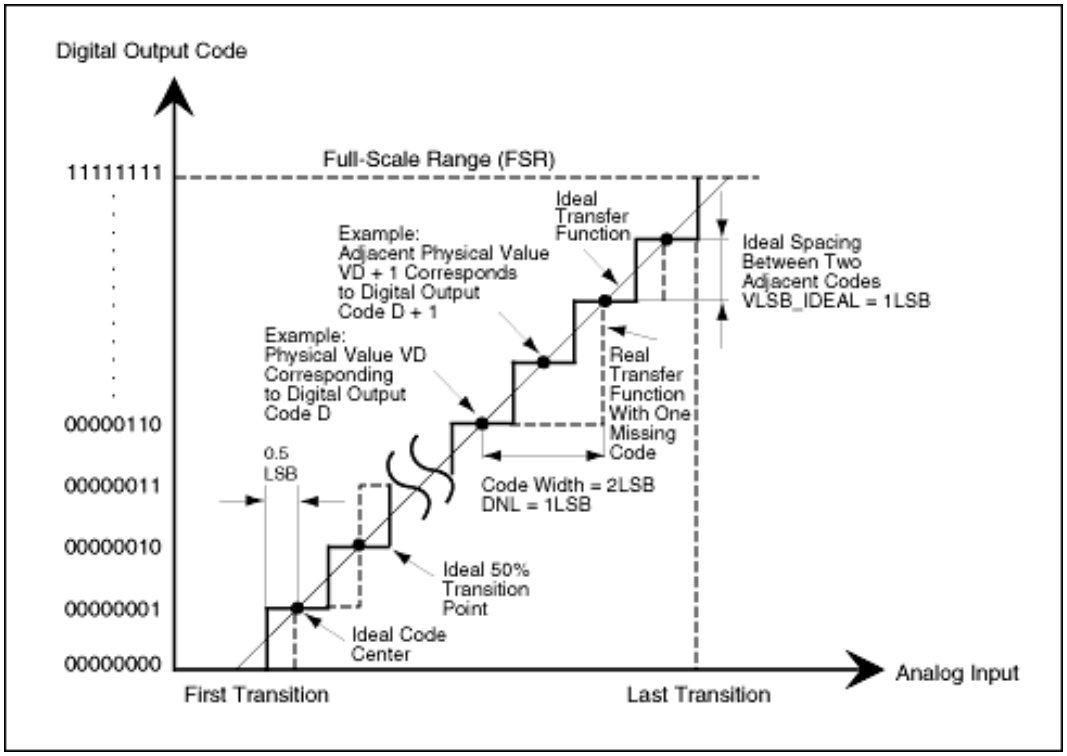
spares

Major issues of delay line in FPGA

- The effectively used logic cell block CLB may be physically placed anywhere in the FPGA chip, usually automatically by the development software. If we let do the software also the routing of the cells is unpredictable. Then propagation delay will not be uniform, resulting in non-linearity. We must control the placement and routing of logic CONSTRAINTS.
- Logic cell delays depend by temperature and power supply : Needs for calibration.
- Moreover every Analog to Digital Converter is affected by DNL and INL



DNL and INL in ADC: bin width



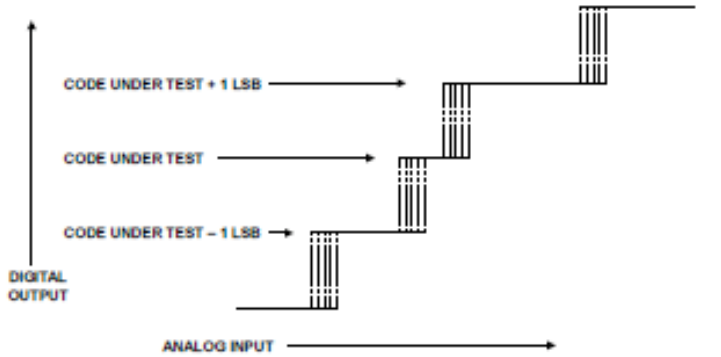
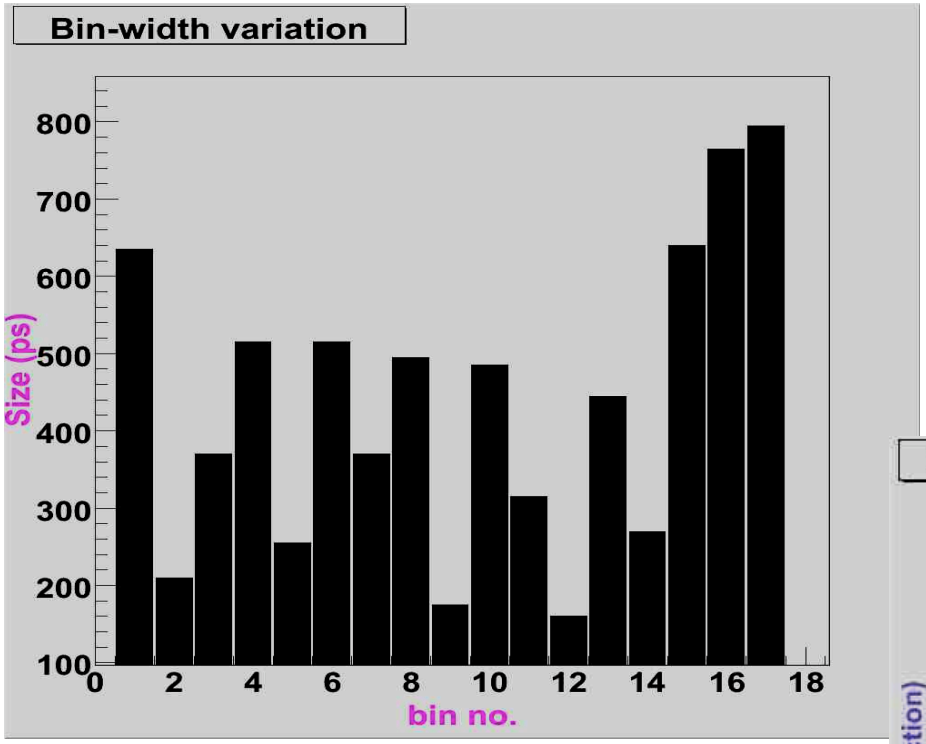


Figure 5.36: ADC Transfer Function With Relatively Low Input-Referred Noise

Figure 5.37: ADC Transfer Function With Relatively High Input-Referred Noise

- WALT KESTER ET AL. in: Walt Kester (Eds.), The Data Conversion Handbook, ADI Central Applications Department, Analog Devices Inc., (Mar. 2004) pp. 5.27-5.44
- Maxim Corporation, Histogram Testing Determines DNL and INL Errors App. Note 2085 (2003) available via http://www.maxim-ic.com/design/techdocs/app-notes/index.mvp
- Maxim Corporation, INL/DNL Measurements for High-Speed Analog-to-Digital Converters App. Note 283 (2001) available via http://www.maxim-ic.com/design/techdocs/app-notes/index.mvp
- S.Dasgupta at INO Coll.Meeting may2010. and J.Kalitz in Metrologia (2004) above-cited

DNL : deviation of actual step-width from the ideal width = 1 LSB.



DNL and INL direct measure and SCM

J.Kalitz in Metrologia (2004) and S.Dasgupta (2010) above-cited .

DNL = (actual step – ideal) / LSB width

$INL_i = \Sigma\ DNL_i / M$