DAQ TB 2012

Masks / Rates

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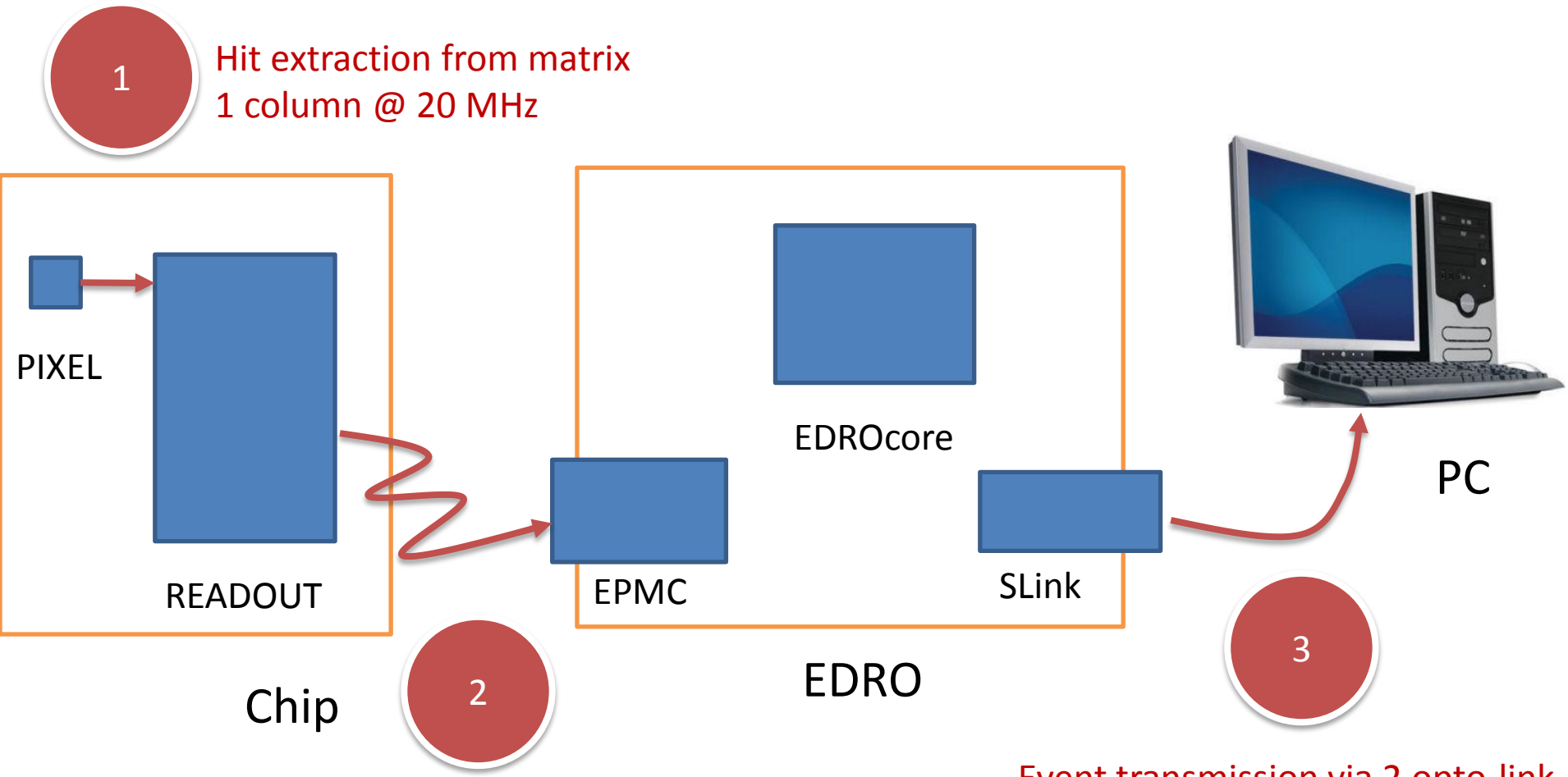
Outline

- Data Flow → crucial channels and bottlenecks
- Masks & Filters: effectiveness and details for:
  - Chip APSEL3D_TC / 4D
  - Chip SPX0
  - Chip INMAPS
- Set Masks on the DAQ system with SlimGui v. 2012

Data Flow – crucial channels & bottlenecks



Channel Saturation Effects

1. Pixels are read out with increasing delay → DEAD TIME

2. Hits cannot flow out of chip → HIT LOSS (SPX0, INMAPS)
   → DEAD TIME (APSEL3D_TC/4D)

3. Hits cannot flow out of EDRO → Back-Pressure
   → HIT LOSS

APSEL3D_TC /4D Mask

Relief on Channel

X

- MP masks (4x4 pixel)
  - Inhibit Latch_enable of MP
  - **3D_TC**: 16 bit
  - **4D**: 256 bit

1

- Row masks
  - **3D_TC**: 8 bit
  - **4D**: 32 bit

1

- DAQ Hit Filter
  - Choice of 20 pixels

3

SPX0 Mask

- MP masks (2x8 pixel)
  - Latch_enable always active
  - Inhibit fastOR
  - 256 bit

1

- DAQ hit filter
  - Choice of 20 pixels

3

INMAPS

Relief on Channel

X

- In-pixel masks
  - Inhibit Latch_enable
  - 4096 bit

1

- Peripheral masks
  - columns:
    - 32 bit
    - Inhibit col. latch_enable
  - rows :
    - 64 bit
    - (32 bit inhibit sparsifiers for SM0, 32 bit for SM1)
    - Latch enable always active

1

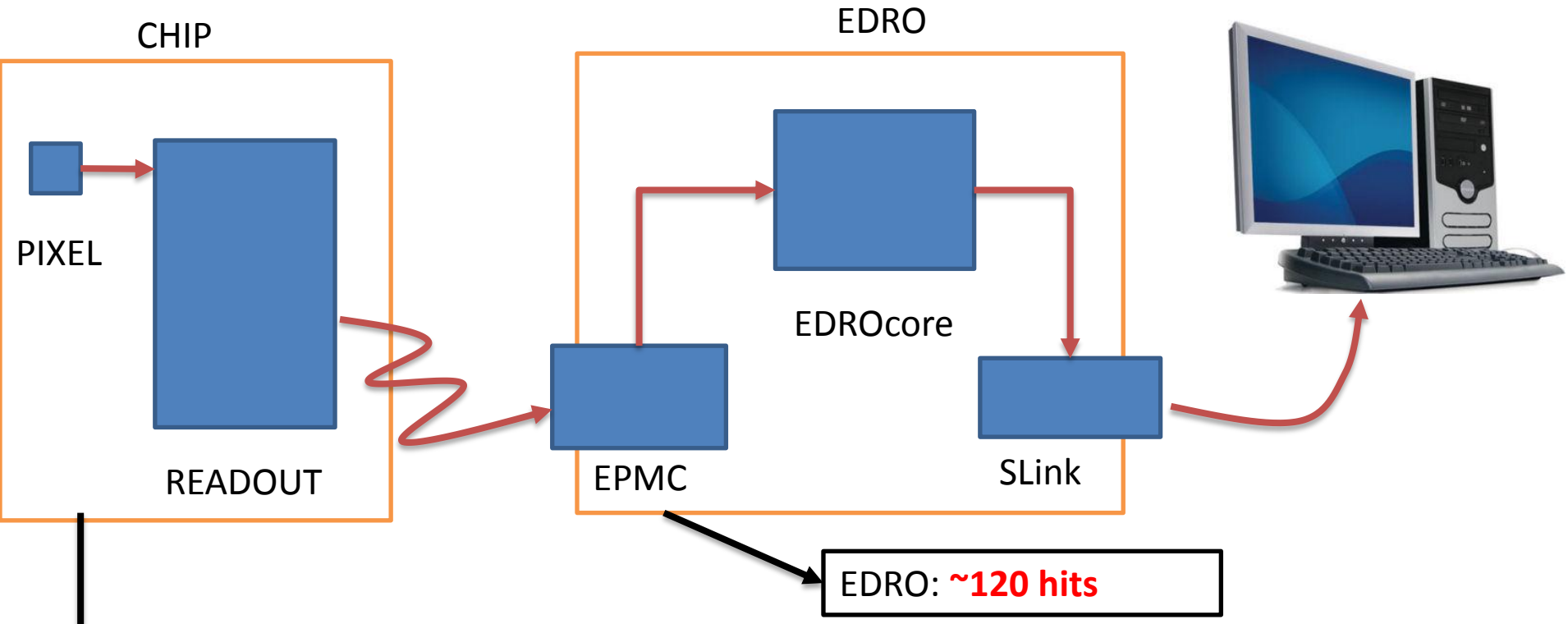
2

- DAQ hit filter
  - Choice of 20 pixels

3

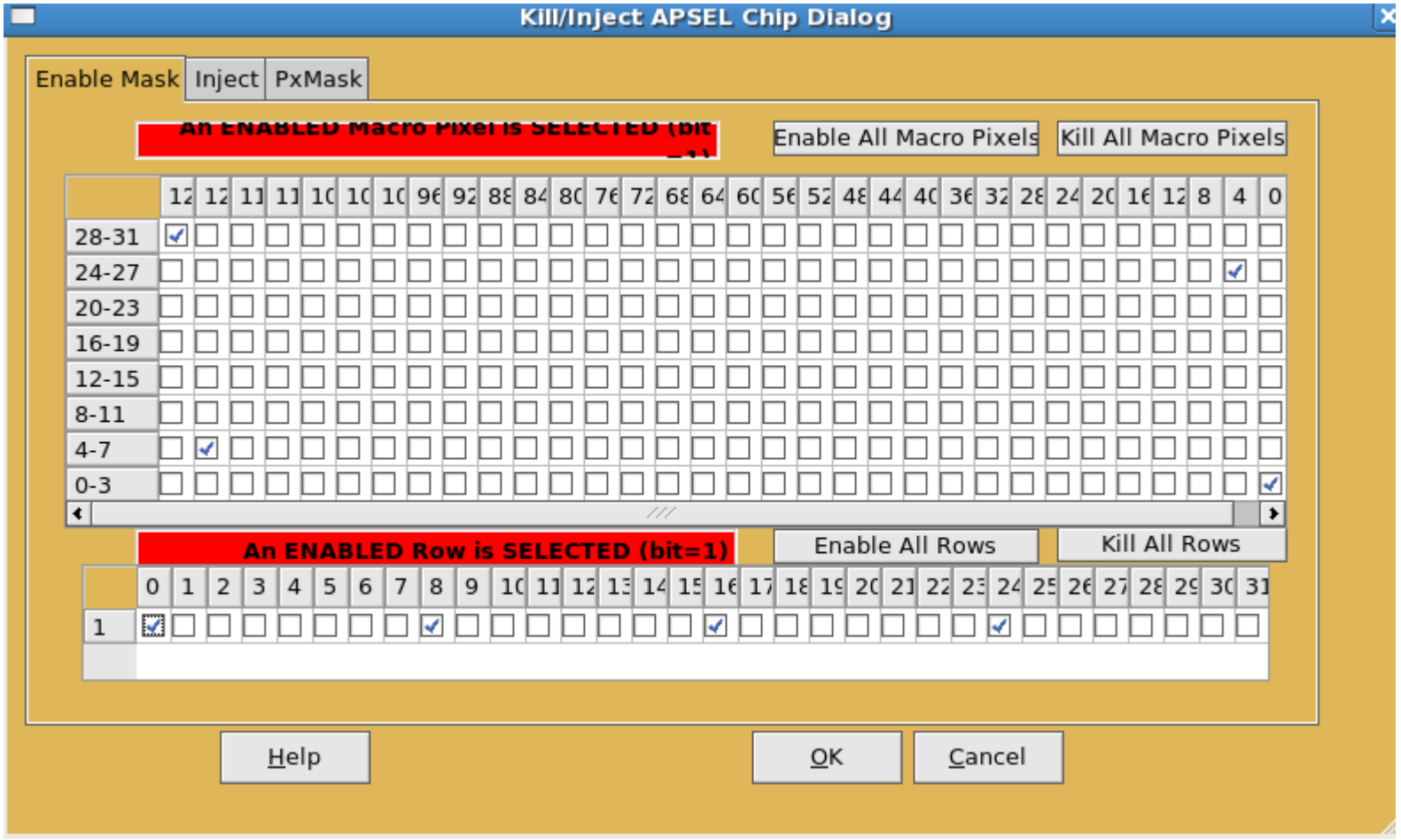
Events & Max Event Size

#define Event : array of hits with same TS

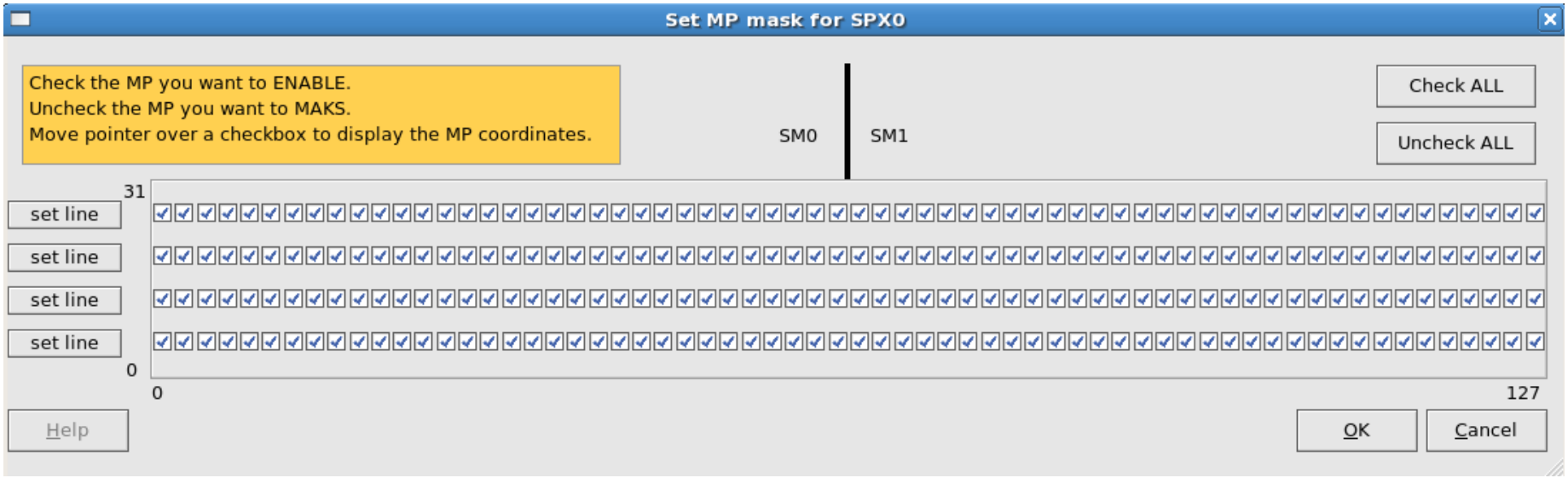


CHIP
Apsel3D_TC/4D : **no hit limits** (readout sweep wait with barrel back-pressure)→dead time
SPX0 : **hits** < 16 to be sure (8 B2 da **8** hit, 2 B1 da 64 hit)
INMAPS : **hits** < 128 (2 B1 da 64 hit)

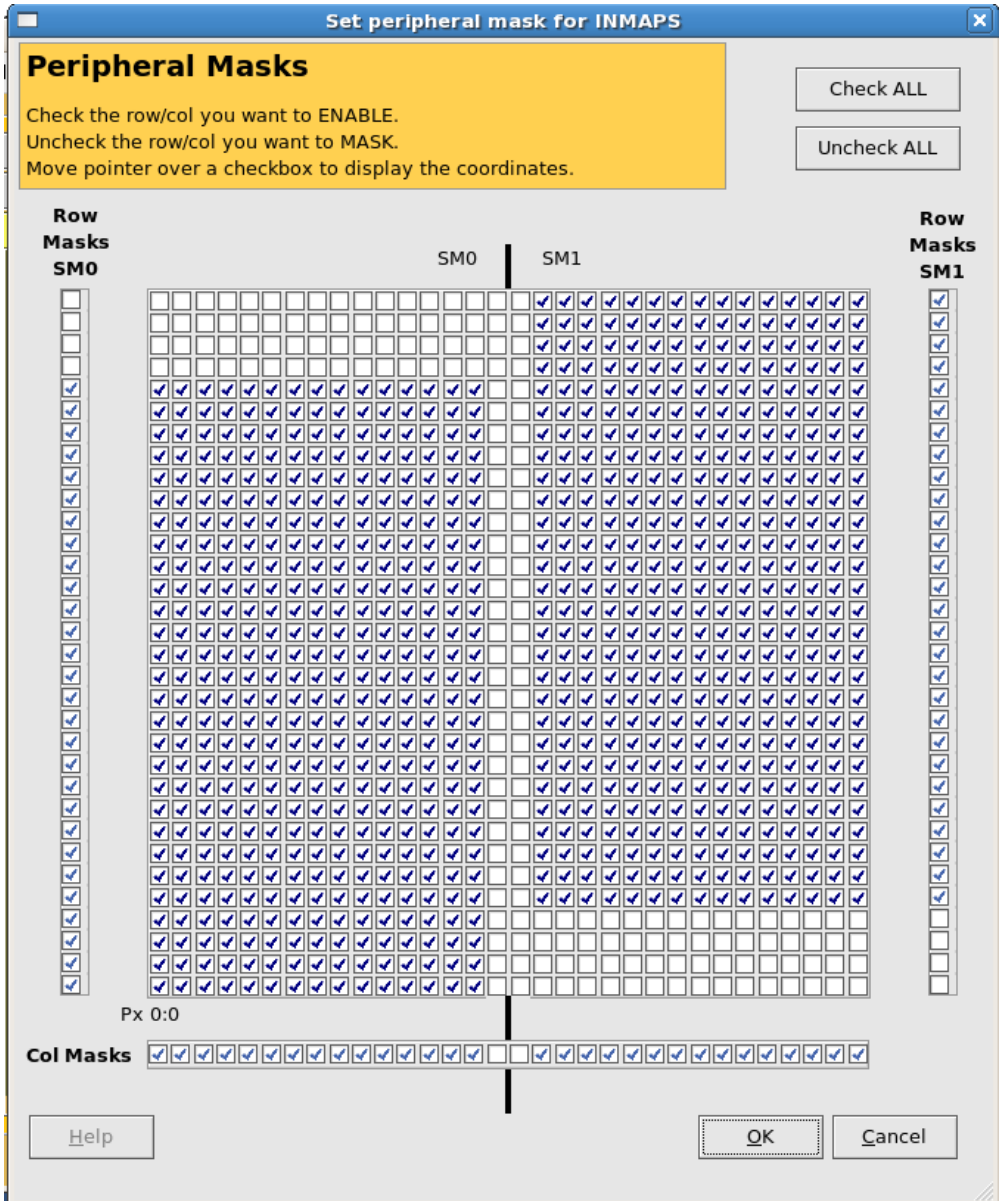
APSEL4D MP mask GUI



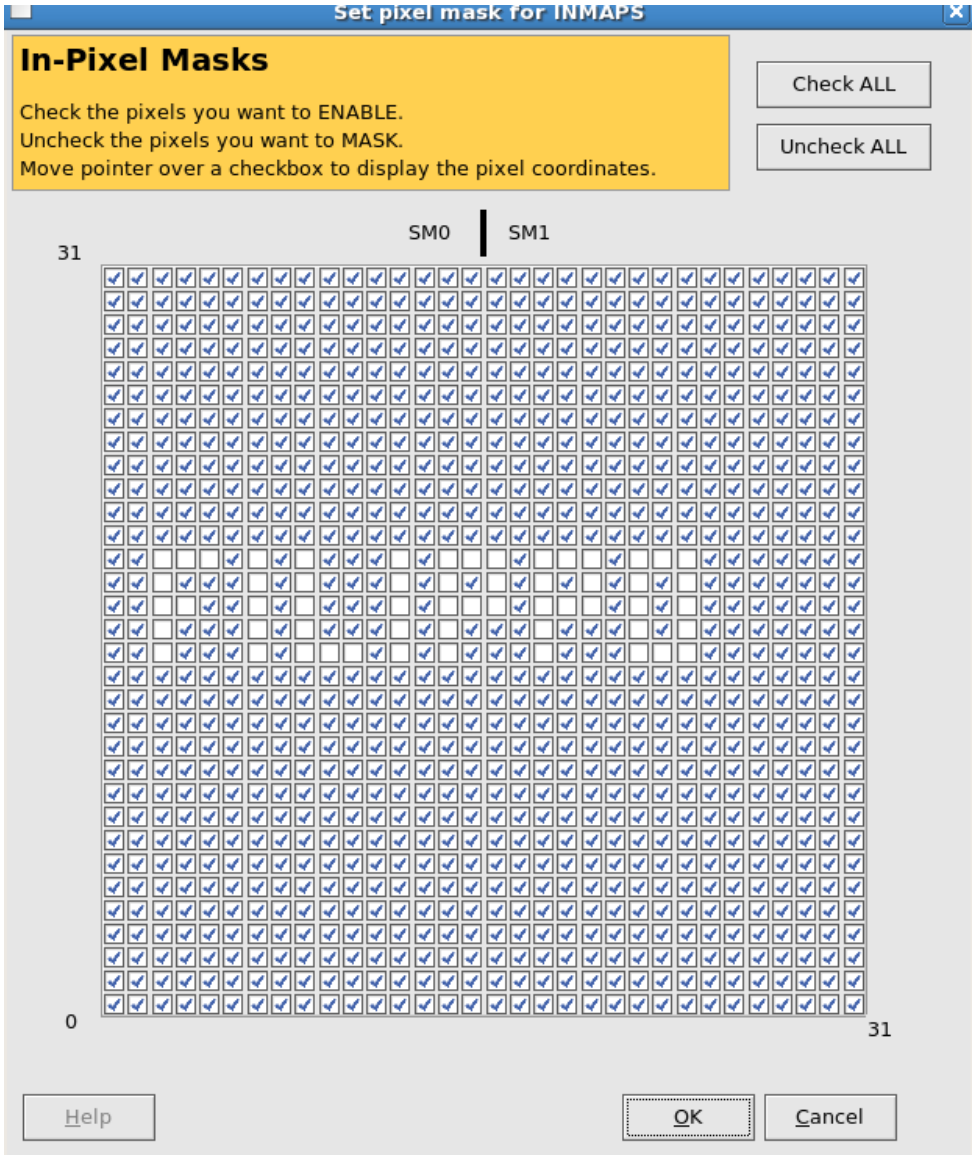
SPX0 Mask GUI



INMAPS Peripheral mask GUI



INMAPS In-pixel Mask GUI



Hit Filter on EPMC card