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Super*B* Detector Technical Design Report

Abstract

This report describes the technical design detector for Super$B$.

Contents

6 Silicon Vertex Tracker

6.1 Overview

The Silicon Vertex Tracker, as in *BABAR*, together with the drift chamber (DCH) and the solenoidal magnet provide track and vertex reconstruction capability for the Super$B$ detector. Precise vertex information, primarily extracted from precise position measurements near the IP by the SVT, is crucial to the measurement of time-dependent CP asymmetries in B^0 decays, which remain a key element of the Super$B$ physics program. In addition, charged particles with transverse momenta lower than 100 MeV/c will not reach the central tracking chamber, so for these particles the SVT must provide the complete tracking information.

6.1.1 SVT and Layer0

The above goals have been reached in the *BABAR* detector with a five-layer silicon strip detector with a low mass design, shown schematically in Fig. 6.1. The *BABAR* SVT provided excellent performance for the whole life of the experiment, thanks to a robust design that took into account the physics requirements as well as enough safety margin, to cope with the machine background, and redundancy considerations [2].

The Super$B$ SVT design, shown schematically in Fig. 6.2, is based on the *BABAR* vertex detector layout with those modifications needed to operate at a luminosity of 10^{36} or more, and with a reduced center-of-mass boost. In particular the SVT will be equipped with an innermost layer closer to the IP (Layer0) to improve vertex resolution and compensate the reduced boost at the Super$B$ accelerator, thus retaining an adequte Δt resolution for B decays for time-dependent CP asymmetries.

Physics studies and background conditions, as explained in detail in the next sections, set stringent requirements on the Layer0 design: radius of about 1.5 cm; resolution of 10-15 μm in both coordinates; low material budget (about 1% X_0); and adequate radiation resistance.

Several options are under study for the Layer0 technology, with different levels of maturity, expected performance and safety margin against background conditions. These include striplets modules based on high resistivity double-sided silicon detector with short strips (tilted with respect to detector's edge), hybrid pixels and other thin pixel sensors based on CMOS Monolithic Active Pixel Sensor (MAPS).

The current baseline configuration of the SVT Layer0 is based on the striplets technology, which has been shown to provide the better physics performance, as detailed in the next sections. However, options based on pixel sensors, which are more robust in high background conditions, are still being developed with specific R&D programs in order to meet the Layer0 requirements, which include low pitch and material budget, high readout speed and radiation hardness. If successful, this will allow the replacement of the Layer0 striplets modules in a "second phase" of the experiment. For this purpose the Super$B$ interaction region and the SVT mechanics will be designed to ensure a relative rapid access to the detector for a replacement of Layer0.

The external SVT layers (1-5), with a radius between 3 and 15 cm, will be built with the same technology used for the *BABAR* SVT (double sided silicon strip sensor), which is adequate for the machine background conditions expected in the Super$B$ accelerator scheme (*i.e.*with low beam currents). Although SVT module design for layer1 to 5 will be very similar to the *BABAR* one, with a larger coverage, a complete new readout electronics chain need to be developed

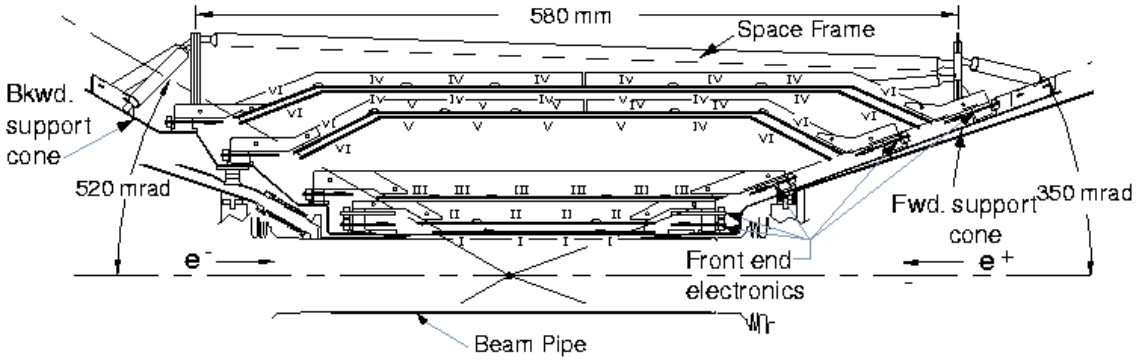

Figure 6.1: Longitudinal section of the *BABAR* SVT

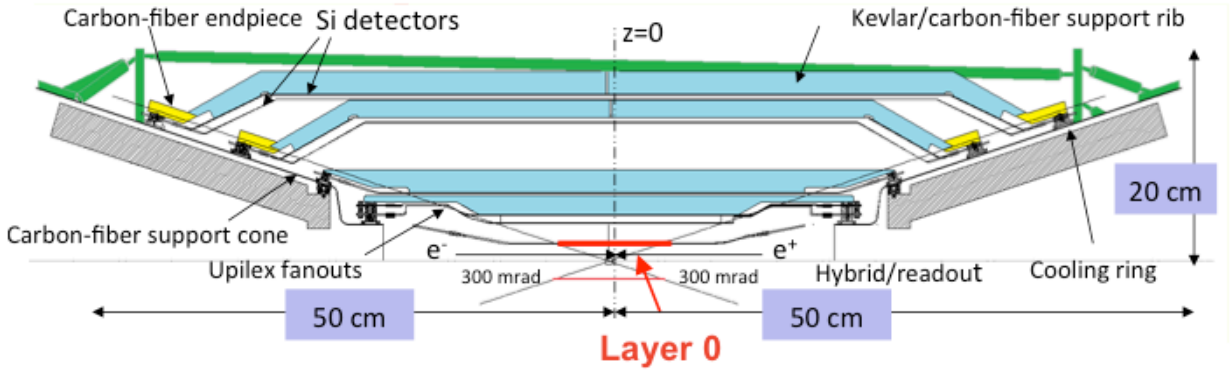

Figure 6.2: Longitudinal section of the Super*B* SVT

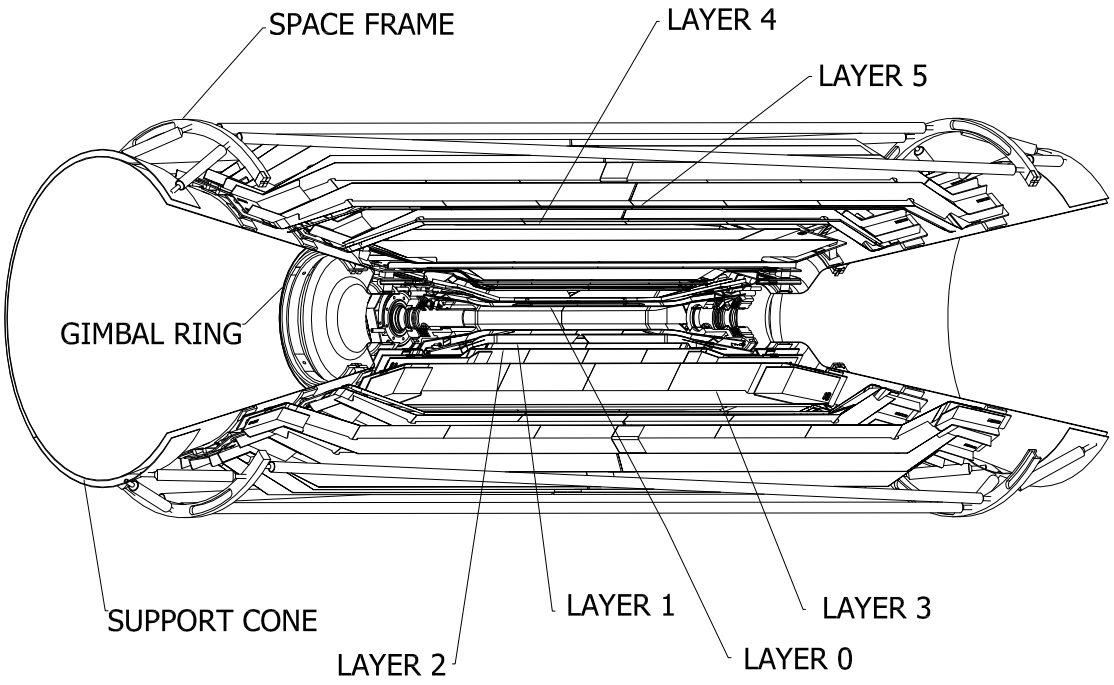

Figure 6.3: Three dimensional cutaway of the SVT.

to cope with the higher background rates expected in Super$B$.

A review of the main SVT requirements will be given in the next section followed by an overview of the general detector layout. A detailed discussion of all the specific design aspects will be covered in the rest of the chapter.

6.1.2 SVT Requirements

6.1.2.1 Resolution

Without the measurement of the B decay vertex, no useful CP asymmetries can be extracted at the $\Upsilon(4S)$. Therefore one of the main goal of the SVT is the determination of the B decay positions, especially along the beam direction (z). Measurements performed in *BABAR*, where the mean separation between B vertices is $\Delta z \simeq \beta\gamma c\tau_B = 250\,\mu$m, demonstrated that good sensitivity to time dependent measurement can be achieved with typical vertex resolution of 50-80 μm in the z coordinate for exclusively reconstructed modes, and 100-150 μm for inclusively modes (tag side in CPV measurements). The reduced Super$B$ boost ($\beta\gamma = 0.24$) with respect to PEP-II ($\beta\gamma = 0.55$) requires an improved vertex resolution, by about a factor 2, in order to mantain a suitable Δt resolution for time dependent analyses.

The *BABAR* resolution was achieved thanks to an intrinsic detector resolution of about 10-15 μm in the first measured point of the SVT, taken at a radius of about 3 cm, and keeping to the minimum the amount of material between the IP and the first measurement. The multiple scattering has in fact an important effect on impact parameter resolution for low momentum tracks and set a lower limit on the useful intrisic resolution on the various SVT layers, corresponding to a point resolution of about 10-15 μm for measurements made close to the IP and 30-40 μm for the outer layers [1].

The required improved track impact parameter and vertex resolution can be reached in Super$B$ with the same intrisic resolution used in

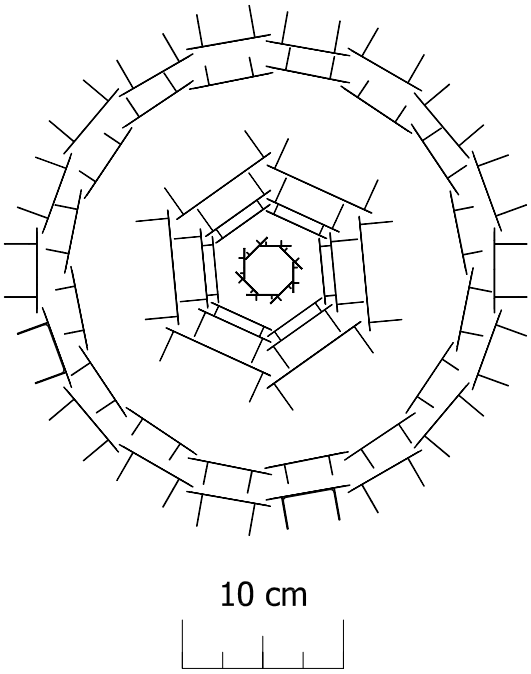

Figure 6.4: Cross section of the SVT in the plane perpendicular to the beam axis. The lines perpendicular to the detectors represent structural support beams.

BABAR, reducing the radius of the first measured SVT point by a factor of 2 (Layer0 radius at about 1.5 cm) and keeping a very low mass design for the beam pipe and the detector itself.

6.1.2.2 Acceptance

The coverage of the SVT must be as complete as technically feasible, given the constraints of the machine components close to the IP. The SVT angular acceptance, constrained by the Super$B$ interaction region design, will be 300 mrad in both the forward and backward directions, corresponding to a solid angle coverage of 95% in the $\Upsilon(4S)$ center-of-mass frame, thus increasing the acceptance with respect to *BABAR* SVT.

There should be as little material as possible within the active tracking volume. The minimization of the material between the IP and the first measurement is crucial to reduce the multiple scattering and preserve the impact parameter resolution. The small beam pipe (1 cm radius) in the dector acceptance requires an active cooling with liquid coolant to evacuate the large power dissipated from image beam currents. The total amount of radial material for the actual design of this new beryllium pipe is estimated to be less than 0.5% X_0. Material located beyond the inner layers does not significantly degrade the measurement of track impact parameters, but does affect the performance of the overall tracking system and leads to increased photon conversions in the active region.

6.1.2.3 Efficiency

Our goal is to achieve close-to-perfect track reconstruction efficiency within the active volume of the tracking detectors when information from both the drift chamber and the SVT is used. The pattern recognition capabilities of the combined tracking system must be robust enough to tolerate background levels up to 5 times nominal. *as defined in background section* Low momentum particles that do not traverse many drift chamber planes, such as many of the charged pions from D^* decays, must be reconstructed in the SVT alone. For this category of tracks, with p_T less than 100 MeV/c, we want to achieve reconstruction efficiencies of at least 80–90%. *check these number with fastsim results in high background* The SVT must also be efficient for particles such as K^0_Ss that decay within the active volume.

Together, these requirements determine the number of measurements along a track and the necessary single-hit efficiency. *do we need to quote some numbers here?.* The *BABAR* SVT design with 5 layers was optimized to ensure enough redundancy to keep an high tracking efficiency even in case of failure of some modules and inefficient detectors. The robustness of this choice was demonstrated with the good detector performance over the entire life of the experiment. The Super$B$ SVT design with 6 layers (inserting the Layer0) is inspired to the same philosophy. Specific simulation studies [3] indicated that a reduction in the number of layers,

from 6 to 5 or 4, give very modest gain in tracking performance while show a sizeble reduction in the efficiency for low momentum tracks in D* reconstruction, in case of non perfect/real detector, or related to inefficiency in high background conditions.

6.1.2.4 Background & Radiation Tolerance

The expected background influences several aspects of the SVT design (segmentation, shaping time, data transmission rates) and sets the requirements for the radiation resistance of all the SVT components. The design of the system has been optimized to withstand at least 5 times the total expected background rates. Whenever possible, detectors and front-end electronics are specified to be able to survive the entire life of the experiment including a safety factor of 5 on the total dose and equivalent neutron fluence: 7.5×5 yrs at nominal peak luminosity of 10^{36}.

As described in Section 6.2, the effect of background depends steeply on radius, as shown in Tab. 6.1.

With the high strip rates expected, especially in the inner layers (0-3), the front-end electronics should be fast enough to avoid pulse overlap and consequent hit inefficiency (shaping time in the range 25-150 ns). Furthermore a good Time Stamp resolution (30 MHz TS clock) is needed to get a good hit time resolution and reduce the occupancy in the offline time window to acceptable levels for reconstruction. An average 2% offline cluster occupancy is reached in each layer, considering the nominal background x5, with offline time windows of 100-150 ns in layers 0-3, while about 500 ns will be selected in layers 4-5, where the longer shaping time is dominating the hit time resolution. See Sections 6.3.5 and 6.6.2 for more details.

In Layer0 the expected integrated dose is about 3 Mrad/yr and the equivalent neutron fluence is about 5×10^{12} n_{eq}/cm^2/yr in the sensor area. In the other SVT layers radiation levels are at least one order of magnitude lower: in Layer1 TID $\simeq$ 0.3 Mrad/yr and an equivalent neutron fluence of about 8×10^{11} n_{eq}/cm^2/yr are expected.

With this scenario in Layer1-5 the sensors are proven to be enough radiation hard to survive the entire life of the experiment, with a safety factor of 5 included, with an acceptable degradation of the Signal to Noise performance, as shown in Section 6.6.2. *review this sentence after proper evaluation of S/N.* As an example this requirement translates for Layer1 to a TID $\simeq$ 15 Mrad and an equivalent neutron fluence of about 3×10^{13} n_{eq}/cm^2 (7.5x5 yrs equivalent).

For Layer0, where the radiation is an order of magnitude higher, a quick replacement of the entire layer is foreseen, as frequent as necessary, depending on the actual background and the radiation hardness of the technology chosen.

6.1.2.5 Reliability

Although the SuperB interaction region and the SVT mechanics will be designed to ensure a relative rapid access to the detector for replacement of Layer0, the acces of the SVT is not possible without a major shutdown. The reliability requirements for the SVT are therefore more stringent than usual for such a device, with implications for engineering design at all levels. The detector layout must provide redundant measurements wherever possible; the electronic readout must be very robust; and the functionality of all components must not be compromised by exposure to the expected radiation levels. The detector monitoring and interlock system must serve as a safeguard against catastrophic failure in the event of a component malfunction or a simple human error.

6.1.3 Baseline Detector Concept

6.1.3.1 Technology

The SVT baseline design is based on double-sided silicon microstrip detectors for all layers. The characteristics of this technology that make it attractive for the Super*B* detector are: high precision for measuring the location of charged particles, tolerance to high background levels, and reduction in mass made possible through double-sided readout. Double-sided silicon detectors have been employed with success already in *BABAR* and in several other large-scale appli-

Table 6.1: Summary of nominal expected background in the sensor area. The design of the SVT has been optimized with ×5 the nominal background. *Elba numbers for rates, New TID-NIEL, syncrotron radiation not included yet.*

Layer	Radius (mm)	Pitch (ϕ–z) (μm)	Total Rate/Area (MHz/cm^2) Track	Cluster	Strip (ϕ–z)	Total Strip Rate (kHz)	TID (Mrad/yr)	NIEL (n/cm^2/yr)
0	15	54–54 (u,v)	1.62	4.10	20–20 (u,v)	187–187	3	5×10^{12}
1	33	50–100	0.217	0.540	2.9–2.4	170–134	0.3	8×10^{11}
2	40	55–100	0.163	0.393	1.9–1.7	134–134	0.2	5×10^{11}
3	59	50-1-00	0.079	0.208	0.54–0.71	116–79	0.1	3×10^{11}
4	120	100–210	0.022	0.037	0.07–0.05	25–13	0.01	2×10^{11}
5	140	100–210	0.014	0.022	0.04–0.03	16–9	0.01	2×10^{11}

cations and are able to meet the performance standards outlined above.

6.1.3.2 Layout

The SVT will provide six measurements, in two orthogonal directions, of the positions of all charged particles with polar angles in the region $17° < \theta < 167°$. A three-dimensional cut-away view of the SVT is shown in Figure 6.3. The Layer0 has eight detector modules while the rest of the detector keep the same modules numbers as in *BABAR* : layers 1-2-3 have six detector modules, arrayed azimuthally around the beam pipe, while the outer two layers consist of 16 and 18 detector modules, respectively. A side view of the detector is shown in Figure 6.2, and an end view is shown in Figure 6.4.

The design of the Layer0 striplets module is completly new, with a quite complex shape, as shown in Fig. 6.5, to fit the very limited space available between the first layer of SVT and the beam pipe. The layout of the other five layers is very similar to the *BABAR* SVT strip modules, shown as a reference in Fig. 6.6 and Fig. 6.7.

The inner detector modules (0-3) are traditional barrel-style structures, while the outer detector modules (4-5) employ an arch structure, in which the detectors are electrically connected across an angle. The bends in the arch modules, proven to be well functional in *BABAR*, minimize the area of silicon required to cover the solid angle and also avoid very large track incident angles.

In order to satisfy the requirement of minimizing material in the detector acceptance region, one of the main features of the SVT design is the mounting of the readout electronics entirely outside the active detector volume. For this reason signals from the silicon strips are carried to the front-end chips by flexible fanout circuits.

There is a 1 cm space between the 300 mrad stay-clear in the forward and backward directions and the first element of the IR region (i.e. the tungsten shield cones) and all of the electronics are mounted here. In both directions, space is very tight, and the electronic and mechanical designs are closely coupled in the narrow region available.

The layout specifications for this six-layer design are given in Table 6.1.3.2 and described in more detail the text.

For Layer0 short strips, oriented at 45 degrees with respect to the detector edges (u, v strips), are adopted on both faces of the sensor in order to reduce the strip length and the related background occupancy to reasonable levels. For layers 1 to 5 the strips on the two sides of the rectangular detectors in the barrel regions are oriented parallel (ϕ strips) or perpendicular (z strips) to the beam line. In the forward and backward regions of the two outer layers, the angle between the strips on the two sides of

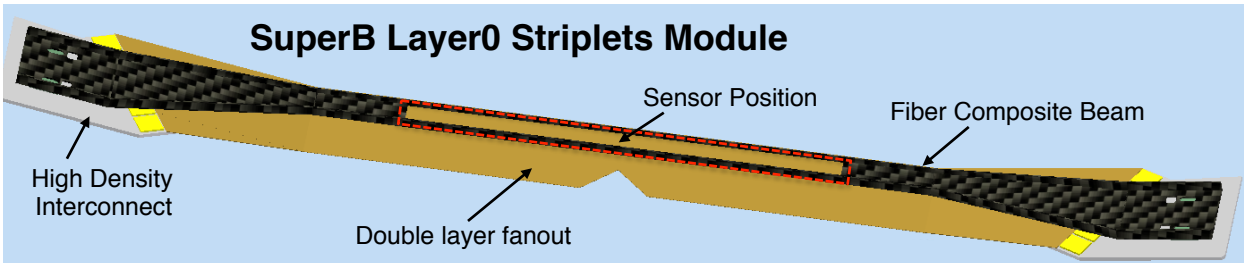

Figure 6.5: Schematic drawing of the Layer0 striplets module

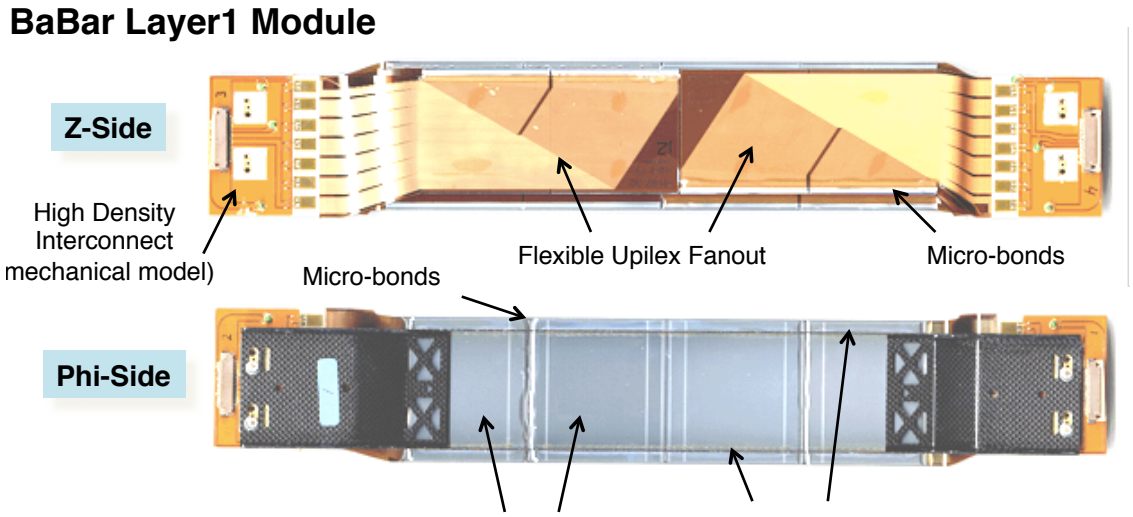

Figure 6.6: Details of the *BABAR* SVT Layer1 module.

the trapezoidal detectors is approximately 90°, and the ϕ strips are tapered. Floating strips are used to improve the position resolution for near-perpendicular angles of incidence; the capacitive coupling between the floating strip and the neighboring strips results in increased charge sharing and better interpolation. For larger incident angles with wider readout pitch minimizes the degradation in resolution that occurs because of the limited track path length associated with each strip. These issues are discussed in more detail in section 6.4.2.

The design has a total of 308 silicon detectors of nine different types. The total silicon area in the SVT is about 1.5 m ^{2}, and the number of readout channels is ∼170,000.

6.1.3.3 Electronic Readout

As emphasized above, all readout electronics are located outside the active volume, below 300 mrad in the forward and backward region. To accomplish this, ϕ strips on the forward or backward half of a detector module are electrically connected with wire bonds. This results in total strip lengths associated with a single readout channel of up to ∼19 cm in the inner layers and up to ∼38 cm in the outer two layers.

The signals from striplets for the Layer0 (u and v strips) and the z strips for all the other layers are brought to the readout electronics using fanout circuits consisting of conductive traces on a thin flexible insulator (for example, copper traces on Upilex as in *BABAR*). The

Table 6.2: *need to update the table* Parameters of the SVT layout.
See text for more detail on the meaning of the different quantities. The intrinsic resolution is calculated at 90° track incidence assuming $S/N = 20 : 1$. The z-ganging/pairing numbers represent the percentage of readout channels connected to the specified strip configuration.

Quantity	Layer 0	Layer 1	Layer 2	Layer 3	Layer 4a	Layer 4b	Layer 5a	Layer 5b
Radius (mm)	15	33	40	59	120	124	140	144
Wafers/Module	1	2	4	4	6	6	8	8
Modules/Layer	8	6	6	6	8	8	9	9
Silicon Area (cm^2)	127	554	787	1655	2459	2548	3502	3610
Overlap in ϕ (%)	2.0	2.4	1.8	1.8	4.0	4.0	2.0	2.0
Readout pitch (μm):								
ϕ (u for Layer 0)	54	50	55	100	82–100		82–100	
z (v for Layer 0)	54	100	100	110	210		210	
Floating Strips:								
ϕ (u for Layer 0)	—	—	—	1	1		1	
z (v for Layer 0)	—	1	1	1	1		1	
Intrinsic Resolution (μm):								
ϕ (u for Layer 0)	10	10	10	10	10–12		10–12	
z (v for Layer 0)	12	12	12	12	25		25	
R.O. Section								
ROS/Module	4	4	4	4	4		4	
ICs/ROS (ϕ-z)	6-6	7-7	7-7	6-10	4-5		4-5	
Readout Channels	24576	21504	21504	24576	36864		41472	
Strip Length Half Module (mm):								
ϕ (u for Layer 0)	20	110	130	190	293	303	369	380
z (v for Layer 0)	20	40	48	70	51–103	103–154	103–154	103–154
Fraction of z-side r.o. channels with Pairing/Ganging:								
None		77%	55%	65%	4%			
Pairing ×2		23%	45%	35%				
Ganging ×2					73%	74%	25%	16%
Gang.×2 + Pair.×2					23%	24%	41%	43%
Ganging ×3						2%	34%	41%

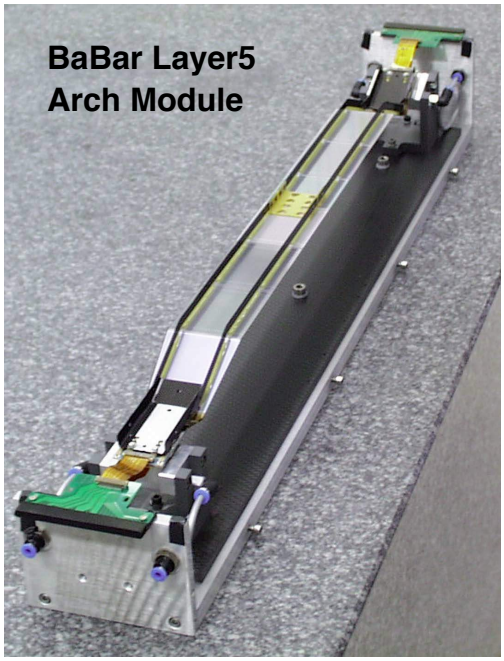

Figure 6.7: Details of the *BABAR* SVT Layer5 arch module.

traces on fanout are wire-bonded to the ends of the silicon strips.

On the z side of the modules the number of readout strips exceed the number of available electronic channels, constrained by the number of chips that can fit in the limited space available. To reduce the number of readout channels needed, the connection scheme for the z fanout circuits includes "pairing" and "ganging" (described in Section 6.4.2) with two or three strips bonded to a single fanout/readout channel. The length of the z strips is much shorter than ϕ strips, typically 4-7 cm in the inner layers and either 10 or 15 cm in the outer layers, where there is either $\times 2$ or $\times 3$ ganging.

Front-end signal processing is performed by ICs mounted on the High-Density Interconnect (HDI), a thick-film hybrid circuit fabricated on aluminum nitride (AlN) substrate. The HDI provides the physical support, it distributes power and signals, and thermally interfaces the ICs to the cooling system.

New front-end custom-design ICs are currently under developmemnt for the Super$B$ SVT [20] since none of the existing chips is matching all the requirements 6.6.2. The signals from the readout strips, after amplification and shaping, are compared to a preset threshold. The time interval during which they exceed the threshold (time over threshold, or TOT) is an analog variable related to the charge induced on the strip. Unlike the ordinary peak-amplitude measurement at the shaper output, the TOT technique has a nonlinear input-to-output relationship which is approximately logarithmic. This is an advantage since it compresses the dynamic range and allows one to achieve good position resolution and large dynamic range with a minimum number of bits. TOT readout has been successfully employed in the front-end chip of the *BABAR* SVT (i.e. Atom chip [2]) providing sufficient analog resolution for position interpolation, time-walk correction, and background rejection.

For each channel with a signal above threshold, the TOT information together with the hit time stamp will be buffered until a trigger is received; it will be then transferred, with the strip number, to an output interface, where data will be serialized and transmitted off chip on output LVDS lines.

The readout IC is expected to be about 6x4 mm^2 and to dissipate about 4.0 mW per channel. The total power that will be generated by the SVT readout chips is ∼700 watt (*considering 4 mW/chan is correct including the digital power?*).

There are four readout sections per detector module, where the module is divided in half along z, and the ϕ and z strips are grouped together separately. The data from one-half of a detector module will be transmitted from the hybrid on a flexible cable to a transition card located approximately 40 cm away, where the signals are converted and transmitted to optical fibers.

6.1.3.4 Module design and Mechanical Support

review this section The silicon detectors and the associated readout electronics are assembled into mechanical units called detector

modules. Each module contains from 1 to 8 silicon detectors, the flex circuits to bring the signal from strip to the front-end chips, and a low-mass beam constructed of carbon and Kevlar fiber-epoxy laminates (i.e. ribs) to stiffen the module structure. The ribs are attached through a carbon fiber end-piece to the HDI hybrid circuit. An Aluminum Nitride substrate for the HDI provides precise mechanical mounting surfaces and it is the heat sink for the electronics.
The module of the Layer0 has peculiar features (see Fig. 6.5). Only one sensor is used, where the strips are still orthogonal on both sides but tilted with a 45° angle with respect to the detector edge. The Layer0 is arranged in an octagonal (i.e. not exagonal) geometry to have shorter strip length. Due to the large number of strip on each side, the fanout circuits must have an extention almost twice the width of the detector and a stack of two fanout layers is required (see details on section 6.5.1). The HDI can allocate the necessary 6 read-out chips by tilting them with a 30° angle.

With this design the module material budget in the active region is very limited, and as in *BABAR* is about 0.45% X_0 per layer. For layers 1 to 5 this is dominated by the 300 μm of the silicon sensor, a contribution of about 0.1 % X_0 is due to the composite ribs, with about 0.05 % X_0 for the z fanout, the one that sits in the active area. In Layer0 striplets the contribution of the flex circuit is considerably higher: the total material for the two multilayer flex circuits, now under development, is about 0.15 % X_0, while about 0.1 % X_0 are accounted for the carbon fiber support structure. With sensor thickness of the stripltes of only 200 μm the total material budget is about 0.45% X_0 also for Layer0.

Layer0 modules are supported on the cold flanges, directly coupled with the Be beam-pipe, allowing the minimization of the distance to the beam pipe and a quick demounting of the layer 0 without touching the SVT. The other five SVT layers are mounted on support cones coupled with the conical tungsten shields with kinematic mounts (i.e. the gimbal rings) that will allow relative motions of the forward backward shields without stress on the silicon detectors. The detector modules from Layers 1 and 2 are glued together with rigid beams, forming sextants which are then mounted from the support cones in the forward and backward directions. Each detector module of Layer 3-4-5 is mounted on the support cones independently of the other modules. In layer 4 and 5, there are two different types of modules in each layer, an inner one, labeled *a*, and an outer one, labeled *b*, occupying slightly different radial positions. Thus there are eight different types of detector modules.

The support cones are laminated carbon-fiber structures which are mounted on the tungsten shield cones. Cooling water flows in brass cooling rings surrounding the outer surface of the cone. Mounting pins in the hybrid structure provide the alignment between the modules and the brass mounts on the cone, and thermal contact is made to provide cooling for the front-end electronics located on the hybrid. The support cones are divided to allow the vertex detector to be assembled in two halves and then mounted on the shielding cones and the beam pipeby clamshelling the pieces together. During the assembly/disassembly procedure the splitting of the support cones with the five SVT layers on, will allows an easy access of the Layer0 without the need to disassemble the entire SVT.

The stiffness of the overall SVT structure is provided by a very low mass space frame, constructed of carbon-fiber tubes, connecting the forward and backward support cones, similar to the one designed for the *BABAR* SVT. The motivation for this space frame stems mainly from the possible relative motion of the two shielding cones during the assembly procedure or in case of an earthquake. *check this and add gimbal ring description* Cooling water, power, and signal lines are routed along the support cones to points outside the active region where manifolds for the cooling water and drivers for the electronics are located.

6.1.4 Layer0 Pixel Upgrade

6.1.4.1 Motivations

With the machine operated at full luminosity, the layer 0 of SVT may benefit from upgrading to a pixellated detector that have more stable performance in case of high background conditions, thanks to a lower background rate expected. A background rate of about 1 MHz/strip (x5 safety included) is expected with a striplets lenght of about 2 cm and 50μm pitch, while only 2.5 KHz/pixel are expected for pixels with a 50x50 μm pitch.

Possible effects of background hits on performance are: the reduction of the hit reconstruction efficiency (due to pile up), the increase of the effective hit resolution, the reduction of efficiency of the pattern recognition for charged tracks along with the increase of fake tracks. Most of these effects have been included in specific simulation studies performed to evaluate the SVT performance in the high background scenario, (i.e. full luminosity including x5 safety factor on nominal background). The results, described in more details in Sec.**??**, showed a significant degradation in the striplets performance with high background occupancy, while the pixel solutions explored showed more stable performance against background conditions. The pixel occupancy is reduced at least by a factor 200 w.r.t striplets considering the smaller electrode dimensions and even including a possible worse time resolution of the pixel w.r.t striplets.

An example of these studies is shown here. The impact of machine background on the SVT performance has been studied evaluating the per-event error on the physics parameter S, adding background hits to signal events. S is measured in time-dependent analyses (corresponds to $\sin(2\beta)$ for $B^0 \to J\psi K^0_S$ decays) and the S per-event error is defined as the error on the parameter S normalized to the number of signal events. In Fig.6.8 the impact of background on the physics parameter S is reported for striplets and pixel, for the case of nominal background and with 5 times background rates.

For the striplets the reduction to the sensitivity to S w.r.t. BaBar is small with nominal background, only about 3%, but it is up to about 15% with 5 times the nominal background. On the contrary with a pixel option, beeing there the effect of background occupancy negligible, the reduction to the sensitivity to S is only 3%, even in the high background scenario, and it is related to the effect of the background in the rest of the SVT.

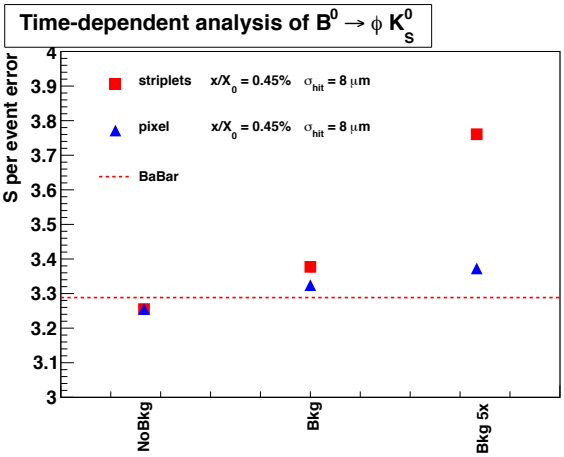

Figure 6.8: Variation of the S per event error in $B^0 \to \phi K^0_S$ time-dependent analysis in presence of background events, for a Layer0 based on striplets or pixel with the same material budget. Efficiency and resolution deterioration are both included in the simulation study.

It is important to stress that in the study reported here the pixel option has the same material budget used for striplets (about 0.45% X_0), same performance without background included. Of course the use of pixel over striplets in high background is less convenient if the material budget of pixels is significantly higher. On the contrary if one can reach a very low material budget with a thin pixel option, below the striplets target, the upgrade to pixel for Layer0 is well motivated also in nominal backround conditions. (see for example Fig.6.18).

While for strip modules most of the material budget is due to the silicon of the sensor itself, in pixel modules there are several other important contributions in the active area. Including the readout electronics, cooling, and the pixel bus for the connection of the front-end chips with the periphery of the module, one one can easily reach a total material budget for pixel above 1% X_0. A discussions on the material for the various pixel options for the Layer0 is presented in the next sections.

6.1.4.2 Technology Options for Layer0 pixel upgrade

Two main technologies are under evaluation for the upgrade of Layer0: hybrid pixel and thinner CMOS Monolithic Active Pixel Sensor (MAPS). Specific R&D programs are ongoing on these options to meet all Layer0 requirements, such as low pitch and material budget, high readout speed and radiation hardness.

A short summary of the current status of the R&D on the different pixel options is given below, while a more detailed review is presented in Sec.6.8.

Hybrid Pixel technology represents a mature and viable solution but reduction in the front-end pitch and in the total material budget, with respect to pixel systems developed for LHC experiments, is required for application in Layer0.

The spatial resolution constraints of 10-15 μm set a limit to the area of the elementary readout cell and, as a consequence, to the amount of functionalities that can be included in the front-end electronics. For a pixel cell 50×50 μm^2 a planar 130 nm CMOS technology may guarantee the required density to implement in-pixel data sparsification and fast time stamping ($< 1\mu s$), as required for the high target hit rate in Layer0 of 100 MHz/cm^2 in order to keep the module bandwidth to acceptable level (<5 Gbit/s).

Denser CMOS technologies, as the 65 nm technology, can be used to increase the functional density in the readout electronics and include such functions as local threshold adjustment and amplitude measurement and storage. In this case, costs for R&D and production would increase significantly. Vertical integration (or 3D) CMOS technologies may represent a lower cost alternative to sub-100 nm CMOS processes to increase the functional density in the pixel cell [33, 34].

A front-end chip for high resistivity pixel sensors with 50×50 μm^2 pitch is under development for the application in Super$B$ A first prototype chip with 4k pixels has been produced with the ST Microelectronics 130 nm process adopting the same readout architecture, with in-pixel sparsification and timestamping, developed within the SLIM5 Collaboration [41] for CMOS Deep NWell MAPS [42, 43]. The chip bump bonded to a high resistivity sensor matrix has been fully characterized, with beams, with good results [29].

In this first prototype only basic functionalities have been implemented. The readout architecture has been recently optimized to sustain efficiently the target Layer0 hit rate of 100 MHz/cm^2 on matrices larger than 50k pixels. The new architecture, that requires a more complex in-pixel logic, implement a data push and a triggered version of the readout [28].

The design of a 3D front-end chip for hybrid pixel with this new readout architecture, and some improved features, is now in progress with the vertical integration CMOS technology offered by the 130 nm Chartered/Tezzaron process.

CMOS MAPS are very appealing for application where the material budget is critical: in this technology the sensor and readout electronics share the same substrate that can be thinned down to several tens of microns. Since a fast readout is another crucial aspect for Layer0 a new Deep NWell MAPS design approach has been developed by the SLIM5 Collaboration[41]) to improve readout speed in CMOS MAPS sensors. This approach allowed for the first time the implementation of thin CMOS sensors with similar functionalities as in hybrid pixels, such as pixel-level sparsification and fast time stamping [42, 28]

Thanks to an intense R&D program the development of DNW CMOS MAPS (with the ST

Microelectronics 130 nm process) has reached a good level of maturity. A limiting factor in this design is the presence of competitive N-Wells, inside the pixel cell, that can subtract charge to the main collecting electrode. The last prototype realized, the APSEL4D chip, a 4k pixel matrix with $50 \times 50\mu m^2$ pitch has been tested with beams [22] reporting a hit efficiency of 92%, related to the pixel cell fill factor (ratio of the DNW area to the total area of N-wells) which is about 90% in the APSEL design. Another critical issue for the application of CMOS MAPS in the Layer0 is their radiation hardness expecially related to bulk damage effect. A significant degradation of the charge collected (about 50%) has been measured after irradiation with neutron up to a fluence of about $7x10^{12}$ n/cm^2, corresponding to about 1.5 years of operation in the Layer0 [32].

Further MAPS performance improvements are currently under investigation with two different approaches: the use of INMAPS CMOS process, featuring a quadruple well and an high resistivity substrate, and 3D CMOS MAPS, realized with vertical integration technology.

In order to increase the charge collection efficiency the INMAPS 180 nm CMOS process is being explored: a deep P-well implant, deposited beneath the competitive N-Wells, can prevent them from stealing charge to the main collecting electrode. Moreover the use of high resistivity substrate, also available in this process, can further improve charge collection and radiation resistance with respect to standard CMOS devices. First prototype INMAPS matrix have been realized with the improved readout architecture suitable for the application in the SuperB Layer0 [29]. The devices, currently under test, showed promizing results, with measured Signal-to-Noise of about 27 for MIPs [19]. Radiation hardness of these devices, at the level required for a safe operation in Layer0 for at least a couple of years ($> 10^{13}$ n/cm^2), is currently under investigation with promizing preliminary results. (ref to layer0 upgrade section).

The realization of 3D MAPS, using two CMOS layers interconnected with vertical integration technology, also offer several advantages with respect to standard 2D MAPS. In these devices one CMOS tier is hosting the sensor with the analog front-end and the second tier is dedicated to the in-pixel digital front-end and the peripheral readout logic. With this splitting of functionalities the collection efficiency can be improved, significantly reducing the N-Well competitve area in the sensor layer. Having more room for the in-pixel logic allows the implementation of a more performant readout architecture. Finally in 3D MAPS the cross-talk between analog and digital blocks can be minimized.

The characterization of first 3D MAPS prototypes, realized with the 130 nm Chartered/Tezzaron 3D process is under way and first beamtest results on the MAPS layer implementing the sensor and the analog front end showed a very good hit efficiency (above 98%).

insert conclusions on the best technology for upgrade considering the actual status of R&D from elba paper

6.1.4.3 Pixel Module & Material Budget

The schematic drawing of the full Layer0 made of 8 pixel modules mounted around the beam pipe is shown in Fig. 6.9.

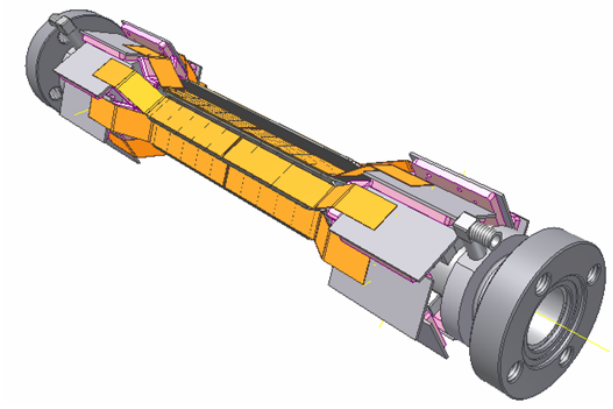

Figure 6.9: Schematic drawing of the full Layer0 made of 8 pixel modules mounted around the beam pipe with a pinwheel arrangement.

Layer0 Module Material Budget (X_0)			
	Striplets	Hybrid Pixel	CMOS MAPS
Sensor	0.21%	0.11-0.21%	0.05%
FE-chip+bump bonding		0.14-0.19%	
Multilayer bus or fanout	0.15%	0.15-0.30%	0.15-0.30%
Module Support & ground plane (include cooling for pixels)	0.09%	0.15%	0.15%
Total Material Budget (X_0)	0.45%	0.55-0.85%	0.35-0.50%

Table 6.3: Layer0 module material budget for the different technologies under evaluation.

In all the pixel options under evaluation, sharing the same multichip module structure, the material budget of all the components must be kept under control to minimize the detrimental effect of multiple scattering.

The main contributions to the material budget for pixel modules with different technologies are discussed in this section and summarized in table 6.3 with a comparison with the striplets option.

In the hybrid pixel solution the contribution of the silicon from the sensor (100-200 μm) and the front-end chip (100-150 μm) can be in the range of 0.25-0.4% X_0. In the CMOS MAPS option the sensor and the front-end electronics are integrated in the same CMOS chip that could be thinned down to 50 μm reducing this contribution down to only 0.05% X_0.

Another important contribution to the material is due to the pixel bus needed for the connection of front-end chips to the periphery of the module. This connection will be realized with an Al/kapton multilayer bus, now under development. With our present requirements on speed (high bandwidth due to a hit rate of 100 MHz/cm2) and power consumption (about 1.5W/cm^2) the estimated material budget for the pixel bus is about 0.15-0.3% X_0, depending on the achievements of present R&D on this item.

The pixel module support structure needs to include a cooling system to evacuate the power dissipated by the front-end electronics, about 1.5W/cm^2, present in the active area. In order to minimize the material budget a light carbon fiber support structure with integrated active cooling, based on microchannel technology [36] and forced liquid convection, has been developed. The support with integrated cooling is build with carbon fiber micro-tubes, with a hydraulic diameter of about 200μm, obtained by a poltrusion process. Measurements on the support prototypes, with a total material budget as low as 0.11% X_0, indicate that such approach is a viable solution to the thermal and structural problem of Layer0 [37] An innovative idea is also under development to integrate into the silicon itself the cooling system based on microchannels made by DRIE technology. The embedded microchannels, with diameters even below 100μm, feature a peculiar geometry, and in the final step a thin oxide layer is deposited to seal the channels, resulting reliable under the operating high-pressure conditions. This technique permits the integration of the cooling system within the detector with obvious advantages on the optimization of thermal bridges and transparency to the incident particles [38].

6.1.5 R&D Main Activities

6.2 Backgrounds R.Cenci - 4 pages

A detailed analysis of background effects is fundamental to have a reliable estimation of performances and expected lifetime of the tracker.

As already described in Chap. 5, in addition to well-known background sources as Touschek and beam-gas, we have a significant contribution from physics processes that happens in the interaction point. The very high luminosity of the machine produces an unprecedented rate for additional pairs and radiative Bhabha processes that, in some areas, is similar or larger than other traditional background sources. The effect of those physics processes cannot be mitigated optimizing the machine optics, because they scale with the luminosity and the machine goal is always to get the luminosity as highest as possible. In addition, if the particles produced by those physics processes are within the detector acceptance, they cannot be easily shielded, because particles from the interesting physics processes would be stopped as well.

The different sources of background have been simulated with a detailed Geant4-based detector model and beamline description (see Sec. 14.1.1). The detailed simulation is needed because not only the detectors themselves, but also the supporting parts (also referred to as "dead material") play an important role in stopping or creating background particles. Then, the raw output of the simulation has to be processed to obtain useful information that can be used for additional specific simulation of the readout electronics and for test with real particle. Simulated background events can also be sampled and added to relevant physics events to estimate the tracking perfomances in real running conditions, as detailed in Sec. 6.3. Background results can have a significant influence on several aspects of the SVT design, like readout segmentation, electronics shaping time, data transmission rate, and radiation hardness (particularly severe for Layer0).

Add a description of the detector model in Bruno ed insert reference to the main Background sections

Crossing multiplicity, deposited energy distruibution, bandwith, crossing with high number of tracks

Describe main feature of each source

6.2.1 Pair production

6.2.2 Radiative Bhabha

6.2.3 Touschek

6.2.4 Beam Gas

6.2.5 Other sources

Include summary tables with rates, doses, equivalent fluences for various layers

6.3 Detector Performance Studies N.Neri - 8 pages

6.3.1 Introduction

The Super$B$ vertex detector can be considered as the evolution of the *BABAR* one. It is capable of maintaining adequate performance for time-dependent measurements in presence of a lower boost of the center-of-mass frame (CM) ($\beta\gamma = 0.24$ compared to $\beta\gamma = 0.55$ of *BABAR*) and much higher background, mainly related to the increased istantaneous luminosity of about a factor 100 higher with respect to *BABAR*.

The beampipe features a reduced radius of about 1.0 cm which allows the positioning of the innermost layer of the SVT (Layer0) at an average radius of about 1.5 cm. The additional Layer0 measurement along with the low radial material budget of the beampipe (0.42% X_0) and of Layer0 (0.45% X_0 with the striplet option), is crucial for improving the decay vertex reconstruction of the B mesons and obtaining adequate proper-time resolution for time-dependent CP violation measurements. In addition, the small size of the luminous region, about $(1 \times 1)\,\mu\text{m}^2$ in the transverse plane, also contributes to the improvement of the decay vertex reconstruction when imposing the constraint that the particles are originated from the interaction point. The baseline solution for the Layer0 is based on short strip technology and an upgrade to pixel is foreseen.

In the following we discuss the baseline layout of the SVT and how the design has been optimized in Section 6.3.2, the impact of the Layer0 on detector performance in Section 6.3.3, and

the tracking performance in Section 6.3.4. The impact of the machine background on SVT performance is discussed in Sections 6.3.5, 6.3.6 and the performance with a Layer0 pixel detector is presented in Section 6.3.7. In Section 6.3.8 it is described the performance for particle identification based on ionization $\mathrm{d}E/\mathrm{d}x$ in the SVT sensors.

6.3.2 The SVT layout

The Super$B$ SVT is composed by 6 layers of double-sided silicon strip detectors and has a symmetric coverage in the laboratory frame down to 300 mrad (17.2°) with respect to the forward and backward direction, corresponding to 95% angular coverage in the CM. The inner three layers perform the track impact parameter measurements, while the outer layers are necessary for pattern recognition and low transverse momentum (p_t) tracking.

The Layer0 strips are short ('striplets') and oriented at ±45° with respect to the beam direction. The Layer1 to Layer5 silicon strip detectors are very similar to the *BABAR* ones in terms of radial position and strip pitches. The optimization of the strip z and ϕ pitches for the strip detectors is discussed in Section 6.4.2. A dedicated study to optimize the SVT layout as a function of number of silicon sensors and radial positions was performed [3]. Several figures of merit were studied: the track parameters resolution, the reconstruction efficiency and kinematic variable resolutions of B decays with low momentum tracks as $B^0 \to D^{*-}K^+$. Since low momentum tracks do no reach the DCH, they are reconstructed using only SVT information. The *BABAR* experiment has shown that at least 4 hits in the ϕ view and 3 hits in the z view are necessary for robust track reconstruction [4, 5]. The main result is that the 6-layer design is superior and more robust compared to the alternatives investigated, *i.e.* 4- and 5-layer layout where intermediate layers are removed. Indeed, when accounting for possible inefficiencies in hit reconstruction, due to damaged modules or high background, the 6-layer design insures higher reconstruction efficiencies for low momentum tracks compared to the other solutions where intermediate layers are removed.

In Table 6.4 the reconstruction efficiencies are reported for the decay $B^0 \to D^{*-}K^+$ for the 4-, 5- and 6-layer configuration in different running conditions: ideal conditions (A), with a damaged module in Layer3 (B) and with additional hit inefficiency in Layer0 with respect to case B (C). The outer radius of the SVT was ultimately constrained to about 20 cm by the DCH inner radius. It was demonstrated that there is no real advantage in increasing the outer layer of the SVT with respect to the *BABAR* design (14.4 cm) [6, 7, 9]. Moreover, construction cost and technical difficulties would increase. Radial positions of the Layer1 to Layer4 have very little impact on track resolution when comparing a layout with detectors equally separated and the *BABAR*-like layout.

Table 6.4: Reconstrucion efficiencies for $B^0 \to D^{*-}K^+$ decays for different SVT layout (4, 5 ,6 layers) and running conditions (A, B, C). Case A correspond to ideal running conditions, B represents SVT with a damaged module in Layer3 with z hit efficiency of 70%. Case C introduces additional inefficiency with respect to case B in Layer0: 60% hit efficiency for z and ϕ views.

	A eff. (%)	B eff. (%)	C eff. (%)
6 layers	66.0 ± 0.3	65.0 ± 0.3	64.0 ± 0.3
5 layers	64.0 ± 0.3	62.0 ± 0.3	60.0 ± 0.3
4 layers	60.0 ± 0.3	56.0 ± 0.3	53.0 ± 0.3

6.3.3 Impact of Layer0 on detector performance

The additional Layer0 measurement is crucial for maintaining adequate resolution on the B^0 meson proper-time difference $\Delta t \simeq \Delta z/(\beta\gamma c)$ in presence of a relatively low CM boost value $\beta\gamma = 0.24$. The average separation Δz between

the decay vertex positions of the two B mesons along the z axis is $\Delta z \simeq \beta\gamma c\tau_B = 110\ \mu$m, where τ_B is the B^0 lifetime of about 1.5 ps. Hence, in order to be able to separate the B mesons in Super$B$, their decay positions have to be determined with a significantly better precision than the average separation Δz. In addition in Super$B$, the B vertex separation in the transverse plane, of about 25 μm, is not completely negligible with respect to the average Δz separation of about 110 μm. It therefore also contributes to the determination of Δt. The reference value for the Δt resolution, $\sigma(\Delta t)$, was determined by the resolution obtained in the *BABAR* experiment according to the Fast Simulation, see Table 6.5. Fig. 6.10 shows the dependence of the per-event error on the physics parameter S as a function of $\sigma(\Delta t)$, with the sensitivity obtained in *BABAR* superimposed. In this simplified model $\sigma(\Delta t)$ corresponds to the width of the core Gaussian of the Δt resolution function. The S per-event error is defined as the error on the parameter S normalized to the number of signal events. S is measured in time-dependent analyses and corresponds to $\sin(2\beta)$ for $B^0 \to J/\psi K^0_S$ decays. The resolution σ_z on the z coordinate of the track depends on the geometry of the vertex detector and the hit resolution. In a simplified model with two hits measured at radii r_0 and r_1 ($r_1 > r_0$) with z hit resolution σ_0 and σ_1 respectively, σ_z can be approximated as:

$$\sigma_z = \frac{\sigma_0^2 + (\sigma_1 r_0/r_1)^2}{1-(r_0/r_1)^2}. \qquad (6.1)$$

In addition, the tracks are deflected due to multiple scattering interactions with the material in the tracking volume. The scattering angle distribution can be approximated by a Gaussian with a width given by [39]:

$$\theta_{\text{m.s.}} = \frac{13.6\,\text{MeV}/c}{p_t\beta}\sqrt{\frac{x}{X_0}}\left[1+0.0038\ln\left(\frac{x}{X_0}\right)\right] \qquad (6.2)$$

where p_t is the transverse momentum, x is the thickness of the material and X_0 is the radiation length. In order to minimize the uncertainty on σ_z it is important to measure the first hit at r_0 as small as possible with a good hit resolution σ_0. Minimizing the material close to the interaction, *e.g.* the beampipe and Layer0 material budget is also important.

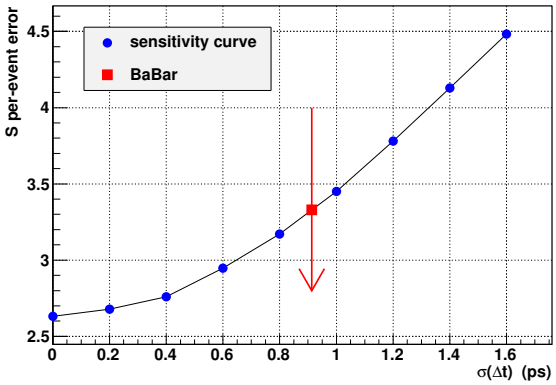

Figure 6.10: The curve represents the dependence of the error on the physics parameter S (*e.g.* $\sin(2\beta)$) as a function of $\sigma(\Delta t)$. The arrow indicates the $\sigma(\Delta t)$ value obtained in *BABAR* according to the Fast Simulation and the square point is the relative value on the sensitivity curve.

Fig. 6.11 shows the residual distributions of B decay vertex z positions for exclusively (top) and inclusively (bottom) reconstructed B decays. Fig. 6.12 shows the Δz (top) and Δt (bottom) residual distributions. One B is exclusively reconstructed in the $B^0 \to \phi K^0_S$ mode (B_{reco}), while the other B is inclusively reconstructed using the remaining tracks of the event and is used also for flavor tagging (B_{tag}). The Fast Simulation results for Super$B$ with Layer0 striplets are compared with the *BABAR* ones and summarized in Table 6.5. In Super$B$ we assume $\sigma_0 = 8\,\mu$m for both u and v hits, as measured on striplets module prototype in a recent beamtest. The Layer0 has a pinwheel configuration with radius in the range $1.53-1.71$ cm and it is modeled in FastSim as a cilinder with average radius of about $r_0 = 1.6$ cm. The total material budget forthe beampipe and the Layer0 striplets is

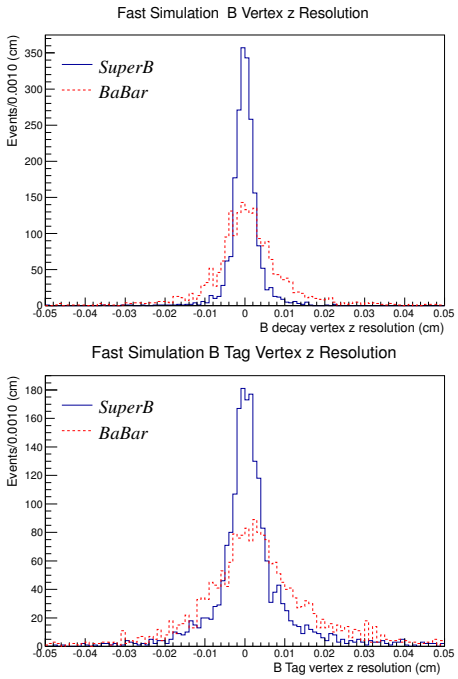

Figure 6.11: B decay vertex z position (top) and B tag z position (bottom) residual distributions in Super$B$ with Layer0 striplets (continuous line) compared with *BABAR* (dashed line) according to Fast Simulation studies.

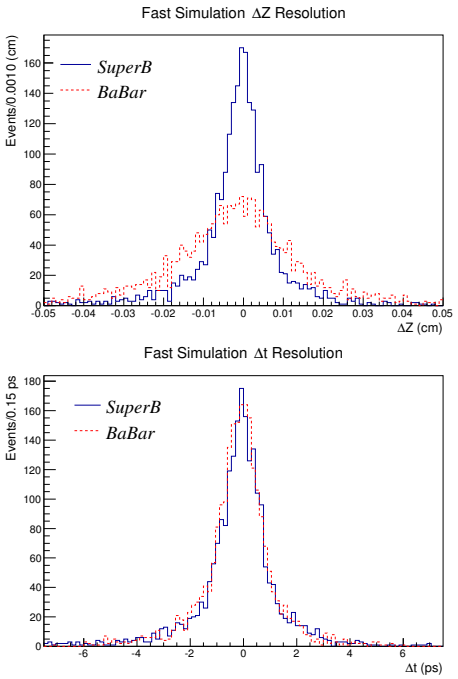

Figure 6.12: Δz (top) and Δt (bottom) residual distributions in Super$B$ with Layer0 striplets (continuous line) compared with *BABAR* (dashed line) according to Fast Simulation studies.

about $x/X_0 \simeq 0.9\%$. For striplets detectors, u and v coordinates are oriented at $\pm 45°$ with respect to the z axis and are perpendicular to each other. In *BABAR* we have $\sigma_0 = 14\,\mu$m for the z hits and $10\,\mu$m resolution for the ϕ hits, with $r_0 = 3.32\,$cm and $x/X_0 \simeq 1.6\%$. In Super$B$, the improved Δz resolution is compensated by the reduced boost value, yielding a Δt resolution very similar to *BABAR*. In Fig. 6.13 is shown the Δt resolution obtainable with different Layer0 radii (r_0= 1.4 and 1.6 cm) and material budgets (x/X_0 ranging from 0.1 to 1.0%). The dashed line represents the reference value of *BABAR*.

The impact of the hit resolution on the decay vertex reconstruction has also been studied. With $8\,\mu$m hit resolution in both views of Layer0, the error on the vertex position due to multiple scattering interactions with the material dominates the overall vertex uncertainty. Even for high momentum tracks from $B^0 \to \pi^+\pi^-$ decays. Hence, without further reduction of the material budget, there is no real advantage in improving the hit resolution with respect to this value. The hit resolution from Layer1 to Layer5 has been chosen according to the *BABAR* SVT design which was optimized for low momentum track reconstruction. The intrinsic detector hit resolution and hit efficiency values used in the Fast Simulation are reported in Table 6.6 for the different SVT layers. The efficiencies have been estimated from simulations taking into account possible hit losses due to the overlap of pulses in the analog section of the FEE with nominal background conditions.

Table 6.5: RMS of the residual distributions for decay vertex z position for exclusively reconstructed $B^0 \to \phi K^0_S$ decays ($B_{\rm reco}$), inclusively reconstructed B decays ($B_{\rm tag}$), Δz and Δt at Super$B$ and compared with *BABAR* results, according to Fast Simulation studies.

	Super$B$	*BABAR*
$B_{\rm reco}$ (μm)	40 ± 1	105 ± 1
$B_{\rm tag}$ (μm)	100 ± 2	145 ± 2
Δz (μm)	105 ± 2	165 ± 2
Δt (ps)	1.40 ± 0.02	1.45 ± 0.02

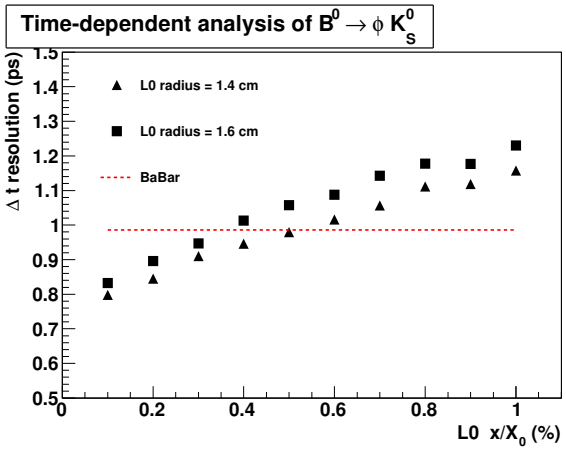

Figure 6.13: Resolution on Δt for different Layer0 configurations in terms of radius (r_0 = 1.4 and 1.6 cm) and material budget (x/X_0 = 0.1 − 1.0%) compared with the reference value of *BABAR* (dashed line).

6.3.4 Tracking performance

The tracking performance at Super$B$ has been studied considering alternative solutions for the SVT and DCH layout [3, 6, 7]. In particular we have studied alternative SVT configurations: with different values of the SVT outer radius (from about 14 to 22 cm), without Layer2 detector, different radial positions of the layers (*e.g.* uniform distance between layers), different hit resolutions accounting for variations of about 50% with respect to the nominal ones reported in Table 6.6. The main result was that the *BABAR*-like layout for Layer1-Layer5 was very close to be the optimal choice in terms of resolution for track parameters. Small improvements in track parameter resolution would have been possible by removing Layer2. On the other hand, the 6-layer layout has been proved to be more robust against possible problems that might cause loss of efficiency in some layers of the detector [3] and was preferred for this reason. Optimization of the strip pitches for the z and ϕ sides of the different layers are discussed in Section 6.4.2. Fig. 6.14 shows the resolution on the impact parameter d_0, as a function of p_t with the *BABAR* and Super$B$ detectors. The d_0 is defined as the distances of the point of closest approach of the track to the z-axis from the origin of the coordinate system in the $x - y$ plane. Results for alternative configurations of the SVT layout, with extended outer radius, with DCH lower radius, and without Layer2, are also shown. A significant improvement in the d_0 resolution of about a factor 2 is achieved with the Super$B$ detector with respect to the *BABAR* one. The alternative SVT layout options investigated give consistent results with the nominal Super$B$ solution.

Table 6.6: Intrinsic detector hit resolution and hit efficiency for the ϕ and z sides (Layer0 u and v sides) for the different layers.

	res. u (μm)	res. v (μm)	eff. u (%)	eff. v (%)
Layer0	8	8	99	99
	res. z (μm)	res. ϕ (μm)	eff. z (%)	eff. ϕ (%)
Layer1	14	10	98	98
Layer2	14	10	98	98
Layer3	14	15	98	96
Layer4	25	15	99	98
Layer5	25	15	99	98

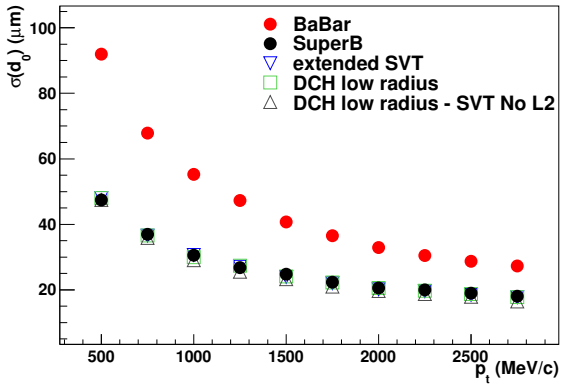

Figure 6.14: Resolution $\sigma(d_0)$ on the impact parameter d_0 as a function of p_t in *BABAR* and for various Super$B$ tracking detector configurations.

6.3.5 Impact of machine background on tracking performance

The background conditions will be more severe in Super$B$ than in *BABAR*, as described in Section 6.2. The fast front-end electronics of the SVT provides very good resolution on the time of passage of the particle or time of arrival of the hit. The Time over Threshold (ToT) of the shaper output is used to correct for the time between the time of arrival of the hit and the time the shaper exceeds threshold. The latter is referred in the following as time stamp (TS) of the hit, and registred with a TS clock. The resolution on the time of arrival of the hit depends on the SVT layer due to the different shaper peaking times of the front-end electronics, and has been estimated using 'ad hoc' simulations [8]. Several peaking times will be available on the strip readout chips, as summarized in Table 6.16. The resolution for all layers and sides is reported in Table 6.7 for the nominal peaking-time configuration and for the shortest peaking times in Layer4 and Layer5. It ranges from about 10 ns for Layer0 up to 50 ns for Layer5. In our studies, hits outside a $\pm 5\sigma$ acceptance time window from the event time (determined by the DCH) are discarded. A similar procedure was used in the reconstruction program of the *BABAR* experiment.

Table 6.7: Resolutions on the time of arrival of the hit for the z and ϕ sides (Layer0 u and v sides) for the different layers with selected peaking times. The "old" detector correspongs to the same detector after 7.5 years of running and includes a safety factor of 5 times the level of radiation with respect to the nominal one.

	shaper peak. time (ns)	time res. "fresh" det. (ns, ns)	time res. "old" det. (ns, ns)
Layer0	25	(9.7, 9.7)	(9.7, 9.7)
Layer1	75	(10.7,10.2)	(11.0,10.8)
Layer2	100	(11.4,12.4)	(12.0,11.5)
Layer3	150	(12.4,11.7)	(15.1,14.1)
Layer4	500	(28.8,24.2)	(41.6,49.4)
Layer5	750	(42.6,34.3)	(54.6,46.7)
Layer4	250	(17.8,15.9)	(21.1,19.3)
Layer5	375	(24.9,20.5)	(27.6,23.8)

The Fast Simulation tool does not apply any pattern recognition algorithm. Tracking performance is based on parameterizations tuned on *BABAR* measured performance. Hits from neighboring tracks may be merged or associated to wrong tracks, but all generated tracks are reconstructed and no fake tracks are added. This fast simulation tool allows to study track parameter resolution, but not the tracking efficiency. The impact of the background on the resolution of the track impact parameters is shown in Fig. 6.15. In order to address the issue of the pattern recognition capability to reconstruct tracks in the high background environment of Super$B$, SVT detector occupancies estimated in Super$B$ have been compared to those observed in *BABAR*. In particular we compared the cluster occupancy, defined as the detector strip occupancy after applying the time window cut, divided by the hit multiplicity in a cluster. The average cluster occupancy over all layers and sides is estimated to be about 0.4% with nom-

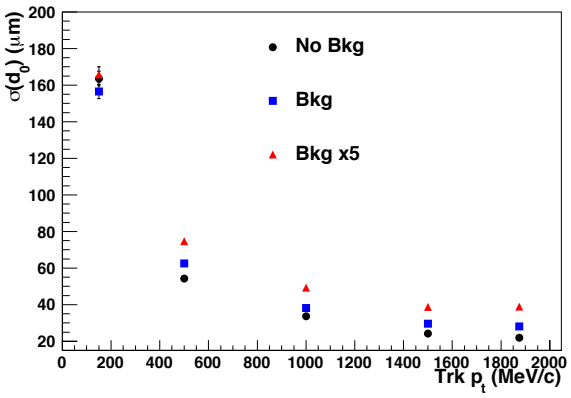

Figure 6.15: Resolution on the impact parameter of the track d_0 as a function of p_t for the Super$B$ detector with Layer0 striplets. The results shown assume no background (points), nominal background (squares) and 5 times the nominal background (triangles).

inal background in Super$B$. This cluster occupancy in Super$B$ is smaller than the maximal value of about 0.7% reached at high luminosity in *BABAR*, thanks to the improved hit time resolution. When considering a scenario with an additional $\times 5$ safety factor on background predictions for Super$B$, the estimated average cluster occupancy is about 2% with nominal peaking-time configuration and about 1.5% with the shortest peaking times in Layer4 and Layer5. *BABAR* studies [11] of SVT performance in high background conditions have been used to estimate the efficiency to assign a hit to a track as a function of the cluster occupancy, that was found to be greater than 95% up to a 3% occupancy [12]. These studies indicate that the pattern recognition should be able to work without major problems also in presence of 5 times the nominal background. Moreover, for low momentum tracks not reaching the DCH, the additional Layer0 measurements should help the pattern recognition when using SVT hits only. Improvements in the pattern recognition algorithm may also be foreseen with respect to what has been used in *BABAR*.

6.3.6 Sensitivity studies for time-dependent analyses

The sensitivity to the physics parameter S has been considered as figure of merit for time-dependent analyses of B^0 decays. Several decay modes have been studied: $B^0 \to \phi K^0_S$, $B^0 \to \pi^+\pi^-$, $B^0 \to J/\psi K^0_S$, $B^0 \to D^+D^-$, but also decay modes such as $B^0 \to K^0_S K^0_S$, $B^0 \to K^0_S\pi^0$ where the impact of the additional Layer0 measurement is less effective due to the presence of neutral and long-lived particles in the final state. The per-event error on the S parameter estimated in Super$B$ with the Fast Simulation is consistent with what is observed with the *BABAR* detector for all decay modes but for $B^0 \to K^0_S K^0_S$ and $B^0 \to K^0_S\pi^0$ decays, where a reduction in sensitivity of about 15% is observed [6, 9]. Only the impact of the Δt resolution on the measurements has been included in the Fast Simulation studies. In particular, possible improvements on the reconstruction efficiency, 95% angular coverage in the CM frame with respect to 91% in *BABAR*, and better flavor tagging performance due to improved particle identification, have not been considered in these studies.

In the case of time-dependent analyses for mixing and CP violation in the neutral D meson system, the determination of the proper time t relies on the measurement of the 3-dimensional flight length ($\vec{L}$) and the momentum $\vec{p}$ of the D^0 according to $t = \frac{\vec{L}\cdot\hat{p}\ M}{|\vec{p}|}$ where M is the D^0 nominal mass. D^0 mesons produced in $e^+e^- \to c\bar{c}$ events gain a natural boost in the reaction. Even though the CM boost is reduced with respect to *BABAR*, the resolution on the D^0 proper time in Super$B$ is about 2 times better [10]. In Fig. 6.16 is reported the distribution of the D^0 proper-time error in Super$B$ and compared with *BABAR*. The average proper-time error is about 0.16 ps in Super$B$ and 0.30 ps in *BABAR* for $D^0 \to K^0_S\pi^+\pi^-$ decays, to be compared with the D^0 lifetime of about 0.41 ps.

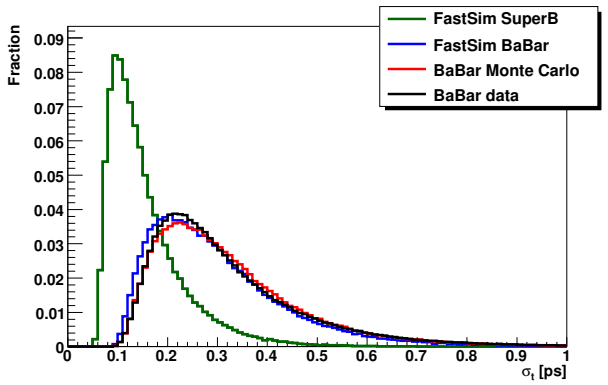

Figure 6.16: D^0 proper-time error distributions obtained with the Super$B$ (green line) and the *BABAR* (blue line) detectors according to Fast Simulation studies. Distributions from *BABAR* Monte Carlo (red line) and data (black line) are also reported in the plot.

The impact of machine background events on the SVT performance has been studied by adding background hits to signal events according to the rates estimated using Full Simulation. Details on the estimates of the machine background events can be found in Section 6.2. Background hits may reduce the hit reconstruction efficiency, increase the effective hit resolution, and reduce the efficiency of pattern recognition for charged tracks, along with the increase of fake tracks. Most of the above effects have been included in our Fast Simulation assuming that the charged track pattern recognition algorithm will work with similar performance to the *BABAR* one, but fake tracks are not simulated. Hit efficiency of the readout chips used in the Fast Simulation studies can be found in Table 6.16 for the case of nominal background and with 5 times the nominal background. In Fig. 6.17 is reported the impact of the machine background events on the physics parameter S for the case of nominal background and with 5 times the nominal background rates. Background hits are rejected if they are not within a time window of $\pm 3\sigma$ ($\pm 5\sigma$) with respect to the time of the event.

The values of the hit time resolution (σ) are reported in Table 6.7. The reduction of the sensitivity to S is quite limited with nominal background ($< 3\%$) and is about 9% (14%) with 5 times the nominal background conditions when applying a $\pm 3\sigma$ ($\pm 5\sigma$) time window cut.

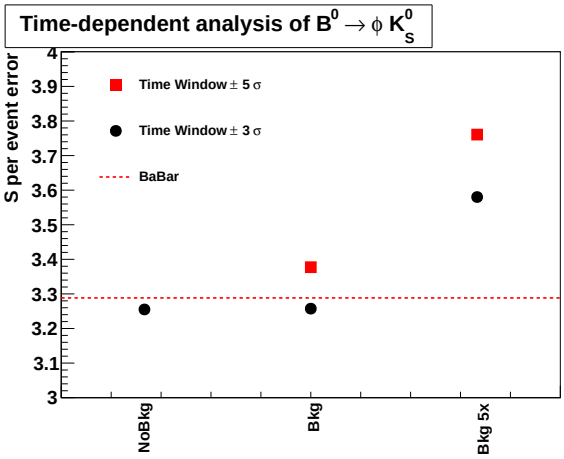

Figure 6.17: Variation of the S per-event error in $B^0 \to \phi K^0_S$ time-dependent analysis in presence of nominal background events and with 5 times the nominal background. A cut on the time of arrival of the hits has been applied at $\pm 3\sigma$ and $\pm 5\sigma$ with respect to the time of the event.

6.3.7 Performance with Layer0 pixel detectors

A Layer0 technology based on a high granularity silicon pixel sensor, *e.g.* with 50×50 μm^2 cell, is considered for an upgrade of the baseline striplets solution. The different Layer0 technology options are described in Sec. 6.8 and are based on hybrid pixels or thin CMOS MAPS. All these solutions adopt a digital sparsified readout with the area of the pixel cell of about $2500 - 3000\,\mu$m^2. The shape of the pixel can be optimized in such a way to reduce the sensor pitch in the z direction and to improve the relative hit resolution while keeping the pixel area constant.

As already discussed in Sec. 6.3.3, the determination of the decay vertex position is driven by the performance of Layer0. The advantage of the Layer0 pixel solution is to guarantee good detector performance also in presence of relatively high background. The detector occupancy, defined as the probability of having a noise hit in the sensitive time window, is about two orders of magnitude lower with respect to the striplets case, taking into account the different detector granularity and resolution on the time of arrival of the hits. Occupancies at the level of $10^{-4} - 10^{-3}$ in a Layer0 pixel detector would correspond to occupancies of $10^{-2} - 10^{-1}$ with the striplets solution, which are about the highest achievable values in the Layer0 striplets at Super$B$. Therefore, the impact of the the background hits on the determination of the decay vertex and of the track impact parameters is moderate at Super$B$ with a Layer0 pixel solution.

Fig. 6.18 shows the sensitivity to the S parameter in time-dependent CP violation analysis of $B \to \phi K^0_S$ decays as a function of the Layer0 radius (r_0 =1.4 and 1.6 cm) and of its material budget ($x/X_0 = 0.1 - 1.0\%$), in case of nominal background and $\times 5$ the nominal background. The dashed line represents the reference value obtained in *BABAR*. Material budget in the range $x/X_0 = 0.35 - 0.50\%$ ($x/X_0 = 0.55 - 0.85\%$) is achievable for a Layer0 pixel solution based on CMOS monolithic active pixel sensors (hybrid pixels) depending on the results of the ongoing R&D activities. The S sensitivity is very similar to the one obtained in *BABAR*. The maximal difference is about 6% (10%) in the worst case considered (including 5 times the nominal background).

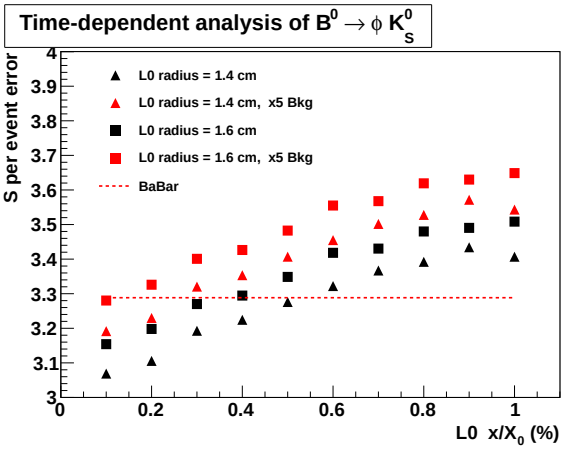

Figure 6.18: S per event error in $B^0 \to \phi K^0_S$ time-dependent analysis for different Layer0 radii (r_0 = 1.4 and 1.6 cm) and material budget ($x/X_0 = 0.1 - 1.0\%$) compared with the reference value of *BABAR* (dashed line). Results in presence of 5 times the nominal background are also reported in the plot.

6.3.8 Particle identification with dE/dx

The measurement of the ToT value by the front-end electronics enables one to obtain the pulse height, and hence the ionization dE/dx in the SVT sensors. The dynamic range of the analog readout is about 10-15 times the value corresponding to minimum ionizing particles, which is sufficient to take advantage of the dE/dx capability of the SVT [13].

Each sensor will provide 2 measurements of dE/dx, one for each sensor side, for a total of 12 dE/dx measurements in the SVT. In *BABAR*, where a total of 10 dE/dx measurements (5 layers) were available, for every track with signals from at least four sensors in the SVT, a 60% truncated mean dE/dx was calculated. The cluster with the smallest dE/dx energy was also removed to reduce sensitivity to electronics noise. For MIPs, it was abtained a resolution on the truncated mean dE/dx of approximately 14%.

The intrinsic smearing from the distribution of the energy deposition in the silicon sensors and from the atomic binding effects in the silicon will dominate the uncertainty on the measured dE/dx [13]. The contribution to the dE/dx uncertainty from the electronic noise should be relatively small. Therefore the resolution on dE/dx for MIPs is expected to be similar to the one achieved in *BABAR*. However,

the dE/dx precision is inversely proportional to the square root of the number of dE/dx samples used for the truncated dE/dx mean calculation [14]. Two additional measurements in the Layer0 should improve the average resolution of a factor $\sqrt{5/6} = 0.9$, where 5 is the average number of dE/dx samples used in *BABAR* and 6 is the expected average number in Super$B$. The e/π separation is expected to be larger than 3σ for momenta lower than 150 MeV/c and will be very useful for rejecting low momentum electrons from background QED processes.

6.4 Silicon Sensors L. Bosisio - 8 pages

Layers 1 to 5 of the SVT will be based on 300 μm thick double-sided silicon strip detectors, with integrated AC-coupling capacitors and polysilicon bias resistors. These devices are a technically mature and conservative solution to the requirements the SVT must meet to provide precise, highly segmented tracking near the interaction point. For the new Layer0, the baseline option also foresees double-sided silicon strip detectors, with short strips ('striplets'), 20 mm long, oriented at ± 45 degrees from the beam direction, fabricated on 200 μm thick substrates. The requirements that the detectors must meet are discussed below.

6.4.1 Requirements

Material budget. To achieve good vertex resolution, it is especially important to minimize the material up to and including the first measurement. This requirement, and the need to provide precise vertexing in both z and $r\phi$ views, leads to the choice of double-sided detectors. For Layers 1 to 5 we plan to use 300 μm thick silicon wafers, which are a standard choice and present acceptable handling properties. For Layer0, given the very stringent limitations on the amount of material, we are forced to go to 200 μm thick substrates.

Efficiency. The silicon detectors must maintain high single-point efficiency in order to achieve the requirements given in Section 6.1 for high overall track reconstruction efficiency. Loss of efficiency can occur from defective sensor strips, from bad interconnections, or from faulty electronics channels. Sensor related inefficiencies can be due to fabrication defects or handling damage, which can result in strips with high leakage currents, poor insulation or broken AC-coupling capacitor. Our goal is to achieve an overall single-detector strip failure rate of less than 1%. The experience gained from from a large production of double-sided AC-coupled detectors for the ALICE Inner Tracking System indicates that a total rate of defective strips below 1% can be achieved with reasonable yield ($> 70\%$).

Resolution. As described in Section 6.1, we require the intrinsic point resolution to be 15 μm or better in both z and ϕ for the inner layers (Table 6.2). These are the point resolutions for tracks at near-normal incidence. As the angle between the track and the plane normal to the strip increases, the resolution initially improves, then degrades. We require the resolution to degrade by no more than a factor of approximately 3 for angles up to 75° from normal incidence.

Radiation hardness. The sensors must hold up to integrated doses of ionizing radiation and to 1 MeV equivalent neutron fluences as reported in table 6.1. This requirement leads to the use of AC-coupled detectors in order to avoid the problems associated with direct coupling of the large leakage currents caused by the irradiation. It also has implications in the choice of the strip biasing scheme, making the punch-through technique unsuitable and limiting the maximum values of the polysilicon resistors.

Another important effect of the irradiation is a change in the effective dopant concentration of the substrate and, as a consequence, on the minimum bias voltage necessary to deplete the sensor and to achieve full collection of the signal charge. An estimate of these effects id given in the next section.

Table 6.8: Physical dimensions, number of strips and pitches for the nine different sensor models. Model VI has a trapezoidal shape.

Sensor Type	0	I	II	III	IVa	IVb	Va	Vb	VI
Dimensions (mm)									
z Length (L)	105.2	111.7	66.4	96.4	114.6	119.8	102.2	106.0	68.0
ϕ Width (W)	15.1	41.3	49.4	71.5	52.8	52.8	52.8	52.8	52.8-43.3
Thickness	0.20	0.30	0.30	0.30	0.30	0.30	0.30	0.30	0.30
PN junction side reads	u	z	z	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ
Strip Pitch (μm)									
z (u for Layer0)	54	50	50	55	105	105	105	105	105
ϕ (v for Layer0)	54	50	55	50	50	50	50	50	50 $\rightarrow$ 41
Readout Pitch (μm)									
z (u for Layer0)	54	100	100	110	210	210	210	210	
ϕ (v for Layer0)	54	50	55	100	100	100	100	100	100 $\rightarrow$ 82
Number of Readout Strips									
z (u for Layer0)	1536	1104	651	865	540	565	481	499	318
ϕ (v for Layer0)	1536	799	874	701	512	512	512	512	512

6.4.2 Sensor design and technology

From the above requirements and from the discussion in Section 6.1, we have arrived at the detector specifications and design parameters described in the following.

Sensor models and sizes. Given the increased module length with respect to the *BABAR* SVT, in order to reduce the insensitive area between adjacent sensors and the complexity of the assembly operations – and to ease the detector alignment task – we seek to minimize the number of sensors making up each SVT module. Taking into account the constraints on the module sizes coming from the overall SVT design (Section 6.1), this goal can be met by designing a specific sensor model for each module type – plus the wedge shaped sensor – and by having the sensors fabricated on 150 mm diameter wafers.
We are thus led to nine different sensor models, whose overall sizes are listed in Table 6.8, together with strip numbers and pitches, to be discussed later.

Although 300 μm thick sensors fabricated on 150 mm substrates are by now an available option from several suppliers, processing the Layer0 double sided sensors on 200 μm thin, 150 mm diameter wafers is a significant challenge, which very few manufacturers are willing to tackle. Unfortunately, while Layers 1-5 could also be assembled from smaller sensors, fitting inside 100 mm wafers, Layer0 sensors require larger wafers. This is due to the requirement to have only one sensor per Layer0 module, which in turn is dictated by the need to minimize insensitive regions and mechanical support structures, and also by limitations on the available number of readout channels. These difficulties are mitigated by the very small number of Layer0 sensors required and the fact that five of them can comfortably fit into a single 150 mm wafer. Because of this, a lower fabrication and assembly yield can be tolerated for Layer0 sensors.

Fabrication technology. The microstrip sensors will be fabricated on n-type wafers, with p^+ strips on the junction side and n^+ strips on the ohmic side, insulated by patterned p^+ implants (p-stops) in between, or by a uniform p-type implant (p-spray). The strips will be AC-coupled,

Table 6.9: Values for the total 1 MeV neutron equivalent fluence Φ_{tot}, effective dopant concentration N_{eff} and total depletion voltage V_{td} after 7.5 years at nominal radiation load, without and with the the 5× safety factor. For all Layers the initial (pre-irradiation) resistivity was assumed to be 7 kΩ cm, corresponding to a donor concentration $N_d = 6.3 \times 10^{11}$ cm^{-3}.

		Nominal radiation load in 7.5 years			With 5× safety factor included		
	Pre-Irrad. V_{td}(V)	Φ_{tot} (cm^{-2})	Post-Irrad. N_{eff} (cm^{-3})	Post-Irrad. V_{td}(V)	5×Φ_{tot} (cm^{-2})	Post-Irrad. N_{eff} (cm^{-3})	Post-Irrad. V_{td}(V)
Layer0	19	2.7 10^{13}	–1.3 10^{12}	40	1.4 10^{14}	–7.3 10^{12}	220
Layer1	44	5.9 10^{12}	–6.4 10^{10}	4.4	3.0 10^{13}	–1.4 10^{12}	100
Layer2	44	3.8 10^{12}	+1.2 10^{11}	8.1	1.9 10^{13}	–8.7 10^{11}	60
Layer3	44	2.3 10^{12}	+2.9 10^{11}	20	1.1 10^{13}	–4.2 10^{11}	29
Layer4	44	1.5 10^{12}	+3.9 10^{11}	27	7.5 10^{12}	–1.8 10^{11}	12
Layer5	44	1.3 10^{12}	+4.1 10^{11}	29	6.6 10^{12}	–1.2 10^{11}	8.0

with integrated capacitors and polysilicon bias resistors. The alternative biasing method, exploiting the punch-through effect, does not offer adequate radiation tolerance.
This has proven to be a mature, reliable technology, requiring no R&D.

Substrate resistivity and depletion voltages. The wafer resistivity is assumed to be in the range 6–8 kΩ cm, corresponding to a depletion voltage of 50–38 V for 300 μm thick sensors. These values seem to be a reasonable compromise between the need to limit the initial depletion voltage and peak electric fields on one hand, and on the other hand the desire to delay the onset of type inversion due to radiation damage.

In fact, the relatively high radiation levels expected will cause a significant displacement damage in the substrate.

The expected 1 MeV neutron equivalent fluences over 7.5 years of operation at nominal luminosity, both without and with an additional safety factor of 5, are reported in Table 6.9 for the various layers, together with the effective dopant concentration N_{eff} and the total depletion voltage V_{td} expected at the end of the irradiation period. For all Layers the initial (pre-irradiation) resistivity was assumed to be 7 kΩ cm, corresponding to a donor concentration $N_d = 6.3 \times 10^{11}$ cm^{-3} and to a total depletion voltage of 19 V for the 200 μm thick Layer0 sensors and 44 V for the 300 μm thick sensors of the other layers. The changes in effective dopant concentration have been predicted using the model and the data given in [16, 17]. Due to the long exposure time, the damage component undergoing short-therm anneal has been neglected; the reverse anneal component has been estimated taking into account, for each operation year, the remaining time until the end of the 7.5 year operation period. A temperature of 20 °C has been assumed. Although the possibility of cooling the SVT sensors to lower temperatures (in the range 8-12 °C) is being evaluated for the purpose of reducing the leakage current, the beneficial effect on the reverse annealing would not be very significant, considering also the fact that the detector would in any case stay at room temperature for extended periods.
With the 5× factor included, the resulting final depletion voltage is still comfortable (below 100 V), except for the Layer0 sensors, for which it would reach 220 V. While this is not an unbearable value, it must be kept in mind that the Layer0 is designed to be replaceable and that the striplet detectors are foreseen to be superseded by pixels in the later part of the Super$B$ operation.

Table 6.10: Estimated strip capacitance and series resistance for the different sensor models.

Detector Model	z readout side (u for model 0)			ϕ readout side (v for model 0)		
	C_{strip}/ℓ (pF/cm)	C_{AC}/ℓ (pF/cm)	R_{series}/ℓ (Ω/cm)	C_{strip}/ℓ (pF/cm)	C_{AC}/ℓ (pF/cm)	R_{series}/ℓ (Ω/cm)
0	2.5	40	9	2.5	30	14
I	1.7	40	5	2.5	30	9
II	1.7	40	4	2.5	30	7
III	1.7	30	7	1.7	40	4
IVa,IVb,Va,Vb	1.7	60	3	1.7	40	4
VI	1.7	60	3	1.7	30	4.5

Table 6.11: Total 1 MeV neutron equivalent fluence Φ_{tot} for the different layers and maximum leakage current I_{leak} for ϕ and z-side strips of a module, after 7.5 years at nominal radiation load, without and with the 5× safety factor. A temperature of 20 °C is assumed.

	Nominal radiation load in 7.5 years			With 5× safety factor included		
	Φ_{tot} (cm^{-2})	ϕ strips I_{leak} (μA)	z strips I_{leak} (μA)	$5\times\Phi_{tot}$ (cm^{-2})	ϕ strips I_{leak} (μA)	z strips I_{leak} (μA)
Layer0	$2.7\ 10^{13}$	0.15	0.15	$1.4\ 10^{14}$	0.75	0.75
Layer1	$5.9\ 10^{12}$	0.28	0.40	$3.0\ 10^{13}$	1.4	2.0
Layer2	$3.8\ 10^{12}$	0.23	0.31	$1.9\ 10^{13}$	1.2	1.6
Layer3	$2.3\ 10^{12}$	0.37	0.30	$1.1\ 10^{13}$	1.8	1.5
Layer4	$1.5\ 10^{12}$	0.39	0.41	$7.5\ 10^{12}$	1.9	2.0
Layer5	$1.3\ 10^{12}$	0.43	0.36	$6.6\ 10^{12}$	2.1	1.8

Configuration of z and ϕ readout strips. The choices regarding the strip readout pitch and which side of the detector (junction or ohmic) should read which coordinate (z or ϕ) largely follow those adopted for the *BABAR* SVT.

At equal pitch, the strip capacitance and, consequently, its noise contribution is somewhat smaller on the junction side than on the ohmic side. Furthermore, the series resistance of the metal strip can be made lower, because the absence of p-stops leaves room for a wider metal readout strip. For these reasons, and because the z vertex measurement is more important from the point of view of physics, we use the junction side for the z strips on the inner Layers 1 and 2 (in Layer0 the two sides read equivalent coordinates, oriented at ±45° from the beam direction). The slightly better performance of the junction side also helps compensate for the additional resistance and capacitance imposed by the longer z fanout circuit.

The choice of the strip pitch is influenced by many factors, such as the number of available readout channels, the strip capacitance, series resistance and leakage current, the limited area available for the bias resistors, the need to maintain a large enough signal from angled tracks. Profiting from the optimization work made for the *BABAR* SVT, and the experience gained from its operation, the following choices have been made:

Table 6.12: Number of the different sensor types per module, area of the installed sensors, number of installed sensors and number of sensors including spares. Spare sensors include one spare module per module type (two for Layer0), plus additional sensors accounting for possible losses during the whole SVT assembly process.

Sensor Type	0	I	II	III	IVa	IVb	Va	Vb	VI	All
Layer0	1	-	-	-	-	-	-	-	-	1
Layer1	-	2	-	-	-	-	-	-	-	2
Layer2	-	-	4	-	-	-	-	-	-	4
Layer3	-	-	-	4	-	-	-	-		4
Layer4a	-	-	-	-	4	-	-	-	2	6
Layer4b	-	-	-	-	-	4	-	-	2	6
Layer5a	-	-	-	-	-	-	6	-	2	8
Layer5b	-	-	-	-	-	-	-	6	2	8
Silicon Area (m^2)	0.013	0.055	0.079	0.167	0.194	0.203	0.291	0.302	0.222	1.52
Nr. of Sensors	8	12	24	24	32	32	54	54	68	308
Nr. Including Spares	20	20	40	35	44	44	72	72	92	439

- both sides of Layer0 are read by strips at 54 μm pitch, without intermediate floating strips;
- the z-side of Layers 1, 2 is read by p-type strips at 100 μm pitch with one intermediate floating strip;
- the z-side of Layer3 is read by n-type strips at 110 μm pitch with one intermediate floating strip;
- the z-side of Layers 4, 5 is read by n-type strips at 210 μm pitch with one intermediate floating strip;
- the ϕ-side of Layer1 is read by n-type strips at 50 μm pitch without intermediate floating strips;
- the ϕ-side of Layer2 is read by n-type strips at 55 μm pitch without intermediate floating strips;
- the ϕ-side of Layers 3, 4, 5 is read by p-type strips at 100 μm pitch with one intermediate floating strip.

The strip pitches and the resulting numbers of strips for the various sensor models are listed in Table 6.8.

Strip capacitance and resistance. Important strip parameters are the capacitance, the resistance and the leakage current, all of which are proportional to the strip length ℓ. For long strips, as will be those of the SVT, the noise contribution of the strip resistance becomes more important, because it is proportional to the the square root of the resistance multiplied by the strip capacitance. This gives an $\ell^{3/2}$ dependence on the strip length, to be compared with an ℓ^1 dependence for the noise contribution of the strip capacitance and an $\ell^{1/2}$ dependence for that of the leakage current. In order to reduce the series resistance of the strips, we plan to increase the thickness of the aluminum metallization beyond the standard value of ~ 1 μm.

Table 6.10 reports the expected values for the total strip capacitance – as deduced from measurements on *BABAR* sensors and other strip sensors – and for the strip series resistance, as calculated from the design width of the strips and a metallization thickness of 2.5 μm.

Table 6.13: List of different mask sets for 150 mm wafers, specifying the content of each wafer layout, the minimum value of the distance between the sensors and the wafer edge, the number of wafers required for each design and the total number of wafers. The numbers quoted include the spare sensors, but not the fabrication yield.

Mask Design	Wafer content	Min. Clearance to Wafer Edge (mm)	Number of Wafers
A	5×Mod 0	10.2	5
B	Mod I + Mod VI	8.2	20
C	Mod III	15.0	35
D	Mod IVa	11.9	44
E	Mod IVb	9.5	44
F	Mod Va + Mod VI	9.8	72
G	Mod Vb + Mod II	6.9	72
Total			287

Strip leakage current. Strip leakage current after the first year of operation will be dominated by carrier generation at radiation-induced defects. Table 6.11 reports the total 1 MeV neutron equivalent fluence for the different layers and the maximum leakage current expected for ϕ and z-side strips, after 7.5 years at nominal radiation load, without and with the 5× safety factor. Because of the long irradiation time, spanning 7.5 years, the currents are calculated taking into account the effect of the annealing, by assuming a current damage coefficient $\alpha = 2.8\times10^{-17}$ A/cm. The values reported in the table refer to a module strip, composed of a few sensor strips daisy-chained together into a readout channel, by direct bonding on ϕ-side and by fanout circuits on z-side. For the z-side, different numbers of strips (up to three) can be connected together to a readout channel within the same module; in this case the table reports are the maximum value of the current.

AC coupling capacitors. The strips are connected to the preamplifiers through a decoupling capacitor, integrated on the detector by interposing a dielectric layer between the p or n-doped strip and the metal strip. AC coupling prevents the amplifier from integrating the leakage current with the signal; handling the high leakage currents due to radiation damage imposes an additional heavy burden on the preamplifier design. On each sensor, the value of the decoupling capacitance must be much larger than the total strip capacitance on the same sensor, a requirement which is easily met by the current fabrication technologies.

Bias resistors. The bias resistors values will range between 1 and 8 MΩ, depending on the layer and the detector side. The choice of the R_B value is constrained by two requirements. A lower limit is determined by the need to limit the noise contribution, which has a $\sqrt{\tau/R_B}$ dependence, and if several strips are ganged together the effective resistance is correspondingly decreased. The requirement that, for floating strips, the product $R_B \cdot C_{TOT}$ must be much larger than the amplifier peaking time in order to allow for capacitive charge partition is fulfilled with ample margin for any reasonable values of R_B. An upper limit to R_B is dictated by the allowable potential drop due to the strip leakage current, which depends mainly on the irradiation level and decreases going from inner to outer layers. The maximum resistance value is also limited in practice by the need to limit the area occupied on the wafer. Values of 40 kΩ/square for the sheet resistance of polysilicon can be comfortably achieved with sufficient reproducibility. Thus, it is possible to fabricate

a 10 MΩ resistor with a 6 μm-wide, 1500 μm-long polysilicon resistor. With a suitable shaping of the polysilicon line, the space required by the resistor will be less than 200 μm at 100 μm pitch (corresponding to strips at 50 μm pitch with resistors placed at alternate ends). A final requirement is that the bias resistance be sufficiently stable against the expected radiation exposure, a condition that is easily satisfied by polysilicon resistors.

Edge region and active area. Considering the space needed to accommodate the biasing resistors and to prevent the depletion region from reaching the cut edge, we specify the active region of the detectors to be 1.4 mm smaller than the physical dimensions, that is, the dead region along each edge has to be no more than 700 μm wide. This is the same specification chosen for the *BABAR* strip detectors and, although stricter than adopted by most silicon sensor designs, has proven to be feasible without difficulty, thanks to the choice of placing the polysilicon resistors in the edge region outside the guard ring. For Layer0 sensors, which have a reduced thickness of 200 μm and smaller value, shorter bias resistors, we specify a 600 μm wide inactive edge region.

6.4.3 z-side strip connection options

On z-side, the readout pitch is set to 100 μm in Layers 1 and 2, 110 μm in Layer3 and 210 μm in Layers 4 and 5, with a 'floating' strip in between, to improve spatial resolution for particle tracks with large incidence angles. Since the number of readout strips exceeds the number of available electronic channels, it is necessary to 'gang' together up to three (depending on the SVT layer) strips. The 'ganging' scheme – adopted in the *BABAR* SVT – connects two or three far apart strips to the same readout channel (Fig. 6.22), thus preserving the strip pitch at the expense of a higher capacitance and series resistance (resulting in higher noise), plus ambiguities in the hit position.
For tracks at small θ angles with respect to the beam direction (that is, large incidence angles on the sensor), the signal-to-noise ratio is further degraded by the fact that a track traverses several z-strips (up to nine in the inner layers) and the signal becomes approximately proportional to the strip readout pitch (only 1/3 the wafer thickness in Layers 1 to 3). This suggest adopting an alternative connection scheme, in which two (or more, at large incidence angles) *adjacent* strips are bonded to a single fanout trace, effectively increasing the strip pitch and the signal into a readout channel, with a less than proportional increase in capacitance, and no increase in series resistance. We call this connection scheme 'pairing'.
At small θ angles, this gives better S/N and, consequently, higher detection efficiency when compared to individually connected strips. The improvement is even more important in comparison to the 'ganging' scheme, where the strip capacitance is proportional to the number of strips ganged together, but the signal remains that of a single strip. Moreover, for paired strips also the fanout capacitance and resistance can be made lower, because of the larger trace pitch.
Due to the lower noise, at small θ angles pairing is also expected to give better spatial resolution with respect to ganging. In order to avoid a significant increase of the input capacitance, pairing will be made between the 'readout' strips (at 100 μm pitch) so that a 'floating' strip is always present *between* two adjacent groups of paired strips. However, we are evaluating the option of connecting also the intermediate (otherwise floating) strips *within* a group of paired strips.

Strip capacitance measurements performed on test sensors [21] confirm that pairing yields significantly lower capacitance with respect to ganging the same number of strips; the advantage in capacitance of pairing with respect to ganging increases for higher pairing/ganging multiplicity. The additional increase in total capacitance when connecting also the intermediate strips is $4-5\%$ on p-side, $\sim 6\%$ on n-side. In front of this, a better charge collection efficiency is expected.

For Layers 1-3 the combination of track incidence angles and strip pitch is such that all strips can be connected to the available readout

channels using a pairing-only scheme. For Layers 4-5, in part because of the presence of the wedge sensors and in part because of the larger ratio of strip to channel numbers, it is necessary to adopt a combined pairing/ganging scheme, as indicated in Table 6.2.

6.4.4 Wafer layout and quantities

Table 6.12 reports the sensor composition of the different detector modules, the number of installed sensors of each type, with the corresponding silicon areas, and the total numbers of sensors including spares. Spare sensors account for one spare module of each type (two for Layer0), plus an additional 20% to compensate for possible losses during the assembly process. We see that the current design employs nine different types of sensors, for a total of 308 installed sensors covering 1.52 m^2. Using 150 mm diameter wafers and a dedicated sensor model for each module type allows to cover the ~ 1.5 times larger area with a smaller number of sensors with respect to *BABAR*, at the expense of having nine different models of sensors. However, through optimized usage of the wafer area it is possible to accommodate all nine sensor types in seven different wafer layouts, i.e. seven mask sets, and to fabricate all 439 sensors (spares included) on 287 wafers. This is illustrated in Table 6.13.

6.4.5 Prototyping and tests

Although both the design and the technology of double-sided microstrip sensors are well developed, and the Super*B* SVT is a direct evolution of the proven *BABAR* design, some specific aspects need to be tested on prototypes before starting the sensor production.

Prototypes of the striplet sensors for Layer0, absent in *BABAR*, have been thoroughly tested on beam at CERN in 2008 and 2011 [22, 23], showing adequate performance for use in the Super*B* SVT.

Additional tests will be required to to check the performance of sensors irradiated up to the maximum levels expected at the Super*B* which, although much lower than those relevant for LHC detectors, significantly exceed the radiation load experienced in *BABAR*. We plan to irradiate with neutrons and/or charged particles existing prototype sensors of design similar to the one foreseen for the SVT and also some spare modules remaining from the *BABAR* production.

At least one small batch of dedicated prototype sensors will be ordered and qualified before issuing the tender for the sensor supply. Given the quite different demands posed by processing double sided sensors on thin 150 mm diameter substrates, and the very small number of wafers required, fabrication of striplet sensors for Layer0 could likely be awarded to a company different from the one supplying the other sensors. Because of their special characteristics and their fragility the striplet sensors will also follow a different, dedicated testing procedure.

A limited number of pre-series sensors will be qualified by a full electrical test at the probe station before releasing the series production. Testing double-sided sensors with automatic loading from a cassette, besides requiring a very specialized custom-made prober, would not allow sufficient flexibility for testing the many different sensor sizes equipping the SVT. The experience gained from testing *BABAR* sensors and, more recently, those for the ALICE experiment [24] shows that the routine parametric test of a double-sided sensor can be performed in about two hours using a semiautomatic probe station, with manual mounting and positioning of the sensors on dedicated support jigs designed and made in house. The time increases, of course, if some peculiar results of the test require additional dedicated measurements.

The number and the detailed characteristics of the measurements that will be included in the routine acceptance test of production sensors will depend on the results of the tests themselves. Starting from a full test on the first batches, it is possible that the set of parameters tested could be reduced if the quality and consistency of the measured characteristics will advise to do so.

Overall, based on past experience, we estimate that the testing of all production sensors

will take about one year if performed at a single location.

6.5 Fanout Circuits L.Vitale - M.Prest2+2 pages

The routing of the signals from the silicon sensors to the HDIs is performed by the so-called *fanout circuits*; they consist in flexible circuits that bring the signals to the end of the detector module (where they are wire bonded) to the front-end electronics IC (located a few tens of centimeters from the IP).

The fanouts for the ϕ and z coordinates are designed to minimize the material crossed by the particle within the angular acceptance. However, while the ϕ fanout circuts are just one-to-one connections, the z ones are more complicated since they cover the full length of the detector modules (up to $\sim$40 cm for the outer layers) and have to provide the interconnection (ganging or pairing) where the number of readout strips exceeds the available readout channels.

In the following sections the details about the chosen technology and the geometrical and electrical properties of the fanout circuits are described; the layer 0 fanout will be analyzed in a dedicated section.

6.5.1 Fanouts for Layer0

The fanout circuit for the innermost layer of the SVT vertex detector is part of the striplet module and it is shown in Fig. 6.5. The complex shape of this passive circuit derives from the geometry of the vertex detector. The Layer0 sensor is tightly surrounded by the other layers of the vertex as shown in Fig. 6.2 and Fig. 6.4. From the mechanical model of the vertex detector it can be shown that the clearances between two adjacent detector layers are not constant along the longitudinal axes. They generally have a minimum in the center of the detector and increase slightly moving away from the center. Such geometries have been studied for each layer and the shape of the fanout maximizes the area available for the circuits avoiding mechanical interferences between the modules. The resulting outline of the Layer0 fanout is shown in Fig. 6.19. The minimum width of the circuit is 29 mm while the overall length is approximately 300 mm. To one detector corresponds one fanout. Half of the strips (768) are read from each side of the circuit.

6.5.1.1 Requirements and Technology

Due to the size, the number of lines and the dimension of the fanout, the requirement of reducing to a minimum the radiation length of each component of the striplet module affects the choice of the technology as well as the line pitch to be used in the design. The technology proposed for the Super$B$ fanout is similar to the one used in the past for the *BABAR* fanouts. The base material is 50 μm polyimide with metal directly deposited on the dielectric, 5 μm of copper or 10 μm aluminum. The direct deposition of the metal on the polyimide improves the manufacturability of the circuit. The maximum trace resolutions for copper or aluminum are different and depend also from the technique used to impress the photoresist that defines the pattern to be etched. Moreover, the maximum trace resolution depends also from the length of the lines to be etched. Typically, with the present best technology available, the minimum line width/space is about 15/15 μm for the copper and approximately 65/65 μm for the aluminum on short traces (up to few centimeters), being on the contrary up to 20/20 μm for copper and 70/70 μm for aluminium on long traces (up to tens of centimeters). The pitch was verified on prototypes. The use of aluminum instead of copper has the advantage to reduce significantly the radiation length of the fanout and represent a novelty to be pursued even if a larger fanout is needed to accomodate the same numbers of connections.

A two layer fanout design has been preferred to a single layer solution for the following reasons:

- the orientation of the sensor strips at $\pm$45 degrees from the beam axis and the aspect ratio of the circuit, long and narrow, re-

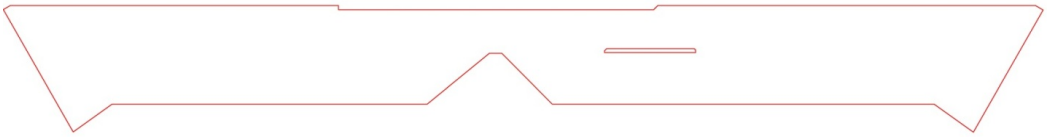

Figure 6.19: Layer0 fanout outline. *(Insert a ruler in the picture)*

quires that the strips are read out from the two long sides of the detector to contain the width of the circuit within the 29 mm;

- the minimum line width/space is approximately 68/68 μm for a two layer solution, while is of the order of 20/20 μm for the single layer one. The former is a standard consolidated solution at least for a copper fanout, while the latter is up to the present technology limit over the length of the Layer0 fanout (300 mm);
- the Layer0 fanout has to be partially bended to be installed in the detector, as shown in Fig. 6.39. The bending takes place outside the sensor area and close to the region where the circuit width increases in a funnel like shape. Having 68 μm lines instead of a $\sim$ 20 μm lines increase reliability;
- the two layer fanout can be made either in copper or in aluminum. The aluminum solution has not been realized before and therefore has to be considered as an R&D effort;
- the length of the fanout does not present any particular technology challenge.

6.5.1.2 Design

The CAD drawing of the module and the layout one of the two layers of the fanout is shown in Fig. 6.20 and Fig. 6.21. The stack up of the fanout is reported in Table 6.14.

From the figures it can be noticed that a cut-out, 1 mm wide, is needed in the central area of each layer to bond some of the strip and at

Table 6.14: Material breakdown of Layer0 fanout, surface coverage and equivalent radiation length x/X_0. The coverage of the surface area is very small for gold since it is present on pad only.

Material	Thickness (μm)	Coverage	x/X_0 (%)
Kapton	50	1	0.017
Cu (Al)	5 (10)	0.5	0.018 (0.006)
Glue	10	1	0.003
Kapton	50	1	0.017
Cu (Al)	5 (10)	0.5	0.018 (0.006)
Au	1.5	$\leq 10^{-2}$	≤ 0.001
Total	120 (130)		0.073 (0.049)

the same time route properly the traces without violating the 68 μm pitch rules. The traces are also tapered and bended at the extremities of the layout to match the pitch of the front end electronics pad to which the fanout lines are wire bonded. Only in the pad region, the layer is gold plated (1.5 μm) for bonding. This solution has been adopted to minimize the radiation length of the assembly. The relaxed 68 μm pitch should result in a simulated crosstalk of about 1% on adjacent traces of the same layer.

Each layer can be individually manufactured, tested and qualified before assembly. After an initial optical inspection of defects, a "bed of nail" test will be performed to measure the electrical characteristics of each trace of the circuit. Only defect-free layers will be glued together to build the two layer fanout assembly. Repairs of defective layer are not foreseen at the moment. The small number of fanout to be produced, 16

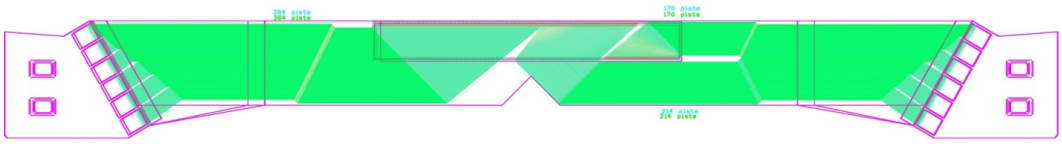

Figure 6.20: CAD drawing of the Layer0 module. *(Insert a ruler in the picture)*

Figure 6.21: Layout of the Layer0 fanout. *(Insert a ruler in the picture)*

pieces, justifies the request of having 100% or more redundancy during production. Moreover the copper solution does not represent a real technological challenge and so it is considered the baseline solution until the aluminum solution is proved feasible and reliable.

6.5.1.3 Prototyping and tests

All fanout assembly will be tested against short and opening. Each trace will be measured in term of resistance and capacitance to the neighbor trace and the date saved for further analysis. No repairs are forecast on the fanout. A first batch of prototypes is in production at the CERN PCB facility. They have the previously shown layout and will be used not only to validate the design and the test procedure but also will be used for mechanical assembly of the striplet modules.

6.5.2 Fanouts for outer layers

6.5.2.1 Requirements

The geometrical requirements will be fixed by the detector designs. From the technological point of view, the design requires a typical line width-space of 45 μm-45 μm and a small region of 15 μm-15 μm. This region is 1.5 mm long and around 6 mm wide and corresponds to the bonding area. No constraints are present on the fanout length given the same machines used for the micropattern gas detector production will be used.

6.5.2.2 Material and production technique

The BaBar fanouts were produced on 50 μm Upilex (by UBE) with a deposit of 150 nm of Cr, 4.5 μm of copper followed by a layer of 150 nm of Cr and 1.5 μm of amorphous gold. The SuperB SVT fanouts will be produced on a similar material by UBE (50 μm of polyimide with 5 μm of copper directly deposited on the base material) which should ensure less defects and thus a better yield. This material will be tested in the prototype phase. The old Upilex is anyway still available if the new material would prove not adequate.

A new technique for the production will be implemented in order to reduce the production times. In the BaBar production line, the photoresist was impressed through a mask after its being deposited on the Upilex requiring to work in a clean room. For SuperB, the idea is to impress the photoresist directly with a laser; this means the photoresist is solid and allows to complete the procedure in a much faster way. This

technique has already been tested on the same pitches foreseen for the SVT fanouts.

The increase in the production speed allows to repeat the production of pieces with defects without delaying the SVT assembly. All the pieces will be gold plated with 1.5 μm of amorphous gold for the bonding.

6.5.2.3 Design

The design will follow the same rules of the BaBar fanouts adapting it to the different length of the modules. Differently from the BaBar pieces, no test-tree is foreseen (see next section). To allow the gold plating, all the lines will be shorted. A suitable cutting device will be developed to cut the shorting line after the visual inspection.

Table 6.15 summarizes the geometrical parameters[1] as well as the number of readout strips and channels, the typical pitch and the total number of required circuits per layer and type.

Fig. 6.22 presents a sketch of the ganging principle proposed for the design of layers z 3-4-5.

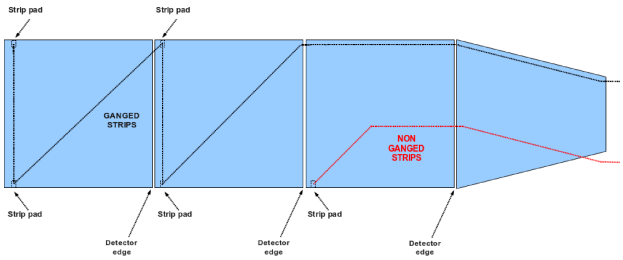

Figure 6.22: Schematic view of two z strips ganged through the fanout circuit.

6.5.2.4 Tests and prototyping

All the fanouts will be automatically optically checked by a dedicated machine which will use the gerber files of the fanouts to find shorts or open lines. The machine can work with 25 μm lines; the region with smaller lines (15 μm with a 15 μm space) will have to be controlled manually.

[1] The fanouts dimensions have been taken from the SVT Mechanics talk presented at the 4^{th} SuperB Collaboration Meeting (June 2012, La Biodola - Elba IT).

Given the much shorter time needed for the production, no correction is foreseen for shorts or open lines; the damaged pieces will be produced again. On the other hand, if a short is present in the larger pitch region, the same correction procedure used for BaBar (involving the use of a microprobe) can be implemented.

As far as the tests are concerned, a batch of fanouts will be produced starting from the BaBar design to check the whole production and test chain. These fanouts in principle can be used with working detectors to test also the assembly procedures.

Figure 6.23 shows the design of a z fanout prototype of layer 3. These prototypes were also used to measure the typical capacitance and resistance. A first measurement of these parameters has been performed on the first batch of prototypes: a value of C/l ~0.6 pF/cm and of R/l ~1.2 Ω/cm has been found.

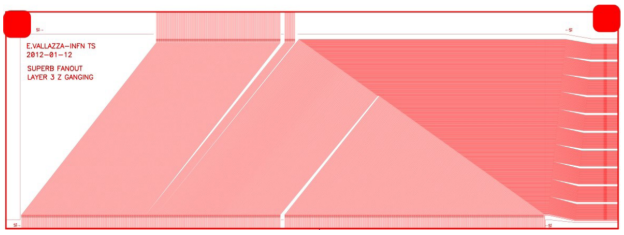

Figure 6.23: Design of a z fanout prototype of layer 3.

Figures 6.24 and 6.25 show a picture of the prototype of the layer 3 z and a step of the cutting procedure.

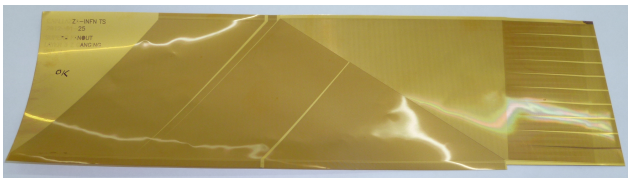

Figure 6.24: Picture of the prototype of the layer 3 z.

Table 6.15: Summary of fanout circuit characteristics.

Layer	Fanout Type	Length (mm)		Number of Readout		Typical Pitch at (μm)		Number of Circuits
		Left	Right	Strips	Channels	Input	Output	
1	z	216.76	217.52	1104	896	100	45	12
	ϕ	105.60	105.82	799	896	50	45	12
2	z	209.00	208.80	1302	896	100	45	12
	ϕ	76.20	76.00	874	896	55	45	12
3	z	250.26	246.26	1730	1280	110	45	12
	ϕ	54.76	53.46	701	1280	100	45	12
4a	z	332.91	328.60	1398	640	210	45	16
	ϕ	35.71	31.40	512	640	82	45	16
4b	z	332.15	327.97	1448	640	210	45	16
	ϕ	24.55	20.37	512	640	82	45	16
5a	z	407.13	411.40	1761	640	210	45	18
	ϕ	32.53	36.80	512	640	82	45	18
5b	z	406.63	411.00	1815	640	210	45	18
	ϕ	20.63	25.00	512	640	82	45	18

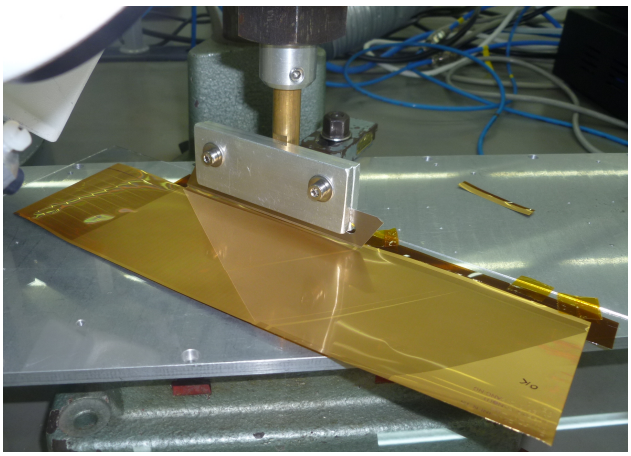

Figure 6.25: Picture of the prototype of the layer 3 z during the cutting procedure.

6.6 Electronics Readout

The SVT electronics chain consists of various separate hardware components. Starting from the detector and going to the ROM boards, the chain contains: a) the readout chips mounted on an HDI placed at the end of the sensor modules; b) wire connections to a transition card (signals in both directions and power lines); c) a transition card, placed about 50-70 cm from the end of the sensors, hosting the wire-to-optical conversion; d) a bidirectional optical line running above 1 Gbit/s; e) a receiver programmable board (front-end board: FEB). A sketch of the full data chain is given in Fig.6.26

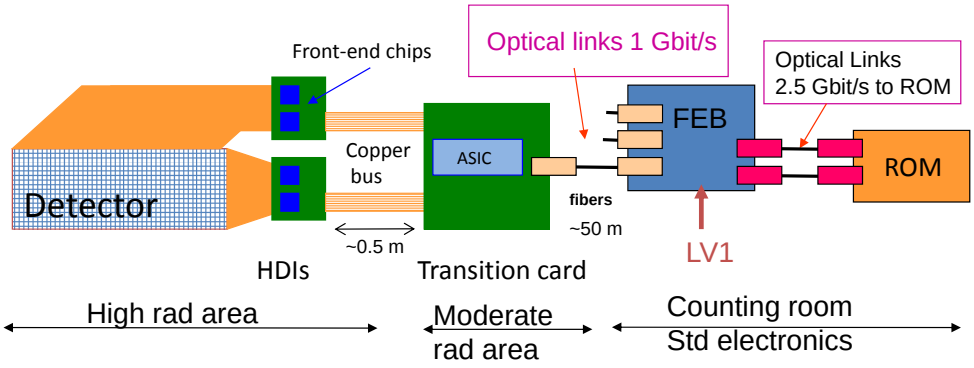

Figure 6.26: Schematic drawing of the full SVT data chain

6.6.1 Readout chips for Strip and Striplet Detectors

The front-end processing of the signals from the silicon strip detectors will be performed by custom-designed ICs mounted on hybrid circuits that distribute power and signals, and thermally interface the ICs to the cooling system. As discussed below, the very different features of inner (Layer 0-3) and outer layers (4 and 5) of the SVT set divergent requirements to the readout chip, which makes it necessary to include programmable features in the readout ICs, in order to adjust operating parameters over a wide range. This obviously holds also in the case a different technology (pixels) is adopted for Layer 0 instead of short strips (striplets). Generally speaking, the ICs will consist of 128 channels, each connected to a detector strip. The signals from the strips, after amplification and shaping will be compared to a preset threshold. If a signal exceeding the threshold is detected, a 4 bit analog information about the signal amplitude will be provided with the Time Over Threshold technique. The analog information is useful for position interpolation, time walk correction, dE/dx measurements, as well as for calibration and monitoring purpose. The dimensions of the readout IC are expected to be about $6{\times}4$ mm^2. As discussed in the SVT HDI subsection of this TDR, the dimensions of the HDI set a 6 mm upper limit on the side of the chip with the bonding pads for the interconnection with the strip sensors. The power dissipation will be below 4 mW/channel including both analog and digital sections. For each channel with a signal above threshold, the strip number, the amplitude information, the chip identification number and the related time stamp will be stored inside the chip waiting for a trigger signal for a time corresponding to the trigger latency (about 6 μs, with 150 kHz trigger rate). When a trigger is received, data will be read out and transmitted off chip, otherwise they will be discarded. The data output from the microstrip detector will be sparsified, i.e. will consist only of those channels generating a hit. The readout integrated circuits must remain functional up to 5 times nominal background.

The option of operating in a data push fashion could be preserved for the external layers, where this will be allowed by the low strip hit rate. This will give the possibility to feed data from these layers to the trigger system.

6.6.2 Readout chips requirements

The microstrip electronics must ensure that the detector system operates with adequate efficiency, but also must be robust and easy to test, and must facilitate testing and monitoring of the microstrip sensors. AC coupling is assumed between the strips and the readout electronics.

- **Mechanical Requirements:**
  Number of channels per chip: 128
  Chip size: width $\leq$6 mm, length $\leq$4 mm

Pitch of input bonding pads: <45 μm

- **Operational Requirements:** Operating temperature: <40 °C
  Radiation tolerance: >3 Mrad/year, >5·10^{12} n_{eq}/cm^2/year (these are the expected values in Layer 0; in outer layers, radiation levels are at least one order of magnitude lower)
  Power dissipation: <4 mW/channel
  Detector and fanout capacitance: 10 pF $\leq C_D \leq$ 70 pF (the chip must be stable when sensor strips are disconnected from the input pads of the analog channels)

- **Dynamic range:** The front-end chips must accept signals from either P and N-side of the strip detectors. A linear response of the analog processing section is required from a minimum input charge corresponding to 0.2 MIP up to a full dynamic range of 10-15 MIP charge for dE/dx measurements.

- **Analog Resolution:** The front-end chips have to provide analog information about the charge collected by the detector, which will be also used for calibrating and monitoring the system. A resolution of 0.2 MIP charge is required for dE/dx measurements. In case of a compression-type ADC, based on the time-over-threshold technique (ToT), this may translate in 4 bits of information.

- **Efficiency:** At design luminosity, the microstrip readout must have a hit efficiency of at least 85% during its entire operational lifetime. This includes any loss of data by readout electronics or readout dead time.

- **Readout bandwidth:** Data coming out of the chip will be substantially reduced by operating in a triggered mode. The chips can use up to 2 output LVDS lines with 180 MHz clock, as it is needed to handle the higher data throughput in inner SVT layers.

- **Radiation Tolerance:** All the components of the microstrip readout system must remain operational over the entire lifetime of the experiment, including a safety factor of 5 on the nominal background expected, this corresponding to 7.5×5 years at nominal peak luminosity of 10^{36}.

  up to 10 years of SuperB running at the nominal luminosity.

- **Peaking Time:** The constraints for the peaking time of the signal at the shaper output are dictated by different needs in inner and outer layers. In Layer 0, the high occupancy due to background and the need to avoid pulse overlap and consequent hit inefficiencies set the required peaking time in the range of t_p=25-50 ns, which also allows for a high time resolution (see below). In the external layers 4 and 5, where background hit frequency is much smaller and where strips are longer and have a larger capacitance, the peaking time will be mostly determined by the need of reducing series noise contributions and has to be in the range of 0.5-1.0 μs.

- **Signal-to-Noise Ratio:** Concerning the signal, this requirement has to take into account the different thickness of silicon detectors in inner (200 μm) and outer (300 μm) layers, as well the signal spread among various strips that depends on the track angle inside detectors and that, again, may vary in different SVT layers. Noise-related parameters (strip capacitance and distributed resistance) also sizably vary across the SVT. A signal-to noise ratio of 20 has to be ensured across the whole SVT and should not decrease

significantly after irradiation. Here are the two extreme cases (where the equivalent noise charge ENC includes the thermal noise contribution from the distributed resistance of the strips):

  - Layer 0 striplets: ENC ≈900 e- at C_D=14.9 pF and at t_p=25 ns
  - Layer 5 strips: ENC ≈1100 e- at C_D=66.2 pF and at t_p=750 ns

- **Threshold and Dispersion:** Each microstrip channel will be read out by comparing its signal to a settable threshold around 0.2 MIP. Threshold dispersion must be low enough that the noise hit rate and the efficiency are degraded to a negligible extent. Typically, this should be 300 rms electrons at most and should be stable during its entire operational lifetime.

- **Comparator Time Resolution:** The comparator must be fast enough to guarantee that the output can be latched in the right time stamp period.

- **Time Stamp:** 30 ns time stamp clock is required for inner layers to get a good hit time resolution in order to reduce the occupancy in the target offline time window (100-150 ns). In the outer layers the time stamp resolution is less critical since the hit time resolution will be dominated by the long pulse shaping time. A single 30 ns time stamp clock in all layers will be used.

- **Chip clock frequency:** Two main clocks will be used inside the readout chip, the time stamp clock (about 30 MHz) and the readout clock (120 MHz or 180 MHz). These clocks will be synchronized with the 60 MHz SuperB system clock. In case the analog-to-digital conversion is based on the Time-Over-Threshold method, a ToT clock has to be generated inside the chip. The ToT clock period should at least match the pulse shaping time to get a good analog resolution. A faster ToT clock could slightly improve the analog resolution but an upper limit (≈3.5) on the ratio between ToT clock frequency and the shaping time frequency is imposed by the required dynamic range needed for low momentum particle dE/dx measurements (≈10-15 MIP) and the number of bits available for ToT. With the experience of the BaBar Atom chip a ToT clock frequency 3 times higher than the pulse shaping frequency could be used.

- **Mask, Kill and Inject:** Each micro-strip channel must be testable by charge injection to the front-end amplifier. By digital control, it shall be possible to turn off any micro-strip element from the readout chain.

- **Maximum data rate:** Simulations show that machine-related backgrounds dominate the overall rates. At nominal background levels (including a safety factor of 5), the maximum hit rate per strip goes from about 1 MHz/strip in Layer 0 to about 50 kHz/strip in Layer 5, z-side.

- **Deadtime limits:** The maximum total deadtime of the system must not exceed 10 % at a 150 kHz trigger rate and background 5 times the nominal expected rate.

- **Trigger specifications:** The trigger has a nominal latency of about 6 μs, a maximum jitter of 0.1 μs, and the minimum time between triggers is 70 ns. The maximum Level 1 Trigger rate is 150 kHz.

- **Cross-talk:** Must be less than 2 %.

- **Control of Analog Circuitry on Power-Up:** Upon power-up, the readout chip shall be operational at default settings.

- **Memory of Downloaded Control of Analog Circuitry:** Changes to default settings shall be downloadable via the readout chip control circuitry, and stored by the readout chip until a new power-up cycle or additional change to default settings.

- **Read-back of Downloadable Information:** All the data that can be downloaded also shall be readable. This includes data that has been modified from the default values and the default values as applied on each chip when not modified.

- **Data Sparsification:** The data output from the microstrip detector shall be only of those channels that are above the settable threshold.

- **Microstrip output data content:** The microstrip hit data must include the time stamp and the microstrip hits (strip number and relevant signal amplitude) for that time stamp. The output data word for each strip hit should contain 16 bits (7 strip address, 4 ToT, 1 type (Hit or Time Stamp) 4 bits to be defined). A 10-bit time stamp information (with 6 additional bits: 1 type, 5 bits to be defined) will be attached to each group of hits associated to a given time stamp (hit readout will be time-ordered).

6.6.3 Readout Chip Implementation

The SuperB SVT readout chips are mixed-signal integrated circuits in a 130 nm CMOS technology and are being designed to comply with the requirements discussed above. Each chip comprises 128 analog channels, each consisting of a charge-sensitive preamplifier, a unipolar semi-Gaussian shaper and a hit discriminator. A polarity selection stage will allow the chip to operate with signals delivered both from n- and p-sides of the SVT double-sided strip detectors. A symmetric baseline restorer may be included to achieve baseline shift suppression. When a hit is detected, a 4 bit analog-to-digital conversion will be performed by means of a Time-Over-Threshold (ToT) detection. The hit information will be buffered until a trigger is received; together with the hit time stamp, it will be then transferred to an output interface, where data will be serialized and transmitted off chip on LVDS output lines. An n-bit data output word will be generated for each hit on a strip. A programming interface accepts commands and data from a serial input bus and programmable registers are used to hold input values for DACs that provide currents and voltages required by the analog section. These registers have other functions, such as controlling data output speed and selecting the pattern for charge injection tests.

Given the very different requirements of inner and outer layers, in terms both of detector parameters and hit frequency, several programmable features will be included in the chips such as the peaking time, the gain and the size of the input device. The block diagram of the analog channel is shown in Fig. 6.27.

The digital readout of the matrix will exploit the architecture that was originally devised for a high-rate, high-efficiency readout of a large CMOS pixel sensor matrix. A schematic concept of the FE chip readout is shown in Fig. 6.54. Each strip has a dedicated array of pre-trigger buffers, which can be filled by hits with different time stamps. The size of this buffer array is determined by the maximum strip hit rate (inner layers) and by the trigger latency. After arrival of a trigger, only hits with the same time stamp as the one provided by the triggering system send their information to the back-end. The array of 128 strips is divided in four sections, each with a dedicated sparsifier encoding the hits in a single clock cycle. The storage element next to each sparsifier (barrel level-2) acts

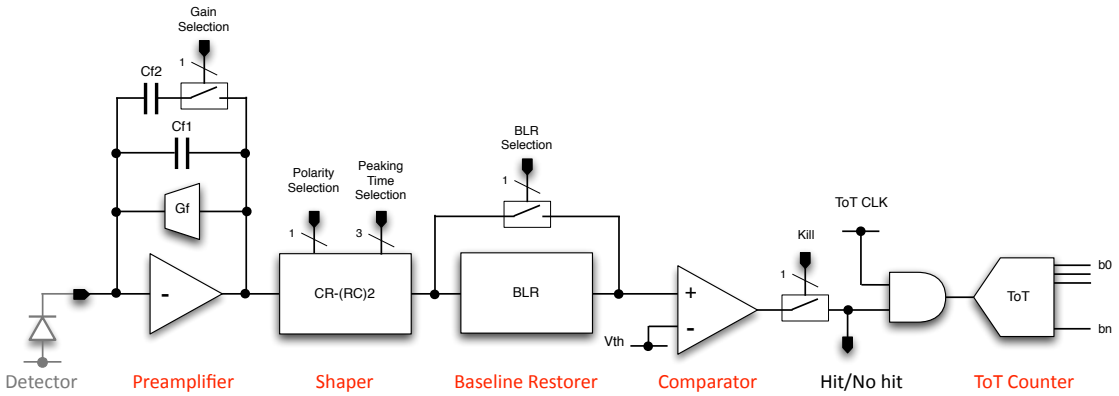

Figure 6.27: Analog channel block diagram.

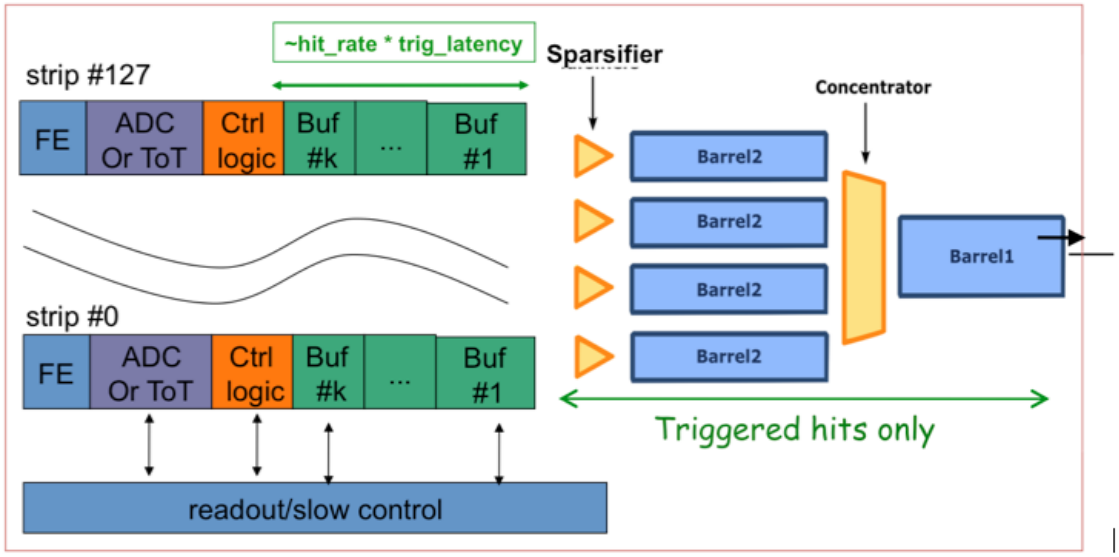

Figure 6.28: Readout architecture of the SVT strip readout chips.

like a FIFO memory conveying data to a barrel-L1 by a concentrator which merges the flux of data and preserves the time order of the hits. This barrel-L1 will drive the output data bus which will use up to 2 output lines depending on the data throughput and will be synchronous to a 180 MHz clock.

6.6.4 R&D for strip readout chips

The R&D to support the development of the SuperB strip readout chips has begun in 2011. The chosen technology for integration is a 130 nm CMOS process: this has an intrinsically high degree of radiation resistance, which can be enhanced with some proper layout prescriptions such as enclosed NMOS transistors and guard rings. There is a large degree of experience with mixed-signal design in this CMOS node that was gained in the last few years inside the HEP community.

The readout architecture is being tested with realistic data created by Monte Carlo analysis of the interaction region. Verilog simulations demonstrate that the chip will be able to operate with a 99 % digital readout efficiency in the worst case condition, which includes a safety factor of 5 in the background levels.

The analog section of the chip is being optimized from the standpoint of noise, comparator threshold dispersion and sensitivity to variations of process parameters. It will be possible to select the peaking time of the signal at the shaper output (25-200 ns for inner layers, 350-750 μs for outer layers) by changing the value of capacitors in the shaper. In this way the noise performances of the chip can be optimized according to the signal occupancy, preserving the required efficiency. Table 6.16 shows the main parameters of the analog section, according to simulation estimates for realistic values of detector parameters and strip hit rates. The loss in efficiency is determined by the limits in the double pulse resolution of the analog section, which depends on the signal peaking time. An acceptable compromise will be found here with the noise performance. Thought the safety factor of 5 used in noise estimation after 7.5 years represents a really worst case, different strategies will be pursued to mitigate the noise increase after irradiation. In particular, especially for Layer4 and 5, S/N may benefit from moving to shorter peaking times after irradiation, as shown in Fig. 6.29, and from reducing the temperature of few degrees w.r.t. ambient temperature. As a further chance, the replacement of the irradiated detectors with fresh ones can also be considered.

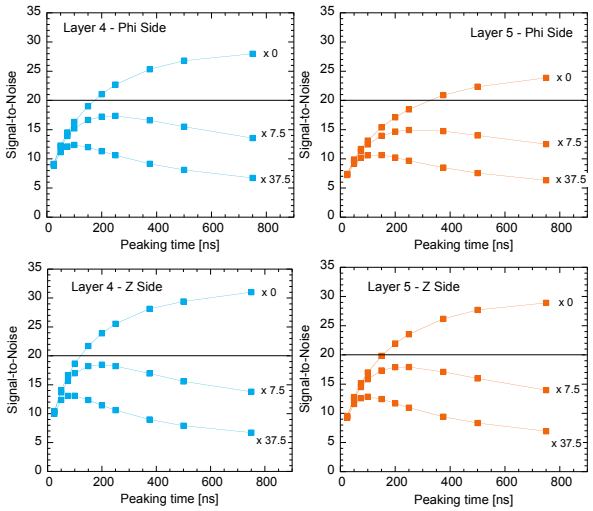

Figure 6.29: Simulated S/N for Layer4-5, as a function of the shaping time, with different background conditions and related sensor leakage current induced by radiation damage.

In 2012, the submission of a chip prototype including 64 analog channels and a reduced-scale version of the readout architecture is foreseen.

The submission of the full-scale, 128-channels chip prototypes is then scheduled in late 2013. This version will have the full functionality of the final production chip.

6.6.5 Hybrid Design M.Citterio - 4

The Super*B* SVT hybrid is conceptually similar to the High Density Interconnect (HDI) hybrid of the *BABAR* SVT. It is a multipurpose structure that has to satisfy essentially three different types of requirements: mechanical, thermal

Table 6.16: Main parameters of the analog section of the SVT strip readout chips.

Layer	C_D [pF] including fanout (with ganging)	t_p [ns] Available	t_p [ns] Selected	Total ENC [e rms]	Total ENC [e rms] after 7.5 years	Total ENC [e rms] after 7.5 years with ×5 safety factor	Hit rate/strip [kHz] nominal	Efficiency 1-N nominal	Efficiency 1-N with ×5 safety factor
0-side u	14.9		25	936	952	1016	187	0.99	095
0-side v	14.9		25	939	956	1019	187	0.99	0.97
1 phi	33.4		75	1122	1197	1457	170	0.98	0.92
1 z	16.2	25-200	75	748	899	1342	134	0.98	0.91
2 phi	37.2		100	1085	1174	1476	134	0.98	0.90
2 z	18.0		100	711	876	1346	134	0.98	0.88
3 phi	35.7		150	897	1125	1763	116	0.96	0.82
3 z	24.6		150	707	935	1540	79	0.98	0.90
4 phi	53.1		500	1121	1709	3090	25	0.98	0.92
4 z	47.2	375, 500	500	836	1555	3041	13.4	0.99	0.95
5 phi	66.2	750	750	1316	2099	3859	16.2	0.98	0.93
5 z	52.2		750	925	1727	3375	8.8	0.99	0.95

and electrical. Each of the six detector layers of the SVT is readout by the readout chips described in the previous section. The readout chips will be mounted on a custom designed ceramic circuit called HDI hybrid. The HDI is a thick-film ceramic circuit fabricated from aluminum nitride (AlN). Since the strip sensors are double sided, the readout chips are mounted on both side of the HDI together with external passive components. The HDI are mounted through "two bushings" on metal cooling rings which are fixed on the carbon fibers support cones. The HDI is connected to the detector by the flexible fanout circuits, described earlier, and to the so called tail, which will be described in the following section of the document. The HDI is the physical support for the readout chip, the thermal interface between the chips and the cooling system, the electrical interconnects among the chips and the electrical connections with other components. It represents also the mechanical interface between modules and the support cone.

6.6.5.1 Hybrid mechanical requirements

The HDI is located outside the active region in a very limited space (approximately 1 cm thick) between the tracking acceptance cone and the accelerator stay-clear volume as shown in Fig. 6.2. The limited space forces the HDI to be of different types. At the moment 4 different models of hybrids are foreseen and they substantially differ in the number of front-end chip (4 to 10) mounted on the hybrid and in shape and dimension. An additional reduction in number of types will be studied only when final readout electronics will be available. The approximate dimensions of the HDIs and the quantity of each HDI type to be installed are summarized in the Table 6.17.

Chips are mounted on both sides of the HDI in order to read the ϕ and z strip of half of the detector module. The number of chips and the association with the layer is summarized in Table 6.17. An important parameter in the design is the total thickness of the HDI including the external mounted components. Based on the

Table 6.17: HDI dimensions and quantities for each SVT layer. The dimensions of the width (w) and the length (l) are in mm. *(Dimensions to be verified from old babar and from new svt mechanical drawings.)*

Layer	View	Module	HDI	Chip	w, l (mm)	type
L0	u v	8	16	6 6	w = xx l = yy	Type 0
L1	z ϕ	6	12	7 7	$w = 50$ $l = 42$	Type I
L2	z ϕ	6	12	7 7	$w = 50$ $l = 42$	Type I
L3	z ϕ	6	12	10 6	$w = 66$ $l = 38$	Type II
L4	z ϕ	16	32	5 4	$w = 34$ $l = 44$	Type III
L5	z ϕ	18	36	5 4	$w = 34$ $l = 44$	Type III

BABAR experience the thickness should be no more than 8 mm. The HDI is the mechanical interface between the detector module and the support cone. Special care must be taken for the mechanical requirements of the AlN substrate and of the technical realization of the circuit:

- accuracy in chip positioning: $\pm 50\,\mu$m;
- planarity tolerance in the stay-clear regions for the contact with the "buttons": $\pm 10\,\mu$m;
- accuracy of cuts of holes for "buttons" and vias: $\pm 50\,\mu$m;
- accuracy in cut of the substrate: $\pm 100\,\mu$m;
- stay-clear region on the front part of the HDI for gluing the fanout (minimum value): 5 mm;
- stay-clear region on the four corners of the HDIs for mechanical tools access: $\sim 2.5 \times 1\,\text{mm}^2$.

At the opposite side in respect to which the fanout is glued a low profile multi-pin Panasonics connector is mounted to contact the HDI to the tail. The mounting requirements of such connectors have also to be respected.

A picture of the layer 0 HDI is shown in Fig. 6.30.

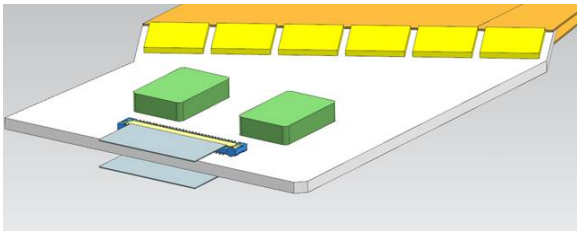

Figure 6.30: In the picture the yellow rectangles represents the readout chip, the green boxes are the thermal contacts ("bushing") and the Panasonics connectors are in blue. Two connectors per HDI are needed.

6.6.5.2 Hybrid Electrical requirements

The HDI must allow all functionality of the readout chip. In particular:

- provide separate analog and digital powers through low impedance planes;

- two different current return, one for the digital current and one for the analog current;
- each power line must be locally filtered;
- differential command, control and data lines have to be distributed from each chip to the Panasonics connector;
- impedance of differential lines have to controlled, 5% to guarantee LVDS communication between front-end chip and transition card;
- whenever possible control and command lines need to be redundant;
- the detector bias voltage must be capacitively coupled to the analog power (representing the analog reference voltage of the readout chip);
- the two readout section (ϕ and z) of the HDI must be capacitively coupled;
- each HDI must host and provide connection to one resistive temperature monitor;
- each HDI must provide connections for remote sensing lines for all the supply voltages;
- detector fan-out are glued on the hybrid edge and chips inputs are wire bonded to the fan-out.

6.6.5.3 Layout requirements and implementation

The layout has to fulfill the electrical requirements. The preamplifier, which is the first step in the signal processing, is particular sensitive to noise. For this reason as a general rule, the layout must be developed to minimize the coupling of the analog and digital sections, crosstalk and noise coming from the power planes must also be minimized. Furthermore power supplies have to be distributed in wide planes to reduce as much as possible trace inductances and achieve good coupling with current return. Each power line is filtered locally with capacitors to the common return. The capacitors have to be reliable for high frequency behavior, aging effect, temperature coefficients, dimension and values. Following the *BABAR* experience, SMD capacitors with X5R dielectric are proposed. To suppress common mode noise coming from the detector, the two HDI readout section (ϕ and z) need to be coupled. The connection between the two HDI sides will be realized with a via close to the Panasonics connector, i.e. in an area where space is not critical. Four or more layers (depending on the specific electric layout) on each side will allow electrical connections between the detector and chips from one side and the chips and the transition cards and power supplies on the other side. The thick film technology proposed for the realization of the HDI is a well known industrial solution so that no R&D is required. All fabrication processes are completely under control and there is also possibility of some rework. Such a kind of hybrid is a robust solution and has proven long-term reliability. Based on the *BABAR* HDI, shown in Fig. 6.31, it is reasonable to assume that each layer has a thickness of about 65 μm (15 μm conductor and 50 μm dielectric), traces are 15 μm thick, 250 μm wide, traces pitch is 400 μm and pads dimensions are $250 \times 400\,\mu\text{m}^2$. Minimum distance between two vias is 400 μm. Likely some of these technological parameters will need to be tuned during the final layout implementation either take advantage of the last available technology or to improve some of the electrical parameters as for example the impedance of the differential lines.

Because multiple layers must be screened on the HDI high quality workmanship has to be followed and layer per layer full inspection will be implemented in close collaboration with the manufacturer. For a good isolation of two conductive layers the dielectric layer must have a minimum thickness of $45 - 50\,\mu$m. This will be realized with three different dielectric depositions (printing and thermal process) and two via filling:

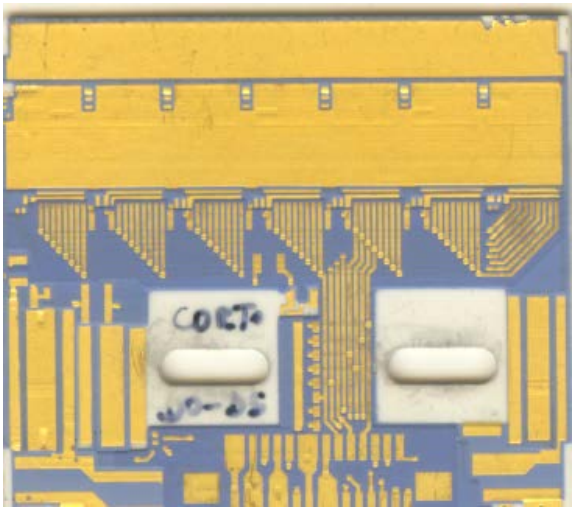

Figure 6.31: *BABAR* HDI, shown as an example of the technology to be used.

- deposition of a conductive layer ($10-15\,\mu$m thick);
- first dielectric deposition ($15\,\mu$m thick);
- first via filling;
- second dielectric deposition ($15\,\mu$m thick);
- last dielectric deposition ($15\,\mu$m thick);
- second via filling;
- deposition of another conductive layer.

Moreover component placement and electrical association of layers will play an important role in design. Again using the experience gained in *BABAR*, the following criteria will be followed:

- separation of components conneted to the analogue and digital part: the components "linked" to the analogue part are mostly placed close to the border of the HDI. The other components are placed in between the mechanical supports;
- dedicated layer/s for clock, control lines and data lines;
- dedicated layers for power/return lines;
- dedicated layer for component mounting. It will contains most of the traces and poad for soldering components. Power sense lines and temperature monitoring will also be on this plane;
- shielding layer will be added if necessary.

Final layout of the HDI will need detail knowledge of IC pinout which is not yet available.

6.6.6 Data Transmission M.Citterio - 5

The SVT data transmission consists of various separate hardware components: the HDIs, the tails, the transition cards and the Front end Boards (FEBs). The characteristics and functionality of the FEBs are described in Sec. .

A simplified drawing of the data transmission chain with the locations of the various components up to the transition card is shown in Fig. 6.32.

The FEBs are connected to the transition card output via optical fibers and are located after the radiation wall. As explained in the previous section in the HDI, the signals generated in the detector are processed and translated in digital data, properly formatted, by the readout ICs. The output data from the ICs are transferred from the HDI to the next component of the data transmission, the tail, without further processing. The limited space available for the HDI prevents mounting additional electronics on the hybrid. The specification/characteristics of the data lines can be summarized as follow:

- the data signals follow a LVDS standard, consequently they are differential signals;
- the number of data lines, per IC, varies from:
  - 1 to 3 if synchronized to a 120 MHz clock
  - 1 to 2 if synchronized to a 180 MHz clock

  depending from the data throughput;

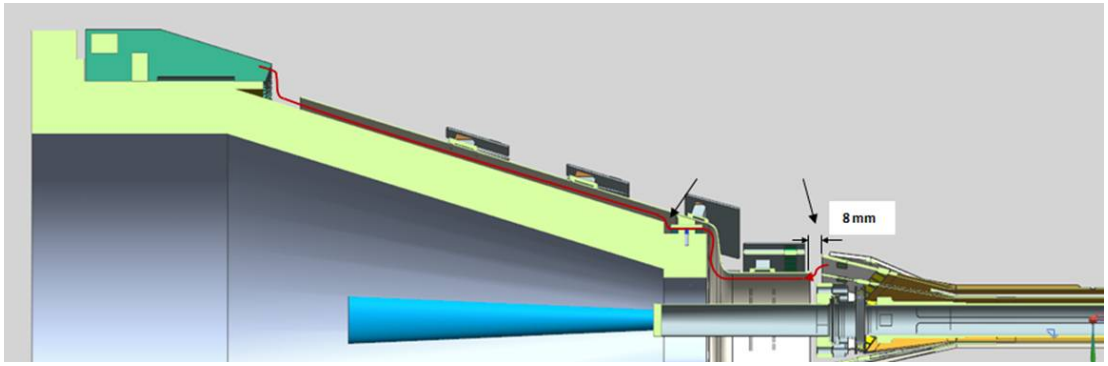

Figure 6.32: Longitudinal view of the combination HDI, tail, transition card. *(better drawing needed: it is not clear where the different pieces are)*

Table 6.18: Number of data lines, tails, transition cards (TCs) and optical fibers for the six layers of the SVT detector.

Layer	View	Modules	HDIs	HDI Type	Chips	Data lines per HDI side (120 MHz)	Data lines per HDI side (180 MHz)	Tails (Cu Bus)	TCs	Optical Fibers
L0	top bottom	8	16	Type 0	6 6	18 18	12 12	32	32	32
L1	z ϕ	6	12	Type I	7 7	14 21	7 14	24	24	24
L2	z ϕ	6	12	Type I	7 7	14 14	7 14	24	24	24
L3	z ϕ	6	12	Type II	10 6	20 12	10 6	24	24	24
L4	z ϕ	16	32	Type III	5 4	10 8	5 4	64	32	32
L5	z ϕ	18	36	Type III	5 4	5 4	5 4	72	36	36

- the data are serialized and encoded using a 8b/10b protocol in the readout chip.

The data lines needed for the different HDIs (reference clock of 120 and 180 MHz) are summarized in Table 6.18.

The large number of data lines suggests that the reference clock should be the 180 MHz one, so that the maximum number of lines is 14 for one side of the HDI Type I. Together with the data lines (and always in LVDS standards) all the ICs of same HDI shares 6 input lines (Reset, Clock, FastClock, Timestamp, Trigger, RegIn) and 1 output line (RegOut).

6.6.6.1 The Tail

The total number of differential lines to be transferred from an HDI to the next processing block of the chain are 21 or less. Because the data rate per line is not excessively high ($\sim$ 180 Mbps) and a custom designed shielded, multilayer copper bus could be used to connect the output of the HDI with the input of the transition card. The lenght of the this bus, called the "tail", is between 50 to 70 cm and changes slighlty from layer to layer. The tail should also have a rectangular section not exceeding $10 \times 4\,\mathrm{mm}^2$, because it has to be pulled along the supporting cone and below the HDI itself during detector integration. In many cases, the tail has to pass be-

tween the HDI thermal standoff, the "buttons", also. Similar dimensional constraints apply to the tail terminating connectors. A very low profle (0.8 mm) narrow pitch (0.35 mm) Panasonics connectors (series AXE, 70 pins) can be utilized for this purpose, Fig. 6.33. By using the repetitive pin sequence Gnd/D+/D-/Gnd it is possible to connect up to 22 LVDS lines (11 per side) to this connector. Each LVDS lines is individually shielded if the lines are realized as strip-lines.

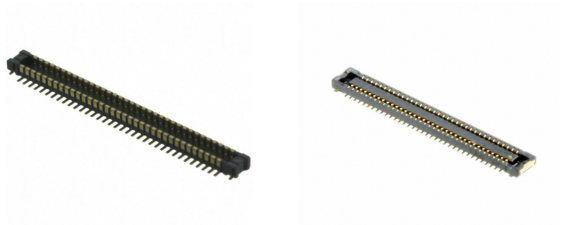

Figure 6.33: Panasonics AXE series connector. Header (left) and socket (right).

The socket (2.5 mm wide) is mounted on the HDI and the transition card, while the header (2.0 mm wide) is mounted on the tail. The dimensions of this surface mount connector are compatible with the space reserved on the HDI for the output connectors. The retention mechanism of this connectors provide an holding force of at least 0.20 N/contact, which ensure a reliable lock between the elements of the data chains. This connector is also adequate for the transition card as explained in the following section. In the present design, the tail is a multilayer flexible katpon circuit, whose main electrical parameters are the following:

- five layer circuit. Stack-up plane/signal/plane/signal/plane;
- LVDS lines: strip lines on the two signal layers;
- LVDS line width/space: 100/100 μm;
- LVDS copper thickness $\sim 20\,\mu$m;
- dielectric thickness: ~ 2.5 mm ;
- Zdiff: ~ 100 Ohm;
- kapton thickness: $50\,\mu$m;
- via diameter: $250 - 300\,\mu$m;
- via clearance: $150\,\mu$m;
- width: 10 mm min, 15.8 mm max (at the connector).

The plane layers available in the stackup can be used both as shield for the LVDS traces as well as Power/Ground planes. The tail does not only carry the digital signals but also the power for the readout ICs. The parameters for the plane segmentation of the prototype design are:

- power plane width: ~ 4.7 mm;
- ground plane width: ~ 9.4 mm;
- metal thickness: $> 50\,\mu$m;
- current capability: $\sim 3 - 3.5$ Amps;
- voltage drop (both ways): ~ 250 mV.

The minimum bending radius of the resulting multilayer circuit has to be careful evaluated to verify that during installation the tail can be bended to the proper shape.

6.6.6.2 The transition card

The next element of the transmission chain is a printed circuit board made in halogen free material, called transition card (TC). The geometrical aspect, dimensions and shape are defined by the detector geometry and is shown in the top left corner of Fig. 6.32 and in more detail in Fig. 6.34.

The transition cards are located approximately 50 cm from the detector sensors and they are electrically connected inbound to the HDI by means of the tail. They are also connected outbound by optical fibers to the FEBs and by cables to the remote power supplies (both low and high voltage).

A transition card has various functions:

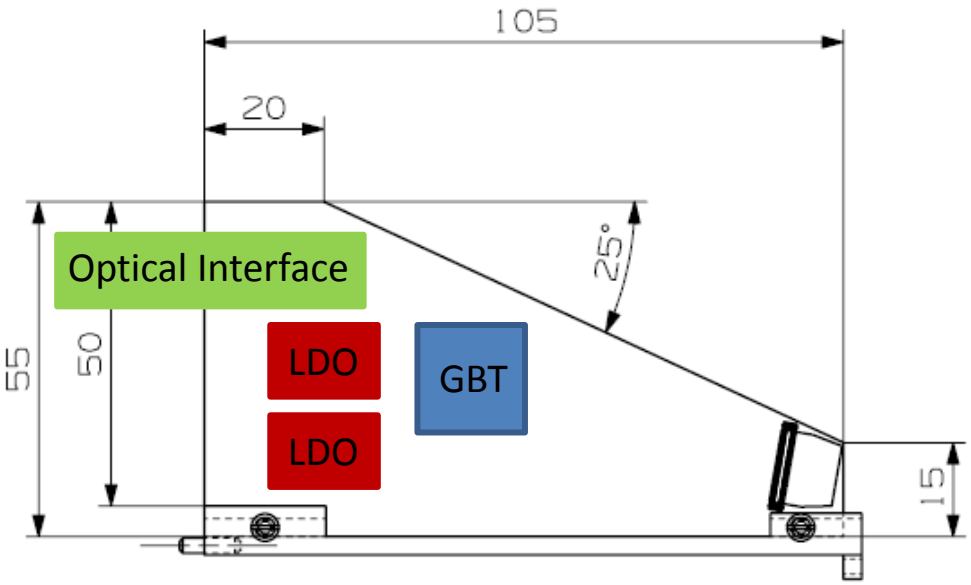

Figure 6.34: Shape/dimensions of a transition card. In the figure are also shown the main active components to be mounted on the PCB (GBT, LDOs, optical transmitter) and the mechanical support, at the bottom, to mount the board. Figure is being updated.

- it will receive and distribute the input and control signals for the front-end chip through the optical fiber from the FEB;
- it will receive, format and serialize, the data coming from the front-end chips;
- it will perform the electrical-to-optical conversion of the data and it will transmit the data to the FEB to begin the data acquisition;
- it will regulate and distribute the power to the front-end chip on the HDIs as well as the HV power for the microstrip detectors. It also filters the supplies to have low ripple voltages sent to the HDIs.

Because the data volume decreases substantially from the innermost to the outermost detector layer (from $\sim$ 1 Gbits/trig, to $\sim$ 0.25 Gbits/trig per TC), one transition card will be used per HDI side for the layers 0 to 3. Instead one transition card will serve both side of the same HDI for the layer 4 and 5.

Such reduction in total number of TC is advantageous both in having a uniform data link speed (<2Gbit/s) with reasonably link utilization for all TCs but also in maximizing the surface area available per TC and increasing the space between two adjacent TCs.

The typical geometrical disposition of the TCs is shown in Fig. 6.35. The minimum space between two cards is 3.6 mm, barely enough to mount the tail. The total number of TC is 86 per detector side (172 in total).

The TC requirements can be fulfilled by having at least the following logic blocks:

- an interface circuit to group, before serialization, the LVDS data lines coming from the HDI;
- a serializer/deserializer;
- an optical transmitter/receiver;

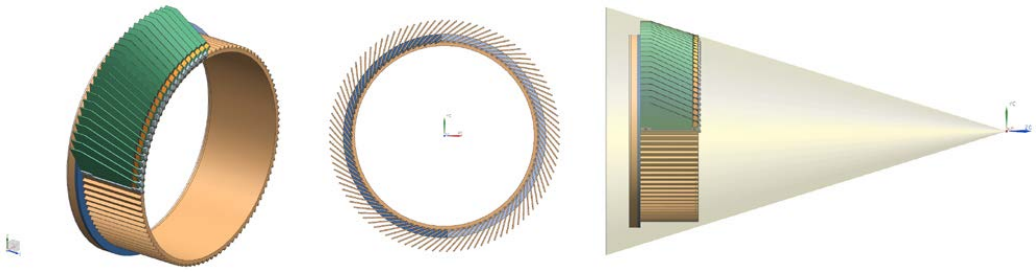

Figure 6.35: Turbine arrangement of the TC on the support cone. *(this figure will be updated. Working on it.)*

- slow control interface for handling the detector control signals.

This device has not been designed yet, however we are closely following various CERN designs to take advantage of the development already started. In particular the CERN GBT project which is well advanced and which is trying to address very similar needs for the LHC experiments [46], is our baseline design for signal transmission.

The contact undertaken with CERN designers have indicated that the GBT IC characteristics match and even exceed SVT requirements in term of data link, being the GBT project intended to operate up to 4.8 Gbit/s.

The physical dimension of the IC, less than 400 mm^2, the power ($\sim$ 2 W/chip) and the expected delivery time (not later than 2013) are compatible with the TC design, construction and test. Moreover the CERN design has been proved to be radiation tolerant up to radiation levels well exceeding the ones expected in Super$B$.

The maximum reference clock of the GBT IC is related to the LHC machine clock (40 MHz). Such a frequency will need to be locally generated at the level of the transition card to properly operate the device. If this reference clock, as recently discussed could be an option at SuperB level, the TC design will take advantage of this possibility.

Similarly the design of the optical interface and the choice of the optical fibers, will take advantage of the results obtained by the CERN VERSATILE LINK project [47], which again is well suited for the SVT application. In particular the new "versatile small form factor transceiver", which design is ongoing at CERN could fit dimensionally in the TC and has provision for connecting two optical fibers in the same package, one fiber for control signals, the other for data.

Finally, at the present stage, the regulation of the low voltages needed for the front-end IC will be implemented by using the same adjustable low dropout voltage regulators (LDOs) widely adopted at LHC: LHC4913. This component, manufactured by ST, has been thoroughly tested against radiation and can generate a clean reference voltage down to 1.25 Volts. It also has remote sense capability to compensate voltage drops between the point of regulation and the point of load due to cables. In the baseline design two LDOs, one for the digital and the other for the digital supply, will be used for each HDI.

A preliminary thermal analysis of the transition card has been performed based on the typical heat dissipation of the various electrical blocks mounted on it. A conservative 5 Watt per TC has been used.

A dedicated cooling system is being designed to effectively remove the heat without increas-

ing the temperature of the surroundings. The thermal connection between the board and the cooling system can be achieved by means of the TC mounting support, the design of which is shown in Fig. 6.35.

6.6.6.3 Prototype production and tests

(The design and production of tail and transition card is on-going.)

6.7 Mechanical Support and Assembly

An overview of the mechanical support and assembly is provided in section 6.1. In this section we provide a more detailed account of the constraints of the mechanical design due to the accelerator components of the Interaction Region (IR) and describe the details of the detector assembly, installation, survey, and monitoring.

6.7.1 IR Components & Constraints

The support structure design of the SVT is dictated by the configuration and assembly procedure of the IR machine components, as well as by the SVT geometry. A schematic drawing of the IR assembly with all the components described in the rest of this section is shown in Fig. 6.36. The whole IR assembly consists of the Beryllium beam-pipe, the SVT, the forward and backward Final Focus (FF) permanent magnets, the conical Tungsten shields for background reduction (see below) and the cryostats of the FF superconducting magnet system.

The background conditions impose the need for a pair of Tungsten conical shield located about 25 cm from the IP on either side. There are two further Tungsten shields of cylindrical shape that are located symmetrically with respect to the IP, starting just at the end of the conical ones and that are rigidly attached to the iron structure of the return yoke of the detector magnet (*find an acronym for thsi for the rest of the section; FCAL is used often in this sections in the wrong way*).
The conical shields and the final focus permanent magnets occupy most of the region below 17.2° (300 mrad) on both sides of the IP . In order to minimize the mass inside the active tracking volume, all the electronics is mounted below the 300 mrad cone. This requires that in backward and forward directions electronics, cooling, cabling and supports must be confined in a volume of about one centimeter thick around the conical shields. The use of this tight space below 300 mrad must be carefully arranged with the needs of the accelerator. The angular acceptance in the laboratory frame of the SVT is therefore restricted to the region $17.2° < \theta < 162.8°$, where θ is the polar angle. The radial position of the SVT fiducial volume is imposed by the inner radius of DCH at about 27 cm.
The Be beam-pipe, cooled by liquid forced convection, is about 2 cm in diameter and 40 cm long. It is positioned symmetrically respect to the IP and it supports directly the Layer0 modules. The eight striplet modules, arranged in a pin wheel geometry, are mounted on the two cooled flanges. The Layer0 is mechanically decoupled from the other SVT layers to allow its replacement without a complete disassembling of all the others SVT modules. The SVT layers from 1 to 5 are supported on the backward and forward sides on the conical shields by two gimbal rings, the kinematic mounts that allow the necessary degree of freedom to prevent SVT over-constraints during the installation/removal operations. The central Be beam-pipe is connected at each end through a bellow and a flange to the beam-pipe coming out of the cryostat of the FF superconducting magnets. In this region the beam pipe is splited in two arms: the LER and HER pipes represent the warm internal vessel of the FF cryostats. The forward and backward cryostats are symmetrically positioned around the IP and they are the extreme components of the IR, with the cryostat beam-pipe terminal flanges placed at about 2.2 m far from the IP, as shown in Fig. 6.36. The cryostat is rigidly connected to the conical shield flanges and, through the terminal back flange, at a very rigid coaxial external tube, allowing a free space of about 2 cm in radius along its extension for the SVT cables way-out.

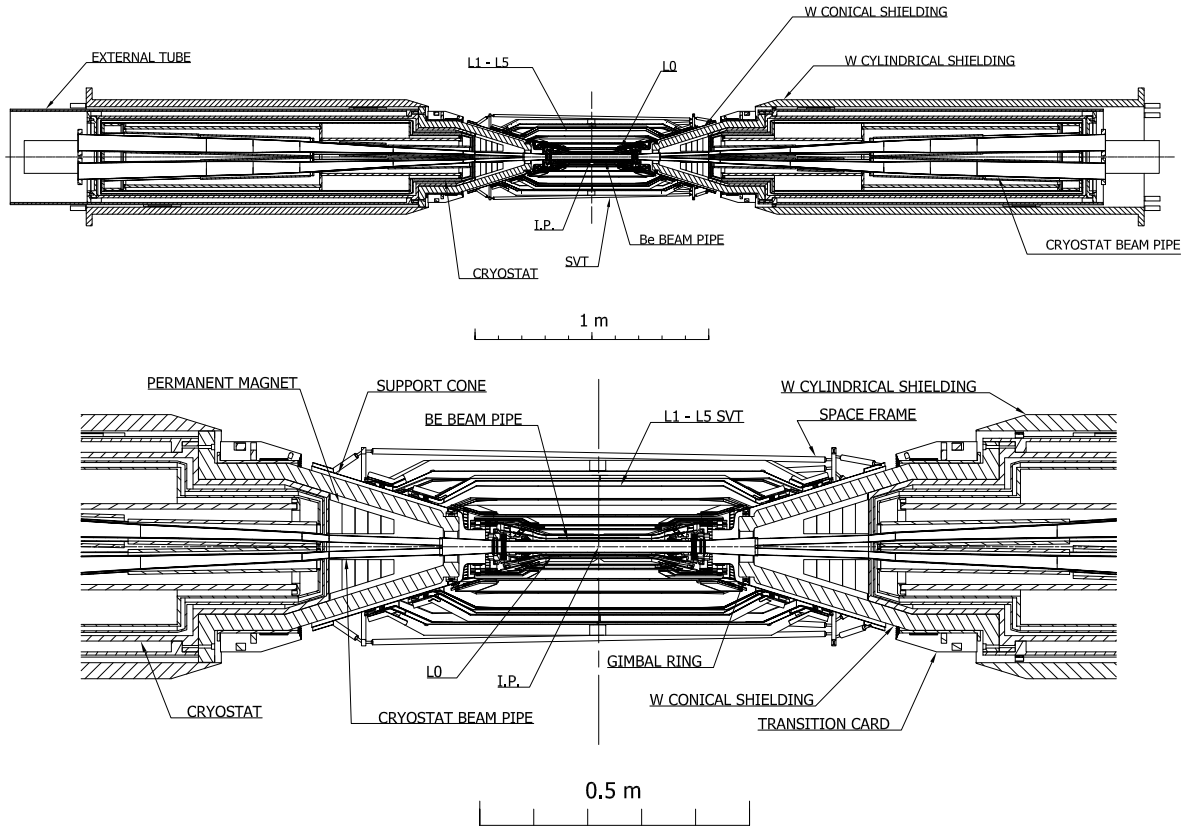

Figure 6.36: Longitudinal section of the IR in the x-z plane (top) with a detailed view (bottom).

Since the L1-L5 and the Layer0 must be installed with all the components of IR system in place, they must be split in two halves and then clam-shelled around the beam-pipe. The whole IR system, just described, will be assembled and aligned in a clean area outside the experimental hall and then transported and installed inside the SuperB detector. From the mechanical point of view, the IR system consists of two very rigid systems (conical shield + cryostat + external tube) joint by a very weak system (the Be beam-pipe and the SVT) that could be damaged during the transportation and installation/removal operation. On the other hand in order to reduce the passive material between the SVT and the DCH, and improve the detector performance, no permanent stiffening structure (i.e. a support tube as in the BaBar detector) is foreseen in SuperB to connect these two rigid systems. Therefore a removable structural support has been designed, in the following called temporary cage, to connect rigidly the backward and forward conical shields. The temporary cage will be inserted to absorb the mechanical stress present at the moment of the first transportation to the experimental hall and during all the installation/removal operations of the IR assembly/SVT/Layer0, and it will be removed for the data taking (see Sec. 6.7.6.2).

6.7.2 Module Layout & Assembly

The SVT is built with detector modules, each mechanically and electrically independent. Each module consists of silicon wafers glued to fiber composite beam, with a high density interconnect (HDI) hybrid circuit at each end. The HDIs are electrically connected to the silicon strips by

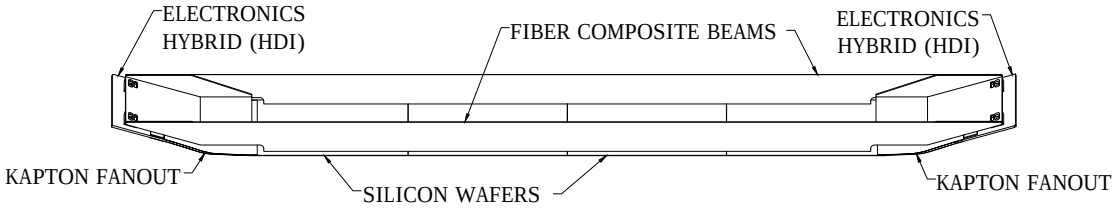

Figure 6.37: Drawing of a layer 3 silicon strip module. *Add a scale to these pictures*

means of flexible circuits and they are mechanically supported by the fiber composite beam. The entire module assembly is a rigid structure that can be tested and transported in its case. As an example a drawing of a detector module from layer 3 is shown in Fig. 6.37.
The assembly of a detector module will follow the procedure used for the *BABAR* SVT modules [2] and begins after the preparation of all the necessary parts. The silicon detectors must be fully tested, including a long-term stability (burn-in) test under full bias voltage. The fanout circuits will be optically inspected and single trace tested for spotting shorts or opens. The readout hybrid must be assembled and tested, with the HDI supports, the front-end chips and additional passive components. Finally, the completed beam structure, which provide mechanical stiffness, must be inspected to ensure it meets the specifications. These individual parts will be fabricated by different laboratories and then shipped to the place where the module assembly is carried out. The hybrids will be tested again after shipment.
The assembly of the inner barrel-shaped modules and the outer arch-shaped modules is necessarily different. However, there are common steps. The procedure is the following:

1. each silicon detector is precisely aligned using its reference crosses and then head to head glued to the adjacent to form the module;

2. the z and ϕ fanouts are glued to the detectors and wire-bonded to the strips. The ganging bonds between ϕ strips are then performed. Electrical tests, including an infrared laser strip scan, are performed to assess the quality of the detector-fanout assembly (DFAs);

3. the silicon detectors and the readout hybrid are held on a suitable fixture and aligned. The fanouts are glued to the hybrids and wire bonded to the input channels of the readout ICs;

4. the final assembly stage is different for different layers. The module of the layer 1 and 2 are then joined together by gluing the beams on the top of layer 1 to the bottom of layer 2 to give a combined structure called the "sextant". For the layer 3, the DFA is bonded flat to the fiber composite beams. For the modules of layer 4 and 5, the flat module is held in a suitable fixture and bent on a very precise mask at the corners of the arch and at the connection to the HDI. The fiber composite beams are glued to the module with fixtures insuring alignment between the silicon detectors and the mounting surfaces on the HDI. This procedure has been already successfully adopted for the external modules of the SVT of the BaBar experiment;

5. once completed, these detector modules are extremely rigid ladders that can be stored and submitted to the final electrical characterization. They are then stored in their shipping boxes for the final installation on the detector.

A drawing of an arch-shaped module is shown in Fig. 6.38.

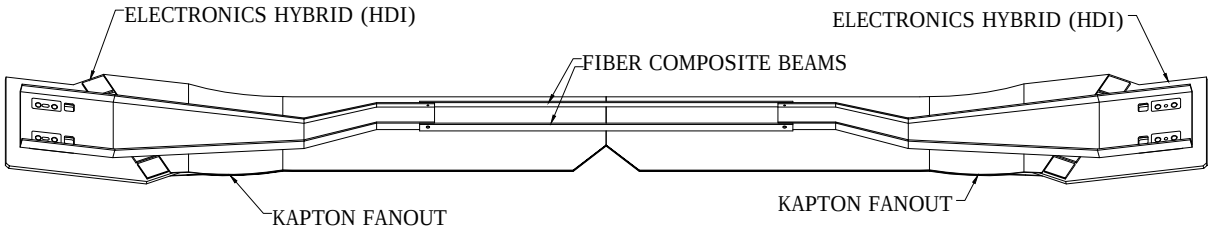

Figure 6.39: Drawing of a Layer0 striplets module.*Add a scale to these pictures*

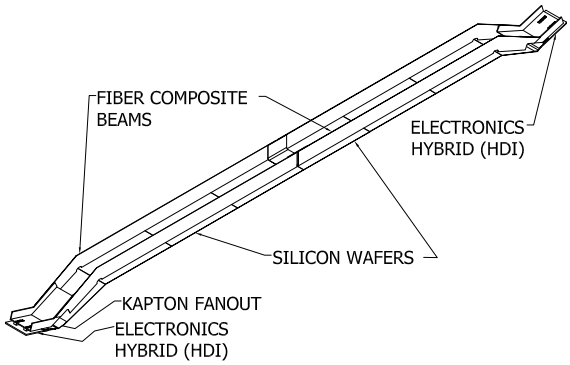

Figure 6.38: Drawing of a layer5 silicon strip arch-module.*Add a scale to these pictures*

The assembly procedures for the Layer0 module (shown in Fig. 6.39) follow in general which we reported for the other SVT layers, although the smaller sensor dimensions represent a greater difficulty in the handling. The procedures are the following:

1. no detector alignment is requested because there is only one detector;

2. the u and v fanouts are glued on each face of the detector on both sides and wire-bonded to the strips. A two-layer fanout is necessary to read out each face;

3. the silicon detectors and the readout hybrid are held on a suitable fixture and aligned. The fanouts are glued to the hybrids and wire bonded to the input channels of the readout ICs. Electrical tests, including an infrared laser strip scan, are performed;

4. in the final assembly stage for Layer0 module there is the requirements of a mask that is able to position the HDI in a in very precise position in a slant plane inclined of 10° in order to be positioned outside the active region. The fiber composite beams are glued to the module with fixtures assuring alignment between the silicon detectors and the mounting surfaces on the HDI.

6.7.3 L1-L5 Half detector assembly

The L1-L5 detector is assembled in halves in order to allow the device to be mounted around the beam pipe. The detector modules are supported at each end by cooling/support rings in brass that are attached on the support cone realized in laminated carbon-fiber. Water circulates in the cooling rings and cools the mounting protrude pieces (buttons) in thermal contact with the HDIs. The cones are split along a vertical plane and have alignment pins and latches that allow them to be connected together around the conical shield. See Fig. 6.40 for a drawing of the suppport cone.

During the half detector assembly, the two half-cones will be held in a fixture which holds them in precise relative position. The detector modules are then mounted on the half-cones to each end. A fixture holds the detector modules during this operation and allow for well-controlled positioning of the module on the half-cones. Pins located in the buttons provide precise positioning of the modules, which are

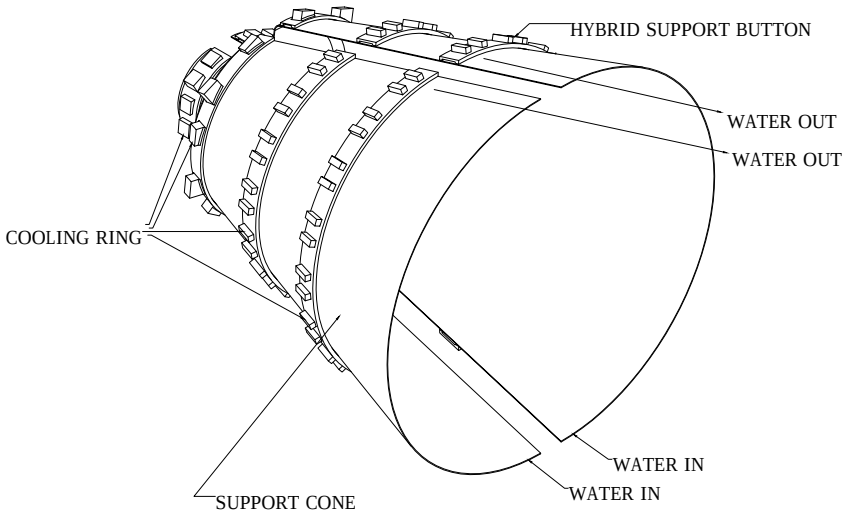

Figure 6.40: The support cone with the four cooling rings for the layer 5, 4, 3 and for the sextants of the layer 1-2.

then screw down. Accurate alignment of the mounting with respect to the silicon wafers is achieved by a pair of mating fixtures. One is a dummy module (mistress mask) and the other simulate the mating surface of the cone (master mask). These fixtures are constructed together and mate perfectly. One is used to verify the right machining of the mounting of the cooling ring on the cones. The other is used to position the mounting point on the HDIs during the assembly of the module.
The connection between the module and the cone (called foot) provides both accurate alignment of the module and a thermal bridge from the HDI to the coolant. A detailed of the forward foot region, which contains the readout electronics and the cooling ring with the mounting buttons is shown in Fig. 6.41.

On the backward side, the foot region is more complicated: in case of bad mounting or temperature variations the elongation of the module in a horizontal plane must be allowed, avoiding over constraint due to the inclined geometry. A detailed of the backward foot region is shown in Fig. 6.42.

After verification of the alignment, the connection between the two HDIs and the support

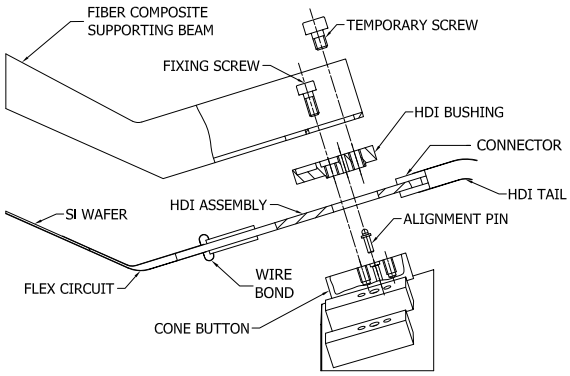

Figure 6.41: The forward foot region.

beam is permanently glued. The glue joint allows for the correction of small errors in the construction of either the cones or the module. After the beam is glued, the module may be removed and remounted on the cone as necessary. The design of the foot allows this glue joint to be cleaved and remade should major repair of the module be required. After the detector module is mounted, it is electrically tested to verify its functionality. As each layer is completed, it is optically surveyed and the data are entered

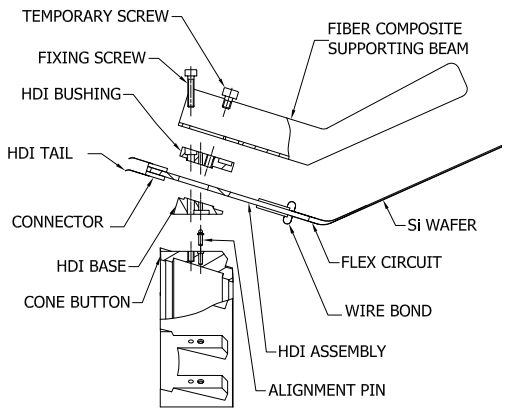

Figure 6.42: The backward foot region.

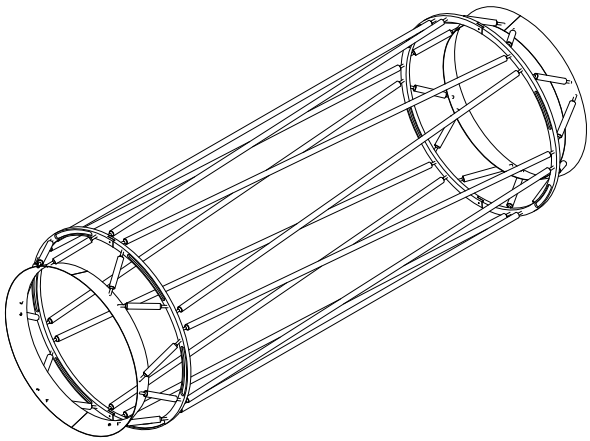

Figure 6.43: The carbon fiber space frame.

in a database. Finally, the two cones are connected together with the space frame, resulting in a completed detector assembly ready to be opened and remount around the layer0.

Space Frame The two carbon fiber support cones are mechanically connected by a low mass carbon fiber space frame (see Fig. 6.43).
The struts of the frame are made of carbon fiber tubing and the rings are carbon fiber skins with foam core. The frame is constructed by gluing the pieces together while they are held rigidly in fixtures. The joints between the struts and the rings use end pieces of carbon fiber material machined to fit the inner diameter of the strut. The space frame must split into two halves just as the cones do. The rings at the ends of the space frame are sections of cones to match the attaching surfaces ao the support cones.

6.7.4 Layer0 Half Detector Assembly

Also the Layer0 detector is assembled in halves in order to be clam shelled around the Be beam-pipe. The detector modules are supported at each end by the cooled half flanges. Cooling water circulates at the internal of each half-flange and cools the mounting protrude wing-pieces supporting the HDIs and in thermal contact with them. The Layer0 half-flanges are mated in the vertical plane and have alignment screw-pins to be wrapped in a precise and reproducible way on the robust stainless steel part of the Be beam-pipe. See Fig. 6.44 for a drawing of the Layer0 half-flanges tight on Be beam-pipe. During the half detector assembly, the two half-flanges will be held in a fixture in a precise relative position. The detector modules are then mounted to the half-flange wing pieces and positioned through precision pins and then screw down. The procedure to mount Layer0 module is the same used for the L1-L5 modules, using similar fixtures in function operability. The connection between the modules and the half-flange wing pieces foot provides accurate and reproducible alignment of the module and conduction of heath from the HDI heath sink to the cooling water circulating in the half-flanges. The technique of the mounting and connection between the HDI and the support beam is the same already described for L1-L5 modules. Also in this case, the glue joint allows for the correction of small errors in the construction of either the half-flange or the module. After each Layer0 detector module is mounted it is electrically tested to verify its functionality. As the Layer 0 is completed, it is optically surveyed and the data are entered in a database. Finally the two half-flange are connected together with a proper fixture forming a rigid half shell and ready to be assembled around the Be beam pipe. An artistic view of the two

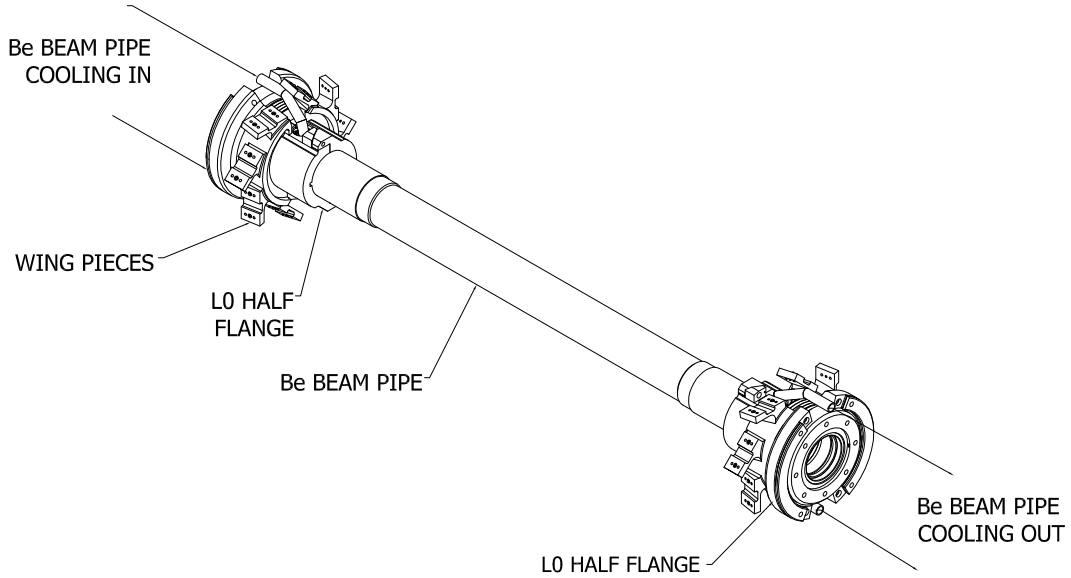

Figure 6.44: The Layer0 half-flanges tight on the Be beam-pipe.

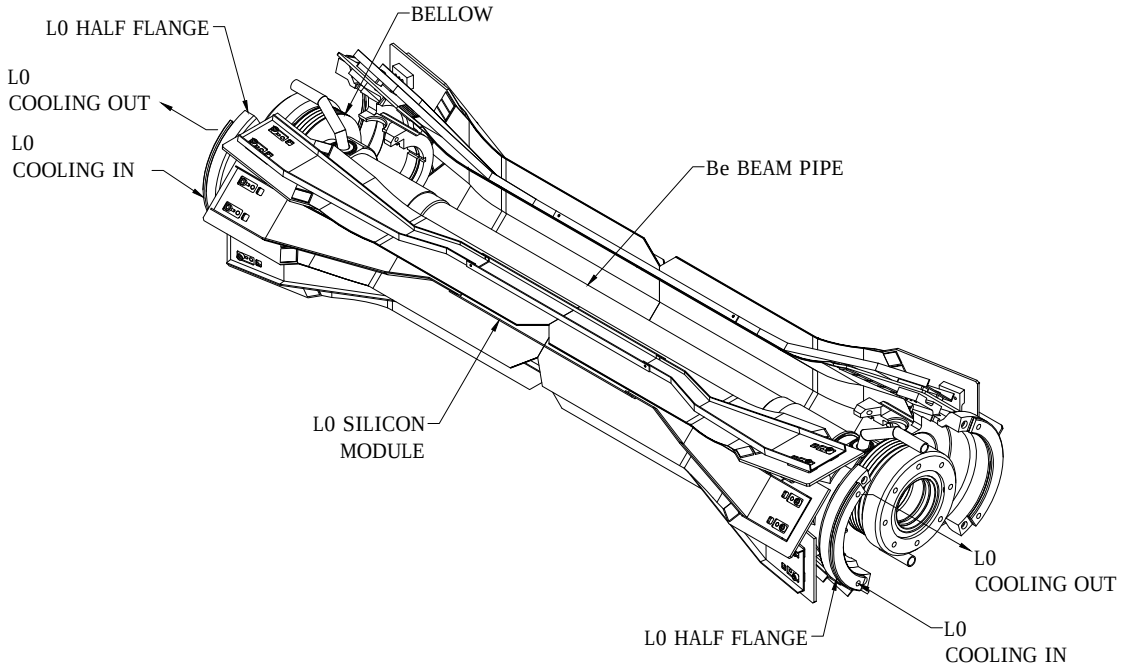

Figure 6.45: The two Layer0 half-shells around the Be beam-pipe.

Layer0 half-shells around the Be beam-pipe, is shown Fig. 6.45.

6.7.5 Mount Layer0 on the Be-pipe and L1-L5 on the conical shield

When the two Layer0 half detector assemblies are completed, they are brought to the staging area where the Be beam pipe, conical shields and cryostats are already mounted. The assembling fixture used to hold Layer0 half-shells, is also used for bring together and clam-shells them around the Be beam-pipe. An isostatic mounting of the Layer0 respect to the Be beam-pipe is equipped, to allow relative motion due to different thermal expansion. Radial and circumferential keys assure precise and reproducible position of the Layer0 flanges and thus of the detectors with respect to the Be beam-pipe. The two half detectors are mated and locked together with pin-screw. The cable from HDIs are attached on the conical shields and routed to the transition cards, which are mounted in cooling support flanges at the end of the conical shield. An optical survey is performed and the detector is tested. In the same way, when the two L1-L5 half-detector assemblies are completed, they are brought to the staging area where both conical shield and Final Focus superconductor Magnet Cryostat are mounted and Layer0 have been assembled on the Be beam-pipe. Fixtures are employed to hold the cones as they are brought together and clam-shelled around the Layer0 and Be beam-pipe. The two half detector assemblies are mated and the latches between them are closed. The cables from HDIs are attached on the cones and routed to the transition cards. The entire detector is then thoroughly tested. Afterwards the Temporary Cage Sectors are mounted on the Conical Shield flanges and rigidly fixed on the Conical Shield flanges. At this point the assembly is relatively rigid and can be transported to the interaction hall and installed in the experiment.

6.7.5.1 Gimball Rings

The detector assembly as described above forms a rigid structure as long as the cones and space frame are connected together. This structure is supported on the conical shields. During the transportation of the IR Assembly to the interaction hall, it is possible for the forward side of IR Assembly as much as 1 mm relative motion with respect to the backward side. This motion is reversible, and they will return to their original alignment when installed in normal condition. In addition, differential thermal expansion may affect the relative alignment of the magnets during periods in which the temperature is not controlled, and relative motion of the magnet and the beam-pipe may occur should there be seismic activity.

The support of the detector on the conical shield must allow this motion without placing stress on the silicon wafers. In addition, the position relative to the IR must be reproducible when installed. These constrains are met by mounting the support cones on a pairs of Gimbal Rings. One gimbal ring connects the forward cone to the Conical Shield to constrain its center, while allowing rotation about the x and y axes. A second set of Gimbal Ring supports the cone in the backward direction in a similar manner, with an additional sleeve that allows both for motion along z and rotation about the z axis.

6.7.6 Installation & Removal of the Complete IR Assembly in SuperB

The clearance between the SVT Layer0 and the beam pipe is of the order of 1 to 2 mm. During the transportation of the IR Assembly, the critical clearances must be monitored in real time to ensure that no accidental damage to the detectors occurs. In its final position, the IR Assembly will be supported along the External Tube on the Cylindrical Shield.
One possible installation/removal scenario employs a crane that handles a long stiff beam that support rigidly the entire IR Assembly trough the forward and backward external tube and it is able to lay carefully this system on the external cradle support shown in Fig: 6.46. This support is aligned with respect to the Cylindrical Shield and positioned in front of the forward end of the detector.
With this procedure it will be possible to slide

(in or out) the IR Assembly inside the DCH using the translation system of the cylindrical shield, described in sec 6.7.6.2, which has been previously aligned with respect to the SuperB detector. Once the IR assembly is in the final position the External Mechanical Cradle is removed.

6.7.6.1 Quick Demounting of the SVT, Layer0 and Be beam-pipe

For a rapid access to some of the IR components (SVT, Layer0 and the Be beam-pipe) the so called quick demounting procedure has been developed to operate on these components inside the experimental hall, avoiding the complete removal of the IR assembly from the SuperB detector, and then reducing the associated down time with respect to what was needed in *BABAR* (several months). This operation can be followed in case the Layer0 needs to be repaired or replaced with a new detector in a short amount of time, as well as for a rapid access to the SVT or the Be beam pipe. *check this is ok also to access the Be beam-pipe* As shown in Fig. 6.46 the procedure foresees to slide the IR assembly only partially outside the detector, leaving it just close to the forward door, in order to access the central region of the IR and perform the work, and then slide the entire IR assembly back inside the detector. The quick demounting operation plans to move rigidly all the IR assembly components along the z axis in the forward direction up to a position that allows the SVT detector to be completely out of the forward side of the iron of the magnet return yoke (forward end plug open), at z=+2650 mm. In this hypothesis it is assumed that the cylindrical backward and forward shields are rigidly attached on a solid structure and perfectly aligned along the z axis direction, having a supporting function in the IR translation.
The stroke necessary for the SVT demounting position is about 3200 mm. The total weight of the IR assembly components is of about 1.65 t.

A beam profile box of about 3×4×3 m^3 volume will be mounted on the forward end of the detector and it will be equipped with the proper filters and fans to maintain ISO 8 cleanness conditions for a four-person team working on the SVT, Layer0, beam-pipe.

6.7.6.2 Temporary Cage and Translation System

The SVT system represents the weak ring of the the IR assembly mechanical chain. The Be-beam pipe is joined to the Cryostat beam-pipe trough a system of flexible bellow flanges. In a different way from *BABAR* where the SVT region was stiffened by the CF support tube, in Super*B* it was decided not to insert any stiffening structure overlaying the DCH with passive material. Therefore it was necessary to design a temporary and removable structural support (the temporary cage). It fixes rigidly the forward and backward conical shields around the SVT region; it is able to absorb all the mechanical stress that could be present during all the installation/removal operations; it can be removed by operating from the forward end region, once the SVT is in data-taking position, removing its passive material between the SVT and the DCH. When the temporary cage is mounted and rigidly connects the two opposite conical shields, the whole IR assembly (forward side + backward sides + SVT) can be considered a rigid body supported by several recirculating spheres. These spheres are embedded in the cylindrical shields, acting on the three rails positioned at 120° that are formed on the external tube profile. The translation system is able to guide the entire IR assembly and prevent any rotation during the installation/removal. The cylindrical shields include also a mechanical system (the Radial Blocking Device) able to block rigidly the IR assembly at the correct position with respect to the IP. This blocking is acted by longitudinal bars that push on a mechanical conical device embedded in the cylindrical shield, able to block radially the external tube respect to the cylindrical shield. This blocking system is also useful at the moment of the temporary cage mounting/demounting on the conical shield flange operations, in order not to transfer any mechanical stress to the SVT detector and the Be beam-pipe.
Due to the presence of translation rails on the

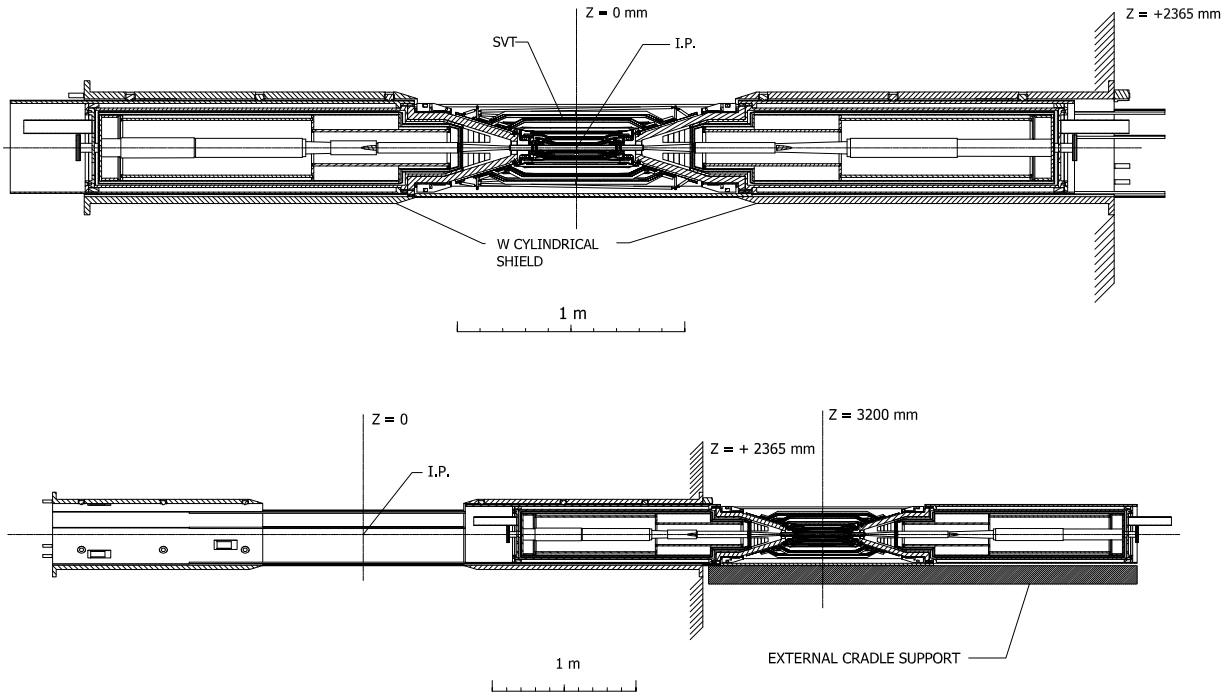

Figure 6.46: Quick demounting operation: a longitudinal section in the y-z plane of the IR system in the initial (top) and final (bottom) position.

external tube, the temporary cage is cylindrically shaped in three independent separate sector, confined in a radial space of about 2 cm between the external tube and the cylindrical shield. The temporary cage sectors are made in a metal sandwich structure with very high flexural resistance. Each temporary cage sector is moved towards the IP position supported by two removable beam-rails mounted and embedded in the cylindrical shield. The beam-rails have a length such to be fixed on the opposite cylindrical shields in order to support the temporary cage sector. The temporary cage sector has a special mechanical connection on the front side in order to perform a coupling in a secure conical way on the backward conical shield flange. On the backward side it has a special radial bushing device able to be fixed to the forward conical flange avoiding any mechanical stress to the SVT detector. The temporary cage sector fixing screws are tighten with a long special screw driver by acting at the working area in front of the forward end of the detector and in front of the Horse Shoes region (backward side). A mechanical Support Cradle Facility has the function of rails prolongation and support for the IR Assembly when it is slided in the final working position outside the forward end of the Super*B* detector (see Fig. 6.46). An artistic view of the IR Assembly showing some components of the installation/removal operation is represented in Fig. 6.47. To enable the sliding of the IR assembly an extra-length and flexible pipe connections have to be foreseen for the cryogenic service to the Cryostat Final Focus Superconductor Magnets. Monitoring position devices are planned to be installed on the cylindrical backward and forward Shields in order to control the distances of the various components during the mounting-demounting operations. Also a strain-gage set is planned to be mounted on the Temporary Cage

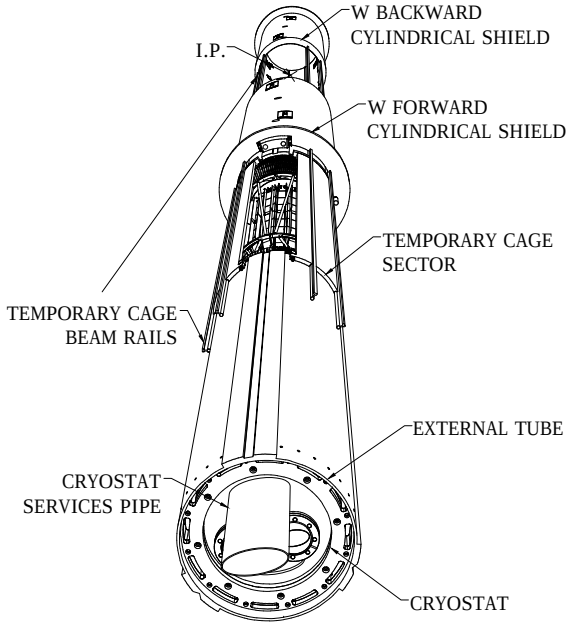

Figure 6.47: An artistic view of the IR Assembly outside the forward end of the Super$B$ detector, showing some components used for the installation/removal operation.

Sectors to monitor the mechanical stress in the different positions during the translation.

6.7.7 Detector Placement and Survey

(Need to implement comments on this section from NN/GR)

The SVT must provide spatial resolution of the order of 10 μm. The final location of each of the wafers relative to each other (local alignment) and to the DCH (global alignment) will be determined by alignment with charged-particle tracks. This requires a certain degree of overlap of the module within a layer. There must be overlap in z as well as ϕ, so as to accurately locate the z position of the wafer in a single module with respect to each other.

Mechanical tolerance and measurements must be such that the process of detector alignment with charged-particle tracks converges in a reasonable time. In BaBar the optical survey precision was estimated to be 5 mum in the wafer plane and 20 mum out of the plane.

This leads to the requirement that the relative position of the various wafers be stable to the 5 μm level over long periods of time (months or more). The position of the entire detector structure with respect to the DCH can be followed more easily, so that variations on the order of few hours can be tracked.

The silicon wafer relative positions should be stable in order avoid frequent local alignments with tracks. Preliminary calculation of the thermal expansion of the entire structure predict on the order of 1 μm/°C over the length of the active region of the detector. If the temperature inside the SVT region is maintained constant within 1 °C, thermal expansion is not a problem.

6.7.8 Detector Monitoring

6.7.8.1 Position Monitoring System

Although the final placement of the silicon wafer will be measured and monitored with charged-particle tracks which traverse the silicon detector and drift chamber, two displacement monitor system will be designed to measure relative changes in the position of the silicon detector with respect to the machine elements and the cylindrical shield. One displacement monitoring system will be used to monitor relative position during transportation of the IR Assembly with the silicon detector inside it and during data taking. This system consist of either capacitive displacement monitor or LED-photodiode reflection monitor which are sensitive to relative displacements between the silicon detector and the machine components such as the beam pipe, magnet and Cylindrical Shield.
In addition, a laser system will monitor displacement of the outer layer of detectors with respect to the drift chamber during the data taking. Given that the SVT layers are not mounted on the same support as the drift chamber, it is possible that motion between the two will occur. To monitor this motion, short infrared lasers pulse are brought in with fiber optics (e.g., 50 μm core diameter) which are attached to the drift chamber. The laser light shines in the active region

and reach the outer layers of the silicon detector.

6.7.8.2 Radiation Monitoring: in MDI

To protect the silicon detector system against potentially damaging beam losses and to monitor the total radiation dose that the detectors and electronics receive, diamond detectors will be installed on a crown around the beam-pipe, in the vicinity of Layer0 . If the radiation dose exceed a certain threshold, a beam dump signal will be sent to the accelerator control-room. This sort of radiation protection system is already been used in the Babar experiment.

6.7.9 R&D Program

The following R&D projects are planned before the final design of the SVT mechanical configuration is finalized.

6.7.9.1 Cables

Prototypes of the cable from the hybrid to the transition card will be constructed. This allows proof the detail of cable routing and mechanical robustness. It will also allows the electrical properties to be measured to verify simulations.

6.7.9.2 Hybrid

Realistic mechanical module of the high Intensity interconnect (HDI) are required. The HDI is a critical element both in the cooling of the electronics and the mounting of the detector modules. Models will be tested for heath transfer capability and for the module mounting schemes.

6.7.9.3 Be Beam pipe

A full scale of Be beam pipe will be constructed with the cooling design actually available. The part in Be will be realized in Aluminum light alloy and the cooling and structural test performed will be renormalized towards Be material.

6.7.9.4 Layer0 Module

A full-scale mock-up of the Layer0 module and its cooled supporting flanges will be constructed . It will be used to verify thermal stability calculations and to investigate the effect of nonuniform beam pipe cooling. It will also be used to design Layer0 assembly fixture and test and practice the assembly technique.

6.7.9.5 Inner layer sextant

A full-scale mock-up of the L1-L2 layer sextants will be constructed. It will also be used to test and practice assembly technique.

6.7.9.6 Arch modules

Full-scale mock-ups of the arch detector module will also be constructed and used with the prototype cones to verify mechanical stability and mounting techniques.

6.7.9.7 Cones and space frame

A set of prototype cones and space frame will be built to provide realistic test of cooling, mechanical rigidity and thermal stability. In addition they will be used to design L1-L5 assembly fixture and test the assembly technique.

6.7.9.8 Full-scale model of IR and Cylindrical Shield

A model of the entire I.R. Assembly with the beam pipe near the I.P. and forward/backward W cylindrical shield will be constructed. This will aid in identifying interference problems and verifying the mounting schemes. It will also provide a test bench for the design of various installation fixtures.

6.7.9.9 Quick Demounting test

Using the full scale model of IR assembly and cylindrical shield it will be also performed a test for the Quick Demounting operation and relative components. Sensor gauges will be installed on the SVT mock up module to measure stress and deformation eventually induced by relative movements of the forward/backward cryostat, although blocked by temporary cage sectors. Also the translation mount/demount stages and blocking IR assembly with respect the Cylindrical shield will be tested .

6.8 Layer0 Upgrade Options

With the machine operated at full luminosity, the layer 0 of the silicon vertex tracker may benefit from upgrading to a pixellated detector. This solution can actually provide some significant advantages with respect to the baseline striplet option (see section 6.3.7). In particular

- the occupancy per detector element from machine background is expected to fall to a few kHz, with a major impact on the speed specifications for the front-end electronics, mainly set by the background hit rate in the case of the striplet readout chip;
- better accuracy in vertex reconstruction can be achieved in presence of relatively high background; the shape of the pixel can be optimized in such a way to reduce the sensor pitch in the z direction while keeping the area in the range of 2500-3000 μm^2, which guarantees enough room for sparse readout functionalities.

A few technology alternatives for pixel detector fabrication are being investigated and R&D activities are in progress to understand advantages and potential issues of the different options.

6.8.1 Technology options

Following is a description of the technology options that are being considered for the upgrade of the SuperB SVT innermost layer.

6.8.1.1 Hybrid pixels

Hybrid pixel technology has reached quite a mature stage of development. Hybrid pixel detectors are currently used in the LHC experiments [48, 49, 50, 51], with pitch in the range from 100 μm to a few hundred μm, and miniaturization is being further pushed forward in view of the upgrade of the same experiments at the High Luminosity LHC (HL-LHC) [52, 53, 54]. Hybrid pixel systems are based on the interconnection between a sensor matrix fabricated in a high resistivity substrate and a readout chip. Bump-bonding with indium or indium-tin or tin-lead alloys is the mainstream technology for readout chip-to-sensor interconnection. The design of a hybrid pixel detector for the SVT innermost layer has to meet some challenging specifications in terms of material budget and spatial resolution. Since the readout chip and the sensor are laid one upon the other, hybrid pixels are intrinsically thicker detectors than microstrips. Interconnect material may further degrade the performance, significantly increasing the radiation length equivalent thickness of the detector. As far as the readout and sensor chips are concerned, substrate thinning to 100-150 μm and subsequent interconnection are within present technology reach. Further thinning may pose some issues in terms of mechanical stability and, as the detector thickness is reduced, of signal-to-noise ratio and/or front-end chip power dissipation. Concerning interconnection, the vertical integration processes currently under investigation in the high energy physics community might help reduce the amount of material. Among the commercially available technologies, the ones provided by the Japanese T-Micro (formerly known as ZyCube), based on so called micro-bumps, and by the US based company Ziptronix, denoted as direct bonding technique, seem the most promising [55]. The Fraunhofer EMFT has developed a bonding technique called SLID and based on a very thin eutectic Cu-Sn alloy to interconnect the chips [56]. The spatial resolution constraints set a limit to the area of the elementary readout cell and, as a consequence, to the amount of functionalities that can be included in the front-end electronics. A planar, 130 nm CMOS technology may guarantee the required density for data sparsification and in-pixel time stamping in a 50×50 μm^2 pixel area (as already observed, a different aspect ratio might be preferred to improve the resolution performance in one particular direction). The above mentioned interconnection techniques can fully comply with the detector pitch requirements (in the case of the T-Micro technology, pitches as small as 8 μm can be achieved). A fine pitch (30 μm minimum), more standard bump-bonding technology is also provided by IZM. This technology has actually been successfully used to bond the SuperPIX0 front-end chip (to be described later

on in this section) to a 200 μm thick pixel detector.
Denser CMOS technologies (belonging to the 90 or 65 nm technology) can be used to increase the functional density in the readout electronics and include such functions as gain calibration, local threshold adjustment and amplitude measurement and storage. In this case, costs for R&D (and, eventually, production) would increase significantly. Vertical integration (or 3D) CMOS technologies may represent a lower cost alternative to sub-100 nm CMOS processes. The technology cross section shown in Fig. 6.48, in particular, points to the main features of the extremely cost-effective process provided by Tezzaron Semiconductor [57] which was used for the design of the SDR1 chip. The Tezzaron process can be used to vertically integrate two (or more) layers, specifically fabricated and processed for this purpose by Chartered Semiconductor (now Globalfoundry) in a 130 nm CMOS technology. In the Tezzaron/Chartered process, wafers are face-to-face bonded by means of thermo-compression techniques. Bond pads on each wafer are laid out on the copper top metal layer and provide the electrical contacts between devices integrated in the two layers. The top tier is thinned down to about 12 μm to expose the through silicon vias (TSV), therefore making connection to the buried circuits possible. Among the options available in the Chartered technology, the low power (1.5 V supply voltage) transistor option is considered the most suitable for detector front-end applications. The technology also provides 6 metal layers (including two top, thick metals), dual gate option (3.3 V I/O transistors) and N- and P-channel devices with multiple threshold voltages. The main advantages deriving from a vertical integration approach to the design of a hybrid pixel front-end chip can be summarized as follows:

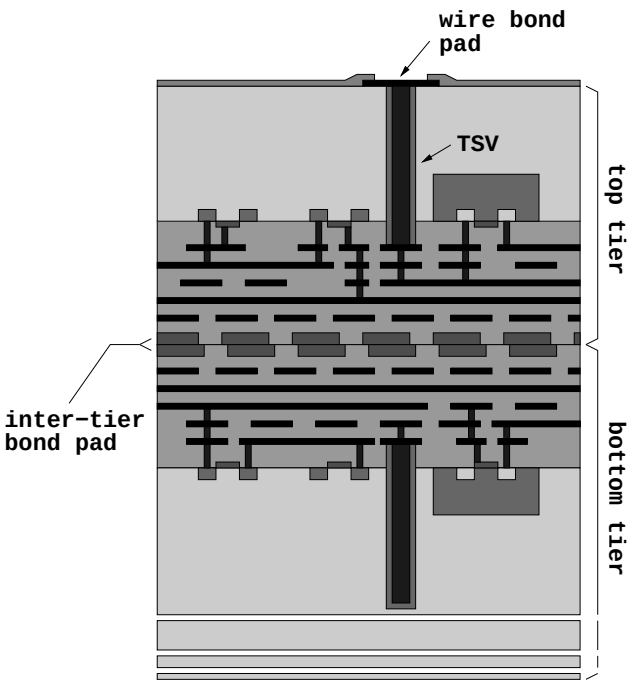

Figure 6.48: cross-sectional view of a double-layer 3D process.

- since the effective area is twice the area of a planar technology from the same CMOS node, a better trade-off can be found between the amount of integrated functionalities and the detector pitch;
- separating the digital from the analog section of the front-end electronics can effectively prevent digital blocks from interfering with the analog section and from capacitively coupling to the sensor through the bump bond pad.

The design of a 3D front-end chip for pixel detectors is in progress in the framework of the VIPIX experiment funded by INFN [58].

6.8.1.2 Deep N-well CMOS monolithic sensors

Deep N-well (DNW) CMOS monolithic active pixel sensors (MAPS) are based on an original design approach proposed a few years ago and developed in the framework of the SLIM5 INFN experiment [41]. The DNW MAPS approach takes advantage of the properties of triple well structures to lay out a sensor with relatively large area (as compared to standard three transistor MAPS [59]) read out by a classical processing chain for capacitive detectors. As shown by the technology cross section in Fig. 6.49, the

sensor, featuring a buried N-type layer with N-wells (NW) on its contour according to a typical deep N-well scheme, collects the charge released by the impinging particle and diffusing through the substrate, whose active volume is limited to the uppermost 20-30 μm thick layer below the collecting electrode. Therefore, within this extent, substrate thinning is not expected to significantly affect charge collection efficiency, while improving momentum resolution performance in charged particle tracking applications. As mentioned above, DNW MAPS have been proposed chiefly to comply with the intense data rates foreseen for tracking applications at the future high energy physics (HEP) facilities. The area taken by the deep N-well collecting electrode can actually be exploited to integrate the NMOS parts of the analog front-end inside the internal P-well. A small amount of standard N-well area can be used for PMOS devices, instrumental to the design of high performance analog and digital blocks taking full advantage of CMOS technology properties. In this way, both analog functions, such as signal shaping, and digital functions, such as time stamping and data storing, buffering and sparsification, can be included in the pixel operation. Note that the presence of N-wells other than the sensor is instead strongly discouraged in standard MAPS design, where the operation of the tiny collecting electrode would be jeopardized by the presence of any N-type diffusion in the surrounding. Based on the concept of the DNW monolithic sensor, the MAPS detectors of the Apsel series (see Section 6.8.2.2), which are among the first monolithic sensors with pixel-level data sparsification [60, 61], have been developed in a planar, 130 nm CMOS technology. In 2008, the Apsel4D, a DNW MAPS with 128×32 elements has been successfully tested at the Proton Synchrotron facility at CERN [62]. More recently, vertical integration technologies, like the ones discussed in the previous section for hybrid pixels, have been considered for the design of 3D DNW monolithic sensors. Some specific advantages can derive from the vertical integration approach to DNW MAPS. In particular, all the

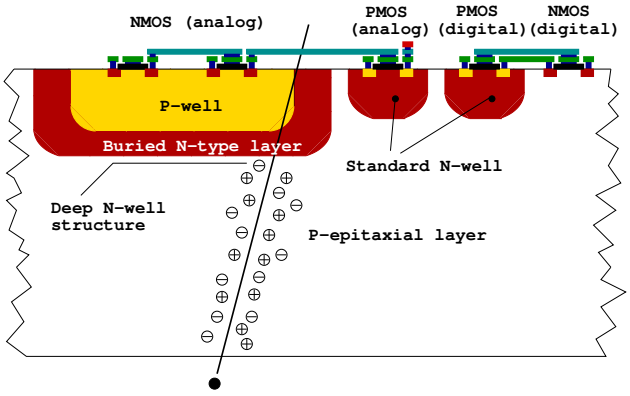

Figure 6.49: simplified cross-sectional view of a DNW MAPS. NMOS devices belonging to the analog section may be built inside the sensor, while the other transistors cover the remaining area of the elementary cell, with PMOSFETs integrated inside standard N-wells.

PMOS devices used in digital blocks can be integrated in a different substrate from the sensor, therefore significantly reducing the amount of N-well area (with its parasitic charge collection effects) in the surroundings of the collecting electrode and improving the detector charge collection efficiency (CCE). The first prototypes of 3D DNW MAPS [63, 64] have been submitted in the framework of the 3D-IC collaboration [65]. Characterization has started in the last quarter of 2011.

6.8.1.3 Monolithic pixels in quadruple-well CMOS technology

In DNW MAPS, charge collection efficiency can be negatively affected, although to a limited extent, by the presence of competitive N-wells including the PMOS transistors of the pixel readout chain, which may subtract charge from the collecting electrode. Inefficiency is related to the relative weight of N-well area with respect to the DNW collecting electrode area. An efficiency of about 92% was demonstrated in the above mentioned test beam at CERN [62]. A novel approach for isolating PMOS N-wells has been

made available with a planar 180 nm CMOS process called INMAPS, featuring a quadruple well structure [61]. Fig. 6.50 shows a simplified cross section of a pixel fabricated with the INMAPS process. By means of an additional processing step, a high energy deep P-well implant is deposited beneath the PMOS N-well (and not under the N-well diode acting as collecting electrode). This implant creates a barrier to charge diffusing in the epitaxial layer, preventing it from being collected by the positively biased N-wells of in-pixel circuits and enabling a theoretical charge collection efficiency of 100%. The NMOS transistors are designed in heavily doped P-wells located in a P-doped epitaxial layer which has been grown upon the low resistivity substrate. Epitaxial layers with different thickness (5, 12 or 18 μm) and resistivity (standard, about 50 Ω·cm, and high resistivity, 1 kΩ·cm) are available. The epitaxial layer is obviously expected to play an important role in improving charge collection performance. Actually, carriers released in the epitaxial layer are kept there by the potential barriers at the P-well/epi-layer and epi-layer/substrate junctions. A test chip, including several different test structures to characterize both the readout electronics and the collecting electrode performance has been submitted in the third quarter of 2011. Results from the preliminary characterization of the prototypes are discussed in Section 6.8.2.3.

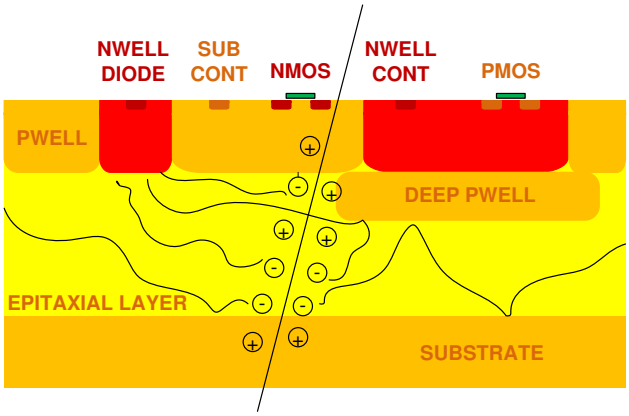

Figure 6.50: cross-sectional view of the INMAPS CMOS technology; emphasis is put on the deep P-well layer.

6.8.2 Overview of the R&D activity

6.8.2.1 Front-end electronics for hybrid pixel detectors in 130 nm CMOS technology

A prototype hybrid pixel detector named SuperPIX0 has been designed as a first iteration step aimed at the development of a device to be used for the layer0 upgrade. The main novelties of this approach are the sensor pitch size (50×50 μm") and thickness (200 μm) as well as the custom front-end chip architecture providing a sparsified and data-driven readout. The SuperPIX0 pixel sensor is made of n-type, Float Zone, high-resistivity silicon wafers, with a nominal resistivity larger than 10 kΩ·cm. The SuperPIX0 chip, fabricated in the STMicroelectronics 130nm CMOS technology, is composed of 4096 channels (50×50 μm^2) arranged into 128 columns by 32 rows. Each cell contains an analog charge processor (shown in Fig. 6.51) where the sensor charge signal is amplified and compared to a chip-wide preset threshold by a discriminator. The in-pixel digital logic, which follows the comparator, stores the hit in an edge-triggered set reset flip-flop and notifies the periphery of the hit. The charge sensitive amplifier uses a single-ended folded cascode topology, which is a common choice for low-voltage, high gain amplifiers. The 20 fF MOS feedback capacitor is discharged by a constant current which can be externally adjusted, giving an output

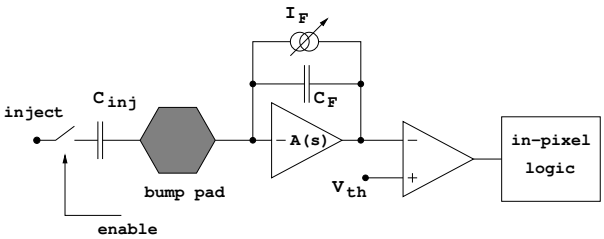

Figure 6.51: block diagram of the analog front-end electronics for the elementary cell of the SuperPIX0 readout chip.

pulse shape that is dependent upon the input charge. The peaking time increases with the collected charge and is in the order of 100 ns for 16000 electrons injected. The charge collected in the detector pixel reaches the preamplifier input via the bump bond connection. Alternatively, a calibration charge can be injected at the preamplifier input through a 10 fF internal injection capacitance so that threshold, noise and crosstalk measurements can be performed. The calibration voltage step is provided externally by a dedicated line. Channel selection is performed by means of a control section implemented in each pixel. This control block, which is a cell of a shift register, enables the injection of the charge through the calibration capacitance. Each pixel features a digital mask used to isolate single noisy channel. This mask is implemented in the readout logic. The input device (whose dimensions were chosen based on detection efficiency optimization criteria [66]) featuring an aspect ratio W/L=18/0.3 and a drain current of about 0.5 μA, is biased in the weak inversion region. A non-minimum length has been chosen to avoid short channel effects. The PMOS current source in the input branch has been sized to have a smaller transconductance than the input transistor. The analog front-end cell uses two power supplies. The analog supply (AVDD) is referenced to AGND, while the digital supply is referenced to DGND. Both supplies have a nominal operating value of 1.2 V. Since single-ended amplifiers are sensitive to voltage fluctuations on the supply lines, the charge preamplifier is connected to the AVDD. The threshold discriminator and voltage references are connected to the AVDD and AGND as well. The in-pixel digital logic is connected to the digital supply. The substrate of the transistors is connected to a separate net and merged to the analog ground at the border of the matrix. The SuperPIX0 chip has been fabricated in a six metal level technology. Special attention has been paid to layout the channel with a proper shielding scheme. Two levels of metal have been used to route the analog signals, two for the digital ones and two for distributing the analog and digital supplies. The

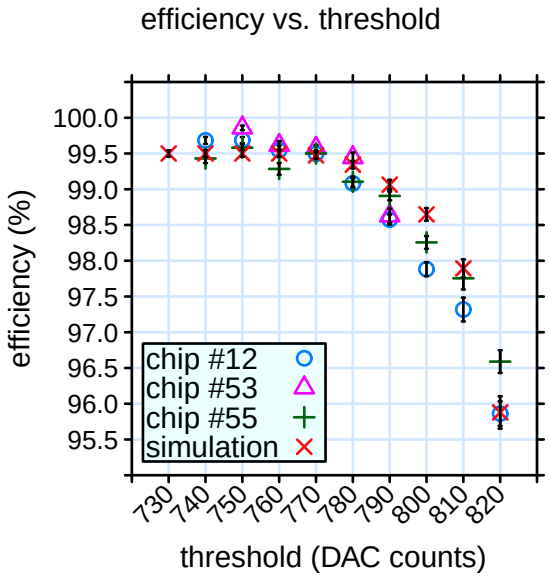

Figure 6.52: Superpix0 efficiency as a function of the voltage discriminator threshold in the case of normal incidence angle.

supply lines, at the same time, shield the analog signals from the digital activity. For nominal bias conditions the power consumption is about 1.5 μW per channel. More details on the design of the analog front-end can be found in the literature [67]. The measured threshold dispersion in the chip is around 490 e- with an average pixel noise of about 60 e- (without the sensor connected). Since the threshold dispersion is a crucial characteristic to be considered in order to meet the required specifications in terms of noise occupancy and efficiency, circuits for threshold fine-adjusting have to be implemented in the next version of the chip. These results have been extracted using the gain measured with an internal calibration circuit, implemented in the pixel, injecting a charge from 0 to 12 fC in each channel preamplifier. An average gain of about 40 mV/fC with a dispersion at the level of 5% has been obtained. The front-end chip has been connected by bump-bonding to a high resistivity pixel sensor matrix of 200 μm thickness. The bump-bonding process has been

performed by the Fraunhofer IZM with electroplating of SnAg solder bumps. Measurements on the bump-bonded chip show a working sensor and a good quality of the interconnection at 50 μm pitch. The measured gain and threshold dispersion are compatible with the ones extracted from the front-end chip only. We observe an increase of the noise of around 20%, up to about 76 e-, due to the added capacitive load of the sensor connected. The Superpix0 chip, bump bonded to a high resistivity silicon pixel detector, was also tested on the beam of the Proton Synchrotron (PS) at CERN. The measured efficiency is shown in Fig. 6.52 as a function of the voltage threshold in the discriminator. Efficiencies larger than 99% were obtained for thresholds up to 1/4 of a MIP, corresponding to more than 10 times the pixel noise.

6.8.2.2 The Apsel DNW MAPS series

DNW MAPS in planar CMOS technology

Deep N-well MAPS were proposed a few years ago as possible candidates for charged-particle tracking applications. The Apsel4D chip is a 4096 element prototype MAPS detector with data-driven readout architecture, implementing twofold sparsification at the pixel level and at the chip periphery. In each elementary cell of the MAPS matrix integrated in the Apsel4D chip, a mixed signal circuit is used to read out and process the charge coming from a deep N-well (DNW) detector. This design approach, relying upon the properties of the triple well structures included in modern CMOS processes, has been described in Section 6.8.1.2. In the so called DNW MAPS is integrated with a relatively large (as compared to standard three transistor MAPS) collecting electrode, featuring a buried N-type layer, with a classical readout chain for time invariant charge amplification and shaping. In the Apsel4D prototype, the elementary MAPS cells feature a 50 μm pitch and a power dissipation of about 30 μW/channel. The block diagram of the pixel analog front-end electronics is shown in Fig. 6.53. The first block of the processing chain, a charge preamplifier, uses a complementary cascode scheme as its forward gain stage, and is responsible for most of the

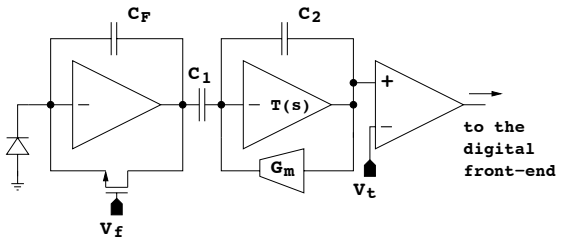

Figure 6.53: block diagram of the analog front-end electronics for the elementary cell of the Apsel4D prototype.

power consumption in the analog section. The feedback capacitor C_F is continuously reset by an NMOS transistor, biased in the deep subthreshold region through the gate voltage V_f. The preamplifier input device, featuring an aspect ratio $W/L = 14\ \mu m/0.25\mu m$ and a drain current of 20 μA, was optimized for a DNW detector about 900 μm^2 in area and with a capacitance C_D of about 300 fF. The charge preamplifier is followed by a CR-RC, bandpass filtering stage, with open loop gain $T(s)$, featuring a programmable peaking time which can be set to 200 or 400 ns. C_1 is a differentiating capacitor at the CR-RC shaper input, while G_m and C_2 are the transconductance and the capacitance in its feedback network. A discriminator is used to compare the processed signal to a global voltage reference V_t, thereby providing hit/no-hit information to the cell digital section. More details on the design of the analog front-end can be found in the literature [68]. A dedicated readout architecture to perform on-chip data sparsification has been implemented in the Apsel4D prototype. The readout logic provides the timestamp information for the hits. The timestamp, which is necessary to identify the event to which the hit belongs, is generated by the bunch-crossing signal. The key requirements in this development are 1) to minimize logical blocks with PMOS inside the active area, thus preserving the collection efficiency, 2) to reduce to a minimum the number of digital lines crossing the sensor area, in particular its dependence on detector size to allow the readout scalability to larger matrices and to reduce the residual

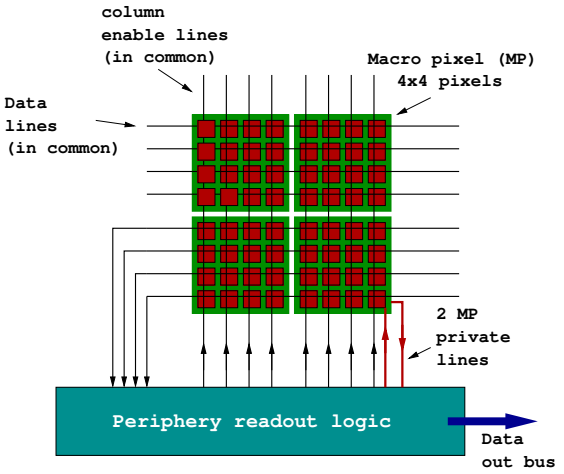

Figure 6.54: schematic concept of the architecture for MAPS matrix readout.

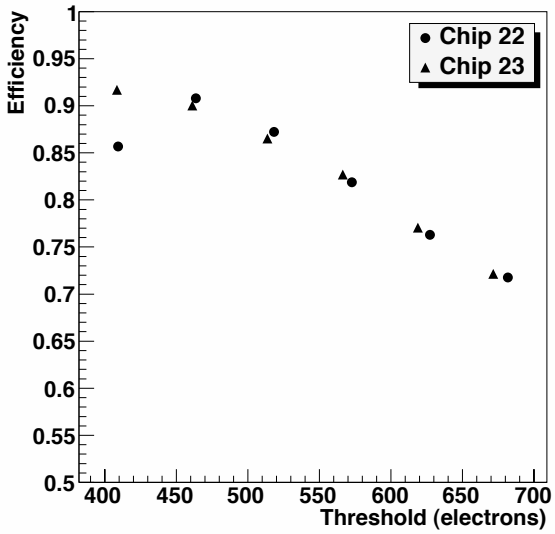

Figure 6.55: efficiency results for two MAPS detectors (the statistical uncertainty on each point is smaller than the size of the plotting symbol).

crosstalk effects, and 3) to minimize the pixel dead time by reading hit pixels out of the matrix as soon as possible. With these criteria a readout logic in the periphery of the matrix has been developed, as schematically shown in Fig 6.54. To minimize the number of digital lines crossing the active area the matrix is organized in MacroPixels (MP) with 4x4 pixels. Each MP has only two private lines for point-to-point connection to the peripheral logic: one line is used to comunicate that the MP has got hits, while the second private line is used to freeze the MP until it has been read out. When the matrix has some hits, the columns containing fired MPs are enabled, one at a time, by vertical lines. Common horizontal lines are shared among pixels in the same row to bring data from the pixels to the periphery, where the association with the proper timestamp is performed before sending the formatted data word to the output bus. The chip has been designed with a mixed mode design approach. While the pixel matrix has a full custom design and layout, the periphery readout architecture has been synthesized in standard cell starting from a VHDL model; automatic place-and-route tools have been used for the layout of the readout logic [60]. The chip has been designed to run with a readout clock up to 100 MHz (20 MHz in test beam), a maximum matrix readout rate of 32 hit pixels/clock cycle and a local buffer of maximum 160 hits to minimize the matrix sweep time. Apsel4D has been successfully tested with 12 GeV/c protons at the PS-T9 beam line at CERN [**?**]. The efficiency of the DNW MAPS as a function of threshold for two devices with different silicon thickness (Chip 22 is 300 μm thick, while Chip 23 is 100 μm thick) has been measured. Figure 6.55 shows the measured hit efficiency, determined as described in a published work [62].

At the lowest thresholds a maximum efficiency of approximately 92% and the expected general behavior of decreasing efficiency with increasing threshold can be observed. The noise occupancy for this range of thresholds was found to vary from 2.5×10^{-3} to 1×10^{-6}. The low efficiency observed for Chip 22 at the lowest threshold appears to have been caused by a readout malfunction. Investigations have shown that a small localized area on the detector had very low efficiency, while the rest of the detector behaved normally with good efficiency. Additionally, the efficiency for detecting hits as a function of the track extrapolation point *within a pixel* has been

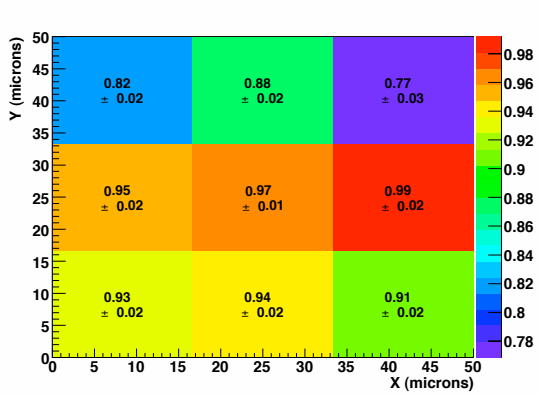

Figure 6.56: hit effiencies measured as a function of position within the pixel (the picture, which is not to scale, represents a single pixel divided into nine sub-cells).

studied. Since the pixel has internal structure, with some areas less sensitive than others, we expect the efficiency to vary as a function of position within the cell. The uncertainty on the track position, including multiple scattering effects is roughly 10 microns, to be compared to the 50 μm pixel dimension. The pixel has been divided into nine square sub-cells of equal area and the hit efficiency within each sub-cell has been measured. The efficiencies thus obtained are "polluted" in some sense due to the migration of tracks among cells. We obtain the true sub-cell efficiencies by unfolding the raw results, taking into account this migration, which we characterize using a simple simulation. The result can be seen in Figure 6.56, where the efficiency measured in each sub-cell is shown. A significant variation in sensitivity within the pixel area can be observed, as expected. In particular, the central region is seen to be virtually 100% efficient, while the upper part of the pixel, especially the upper right-hand sub-cell, shows lower efficiency due to the presence of competitive n-wells. The position of this pixel map relative to the physical pixel is not fixed. This is a consequence of the alignment, which determines the absolute detector position by minimizing track-hit residuals, as described above. If the pixel area is not uniformly efficient, the pixel center as determined by the alignment will correspond to the barycenter of the pixel efficiency map. Thus, it is not possible to overlay Figure 6.56 on a drawing of the pixel layout, without adding additional information, for example a simulation of internal pixel efficiency. The efficiency as a function of position on the MAPS matrix has also been investigated, since disuniformity could indicate inefficiencies caused by the readout. Generally, a uniform efficiency across the area of the MAPS matrix was observed. The intrinsic resolution σ_{hit} for the MAPS devices was measured as already described in a published paper [**?**]. The expected resolution for cases where the hit consists of a single pixel is given by $50/\sqrt{12} = 14.4$ μm, where 50 microns is the pixel dimension.

DNW MAPS in 3D CMOS technology As already mentioned in Section 6.8.1.2, the DNW monolithic sensors have been designed and fabricated also in the Tezzaron/Globalfoundry technology, based on the vertical integration of two 130 nm CMOS layers. The conceptual step from the DNW MAPS in a planar CMOS technology to its vertically integrated version is illustrated in Fig 6.57, showing a cross-sectional view of a

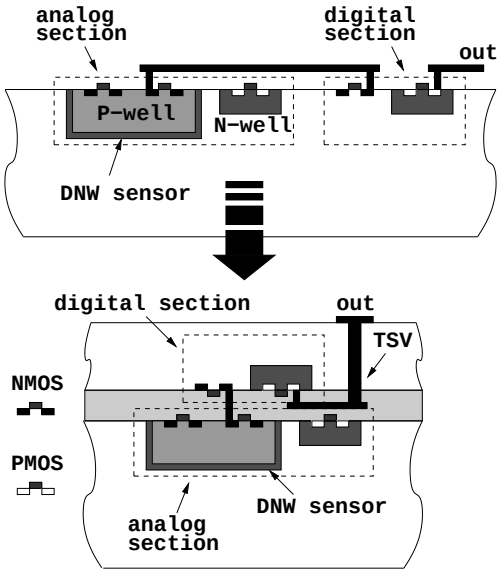

Figure 6.57: cross-sectional view of a DNW CMOS MAPS: from a planar CMOS technology to a 3D process

2D MAPS and of its 3D translation. The prototype include two small 3×3 matrices for analog readout and charge collection characterization and a larger one, 8×32 in size, equipped with a digital readout circuit with data sparsification and time stamping features. The pixel pitch is 40 μm. A number of different problems were encountered during fabrication of the first device batch. Among them, the misalignment between the two tiers prevented the analog and digital sections in each pixel cell to communicate to each other [69]. At the time of the TDR writing, other 3D wafers are being processed and devices from the first run are under characterization.

Fig. 6.58 shows the analog front-end channel of the 3D DNW MAPS (quite similar to the analog processor of the SuperPIX0 chip, see Fig. 6.51), simply consisting of a charge preamplifier, whose bandwidth was purposely limited to improve the signal-to-noise ratio (so called shaperless configuration). Equivalent noise charge of between 30 and 40 electrons (in good agreement with circuit simulations) and a charge sensitivity of about 300 mV/fC (a factor of 2 smaller than in simulations) were obtained from prototype characterization. Fig. 6.59 shows the ^{90}Sr spectrum detected by the cluster of 3×3 pixels in a small matrix.

The most probable value of the collected charge is about 100 electrons. Pseudo-3D DNW MAPS (here, the term pseudo-3D refers to devices consisting of just one tier but suitable for 3D integration) have been tested on the PS

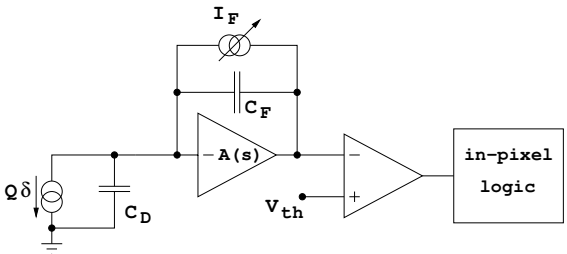

Figure 6.58: block diagram of the analog front-end electronics for the elementary cell of the 3D DNW MAPS of the apsel family.

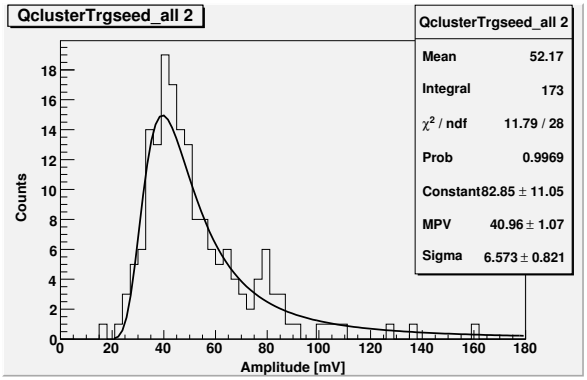

Figure 6.59: spectrum of a ^{90}Sr source detected by a 3×3 matrix of 3D DNW MAPS.

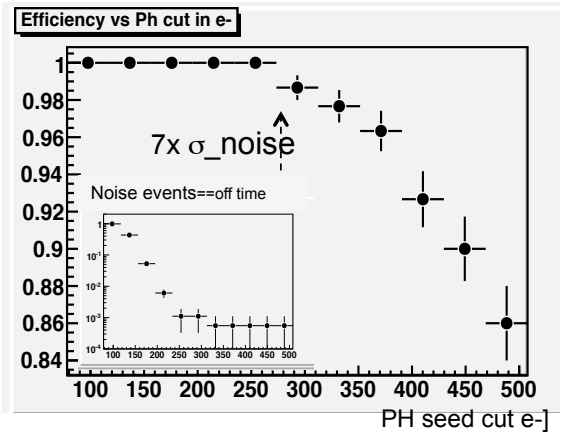

Figure 6.60: Detection efficiency of a pseudo-3D DNW MAPS as a function of the cut on the pulse height of the detected events. The efficiency is 1 up to threshold values of 7 times the pixel noise.

beam at CERN. Very promising results were obtained in terms of detection efficiency, as displayed in Fig. 6.60.

6.8.2.3 The Apsel4well quadruple well monolithic sensor

As already mentioned in section 6.8.1.3, a test chip in the INMAPS, 180 nm CMOS technology, called Apsel4well, has been submitted in Au-

gust 2011. The chip includes four 3×3 matrices with different number (2 or 4) of the collecting electrodes (each consisting of a 1.5 μm×1.5 μm N-well diffusion), with or without the shielding deep P-well implant, with or without enclosed layout transistors as the input device of the charge preamplifier. The prototype also contains a 32×32 matrix with sparsified digital readout. The test of the first version of the chip, featuring a 5 μm thick epitaxial layer with standard resistivity (about 10 Ω·cm), was in progress during the writing of this TDR. Monolithic sensors with a thicker (12 μm) and more resistive (about 1 kΩ·cm) are expected to be out of the foundry by June 2012. Fig. 6.61 shows the analog readout channel of the Apsel4well

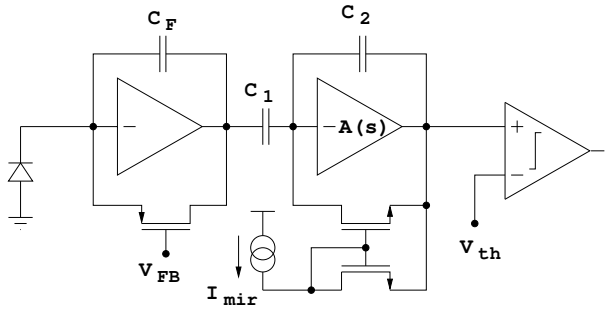

Figure 6.61: block diagram of the analog front-end electronics for the elementary cell of Apsel4well monolithic sensor.

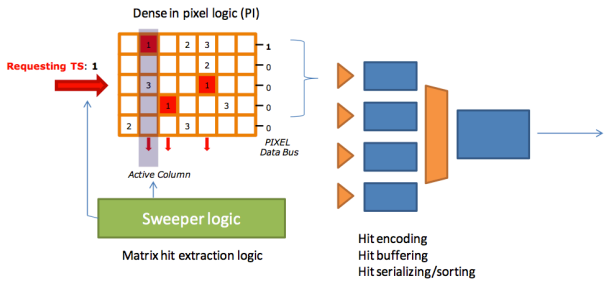

Figure 6.62: conceptual view of the digital readout architecture of the Apsel4well chip operated in the triggered mode.

MAPS. It includes a charge preamplifier, a shaping stage with a current mirror in the feedback network and a two-stage threshold discriminator. Several digital blocks are also integrated in each individual pixel element for data sparsification and time stamping purposes. Time from a peripheral Gray counter is distributed to each pixel in the matrix and is latched to a time stamp register upon arrival of a hit. When a timestamp request is sent to the matrix, a pixel FastOR signal activates if the latched timestamp is the same as the requestd one. The columns with an active FastOR signal are enabled and read out in a sequence; 1 clock cycle per column is needed. A conceptual view of the digital readout architecture is shown in Fig. 6.62. Readout circuits can be operated either in triggered or in data-push mode. They take care of encoding, buffering and serializing/sorting the hits retrieved from the sensor matrix. In order to achieve the remarkably high readout frequency set by the SuperB experiment, the architecture can be subdivided in a number of modules, each serving a submatrix. This choice improves the scalability features of the readout section and makes it suitable for experiment scale detectors. Efficiency well in excess of 99% have been obtained in Monte Carlo simulations with hit rates of 100 MHz/cm^2. Fig. 6.63 shows the signal at the shaper output as a response to an input charge signal with varying amplitude. Figures provided by the preliminary experimental characterization of the analog section are very close to simulation data, with a gain of about 960 mV/fC and an equivalent noise charge of about 30 electrons. The plot in Fig. 6.64 represents the collected charge in a Apsel4well pixel (12 μm epitaxial layer thickness, standard resistivity) illuminated with an infrared laser source. The layout of the N-wells (both the collecting electrodes and the N-wells for PMOS transistors) included in the elementary cell is superimposed onto the plot. The position of the collecting electrodes is easily detectable.

6.8.3 Radiation tolerance

Hybrid pixels. The high degree of radiation tolerance of modern CMOS technologies, com-

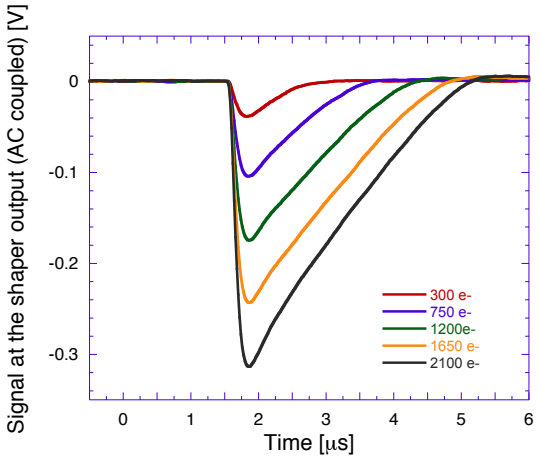

Figure 6.63: signal at the shaper output as a response to an input charge signal with varying amplitude in an Apsel4well sensor.

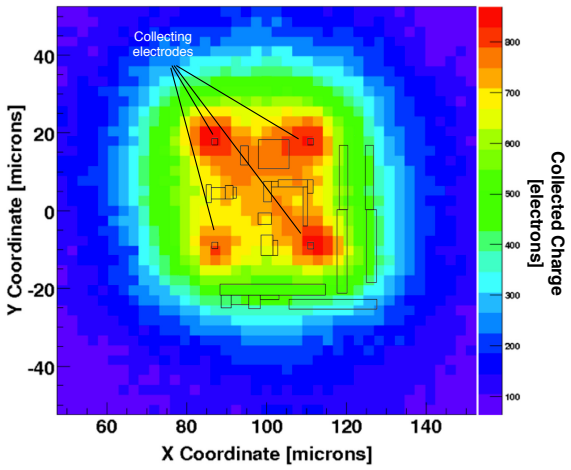

Figure 6.64: collected charge in a Apsel4well pixel illuminated with an infrared laser source.

ing as a byproduct of the aggressive scaling down of device minimum feature size, is having a beneficial impact in high energy physics applications. Beginning with the 130 nm CMOS processes, which entered the sub-3 nm gate oxide thickness regime, direct tunneling contribution to the gate current has assumed a significant role as compared to trap assisted mechanisms [70]. This may account for the very high degree of radiation hardness featured by devices belonging to the most recent technology nodes, which might benefit from relatively fast annealing of holes trapped in the ultrathin gate oxides. Tolerance to a few hundred of Mrad(SiO_2) has been recently proven in front-end circuits for hybrid pixel detectors [52]. Charge trapping in the thicker shallow trench isolation (STI) oxides is considered as the main residual damage mechanism in 130 nm N-channel MOSFETs exposed to ionizing radiation [71, 72], especially in narrow channel transistors [73]. Ionizing radiation was found to affect also the 90 nm and 65 nm CMOS nodes, although to an ever slighter extent, likely due to a decrease in the substrate doping concentration and/or in the STI thickness. As far a as analog front-end design is concerned, ionizing radiation damage mainly results in an increase in low frequency noise, which is more significant in multifinger devices operated at a small current density. This might be a concern in the case of the front-end electronics for hybrid pixel detectors, where the input device of the charge preamplifier is operated at drain currents in the few μA range owing to low power constraints. However, at short peaking times, typically below 100 ns, the effects of the increase in low

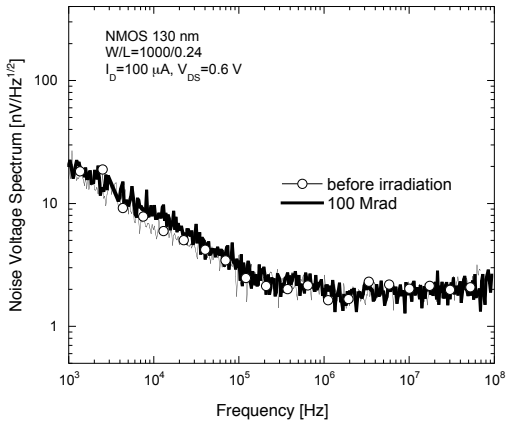

Figure 6.65: noise voltage spectrum for a 130 nm NMOS device with enclosed layout.

frequency noise on the readout channel performance is negligible. Also, use of enclosed layout techniques for the design of the preamplifier input transistor (and of devices in other critical parts of the front-end) minimizes the device sensitivity to radiation [74]. For this purpose, Fig. 6.65 shows the noise voltage spectrum for a 130 nm NMOS transistor with enclosed layout, featuring no significant changes after irradiation with a 100 Mrad(SiO_2) total ionizing dose. On the other hand, CMOS technologies are virtually insensitive to bulk damage, since MOSFET transistor operation is based on the drift of majority carriers in a surface channel.

DNW CMOS MAPS DNW MAPS have been thoroughly characterized from the standpoint of radiation hardness to evaluate their limitations in harsh radiation environments. In particular, the effects of ionizing radiation, with total doses of about 10 Mrad(SiO_2), have been investigated by exposing DNW MAPS sensors to a ^{60}Co source [75]. In that case, some performance degradation was detected in the noise and gain of the front-end electronics and in the sensor leakage current, while no significant change was observed as far as the charge collection properties are concerned. Fig. 6.66 shows the equivalent noise charge as a function of the absorbed dose and after the annealing cycle for a DNW monolithic sensor. The significant change can be ascribed to the increase in the flicker noise of the preamplifier input device as a consequence of parasitic lateral transistors being turned on by positive charge buildup in the shallow trench isolation oxides and contributing to the overall noise. Use of an enclosed layout approach is expected to significantly reduce the effect of ionizing radiation. At the same time, the peak is shifted towards lower amplitude values, as a result of a decrease in the front-end charge sensitivity also due to charge build up in the STI of some critical devices. DNW MAPS of the same kind have also been irradiated with neutrons from a Triga MARK II nuclear reactor to test bulk damage effects [76]. The final fluence, 6.7×10^{12} 1-MeV-neutron equivalent/cm^2, was reached after a few, intermediate steps. The

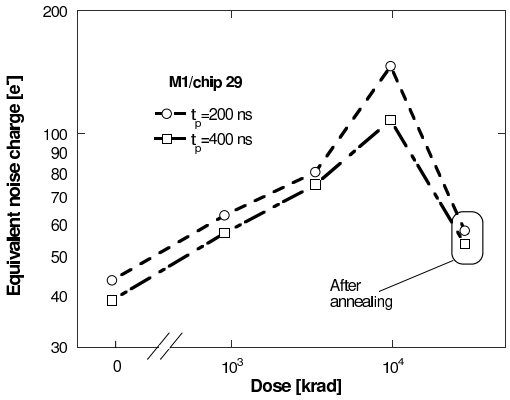

Figure 6.66: equivalent noise charge as a function of the absorbed dose and after the annealing cycle for DNW monolithic sensor. ENC is plotted for the two available peaking times.

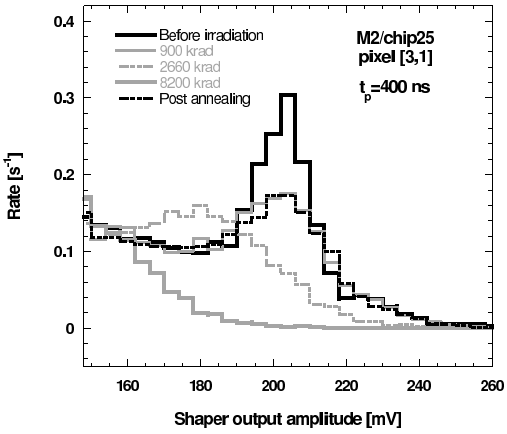

Figure 6.67: event count rate for a DNW monolithic sensor exposed to a ^{55}Fe source before irradiation, after exposure to γ-rays and after the annealing cycle.

devices under test (DUT) were characterized by means of several different techniques, including charge injection at the front-end input through an external pulser, sensor stimulation with an infrared laser and spectral measurements with ^{55}Fe and ^{90}Sr radioactive sources. Neutron irradiation was found to have no sizable effects on the front-end electronics performance. This can be reasonably expected from CMOS devices,

Fig. 6.67 shows event count rate for a DNW monolithic sensor exposed to a ^{55}Fe source before irradiation, after exposure to γ-rays and after the annealing cycle. As the absorbed dose increases, the 5.9 keV peak gets broader as a consequence of the noise increase (in fair agreement with data in Fig. 6.66.

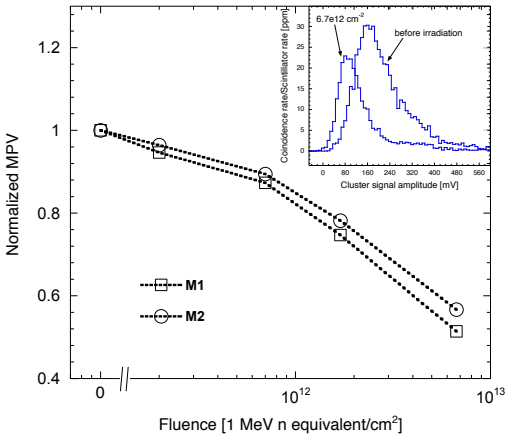

Figure 6.68: most probable value (MPV) of the ^{90}Sr spectra (shown in the inset for one of the tested chips before irradiation and after exposure to a 6.7×10^{12}cm^{-2} neutron fluence) normalized to the pre-irradiation value as a function of the fluence for DNW MAPS with different sensor layout.

whose operation is based on the drift of majority carriers in a surface channel, resulting in a high degree of tolerance to bulk damage. Exposure to neutrons was instead found to affect mainly the charge collection properties of the sensors with a reduction in the order of 50% at the maximum integrated fluence. Fig. 6.68 shows the most probable value (MPV) of the ^{90}Sr spectra normalized to the pre-irradiation value as a function of the fluence for DNW MAPS with different sensor layout. A substantial decrease can be observed, to be ascribed to a degradation in the minority carrier lifetime. A higher degree of tolerance was instead demonstrated in monolithic sensors with high resisitivity (1 kΩ·cm) epitaxial layer [77]. Actually, doping concentration plays a role in determining the equilib- rium Fermi level, which in turn influences the effectiveness of neutron-induced defects as recombination centers [78].

6.9 Services and Utilities - 4 pages

6.9.1 Service and Utilities

The vertex detector requires the following services, which must be brought inside the support tube to a location near the outboard of the W conical shield.

6.9.1.1 Power Supply

The readout ICs require two low-voltage power supply lines (analog and digital); the silicon sensors need the bias voltage. Each power supply board must provide a unique low voltage level for each HDI side (referenced to the bias level of the silicon sensor's side). The further split between the analog and digital power takes place on the HDI. The bias voltage will be raised during the experiment life up to 200 V for the Layer0, to fully deplete the sensor in presence of radiation damage. The power supplies will be specially procured to match the vertex detector specifications to take under control the electronic noise.

6.9.1.2 Cooling water

The readout electronics and transition card will be water cooled. Two sets of water connections for each cone (since each cone is constructed from two halves) and two set for each L0 cold flange (since each flange is constructed from two halves) will be required . In the same way, two water connection for each transition card support is needed (since each transition card support is constructed in two halves). Also a connection for the cooled Be beam pipe is needed. The cooling water will be supplied by a special low volume chiller system dedicated to the vertex detector system.

6.9.1.3 Dry air or nitrogen

The vertex detector requires a dry, stable environment. Cooled and dry air or nitrogen from each side is planned to be flux at the internal of the SVT volume, the needed flow will be planned in relation of the silicon detector temperature required on the base of the background simulation study.

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