INFN/AExxx, LAL-xxx, SLAC-R-xxx

Super$B$ Detector Technical Design Report

Abstract

This report describes the technical design detector for Super$B$.

Contents

13 Subdetector Electronics and Infrastructure

Breton/Marconi/Luitz

The general design approach is to standardize components across the system as much as possible, to use mezzanine boards to isolate sub-system-specific functions differing from the standard design, and to use commercially available common off-the-shelf (COTS) components where viable.

present summary table(s) of data rates, link counts, etc. here

13.1 Subsystem-specific Electronics

13.1.1 SVT Electronics

The full details of the SVT electronics has been given in chap. **??**. Here we recall the main features relevant for the data collection, trigger distribution, system programming and monitoring.

In the baseline SVT option, the detector will be equipped with double sided silicon strips (or striplets) in all layers. Custom front-end chips will be used to read the detector and transform as soon as possible the analog information of a particle traversing the detector in a digital one, characterized by position (layer, strip), energy deposit (signal time over threshold) and time. At least two different custom chips will be developed to handle separately the first layers (expecially layer 0), characterized by high occupancy and short strips (good signal/noise) and the external layers (layer 4 and layer 5) where the main concern is the length of the strips (worse signal/noise) and not the occupancy. Both front-end chips will have the same digital readout architecture and will present the same interface to the DAQ chain, although with different settings. Possible upgrades of the SVT internal layers might require to move to a pixellated detector, for which a different custom front-end chip will be designed. The digital architecture of the pixel chips, partially already develloped, will be based on the same general readout architecture so that from the point of view of trigger and DAQ system they will share the same interface.

Common characteristics of the chips will be capability to work both in data-push and data-pull mode, the presence of internal buffers to allow for a trigger latency up to 10 μs, the use of a periodic signal to time-tag the recorded hits, the serialized hit output and the chip programmability via (two) digital lines.

The full SVT data chain will therefore be able to provide and distribute all the signals, clocks, triggers, time-tagging signal to all the front-end chips in a system-wide synchronous way.

A sketch of the full data chain is given in Fig. 13.1. Starting from the detector and going to the ROM boards, the chain contains: a) the front-end chips mounted on an HDI placed immediately at the end of the sensor modules; b) wire connections to a transition card (signals in both directions and power lines); c) a transition card, placed about 50 cm from the end of the sensors, hosting the wire-to-optical conversion; d) a bidirectional optical line running above 1 Gbit/s; e) a receiver programmable board (front-end board: FEB).

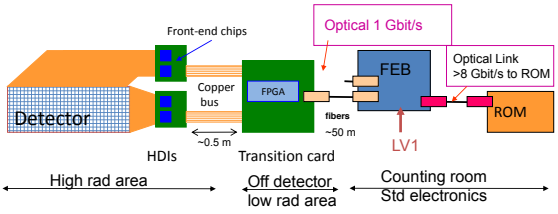

Figure 13.1: SVT Electronics

Each HDI will host from 5 to 14 FE chips servicing a side of the silicon strip module (a so called ROS: Read-Out Section). All the chips will share the same input lines (currently: reset, clock, fastclock, trigger, time-stamp, registerIn) and at least a registerOut line. Programming of the chips can be done individually by addressing a sigle chip or via broadcast command sent to all the chips in an HDI. Hits will be serialized on a programmable number of lines (1,2,4 or 8) using the fastclock signal. Each HDI will have a maximum number of 16 output lines running at the fastclock rate.

The role of the transition card is threefold: a) it will distribute the power to the HDI, b) it will receive all the input signals for the front-end chips via the optical line connected to the programmable board and c) it will ship the data to the programmable board for data acquisition. For the inner layers (0-3) there will be a transition card for each HDI. For the outer layers (4-5) it will be possible to group the data of the two HDIs servicing the two sides of the same silicon sensor into the same transition card, reducing in this way the total number of optical links needed.

The received programmable board (FEB) will handle all the comunications with the front-end chips, the FTCS, the ECS and the upper DAQ systems. Each FEB board will be connected to a variable number of transition cards (up to 12 in the current design). Important and critical roles of this board are the clock distribution, the trigger handling and the data collection. The clock-like signals, such as an experiment clock (about 60 MHz), a fast clock (120-180 MHz) and a time-stamping clock (up to 30 MHz), have to be distributed in a system-wide synchronous manner. Special care will be taken to measure at each power-up the latencies of all the serializers and deserializers in the signal and DAQ chain so that the sent signals can be suitably adjusted in phase in order to have a system synchronous at the sensor (or front-end) level. The time-stamping clock will be used to time-tag the hits and can be different for the inner layers, where the high track rate requires short signal shaping times and short daq time windows and outer layers where the long strips and lower track rates allow for a longer shaping times (800 ns - 1 μs) and longer DAQ windows. The estimation of data volumes have been performed assuming a time-stamping of 30 ns period in the inner and outer layers. The acquisition window will be defined in a time window centered around the L1 trigger window and lasting at least 10 time-stamps (300 ns) for the inner layers and 33 time-stamps (990 ns) or more for the outer layers. The trigger request will be sent to the chips via the optical links. The most important function of the board is to collect the data coming out of the front-end chips both for monitoring and for the final daq. The data will be deserialized in the board and the redundant information will be stripped. A possible further data compression can be envisaged in order to reduce the final data volume. Finally the data will be sent-out via an optical link to a ROM module.

Data volumes. As discussed in the SVT chapter, the data rates and volumes are dominated by the background. In the design of the SVT front-end chips and DAQ chain, the latest background Bruno simulations have been considered at the nominal luminosity and a safety factor of 5 has been applied on the simulation results (design inputs). Due to the strong non-uniformity of the particle rate on the sensors, the front-end chip characteristics have been adapted to the peak hit rates, while the data volumes have been extracted from the mean rates for each layer. To evaluate the data rate a 150 kHz trigger rate with 10 μs of maximum latency and 100 ns of time jitter has been considered. An hit size of 16 bits is used as the FE chip output in the calculation that becomes 20 bits during serialization due to the 8b/10b protocol. The bandwidth needed by a layer0 ROS in a data-push configuration is of the order of 20 Gbit/s/ROS. A difficult-to-handle rate that moved us to consider a fully triggered SVT. In table 13.1 for each layer type the mean expected data load is shown.

For events accepted by the L1 trigger, the bandwidth requirement is only 1 Gbit/s and

Table 13.1: Electronic load on each layer, Readout section and optical link.

Layer	Layer type	chips/ ROS	available channels	Backgnd (MHz/cm^2)	Gbits/trig (per GROS)	FE Board	Event Size (kB)
0	let u	6	768	151	0.99	4	5.3
0	striplet v	6	768	151	0.99	4	5.3
1	strip z	7	896	14.0	0.56	1	2.2
1	strip phi	7	896	16.0	0.64	1	2.6
2	strip z	7	896	9.6	0.54	1	2.2
2	strip phi	7	896	10.3	0.58	1	2.3
3	strip z	10	1280	4.2	0.50	1	2.0
3	strip phi	6	768	3.0	0.36	1	1.5
4a	strip z	5	640	0.28	0.26	1	1.4
4a	strip phi	4	512	0.43	0.38	1	2.0
4b	strip z	5	640	0.28	0.26	1	1.4
4b	strip phi	4	512	0.43	0.40	1	2.1
5a	strip z	5	640	0.15	0.17	1	1.0
5a	strip phi	4	512	0.22	0.24	1	1.5
5b	strip z	5	640	0.15	0.17	1	1.0
5b	strip phi	4	512	0.22	0.24	1	1.5

data from each ROS can be transferred on optical links to the front-end boards (FEB) and then to ROMs through the >8 Gbit/s optical readout links.

13.1.1.1 SVT Summary

In total, the SVT electronics requires 18 FEBs and 18 ROMs, 18 optical links at 10 Gbit/s, 172 links at 1 Gbit/s (radiation hard). The average SVT event size is 88 kB, 30% coming only from the layer0.

Number of Control Links	update
Number of Data Links	update
Total Event Size	88 kbyte
On-Detector Power Consumption	2.6kW check

Table 13.2: SVT summary

13.1.2 DCH Electronics

13.1.2.1 Design Goals

The Super*B* Drift Chamber (DCH) Front End Electronics (FEE) is designed to extract and process the about 8000 sense wire signals for tracking and energy loss measurements purpose and to provide informations for Global Trigger generation (trigger primitives).
Two possible scenarios have been foreseen for the dE/dx measurement. The first one is based on the measurement of the sense wires integrated charge (Standard Readout), while the second one is based on electron clusters detection (Sampled Waveforms). A description of the requirements for the two scenarios can be found in the DCH chapter.

13.1.2.2 DCH Front-end system (block diagram)

The DCH FEE chain block diagram is the same for the two options and is shown in Fig.13.2 for the Standard Readout case. The chain is split in two blocks:

- ON DETECTOR electronics: HV distribution and preamplifier boards located on the backward end-plate to preserve sense wire Signal to Noise Ratio.

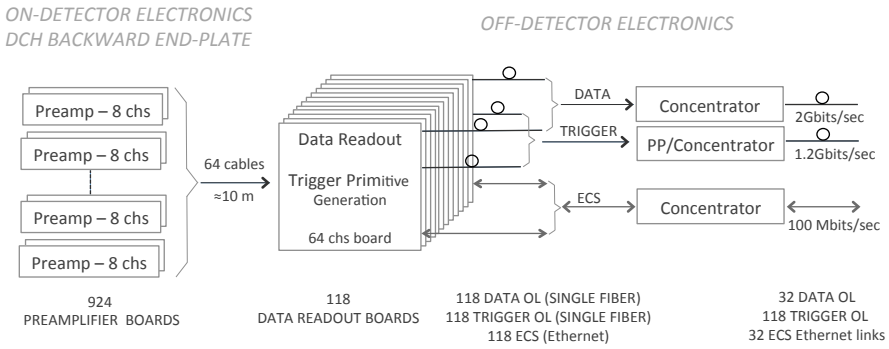

Figure 13.2: DCH front-end block diagram (Standard Readout)

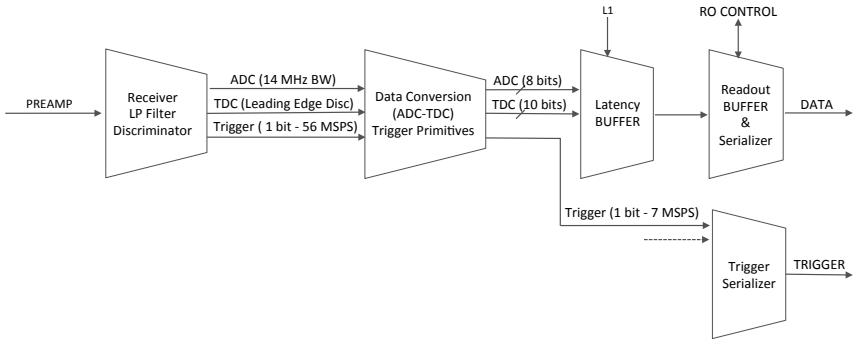

Figure 13.3: Front End Board Block Diagram (Standard Readout)

- OFF DETECTOR electronics: Data Readout and Concentrator Boards located on the top-side of the experiment.

13.1.2.3 Standard Readout - OFF DETECTOR electronics

Front End Boards - Block Diagram Front End Boards (FEB) will host up to 64 channels and will be made of three stages as shown in fig.13.3. The first one receives signals from preamplifiers and generates analog and discriminated outputs. The second stage provides digitization for charge and time measurements and includes the logic for trigger primitives generation as well. Finally, the third stage contains the Latency and Readout Buffers and the dedicated control logic. FEBs will include an ECS section as well (not shown in the block diagram) for parameters setting/sensing and FEE chain test.
Input signal connections will be implemented by means of twisted or mini-coaxial cables, while output connections will depend on the data path. DAQ chain and Trigger chain data path will use optical links while ECS will use copper links (see ETD Control System chapter).

Front-End-Boards - Receiver Section This stage amplify and split the preamplifier output signal to feed an anti-aliasing 14 MHz low-pass filter (charge measurements) and a leading edge discriminator (time measurements).

Front-End-Boards - Digitization Section The 14 MHz filter output signal is routed to an eight bits and (about) 28 MSPS FADC whose outputs feed a section of the system Latency Buffer implemented in a FPGA. Thirty-two FADC output samples (corresponding to about 1.14 μs, enough to span the full signal development) will be readout in presence of a Level 1 (L1) trigger

and, eventually, stored in a Readout Buffer.
The comparator output is routed to a FPGA where it is spit in two paths. The first one is sent to a TDC (implemented in the FPGA itself using the oversampling method) for time measurement. The second one, synchronized with the system clock and conveniently stretched to remove redundant informations, is sent to the DCH Trigger Segment Finding (TSF) modules (see ETD Trigger chapter).
The TDC outputs are routed to the second section of the Latency Buffer that, again, will be readout in presence of a L1 trigger signal.
The event data structure will not have a fixed length as L1 triggers spaced less than single event readout time will extend the time window to include the new event. Nevertheless, the board structure will be also compatible with local Feature EXtraction (FEX) implementation, i.e. the extraction of relevant information from the digitized data. In case of FEX implementation the transferred data stream would have a fixed length; an example of a possible readout data structure is shown shown in table 13.3.
In both cases the first, non zero, FADC output can be used for amplitude correction in discriminated data then minimizing input signal slewing effects.

Table 13.3: FEX based data stream (fixed length structure)

Data stream example
Digitizer Module Address (2 bytes)
Flag (1 byte)
Trigger Tag (1 byte)
Counter (1 byte)
Charge (2 bytes)
Time (2 Bytes)
1st ADC sample (different from baseline) for time walk correction (1 byte)

13.1.2.4 Sampled Waveforms - OFF DETECTOR electronics

The Cluster Counting technique for dE/dx measurement is based on the detection of electron clusters (primary ionization measurement) then high bandwidth devices and high sampling frequency digitizers (at least 1 GSPS) must be used.
Moreover, because data throughput must sustain the Super$B$ foreseen 150 kHz average trigger rate, a very fast processing is required. The constraint, at the state of art of technology, result in a huge power requirement and, as a consequence, in a low FEB modularity. Concerning tracking requirements, if we assume that full efficiency in single electron cluster detection is achieved, Cluster Counting measurement already includes information for tracking purpose (it is just required to store clusters arrival time instead of simply counting them).
Sampled Waveforms DCH FEE chain block diagram is similar to the diagram shown in fig.13.2; but, because of the lower board modularity both the number of crates and boards increase significantly (see table 13.4).

Front End Boards Front End Boards will be based on high sampling rate ($\geq$ 1 GSPS) digitizer, then a limited number of channels can be packaged in a single board, mainly because of power requirements. At present, up to 8 channels working at 1 GSPS have been packaged in a single VME 6U board. Nevertheless, in the next future, board modularity could get to 16 (or 24) with small increase in power requirements.
The circuit structure is very close to the block diagram shown in 13.3. Differences arise in digitizing section as no TDC is required for time measurements and also trigger primitives are generated from FADC outputs.
A sensitive issue concerns the FEX. Because of the large amount of data per channel (about 1 thousand of bytes) we can not transfer raw data to the DAQ then FEX must be implemented in the FEB itself. Thus when an L1 accept is raised all the event samples must be examined to identify clusters. The time required to implement the procedure is still compatible with the average trigger rate foreseen at the nominal Super$B$ luminosity ($\sim$ 150 kHz), but it could be a limit if the luminosity increases.
Another issue concerns the radiation background, as high performances RAM based FPGA must be used in the design.

Table 13.4: Number of links (Data, ECS, Trig), FEBs and crates for 64 channels Standard Readout (SR) and 16 channels Sampled Waveforms (SW) board modularity

	Mod	Data	ECS	Trig	Boards	Crates
SR	64	32	32	118	118	8
SW	16	32	32	118	462	29

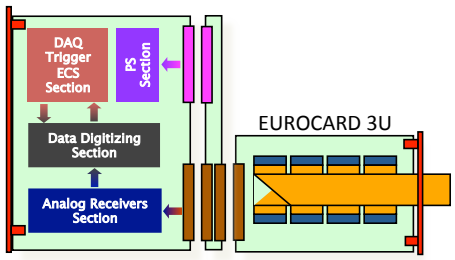

Figure 13.4: VFEB - FEB connections (FEB board - Custom Backplane - Interconnection Board

13.1.2.5 Front End Crates

Each Front End Crate will host up to 16 FEB, a Power Supply board for VFEB, Data Concentrators and, eventually, Trigger Patch Panel o Trigger Concentrator. Custom backplanes will be designed to:

- distribute power and common signals to the FEBs
- allow the use of Interconnection Boards to collect low modularity VFEB cables (fig 13.4)
- route some of the trigger signals to the neighbors boards (see ETD Trigger chapter) and (eventually) to distribute common signals to the boards

13.1.2.6 Number of crates and links

Table 13.4 shows the estimation of the number of links, boards and crates required for both DAQ and Trigger FEE chains (each crate is supposed to host up to 16 FEB). As shown in the table the number of Trigger OL do not change despite the different FEB number for Standard Readout or Sampled Waveforms scenarios. This is because the Sampled Waveform option foresees a Concentrator board also for the trigger chain to compensate for FEBs low modulerity. The board will collect Trigger OL coming from several FEBs and will deliver a single OL to the TFS modules.
The estimation has been done assuming:

- 150 kHz L1 trigger rate, 7392 sense wires (subdivided in 10 super-layers)
- 10% chamber occupancy in 1 μs time window
- 48 bytes per channel data transfer
- single link bandwidth is 2 Gbits/sec for DAQ data path and 1.2 Gbits/sec for Trigger data path

13.1.2.7 ECS

Each FEB will host a mezzanine board to manage ECS communication. Besides the control of the board, ECS mezzanine should provide the capability of data readout for debugging purpose. Detail can be found in the ETD ECS chapter.

13.1.2.8 Cabling

Because the large number of channels involved, DCH cable layout must be carefully designed. The main requirement concerns the possibility of replacing, in case of failure, a VFEB without disconnecting too many cables. Thus, signal and HV cables should be routed through the chamber outermost layer to minimize cables overlap. Table 13.5 shows the foreseen number of cables and a rough estimation of cable sizes.

13.1.2.9 Power Requirements

A very preliminary power requirement estimation is shown in table 13.6. The estimation for ON-DETECTOR electronics is based on preamplifier simulation and prototype test, while estimation for OFF-DETECTOR electronics come from the state of art of digitizing board available. Local (VFEB) voltage regulation is supposed to be implemented by means of linear low-drop hard-rad regulator.

Table 13.5: Estimation of the number and dimension of DCH cables (7392 sense wires - VFEB modularity = 8 channels)

	LVPS	HV	Signal (coax)	Signal (twisted)
Quantity	118	32	7392	924
N of cores	16	25	1	16
Cond. area (mm^2)	0.5	0.07		
Overall diam. (mm)	12	12	1.8	6.5

Table 13.6: Power requirement estimation for bot Standard Readout (SR) and Sampled Waveform (SW)

	Channel	Board	Overall
SR VFEB	30 mW		250 W
SW VFEB	150 mW		1.2 kW
SR FEB		40 W	5 kW
SW FEB		40 W	19 kW
SR & CC Data Conc.		30 W	240 W
SW Trig Conc.		30 W	870 W

13.1.2.10 DCH Summary

Number of Control Links	32
Number of Data Links	32
Total Event Size	update
On-Detector Power Consumption	0.25-1.2kW

Table 13.7: DCH summary

13.1.3 PID Electronics

The electronics will equip the 18,432 channels of the 12 sectors of the FDIRC. The electronics chain is based on a high resolution/ high count rate TDC, a time associated charge measurement over 12 bits and an event data packing sending event data frames to the data acquisition system (DAQ). The target performance of the overall electronics chain is a time precision of 200ps rms. This chain has to deal with a count rate per channel up to 500 KHz, a trigger rate up to 150 KHz and a minimum spacing between triggers of about 50 ns.

The estimated radiation level is expected to be about 100 rads per year. The use of radiation tolerant components or off-the-shelf radiation-qualified components is mandatory. However, the expected energy of the particles may make the latch-up effect almost impossible. Thus, the design has to take into account only Single Event Upsets. We selected the ACTEL family FPGA components for their non-volatile flash technology configuration memories, which are well adapted to radiation environment.

The baseline design assumes a 16-channel TDC ASIC with steps of 200 ps and a overall precision of 100 ps rms, embedding an analog pipeline in order to provide an amplitude measurement associated with the hit time. Thanks to a 12-bit ADC, the charge measurement will be used for electronics calibration, monitoring and survey purposes. The front-end (FE) board FPGA synchronizes the process, associates the time and charge information and finally packs them into a data frame which is sent via the backplane to the FBLOCK control board (FBC). The FBC is in charge of distributing signals coming from the FCTS and ECS, packing the data received from the FE boards to an n-event frame including control bits and transferring it to the DAQ.

13.1.3.1 The Front-end Crate

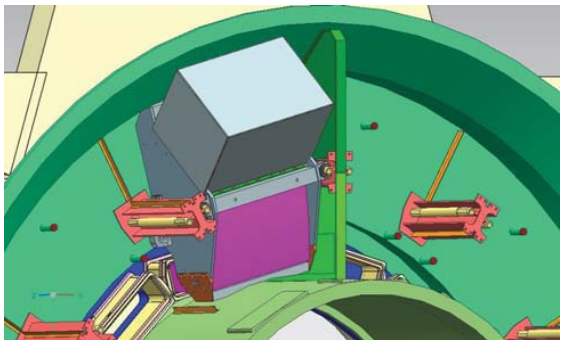

Figure 13.5: The FBLOCK equipped with the boards and fan tray

The board input will fit the topological distribution of the PMTs on the FBLOCK. The PMTs are arranged as a matrix of 6 in vertical direction by 8 in horizontal direction. Each column of 6 PMTs will fit to one FE board. One vertical backplane (PMT Backplane) will interface between the 4 connectors of each PMT base

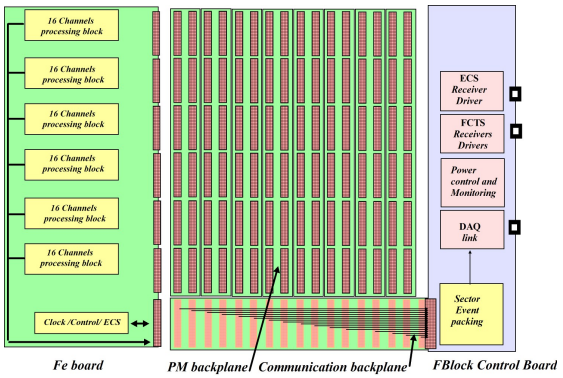

Figure 13.6: The Frontend Crate

to one connector of FE board. The PMT Backplane is also in charge of distributing the High Voltage, thus avoiding HV cables to pass over the electronics. The FB crate will use as much as possible the elements of a commercial crate, in order to avoid the design of too many specific elements like board guides.

13.1.3.2 The Communication Backplane

The communication backplane distributes the ECS and FCTS signals from the FBC to the 8 FE boards thanks to point to point LVDS links. It connects each FE board to the FBC for data transfer.

13.1.3.3 The PMT Backplane

The PMT backplane is an assembly of 8 motherboards, each corresponding to a column of 6 PMTs.

13.1.3.4 Cooling and Power Supply

The cooling system must be designed in order to maintain the electronics located inside at a constant temperature close to the optimum of 30 degrees. The air inside the volume must be extracted while the dry, clean temperature controlled air will be flowing inside. Each FB crate will have its own fan tray like in a commercial crate. 4000 m3/h can be considered as the baseline value for the whole detector. The crate and boards will be cooled by a water based cooler system.

13.1.3.5 The Front-end Board

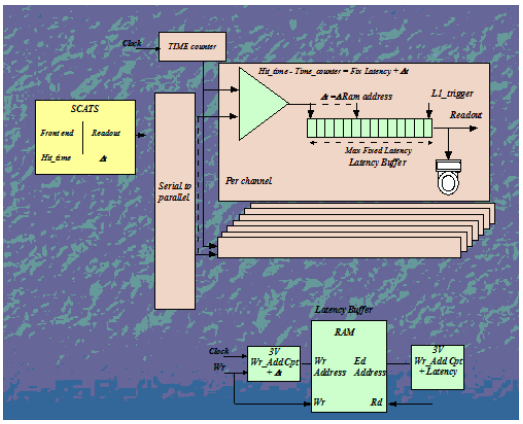

Figure 13.7: The PID Front-end Board

One FE board (Fig. 13.7) is constituted of 6 channel-processing blocks thus handling a total of 96 channels. The channel-processing block is based on one SCATS chip, one ADC, one ACTEL FPGA and the associated glue logics. The FPGA receives event data from the TDC and the converted associated charge from the ADC. The 16-bit data bus coming out of the TDC is de-serialized and split into 16 data bus corresponding to the 16 channels. A dedicated mechanism inside the FPGA permits to insert the events at their proper position, with respect to the hit time, in the event buffer. At this level, the design perfectly fits with the common proposal for the latency buffer and derandomizer (CFEE). Event data is stored in the event buffer where it is kept until either been thrown away if it is too old, or sent to the derandomizer located in the master FPGA upon the reception of the L1 trigger.

The master FPGA receives event data from the 6 channel processing blocks, packs it in a frame with parity bits for data checking and transmits it in a serial differential LVDS format to the FBC via the communication backplane.

13.1.3.6 The Crate Controller Board (FBC)

The master FPGA receives event data from the 6 channel processing blocks, packs it in a frame with parity bits for data checking and transmits

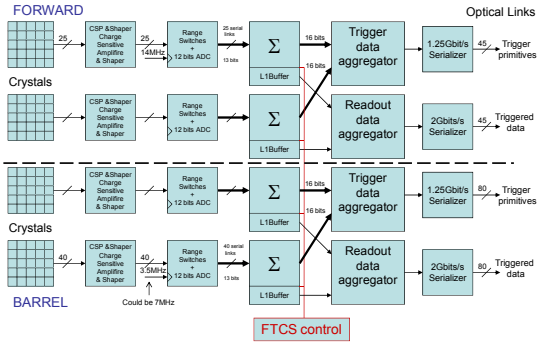

Figure 13.8: EMC Electronics

it in a serial differential LVDS format to the FBC via the communication backplane.

13.1.3.7 PID Summary

There is thus one link per sector, leading to a total of 12 readout links for the whole FDIRC. Each link has a mean occupancy of 15%, thus far below the limit fixed to 90% by ETD official rules.There is thus one link per sector, leading to a total of 12 readout links for the whole FDIRC. Each link has a mean occupancy of 15%, thus far below the limit fixed to 90% by ETD official rules.

Number of Control Links	12
Number of Data Links	12
Total Event Size	5 kbyte
On-Detector Power Consumption	15kW

Table 13.8: PID summary

13.1.4 EMC Electronics

This is still the version from the Whitepaper!!!

Two options have been considered for the EMC system design—a *BABAR*-like push architecture where all calorimeter data are sent over synchronous optical 1 Gbit/s links to L1 latency buffers residing in the trigger system, or a "triggered" pull architecture where the trigger system receives only sums of crystals (via synchronous 1 Gbit/s links), and only events accepted by the trigger are sent to the ROMs through standard 2 Gbit/s optical links.

The triggered option, shown in Fig. 13.8, requires a much smaller number of links and has been chosen as the baseline implementation. The reasons for this choice and the implications are discussed in more detail below.

To support the activated liquid-source calibration, where no central trigger can be provided, both the barrel and the end-cap readout systems need to support a free running "self-triggered" mode where only samples with an actual pulse are sent to the ROM. Pulse detection may require digital signal processing to suppress noisy channels.

Forward Calorimeter The 4500 crystals are read out with PIN or APD photodiodes. A charge preamplifier translates the charge into voltage and the shaper uses a 100 ns shaping time to provide a pulse with a FWHM of 240 ns.

The shaped signal is amplified with two gains ($\times 1$ and $\times 64$). At the end of the analog chain, an auto-range circuit decides which gain will be digitized by a 12 bit pipeline ADC running at 14 MHz. The 12 bits of the ADC plus one bit for the range thus cover the full scale from 10 MeV to 10 GeV with a resolution better than 1%. A gain is set during calibration using a programmable gain amplifier in order to optimize the scale used during calibration with a neutron-activated liquid-source system providing gamma photons around 6 MeV.

Following the *BABAR* detector design, a push architecture with a full granularity readout scheme was first explored. In this approach, the information from 4 channels is grouped, using copper serial links, reaching an aggregate rate of 0.832 Gbit/s per link to use up most of the synchronous optical link's 1 Gbit/s bandwidth. A total of 1125 links are required. The main advantage of this architecture is the flexibility of the trigger algorithm that can be implemented off-detector using state of the art FPGAs without constraining their radiation resistance. The main drawback is the large cost due to the huge number of links.

The number of links can be reduced by summing channels together on the detector side, and

Number of Control Links	
Number of Data Links	
Total Event Size	
On-Detector Power Consumption	

Table 13.9: EMC summary

only sending the sums to the trigger. The natural granularity of the forward detector is a module which is composed of 25 crystals. In this case, data coming from 25 crystals is summed together, forming a word of 16 bits. Then the sums coming from 4 modules are aggregated together to produce a payload of 0.896 Gbit/s. In this case, the number of synchronous links toward the trigger is only 45. The same number of links would be sufficient to send the full detector data with a 500 ns trigger window. This architecture limits the trigger granularity, and implies more complex electronics on the detector side, but reduces the number of links by a large factor (from 1125 down to 90). However, it cannot be excluded that a faster chipset will appear on the market which could significantly reduce this implied benefit.

Barrel Calorimeter The EMC barrel reuses the 5760 crystals and PIN diodes from *BABAR*, with, however, the shaping time reduced from $1\,\mu$s to 500 ns and the sampling rate doubled from 3.5 MHz to 7MHz. The same considerations about serial links discussed above for the forward EMC apply to the barrel EMC. If full granularity data were pushed synchronously to the trigger, about 520 optical links would be necessary.

The number of synchronous trigger links can be drastically reduced by performing sums of 4×3 cells on the detector side, so that 6 such energy sums could be continuously transmitted through a single optical serial link. This permits a reduction in the number of trigger links so as to match the topology of the calorimeter electronics boxes, which are split into 40 ϕ sectors on both sides of the detector. Therefore, the total number of links would be 80 both for the trigger and the data readout toward the ROMs, including a substantial safety margin (> 1.5).

13.1.4.1 EMC Summary

13.1.5 IFR Electronics

ver 0.5 sep 18 2012, Angelo Cotta Ramusino

The full description of the IFR readout electronics, going from the design constraints determined by the IFR detector's features to the detailes of the adopted baseline design is given in the subdetector chapter. The present subchapter is meant to highlight those features of the IFR electronics description which are most related to the Super$B$'s common ETD and ECS infrastructures. The active layers of the IFR are equipped with modules in which the detector elements (of different widths for the PHY and the Z views in the barrel) are assembled in two orthogonal layers. The overall IFR electronics channel count amounts to 11604 for the barrel section and 9540 for the endcaps, assuming that, for both sections, the IFR is instrumented with 9 active layers.

BARREL	
Maximum channel count per module:	32
Number of MOD32 processing units per module	**1**
TOTAL NUMBER OF MODULES IN BARREL	**384**
Total Number of MOD32 processing units	**384**
Sampling period = 1 / FCTS_clock (ns)	17,86
Number of samples in the trigger matching window (including framing words)	**16**
ENDCAP EVENT SIZE (kB)	**24,58**
TRIGGER RATE (kHz)	**150**
TOTAL ENDCAP BANDWIDTH (Gbps) (including 8b/10b encoding overhead)	**36,86**
Number of data links from the endcap detectors	24
Bandwidth per link (Gbps)	1,536

Figure 13.9: Estimation of the event size and data bandwidth for the IFR "Barrel" section

The IFR detector will be read out in "binary mode": the output of each SiPM device will be amplified, shaped and compared to a threshold, the binary status of each comparator's output being the variable to be recorded to reconstruct the particle tracks within the IFR detector. The downstream stages of the IFR electronics are the "digitizers" which sample the comparators' outputs at Super$B$ clock rate and store the samples into local "on-detector" circular memories. These buffers are designed to keep the data for a time interval at least equal to the Super$B$ trigger command latency. The last stage of the "on-detector" readout system is based on Finite State Machines (FSM for short) which extract, from the local latency buffers, the data selected by the FCTS trigger command.

ENDCAP	
Average channel count per module	92
Number of MOD32 processing units per module	**3**
TOTAL NUMBER OF MODULES IN ENDCAPS	**108**
Total Number of MOD32 processing units	**324**
Sampling period = 1 / FCTS_clock (ns)	17,86
Number of samples in the trigger matching window (including framing words)	**16**
ENDCAP EVENT SIZE (kB)	**20,736**
TRIGGER RATE (kHz)	**150**
TOTAL ENDCAP BANDWIDTH (Gbps) (including 8b/10b encoding overhead)	**31,104**
Number of data links from the endcap detectors	16
Bandwidth per link (Gbps)	1,944

Figure 13.10: Estimation of the event size and data bandwidth for the IFR "Endcap" section

In the baseline version of the IFR electronics design the digitizer blocks introduced above have 32 input channels. The "trigger matched" data output by each digitizer in response to a received trigger pulse is sent, via serial links on copper, to the "data merger" units. These units assemble the trigger matched data from a number of front end digitizers into event data packets of suitable size and forward them to the ROMs via the Super$B$ fast data links. The application of the binary readout scheme to the IFR prototype detector developed in the R&D

phase has allowed the determination of parameters, such as the sampling frequency and the number of samples, which are relevant to the performance of IFR readout system.

Tables in figures 13.9 and 13.10 show the estimated event size and data bandwidth required for the IFR readout at the nominal SuperB trigger rate of 150kHz. The figures presented in the tables take into account a trigger jitter of 100ns. The event size and required bandwidth could be reduced by applying the data reduction scheme proposed by the ETD group: if a new trigger would select data that has already been sent in response to a previous one, the repeating data is not retransmitted and a pointer to the start of the repeating data within the previous packet would be sent instead.

LAYER WIDTH	LAYER	No. Modules per layer	LAYER ENABLE	PHI ASSUMING 50MM BARS	ZETA ASSUMING 106MM BARS
1963	1	6	1	13	17
1987	2	6	1	13	17
2050	3	6	1	13	17
2113	4	6		14	17
2176	5	6		14	17
2240	6	6		14	17
2304	7	6	1	15	17
2367	8	6		15	17
2431	9	8		12	17
2494	10	8		12	17
2569	11	8	1	12	17
2641	12	8		13	17
2712	13	8		13	17
2784	14	8	1	13	17
2879	15	8		14	17
2973	16	8	1	14	17
3068	17	8		15	17
3144	18	8	1	15	15
3296	19	8	1	16	15
NUMBER OF MODULES per sextant:		64		TOTAL PER SEXTANT	1940
TOTAL NUMBER OF MODULES	384			TOTAL CHANNELS PER BARREL	11640

Figure 13.11: Block diagram of the IFR readout ASIC

While a readout system based on "COTS" ("Components Off The Shelf") was designed and successfully exploited for the readout of the IFR prototype, the front end stages of the electronic readout chain for the Super$B$ IFR detector, for the reasons illustrated in the IFR subdetector chapter, will be implemented in an ASIC, whose block diagram is shown in figure 13.11.

The IFR scintillation detectors, each equipped with a single-photon counting device (silicon photomultiplier or SiPM for short), are grouped in modules which are inserted in selected gaps of the flux return steel or around it. The signals from all SiPMs of a module are carried by thin coaxial cables which exit the module's aluminum enclosure and are mass-terminated to a high density connector on a carrier PCB (printed circuit board). The average length of the coaxial assemblies connecting the sources (SiPMs) to the first amplification stages is in the order of a few meters because it is convenient to locate the ASICs' carrying boards where they would be accessible for any maintenance eventually needed.

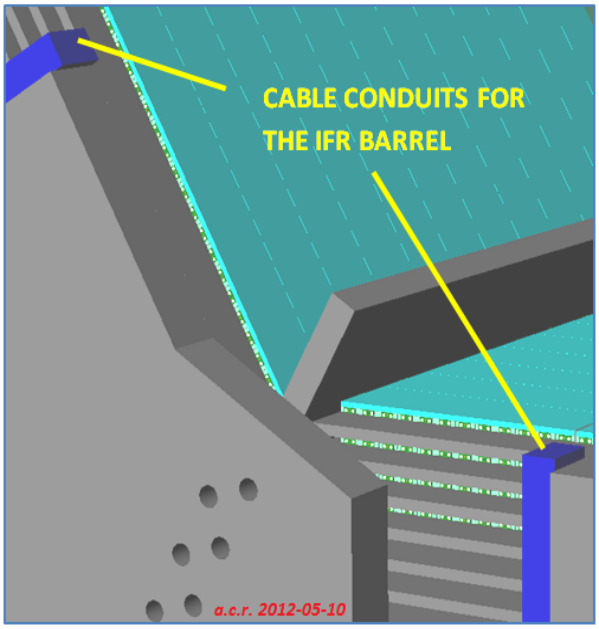

Figure 13.12: The IFR cable conduits for 2 sextants

Fig. 13.12 shows the situation for the IFR barrel: in this representation the metal enclosures of the modules are not shown; the closest convenient locations for the ASICs carrying boards are indicated by the yellow callouts.The front end cards are installed inside the 3" x 5" cable conduits as suggested in figure 13.13. While the figure only shows the dou-

ble shielded, multi differential-pair cables (green jacket) needed to route the front end cards' output serial lines to the data merger units, the cable conduits are also meant to host cables for the distribution of the SiPM bias voltages (one bias voltage common to all SiPMs of a module), of the fast (FCS) and slow (ECS) commands and, finally, of the supply voltages for the front end cards.

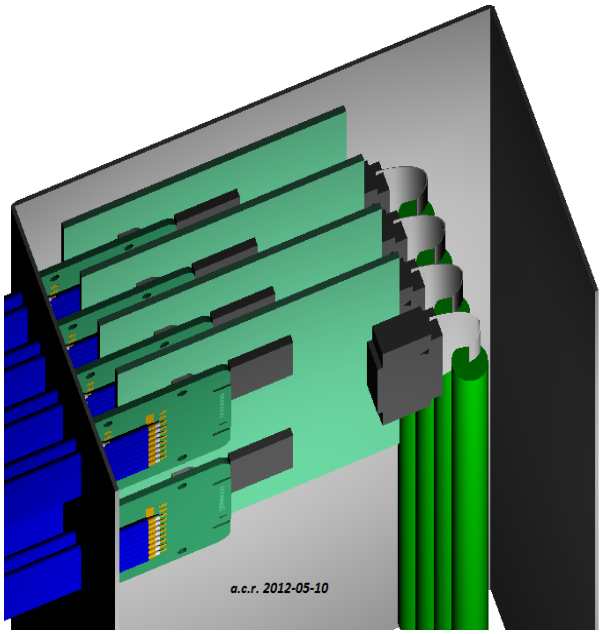

Figure 13.13: Detail of front end cards installed in the IFR cable conduit

Figure 13.14 shows the perspective view of the two doors of an endcap: the yellow callouts indicate the openings in the side-lining steel through which the data, control and power cables for the detector modules will be routed. The signals emerging from these openings are routed to the crates indicated by the red callouts. For the endcap section of the IFR, the front end cards carrying the IFR read out ASICs could be installed directly in the crate and connected to the data merger cards through the crate's backplane interconnections.

The "data merger" crates are interfaced to the Super*B* FCTS (Fast Control and Timing System) and ECS (Experiment Control System) from which they receive and execute the commands controlling the data acquisition and the detector configuration respectively. The data merger units also collect the trigger matched data from the front end cards and merge the input streams into the output packets sent, via the high speed optical data links, to the SuperB ROM (ReadOut Modules).

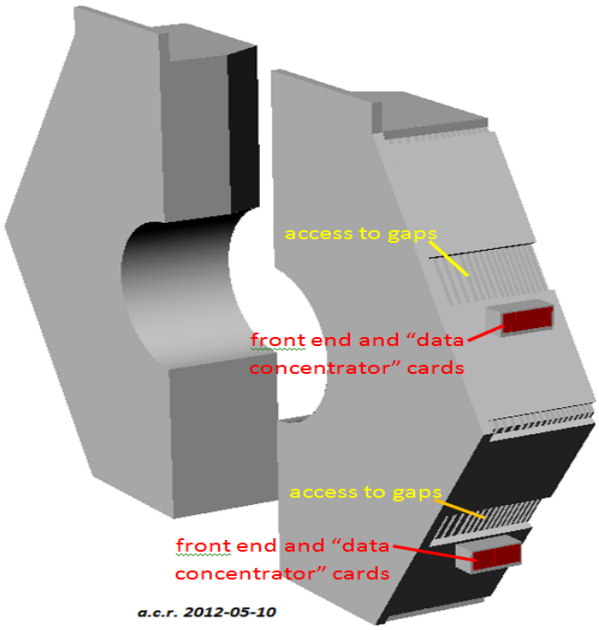

Figure 13.14: Perspective view of IFR endcaps

The IFR barrel will be equipped with a total of 6 "data merger" crates while 8 are foreseen for the endcaps. Further details on partitioning, location and construction of the data merger crates are given in the IFR subdetector chapter, which also provides a description of the services needed by the IFR readout in the experimental hall: - SiPM supply voltages: 384 (barrel) + 324 (endcaps) = 708 "HV" channels with: maximum output voltage 100V, 10 bit resolution, maximum output current 25mA. The power dissipated by the SiPMs in the whole IFR under nominal operating conditions is of the order of a few tens of Watts - front end cards supply voltages: 354 + 354 "LV" supply channels with: +3.3V or -3.3V output voltage respectively, maximum output current 1A, IR drop compensation The power dissipated by the front end stages for each 32 SiPM group is

around 1.6W and thus the power dissipated by the front end stages is about 620W for the barrel and 520W for the endcap - cooling: the temperature of the IFR steel should be controlled to within a few degrees, as it was for BaBar; the design of the barrel cooling system should then take into account the estimated 1140W dissipated in total by the front end stages of the IFR barrel and endcap electronics.

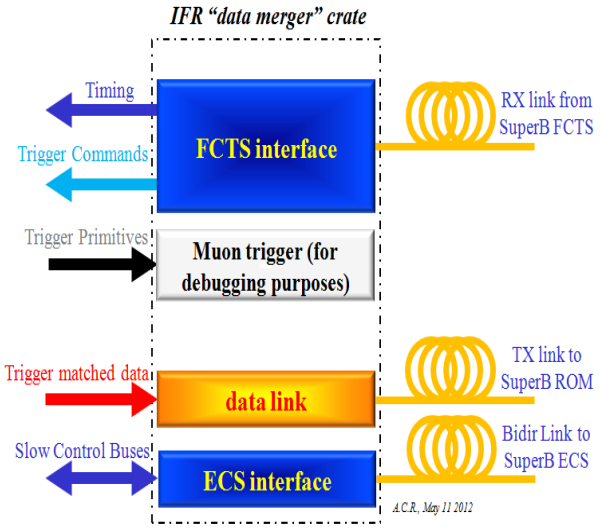

Figure 13.15: Main functions performed by the electronic units in the "data merger" crate

13.1.5.1 IFR Summary

Number of Control Links	20
Number of Data Links	40
Total Event Size	45 kbyte
On-Detector Power Consumption	1.2kW

Table 13.10: PID summary

13.2 Electronics Infrastructure

13.2.1 Power supplies, grounding and cabling

Gianluigi Pessina

13.2.1.1 Power Supply to the Front-end:

The voltage supply system is normally composed by a cascade of AC/DC, DC/DC and linear regulators. Depending on the power dissipation and noise requirements some of the above elements can be avoided. The supply system of an accelerator-based experiment has known additional constraints to be satisfied. The large particle fluence and the presence of a strong magnetic field can have an impact on the aging and behavior of the electronic equipment. The first constraint is addressed only by adopting radiation hardened (rad-hard) technology and using suitable layout recipes for the monolithic circuits. This is common to all the devices that sit in the detector area. Magnetic field has generally less impact except for AC/DC and DC/DC converters that need to use inductances and/or transformers, having ferromagnetic cores.

Power Supply outside the detector area: In the following we will describe our solution, able to face the above constraints. The strategy we would adopt is to minimize the number of regulators in the detector area. The distance between the regulators and the front-end can be a few tens of meters. The energy the cable is able to store in its inductive component can be large and attention must be adopted to protect the connected electronic equipment in case of accidental short circuit to ground. Fig. 13.16 shows an example of the recovery from a short circuit of 50 m cable with 4 mm^2 section. The short circuit current was limited to 20 A. A N-MOS, IPP50CN10NG, with 50 $m\Omega$ ON resistance simulated the short circuit and it breaks down above about 100 V when in open state, that explains the reason of the clipping. The measurement has been taken in the worst condition of no applied load. It is clear from this that an accidental short circuit is very critical in producing possibly destructive damaging.

We have found that most of the cables with 3 or 4 poles and cross-section between 1.5 mm^2 and 4 mm^2 have an inductance per unit length,

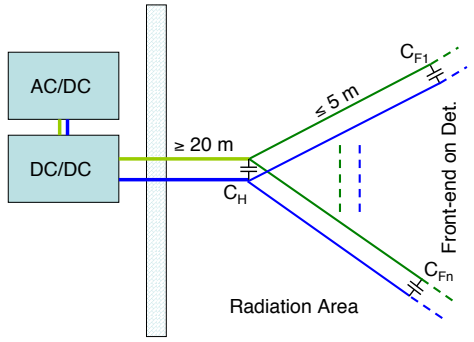

Figure 13.17: Possible layout for a sub-detector for what concerns voltage supply.

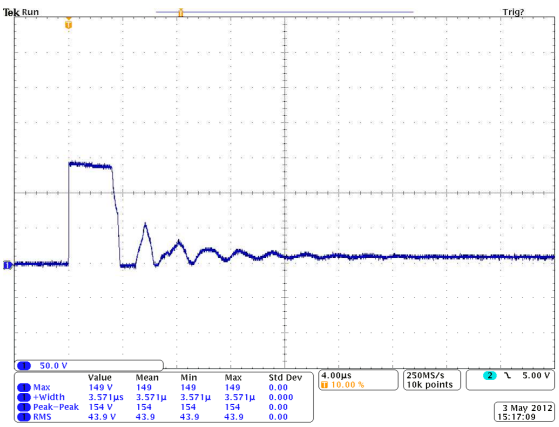

Figure 13.16: Signal at the end of a 50 m cable after a short circuit. The clipping at 150 V is due to the breakdown of the MOS switch used.

L_M, of the order of $0.7\,\mu H/m$, from DC to few hundred of KHz. Calling I_{short} the maximum delivering current available from the power supply and l the cable length, then:

$$E_{energy} = \frac{1}{2} L_M l I_{short}^2 \qquad (13.1)$$

is the available energy driven to the load in case of accidental short circuit. To limit the voltage at a safe level our straightforward solution is to add in parallel to the load a capacitance able to store such released energy. This can be done if we satisfy that:

$$\frac{1}{2} C_{lim} V_{over}^2 = \frac{1}{2} L_M l I_{short}^2 \qquad (13.2)$$

where V_{over} is the maximum voltage that must not be exceeded and C_{lim} is the capacitance whose value must be chosen to satisfy the eq. with the given voltage V_{over}. As an instance, with $50\,m$ of cable length, $I_{short} = 20\,A$ and $C_{lim} = 160\,\mu F$ the maximum over voltage excursion would be less than $9.5\,V$.

Adopting the introduced technique a hub with a distribution to several shorter cables can be implemented as shown in Fig. 13.17. A large value capacitance, C_H, is at the end of the cable that connects the DC/DC regulators from the outside to the inside of the detector area. In our example we continue with considering $50\,m$ of cable length and $C_H = 160\,\mu F$. From this point several shorter cables, or stubs, connect the various parts of the detector or sub-detector front-end. To save space, the sections of these last cables can be smaller since they have each to manage a smaller current. At the end of each of these stubs, $5\,m$ in our present example, a smaller value capacitance, C_{Fx}, $(33\,\mu F)$ is connected. In case of short at the end of a stub all the current flows into it. But as soon as the short is opened capacitance C_H absorbs the energy of the longer cable, while the energy of the shorted stub is managed by the corresponding capacitance C_{Fx}. Fig. 13.18 shows that the signal at the end of the $50\,m$ cable has an over voltage of only about 10 %. The maximum current was $20\,A$ and it can be seen that the baseline before the short is released is about $2\,V$, the dropout generated by the $20\,A$ current across about $0.1\,\Omega$ given by the sum of the stub (as a reference a section of $1\,mm^2$ has an impedance of about $16\,\Omega/Km$) and the ON resistance of the N-MOS. Fig. 13.19 shows the over voltage present at the stub end where the short is generated and released; again the over voltage is contained within about 10 %. As it can be appreciated, the baseline that precedes the release of the short is about $1\,V$, namely $20\,A$ developed across the about $50\,m\Omega$ ON resistance of the N-MOS. In the test setup of the laboratory we implemented 2 stubs and Fig. 13.20 is the signal at the stub end where the short circuit was

not present. Again the over voltage is respecting the safety conditions. The principle applies well also if a low regulated voltage is considered and Fig. 13.21 is an example of release from a short of more than $25\,A$ on a $5\,m$ cable ($2.5\,mm^2$ of cross-section) loaded with $160\,\mu F$ capacitance.

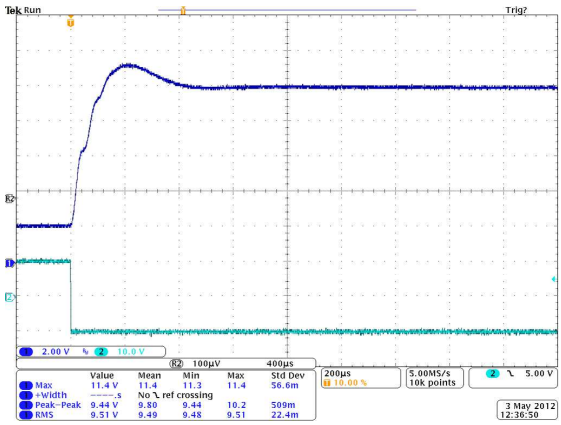

Figure 13.18: Signal at the end of a $50\,m$ cable (blue line) after that a short circuit is generated at one end of a stub. The $50\,m$ cable is loaded with a $160\,\mu F$ capacitor and the short current is $20\,A$; the supply voltage is $10\,V$. Every stub is loaded with $33\,\mu F$. The green line is the voltage driver at the gate of the switched N-MOS.

The suppression capacitance must show a very small series resistance and inductance. Capacitors with plastic dielectric such as Metalized Polypropylene Film satisfy this condition. As an example the $160\,\mu F$ we have adopted for the test has only $2.2\,m\Omega$ of series resistance, but, being big in volume, it shows a series inductance of a few tens of nH. To compensate for this last effect a smaller value (and volume) capacitance ($1\,\mu F$) is put in parallel, able to account for the fast part of the rising signal. Metalized Polypropylene Film capacitances have a range of values limited to a few hundreds of μF. As a consequence, a limited value of current per cable, $10\,A$ to $20\,A$, results in a good compromise. Many commercial regulators, also in the form of the so called bricks and half-bricks layouts, are available on the shelf at low cost. This strategy is particularly usefully for minimizing the dropout along the cable and it is of particular concern when a low voltage is needed.

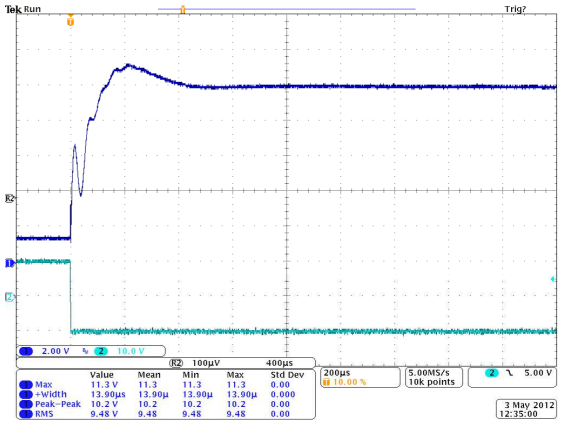

Figure 13.19: Signal at the end of a stub of Fig. 13.17 after a short circuit (blue line). Two stubs were present in the test setup. C_H is $160\,\mu F$, the C_{Fx} are $33\,\mu F$ and the short current is $20\,A$; the supply voltage is $10\,V$. The green line is the voltage driver at the gate of the switched N-MOS.

We cannot forget that an over-voltage can happen due to a possible malfunctioning of the regulator. To reject rapidly and with good precision this effect a stack of fast diodes is a good choice. For instance with a voltage supply of $10\,V$ the series connection of about 20 diodes allows to maintain the safe operating condition provided that they are in contact with a heat sink in case the problem persists for a while. The location of the stack of diodes can be close to the regulator and space occupation would not constitute a problem.

Noise cabling and shielding: The combination of the inductance component of the wires and the suppression capacitance has a twofold utility as it behaves also as a low pass filter. Fig. 13.22 shows the noise at the end of the $50\,m$ cable plus $2 \times 5\,m$ stubs when $160\,\mu F$ plus $2 \times 33\,\mu F$ capacitances load the combination. The applied supply voltage was $10\,V$ and the load $3.3\,\Omega$. In this case a standard commercial regulator has

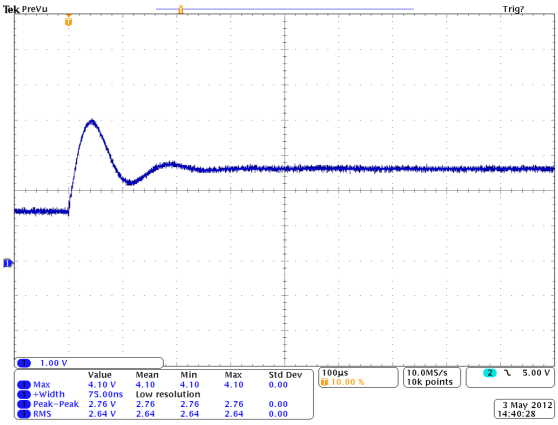

Figure 13.21: Short circuit release on a $5\,m$ cable with $2.5\,mm^2$ cross-section.

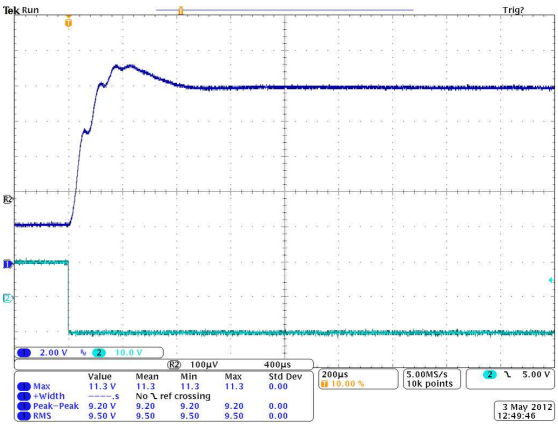

Figure 13.20: Signal at the end of a stub of Fig. 13.17 after a short circuit (blue line) happened at another stub. Two stubs were present in the test setup. C_H is $160\,\mu F$, the C_{Fx} are $33\,\mu F$ and the short current is $20\,A$; the supply voltage is $10\,V$. The green line is the voltage driver at the gate of the switched N-MOS.

been used. Very low noise DC/DC regulators have been designed [30] and Fig. 13.23 shows the noise performance under the same conditions. Even better performances can be obtained by cascading the DC/DC to a linear regulator of very good quality [31].

Low noise results are obtained if care is considered on the type of cables adopted. In all the measurements described so far cables used were all armored. This precaution allows to shield the supply voltage from outside disturbances but also to avoid to create disturbances to the outside world. We intend to adopt this kind of layout solution for the final experimental setup. In addition, where needed, we intend to add a double shield by inserting the cables inside a tubular copper mesh.

The connection scheme of Fig. 13.17 is, in a natural way, suitable to route ground. Let's suppose that the ground of every detector or sub-detector to which the cables are routed have their ground isolated. Then, we can route a tinned copper wire (or a copper bar) very close to the power supply cables so as to suppress area sensitive to EMI interferences. Such a routing scheme allows a 'star' connection with only one ground contact node (we remember that AC/DC and DC/DC regulators are floating), that is the standard requirement.

Shielding is considered for whose region were the electric or magnetic field can affect the performances. The shields can be considered for the whole sub-detector or individually on a channel by channel basis. This is particularly true with the effect of magnetic field on those detectors that extend on a large volume, such as photomultiplier tubes (PMTs). Past experience showed that in these cases a local shield implemented with mu-metal around every PMT is essential.

Power Supply in the detector area: We are considering the opportunity to use both DC/DC and linear regulators inside the detector area. Inductances and transformers cannot be based on a ferromagnetic coil. As a consequence they are limited in range of values and the switching speed of the DC/DC must be very large. This is the case for the monolithic DC/DC regulator we are considering [32], developed in $0.35\,\mu m$ CMOS technology based on rad-hard layout and components, and having a switching frequency of the modulator of a few MHz, which allows the use of a coil-free inductance. Based on the same technology a linear regulator is also available [33].

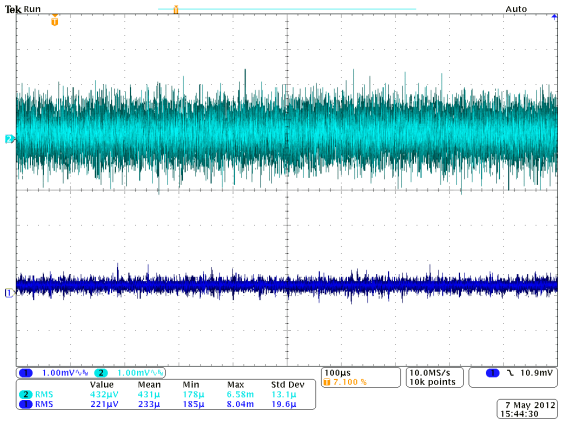

Figure 13.23: Very low noise DC/DC regulator [30]. Measurements condition and setup as for Fig. 13.22

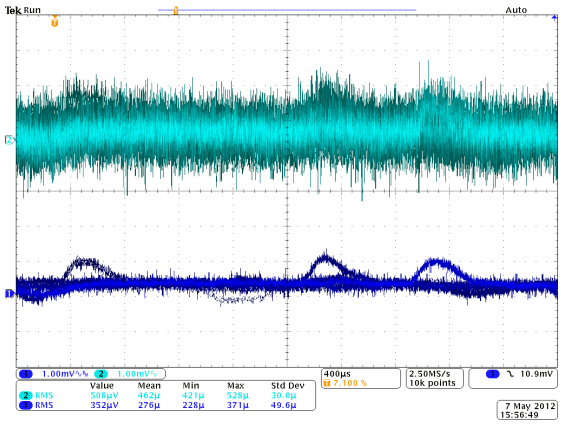

Figure 13.22: Noise after $50\,m$ cable loaded with $160 + 2 \times 33\,\mu F$ capacitance at $10\,V$ and with $3.3\,\Omega$ load. Upper noise is with the full $350\,MHz$ bandwidth of the oscilloscope, Lower noise has the scope bandwidth limited to $20\,MHz$.

13.2.1.2 High Voltage Power Supply to the Detectors:

High voltage power supplies suffer of similar problems as AC/DC and DC/DC regulators. As a consequence these regulators must be located outside the detector, sub-detector area (we do not know about any commercial rad-hard high voltage regulator). The energy released to the load in case of accidental short circuit would be not an issue thanks to the fact the, normally, such regulators have their driving current limited to a few hundred of μA. As an instance, if we load the line with a $1\,nF$ high voltage capacitor and considering $1\,A$ the short circuit current we expect an over-voltage of about $0.2\,V$. Finally, commercial over-voltage protectors based on gas discharge tubes are very efficient and fast.

13.2.2 Grounding and Shielding

This section has been incorporated in the Power Supply section

13.2.3 Cable Plant

This section has been incorporated in the Power Supply section

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