Use of Associative Memories for tracker L1 triggering in LHC environment.

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CMS Upgrade Week: Tracking Trigger, May 21-25, 2012

Framework

- This work has been carried out in the framework of an Italian National Research Project (PRIN).
- It is in collaboration with **italian ATLAS groups** who are implementing the **FTK Vertical Slice project.**
- It has been presented at: **RT2012** ***IEEE2012 Conferenze***, Berkeley, *June 2012.*
- *Also at CMS Upgrade Week and WIT2012*

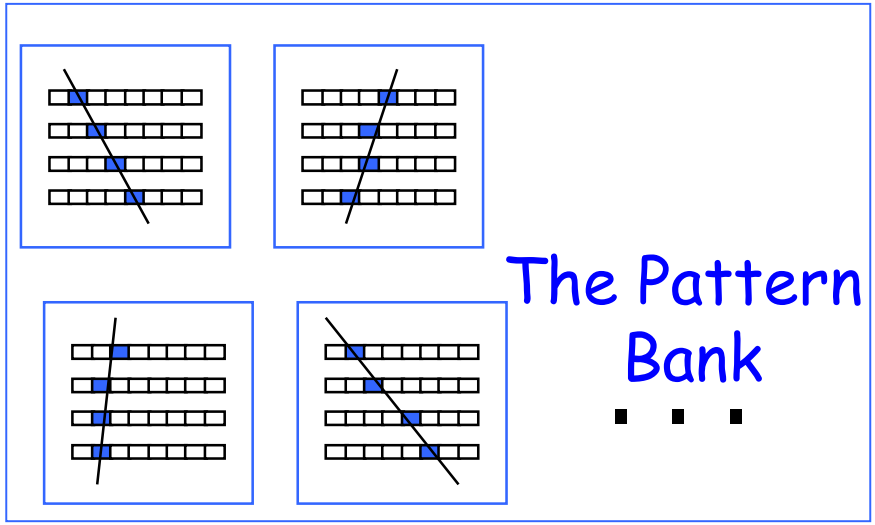
Use of Tracker for L1 trigger is important at LHC-HL
(you already know why...)

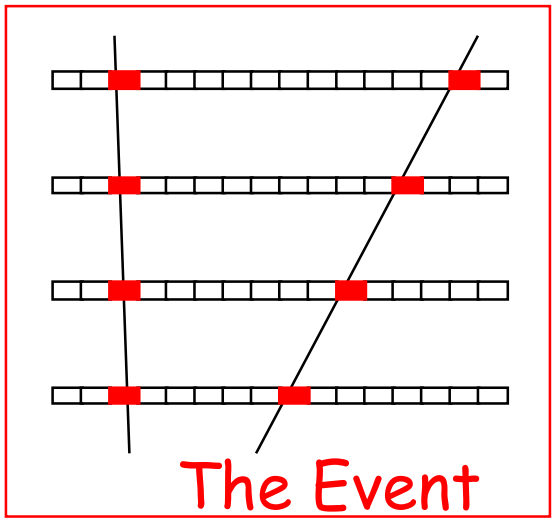
Track reconstruction and pattern matching

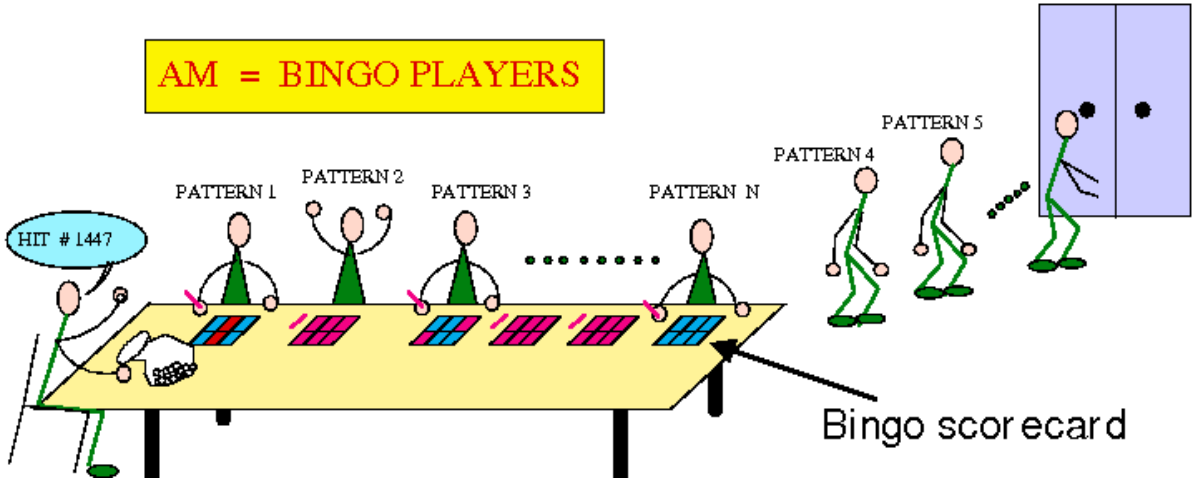
Pattern matching algorithm

The pattern matching compares the event with ALL the candidates tracks stored in a local memory (Pattern Bank).

The pattern matching can be very fast for online track reconstruction thanks to the Associative Memory (AM) parallelism **[see CDF use-case]**

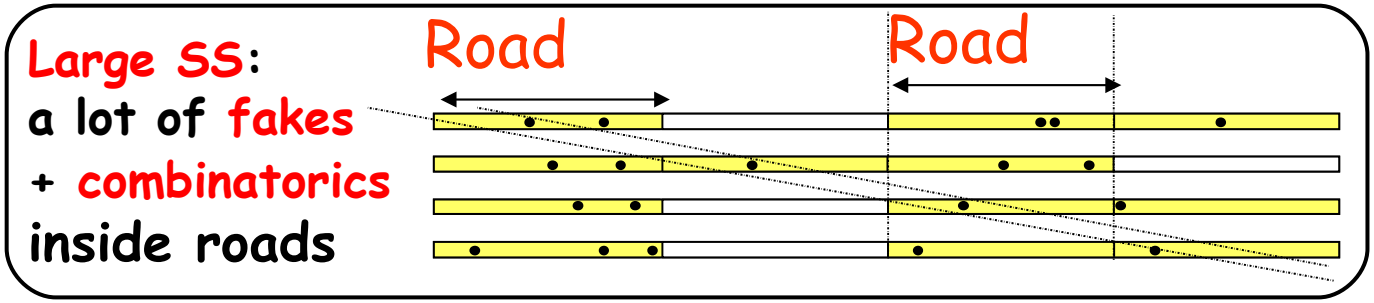




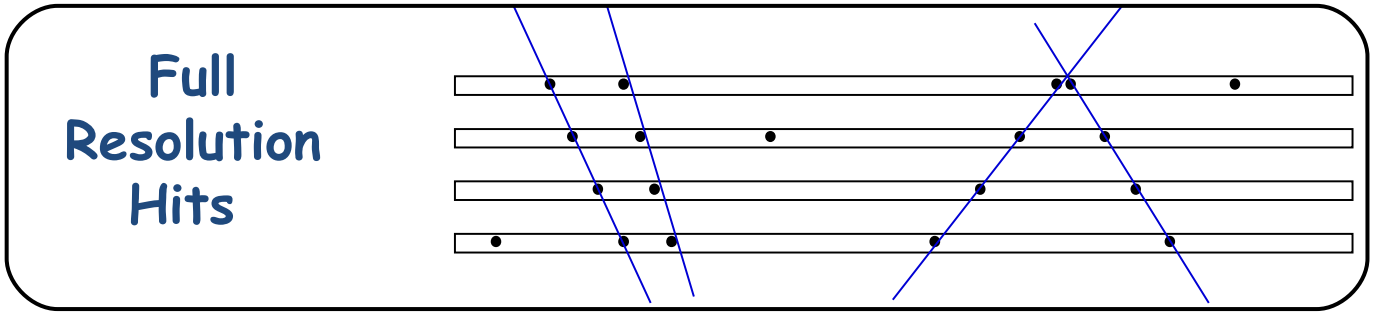


Pattern Matching and Track Fitting

First Step: by **AMBoard** (large road size) →
lower track resolution →
less patterns



Second Step: by **Auxiliary Board** (small road size) →
higher track resolution

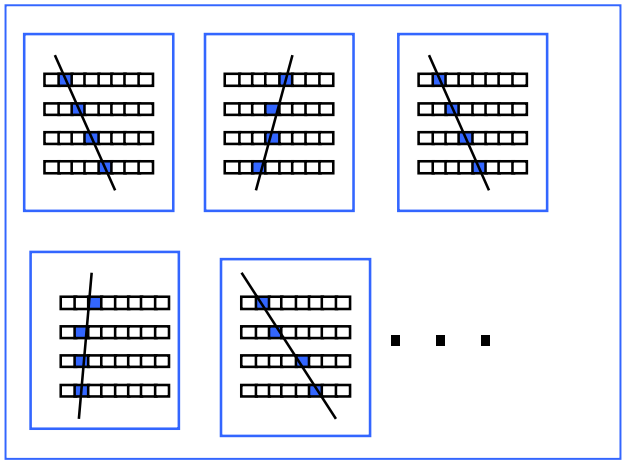


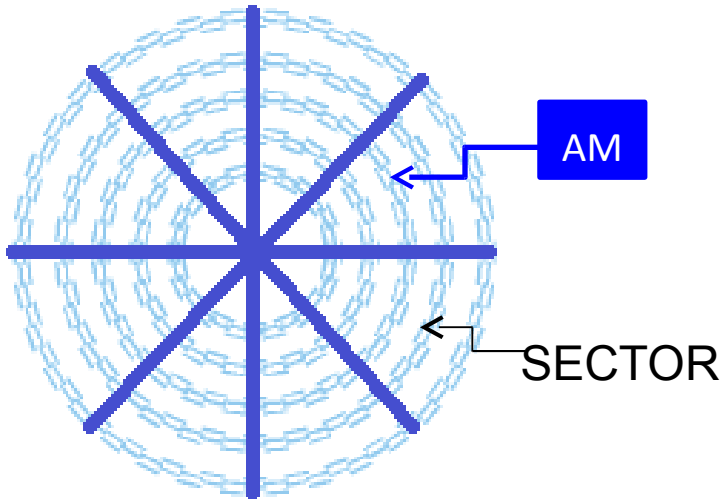
L2 trigger with AM

The Associative Memories can be used both at L1 and L2 trigger

L2: Lower input rate (100kHz), ordered events, longer latency *(~25µsec for FTK)*

=> one big pattern bank to process 1 event at a time





1 sector* => *1 bank* = *1 logical unit* => *1 (crate of) AM card(s)

L2 trigger with AM

The longer latency could be used in at least two ways:

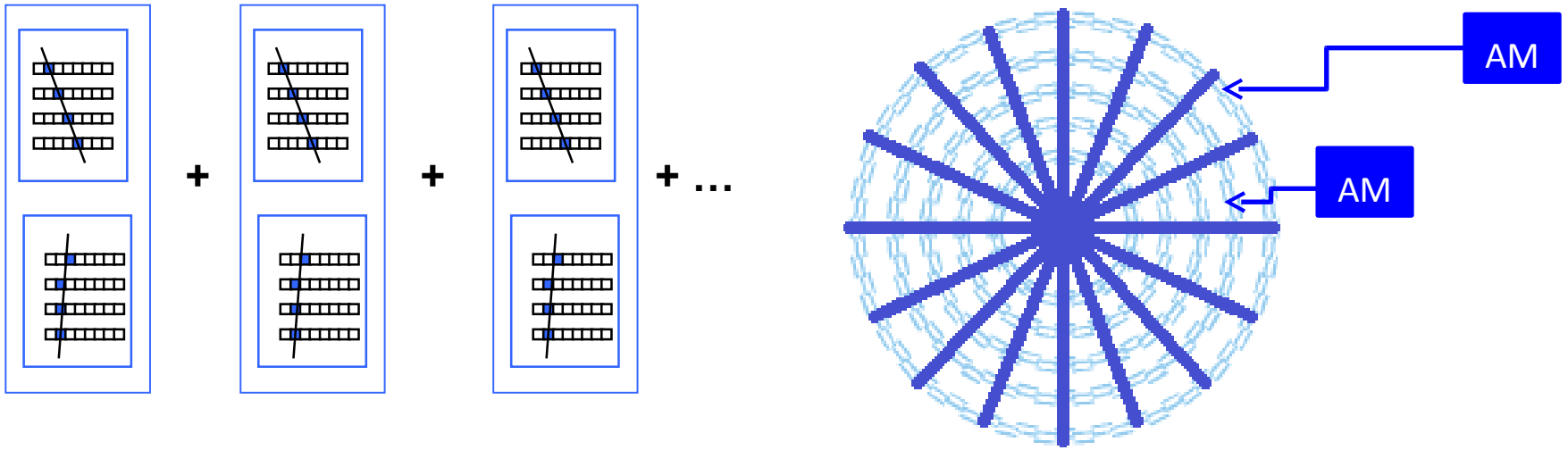
1) To reduce the number of sectors maintaning the same track resolution (save AM Hardware) => big pattern banks

2) To maintain the same number of sectors with better track resolution (gain on fake rejection at low level) ==> big pattern banks

Or any linear combination....

L1 trigger with AM

L1: High input rate (40MHz), mixed events, low latency *(~6usec)*



The shorter latency implies *an increased number of sectors (increased number of AM crates)* to process the events.

L1 trigger with AM

more sectors needed to reduced the amount of hits to be processed by one AM card;

more sectors
=> **smaller sectors**
=> **smaller number of patterns**
at same track resolution

smaller number of patterns are **NEEDED** to process in parallel by the same AM card several events coming from the same sector.

R&D of Associative Memories HW and FW

1) AMBSLIM firmware development

- Version of firmware of board that manage different event at the same time
- Timing measurement

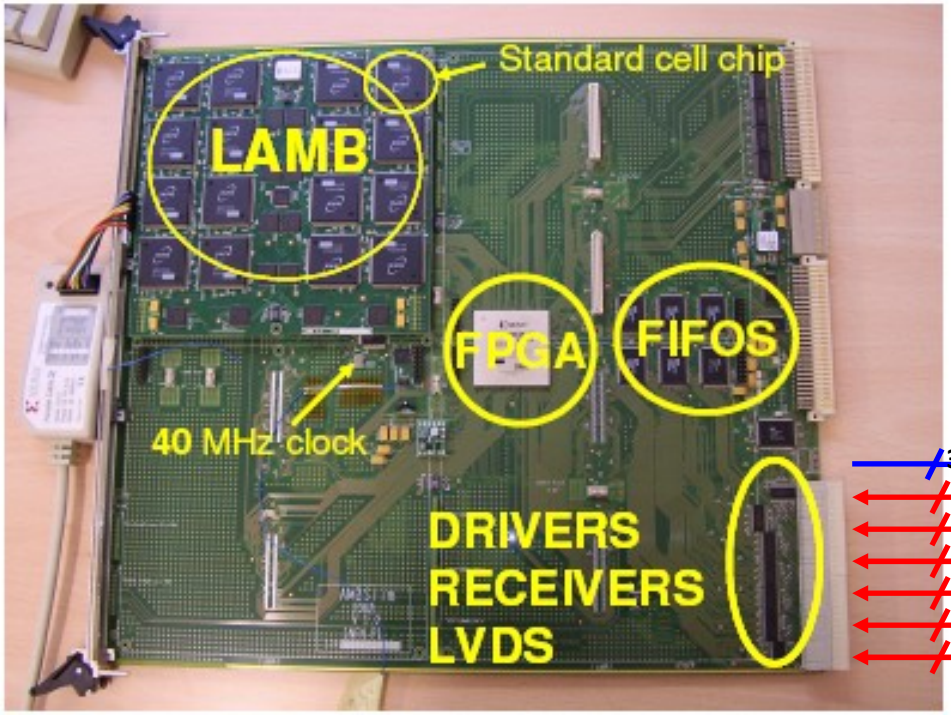
2) AMBFTK

- Test of hardware

3) New version of LAMB

AMBSlim firmware development
AMBSlim board

A single motherboard for **L1** and **L2** trigger applications (AMBSLIM, SLIM5 experiment) thanks to flexibility of the powerful **control FPGA**.

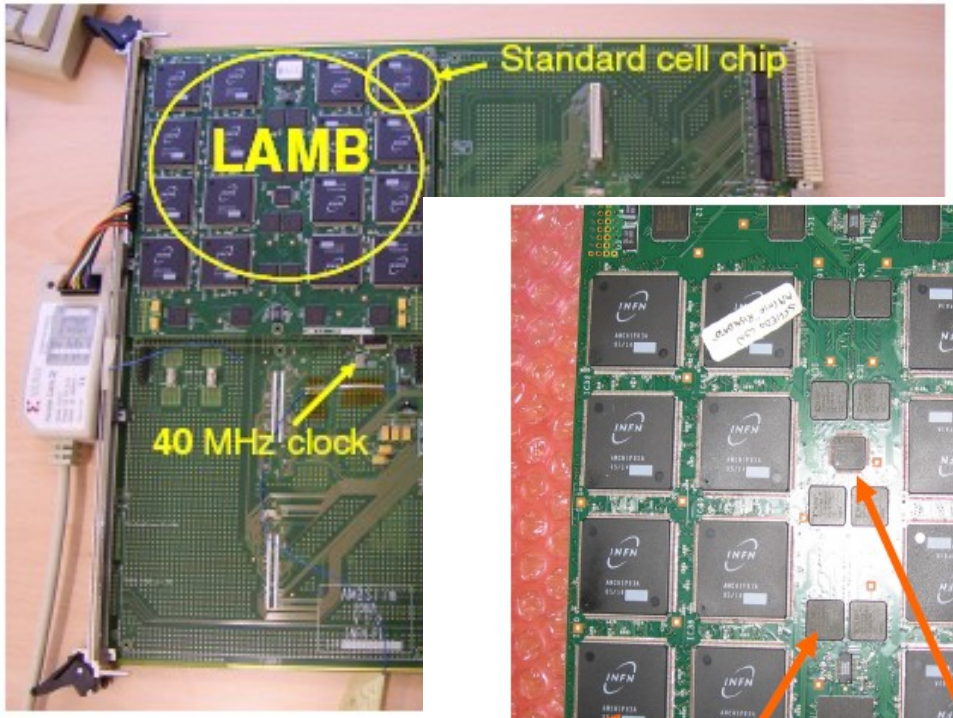


FPGA: **XILINX**
VIRTEX2pro 1696 pin

HOLD	6+1 control channels
ROAD	1 output bus (29+1bit)
HIT	6 input buses (18+3 bit)

AMBSlim firmware development: CDF LAMB

A single motherboard for **L1** and **L2** trigger applications (AMBSLIM, SLIM5 experiment) thanks to flexibility of the powerful **control FPGA**.



32 AM chips

INDI

Glue chip

BOUSCA chip

FPGA: **XILINX** VIRTEX2pro 1696 pin

6 input buses (21bit each)

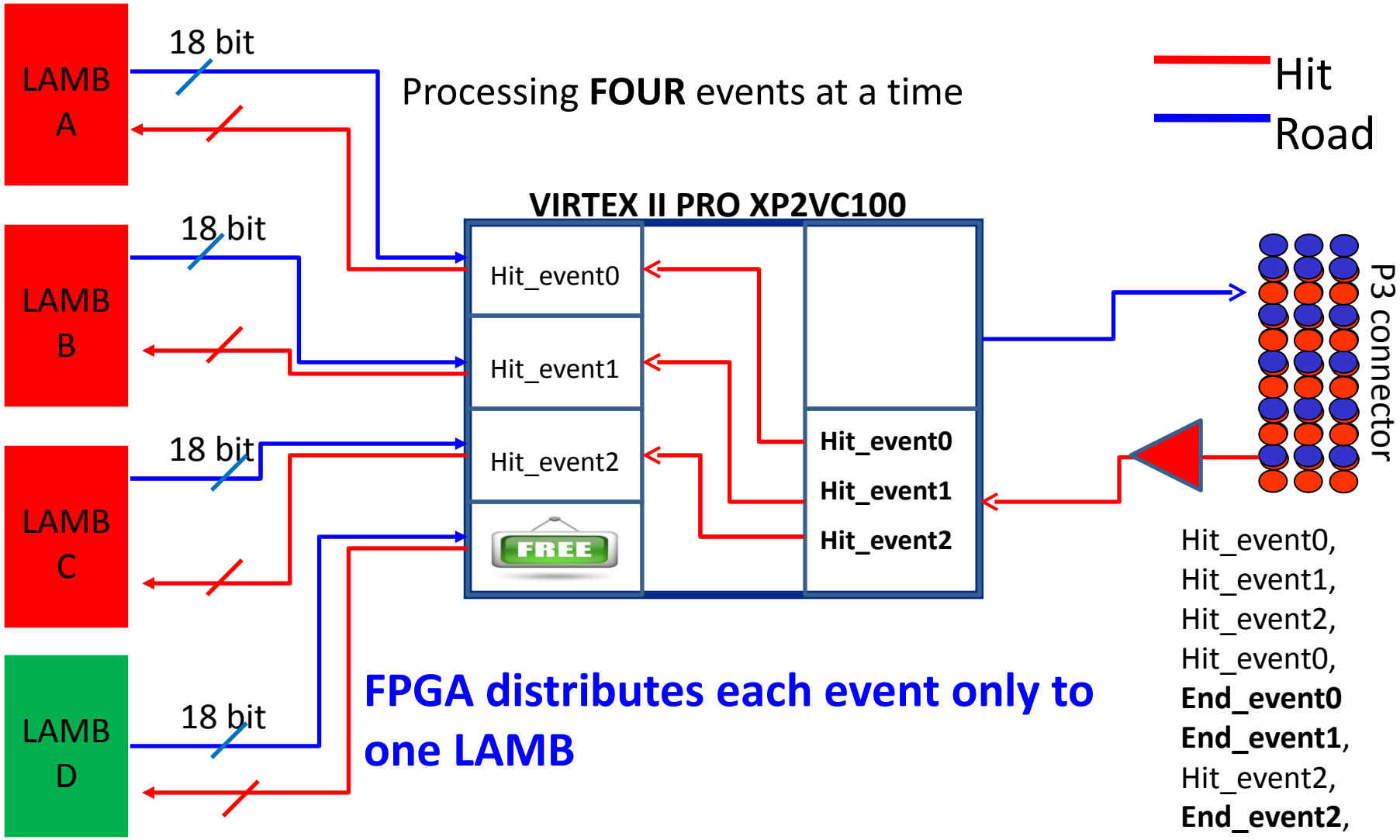
1 output bus (30bit)

1 AMchip: 5Kpattern

INDI: Input Distributor (fan-out) **(STAR)**

GLUE: mux roads from Ams **(Pipeline)**

AMBSlim Logic Control for L1



FPGA distributes each event only to one LAMB

AMBSLIM firmware development Status:

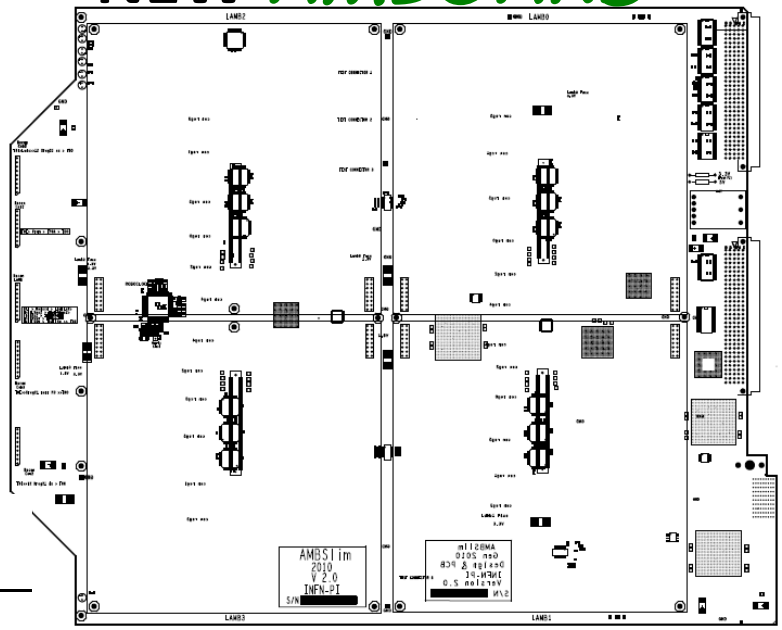
- A first version of firmware is simulated
- … it should be tested .
- The event processing time in the L1 trigger has to be measured.

Existing hardware: AMBFTK

NEW *AMCHIP*

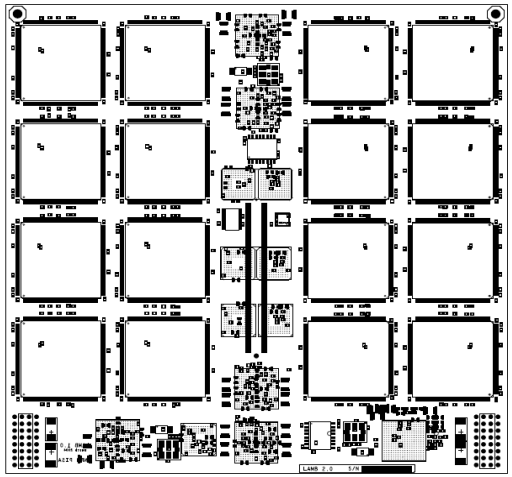
OLD	NEW	
40	**100**	MHz
6	**8**	#input parallel buses
4.3	**12**	Input BW Gbit/s
1	**1**	# output bus

NEW *AMBOARD*



OLD	NEW	
6	**12**	#input bus
1	**16**	# output bus

NEW *LAMB*



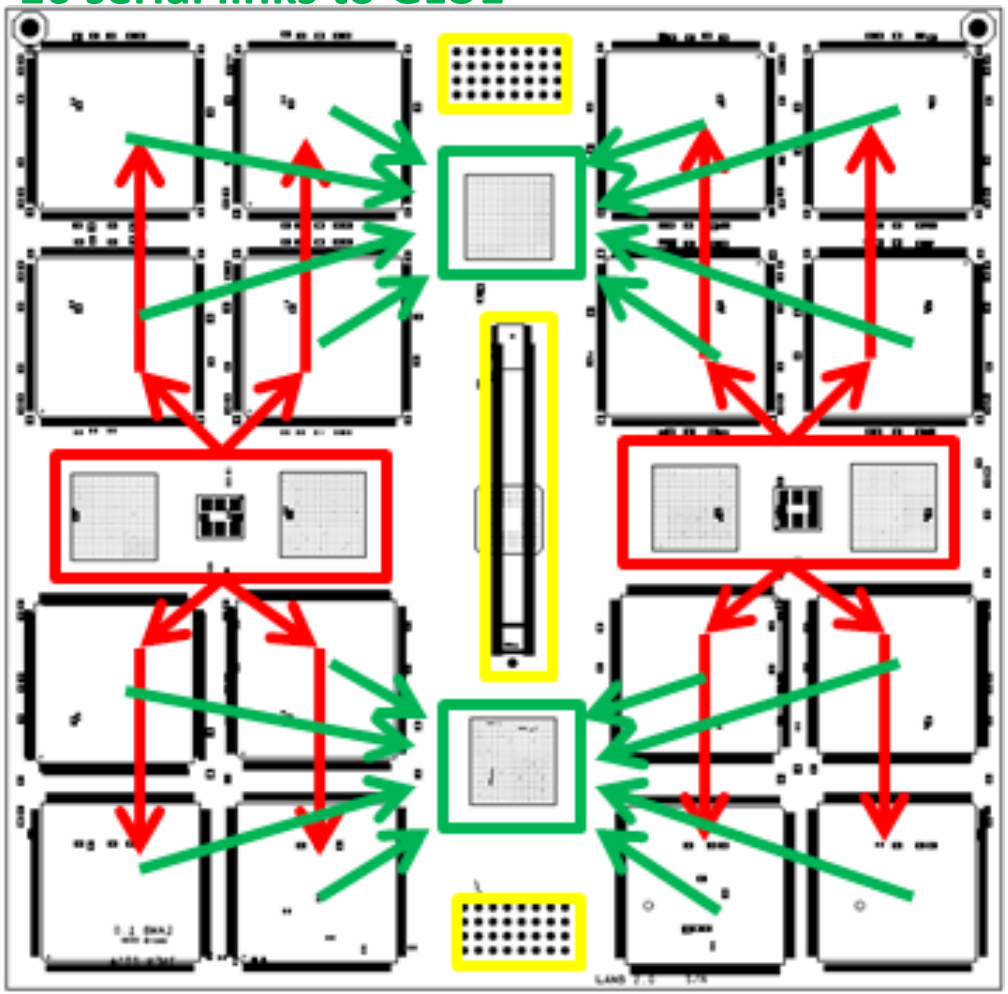
OLD	NEW	
6	**8**	#input buses
0	**4**	# serial link bus
6	**4**	# parallel link bus
1	**4**	# output bus

Existing hardware: AMBFTK

- From P3 connector
  - For the hit
    - 12 bus → each bus 15 bit @ 100MHz → **18Gbps**
  - For the road
    - 16 bus → each bus 14 bit @ 100MHz → **22.4Gbps**
- Number of pattern for each LAMB
  - 80k pattern/chip → **2.56Mpattern/LAMB**
- Indipendent link for the output road from LAMB

Upgrade HW: Star LAMB for L1

16 serial links to GLUE



Spartan 6 – Input Distributor for serial buses

Spartan 6 – GLUE for output road

Star Connection

- All output flux from AMchip are connected at the GLUE

Serial Link

- Communication AMBOARD – LA be ALL serial

Consideration of event processing at L1: CMS Specification

- CMS specification
  - Latency → 3usec
  - Bunch Crossing → 40MHz
  - N°hit/event/layer → 50

(accurate simulation needed)

Consideration of event processing at L1: First scenario

- Consider one AMBoard to process one event
  - Input bandwidth AMBoard/layer = 1.5 Gbps
  - Input bandwidth of event → 15 bit * 50 hit * 40MHz → 30 Gbps
  - => BW AMBoard/BW event → 20 boards needed to manage the event
  - Total number of patterns is:

    32k/chip * 128chip = 4M pattern /AMB

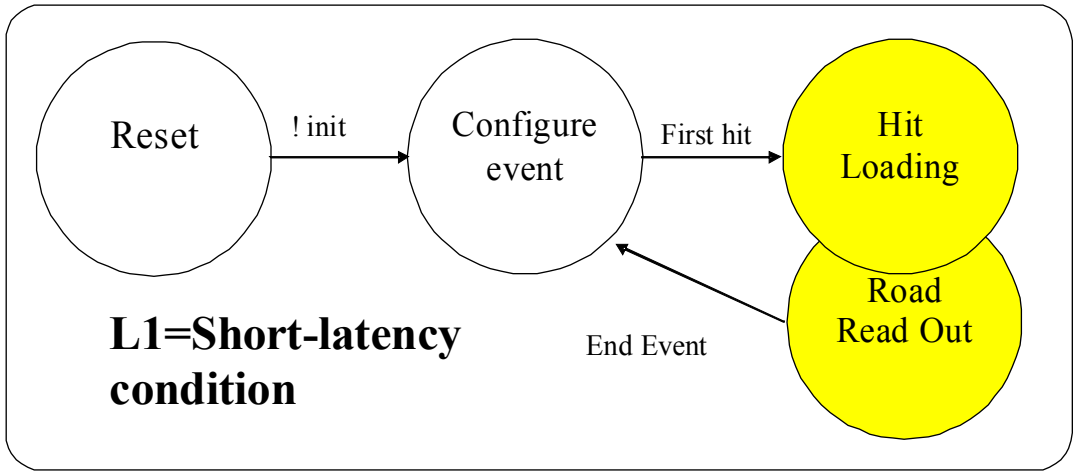
Consideration of event processing at L1: Second scenario

- Consider one LAMB for process one event
  - Means 4 P3 one for each LAMB or the input frequency of AMBoard is 400MHz
  - Input bandwidth AMBoard = 1.5 Gbps * 4 = 6.0 Gbps
  - Input bandwidth of event → 15 bit * 50 hit * 40MHz → 30 Gbps
  - => BW AMBoard/BW event → 5 AMBoard are needed to process the event
  - Total number of patterns is:

    32k/chip * 32chip/LAMB = 1M pattern /LAMB

HOW to measure the event processing time

The measurement have to be performed in the L1 working condition



Matching Criteria

- Configure AMBoard
- Loading hit
- Read-out road

$$T_{LATENCY} = DELAY \cdot P_{CLOCK} + \frac{N^{\circ}\,Hit\_Max}{layer} \cdot P_{CLOCK} + N^{\circ}\,Road \cdot P_{CLOCK}$$

- Fixed DELAY
- Time to download hit into AMBoard
- Time to readout matched road

P_{CLOCK} = 10nsec

Conclusions

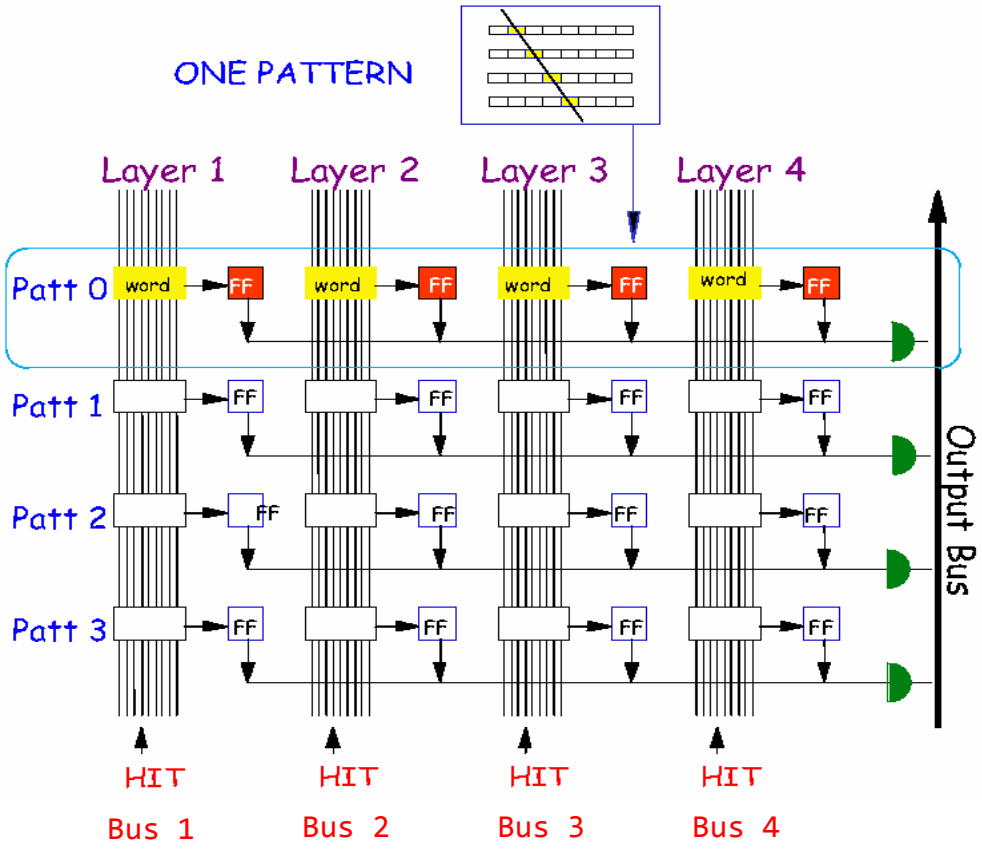
- The use of the Associative Memory for Tracker L2 trigger has already been proved by CDF. ATLAS is also currently implementing the FTK Vertical Slice.

- **Exploiting the existing HW it is possible to test some ideas about the AM use for L1 tracker trigger (new FW).**

- We are working on some HW upgrade **(new version of AM card)** necessary to proceed further to assess the possibility of AM use for L1 tracker trigger in the CMS LHC-HL environment.

BACKUP

Associative Memory Architecture



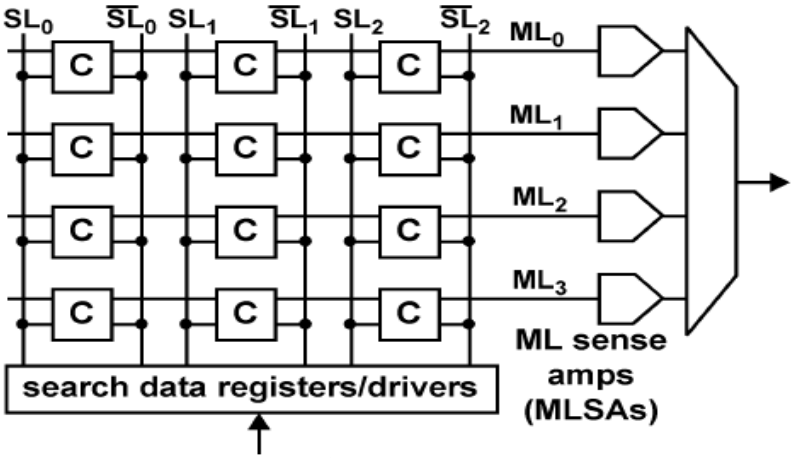
- Dedicated device:
  Maximum parallelism !
- Each pattern with
  private comparator
- Tracks found during
  detector readout !

HIT = detector channel fired by a particle

ROAD = fired patterns

What are Associative Memories?

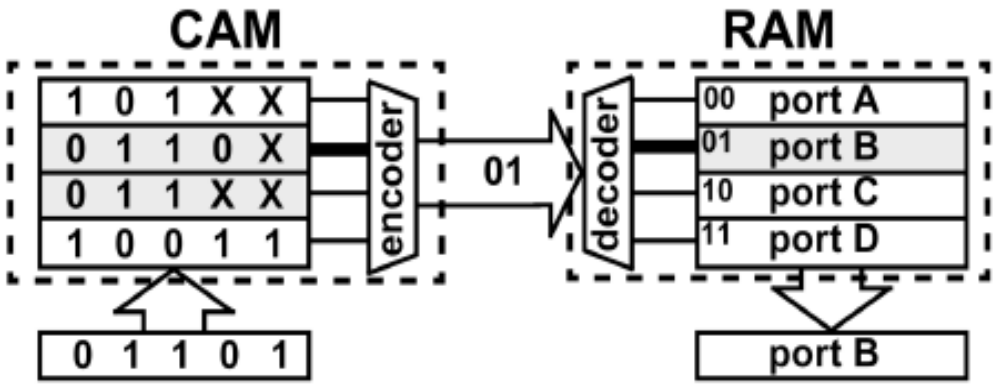
Associative Memories (AM) derive from the **Content Addressable Memories** (CAM)



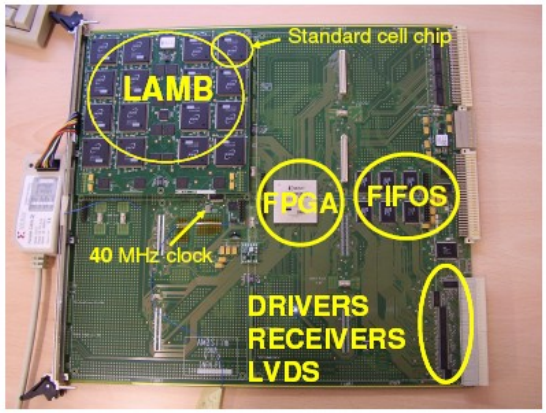
Each cell C contains a bit. A column is a word.

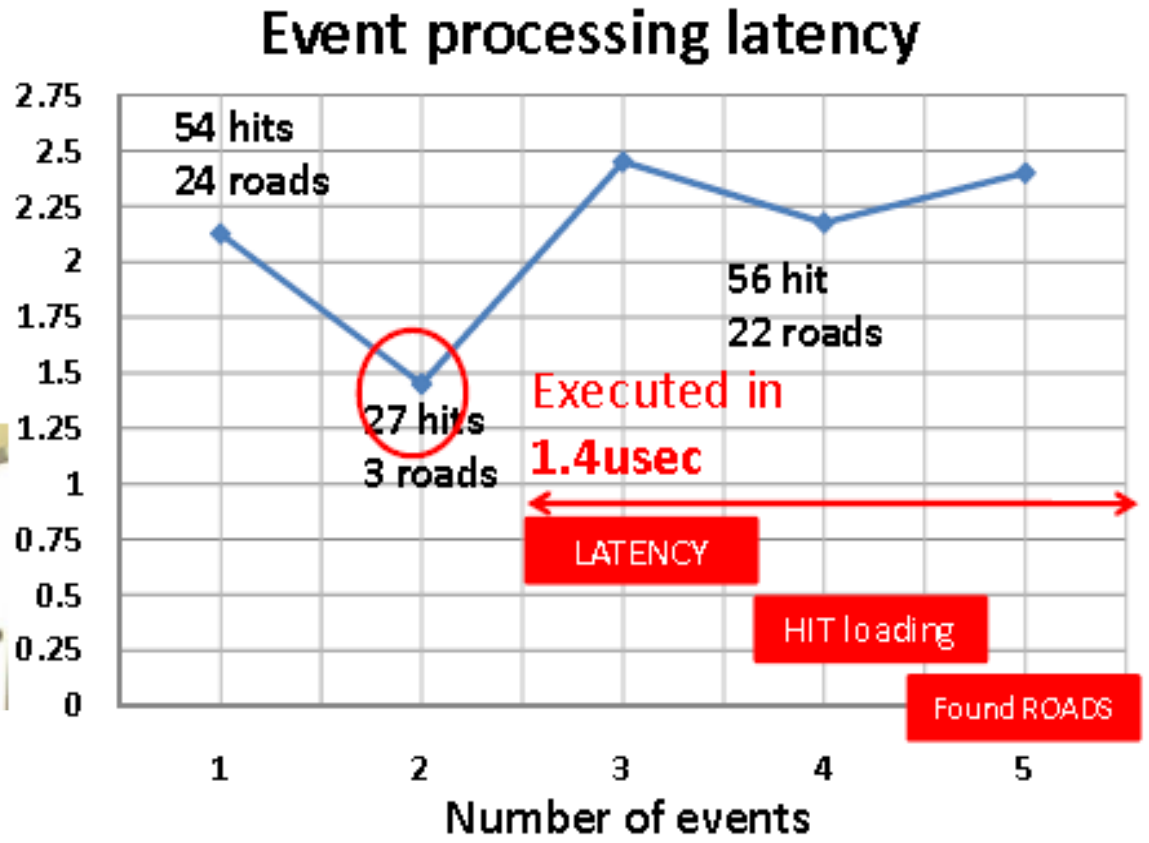
All words are compared at the same time with an input word.

If one word matches the input word its address is transmitted as output.



Limitation of current LAMB for L1 trigger

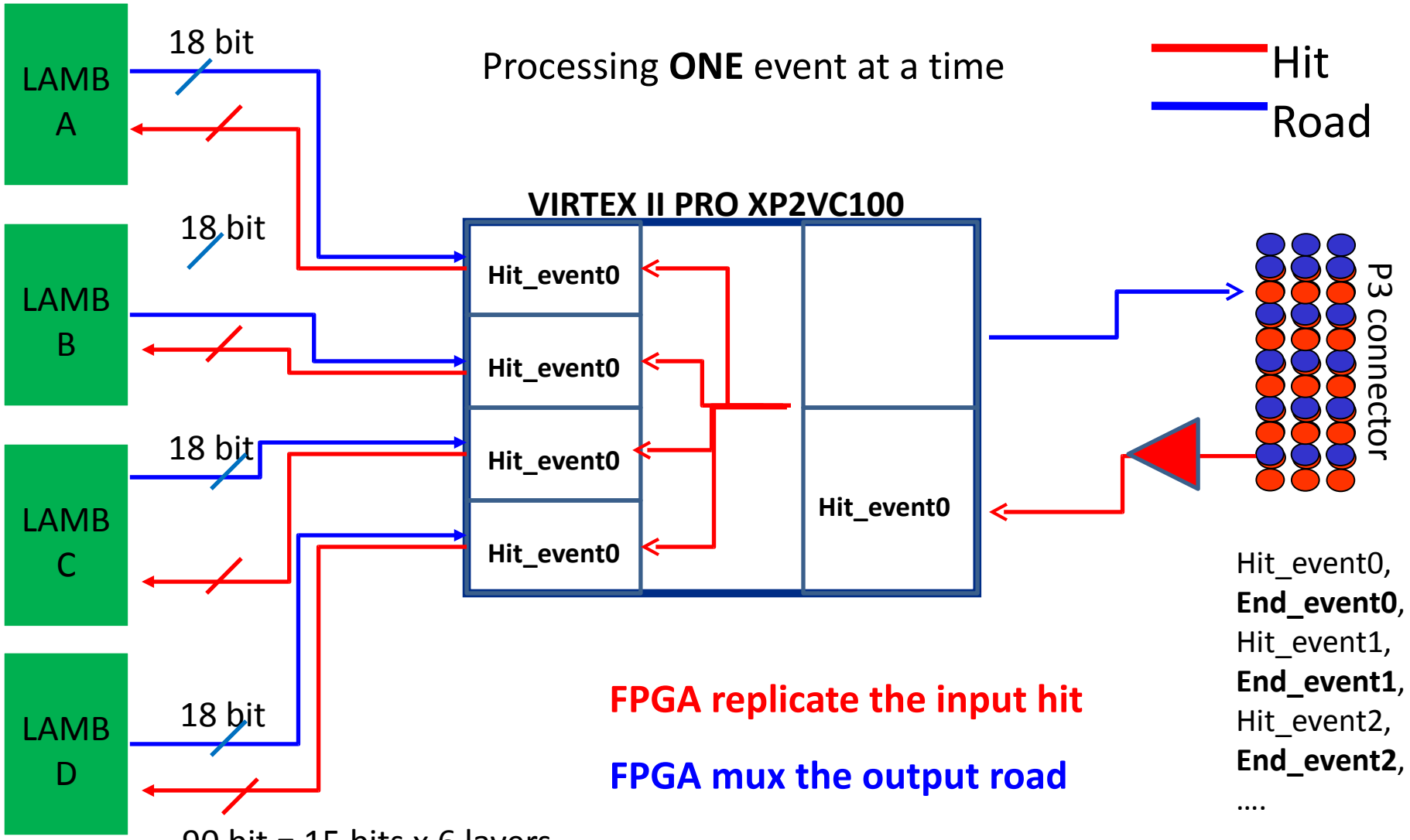




Period of clock **25ns** => reduce to **10ns (new AMChip)**

25 cycle to empty AMBoard – AMchip pipeline => **can be reduced**

AMBoard Logic Control (L2)



How many patterns we could fit in modern FPGAs?

e present: choice based on cost and package:
6SLX150T-4CSG484 (19x19 mm^2) 4 GTPs 296 pins (our package is LQFP208)
3 $ today → 16400 AMchips → **6 M$**
23 k slices, even assuming **~8 slices/pattern →**
~2.9 k patterns/FPGA <<< 80 kpat/(our Amchip: 12x12 mm^2 65 nm)

The future http://www.xilinx.com/technology/roadmap/7-series-fpgas.htm
Best Virtex 7 XC7V200T (new family not available now)
305 k slices → ~ 38 kpatterns/FPGA < 80 kpat/(our Amchip)
Using FFs: **2,443 Mff → ~120 FF/pattern → ~ 20,4 kpat/FPGA**
Even using Slices and FFs together < 80 kpat/(our Amchip)

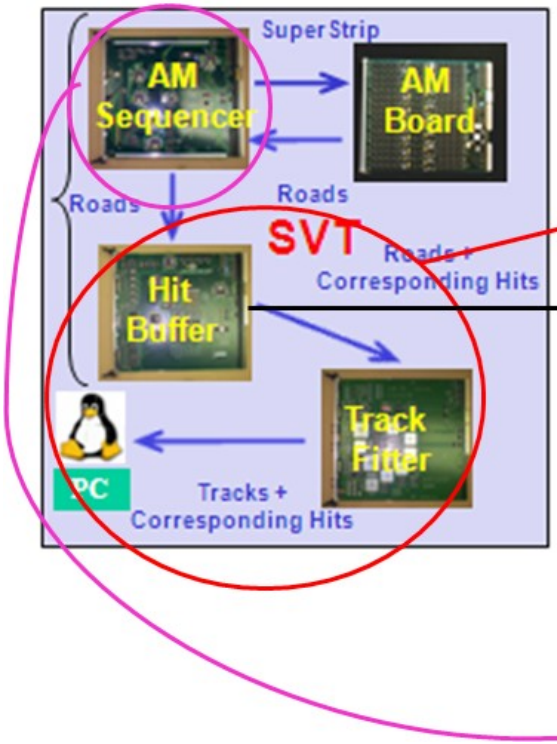
Even choosing the **best device of next years**
Even if we don't care about **cost and package**
Even with very **optimistic hypothesis** on a difficult design

we don't get our **AMchip power!**

Logic density increases with time: Track Fitting possible @L1 in Phase II

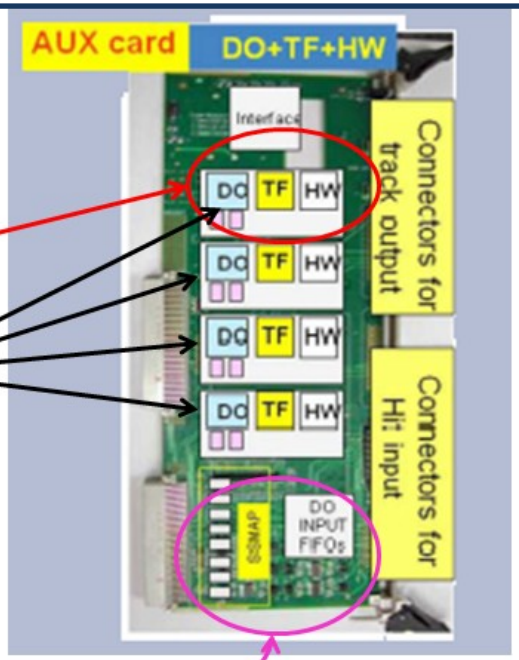
SVT: yesterday

AMSequencer – Hit Buffer - Track Fitter
= 3 9U VME boards



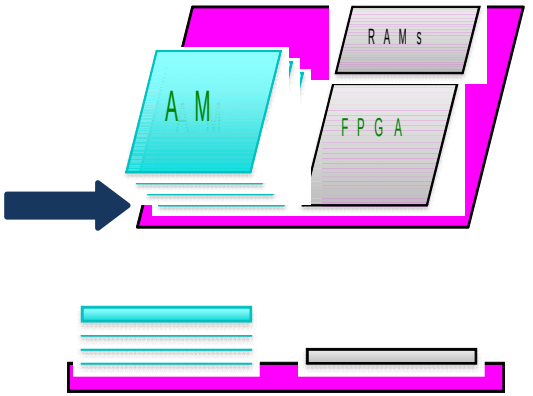
FTK: today

All in a mezzanine!
It's possible to multiply x 4



2020?

All in the AMchip!
It's possible to multiply x 128



LOW Latency
LOW cost