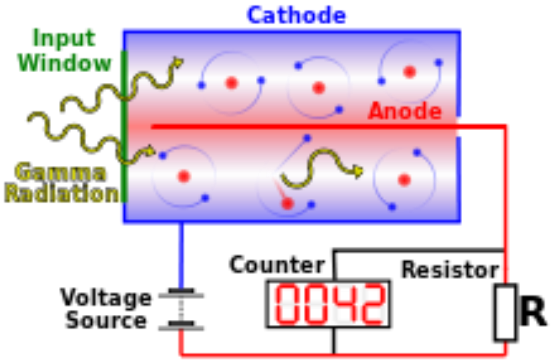
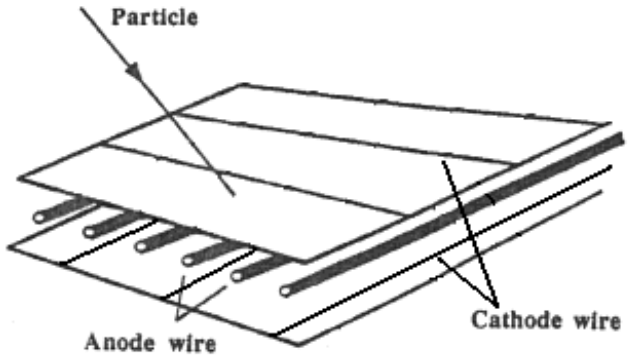
Results of 3 years of PhD (and counting)

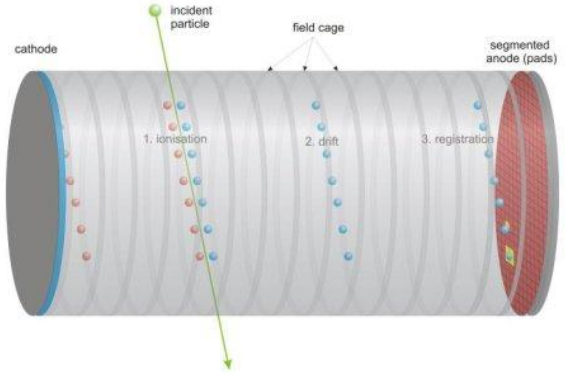
Francesco Zappon

Outline:

- Framework: gaseous detectors
- Micro Pattern Gaseous Detectors (MPGD): GridPix
- New chip prototype for MPGD: GOSSIPO family
  1. GOSSIPO-2
  2. GOSSIPO-3
  3. GOSSIPO-4







Geiger-Muller counter | Multi Wire Proportional Chamber | Time Projection Chamber

They are all gaseous detectors

↓

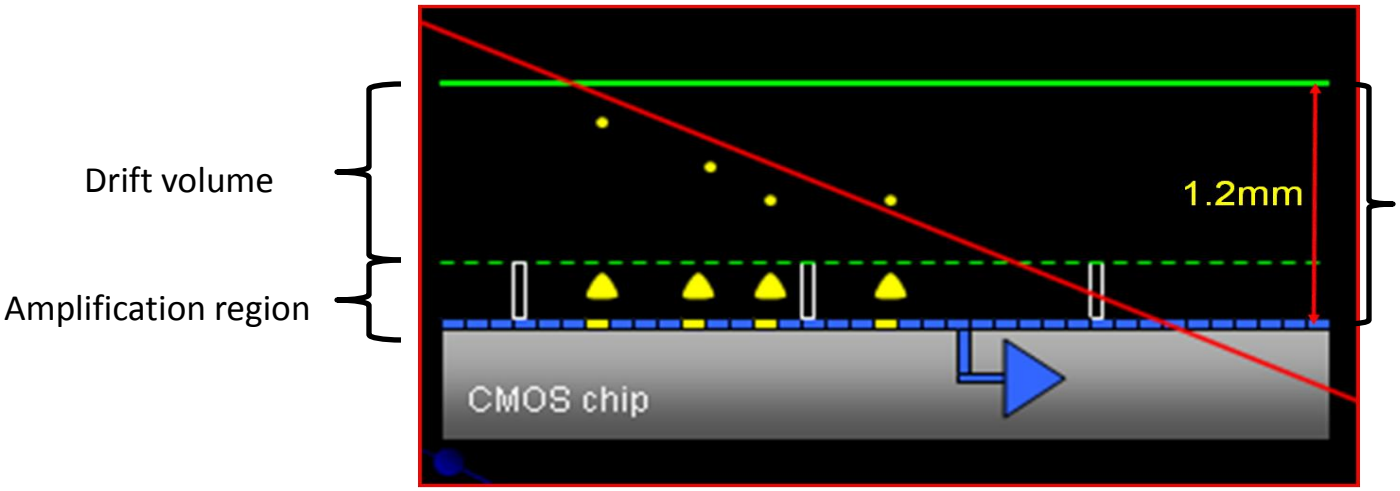
Key aspect: gas amplification to have a detectable signal

↓

But we want to do tracking → we need better resolution

↓

Go to the micro-world



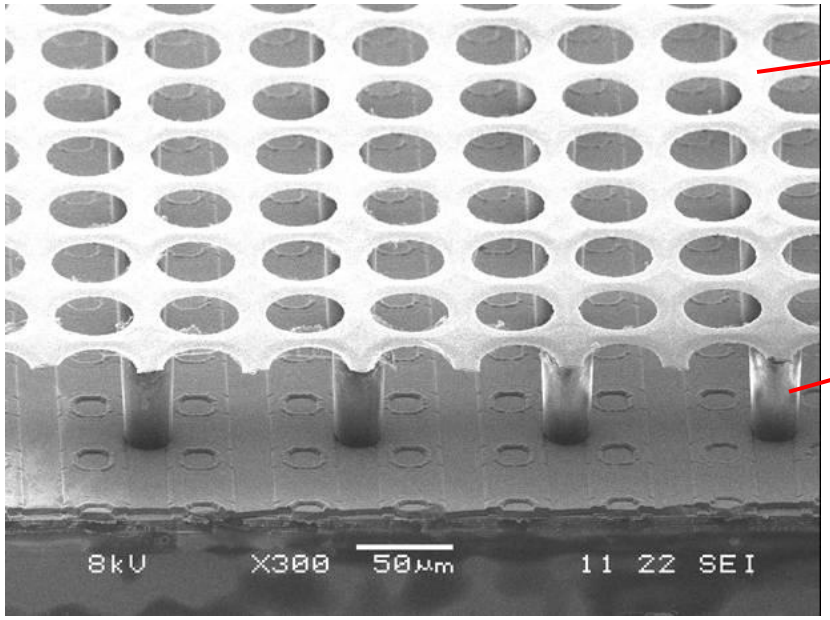
Picture not on scale: InGrid (Integrated Grid) is 50 µm above the chip; cathode, that determines the drift volume, is at variable height

Goal: perform a 3D reconstruction of a particle's track

- A particle passing through the Drift volume ionizes the gas
- Electrons drift to the anode by means of an electric field
- Amplification occurs in the region between the grid and the chip: electron avalanche
- x-y information is provided by the pixel structure of the readout chip
- z information is provided by the measured drift time

Advantages:

- Low mass detector
- In principle, 3D track reconstruction using only 1 plane of detectors
- Radiation hard

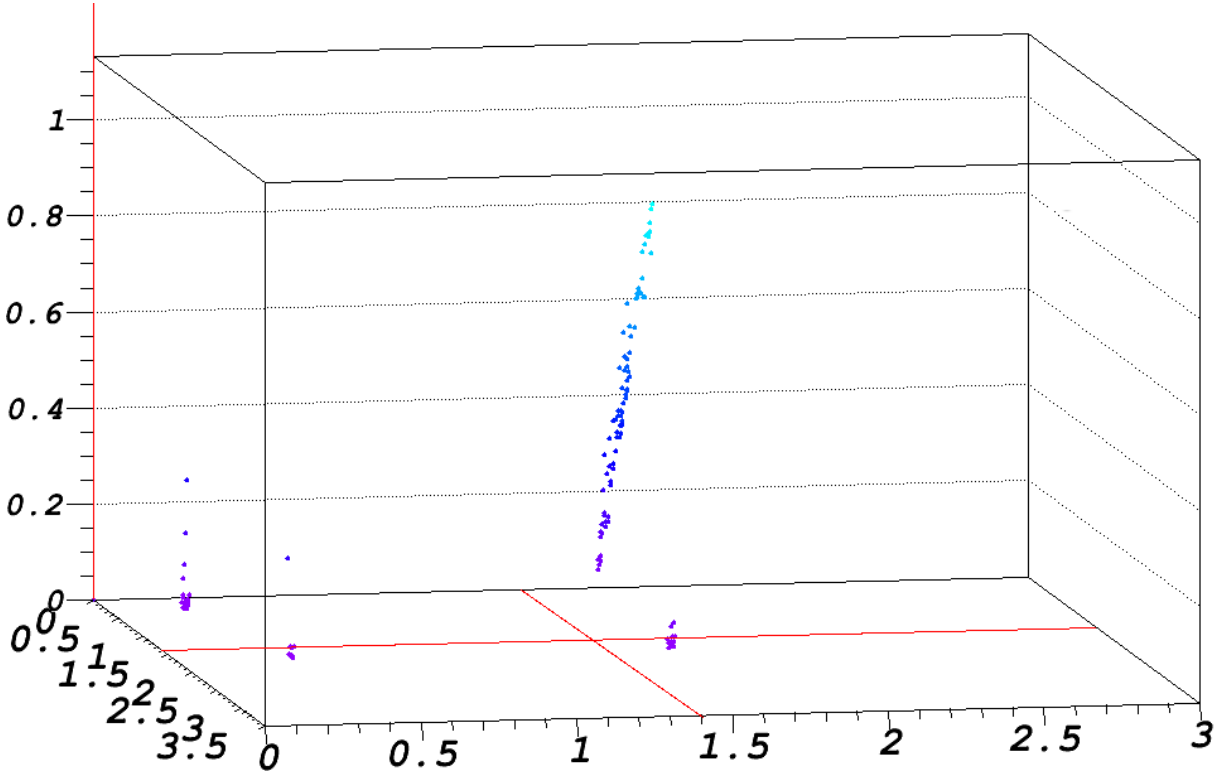


Currently GridPix detectors are built using the TimePix chip

Grid is built using MEMS technology: post-processing of the wafer

Current features:
- 10 ns resolution of TimePix chip
- detectors with different drift volume thickness (1 mm,…,2 cm)
- different gas mixtures being tested

GridPix event example



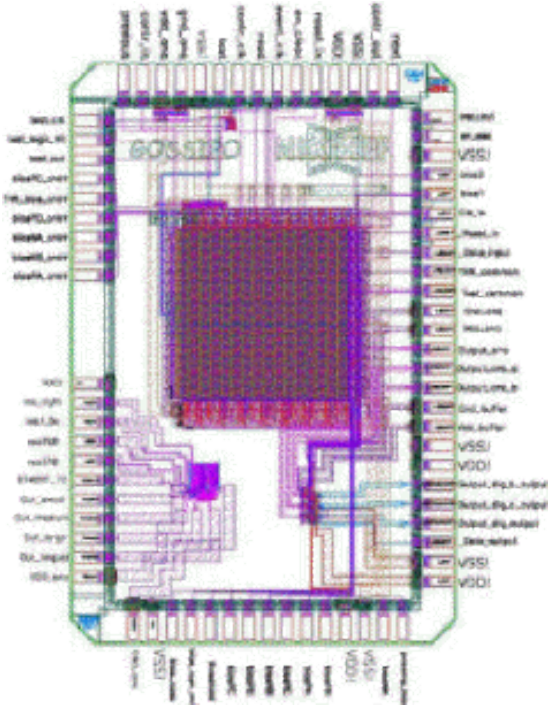
Improvements: the goal is to have a small drift volume and still be able to perform good tracking. To do this you can:

- improve the time resolution → new readout pixel chip
- find the best gas for your application → detector test
- correct for intrinsic effects (i.e.: time-walk) → offline analysis

At Nikhef there is a R&D program together with the Electronics group to develop a new chip suited for GridPix application: GOSSIPO family of chips

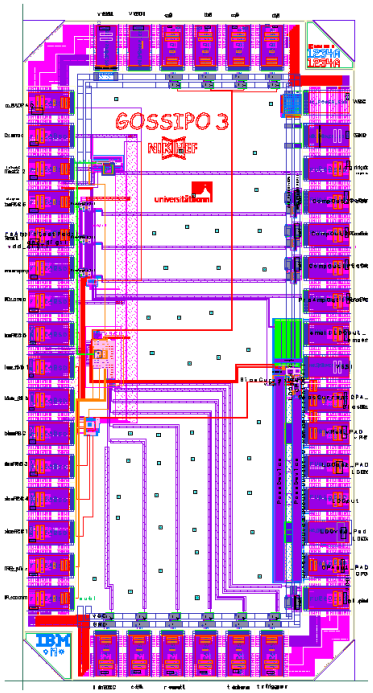
My work is focused on this group of chips

GOSSIPO-2



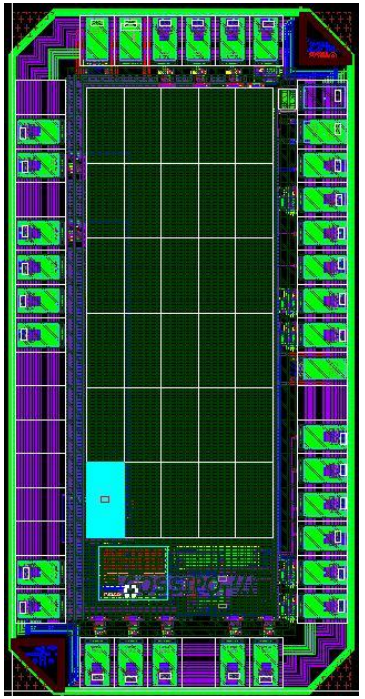
Detector performance

GOSSIPO-3

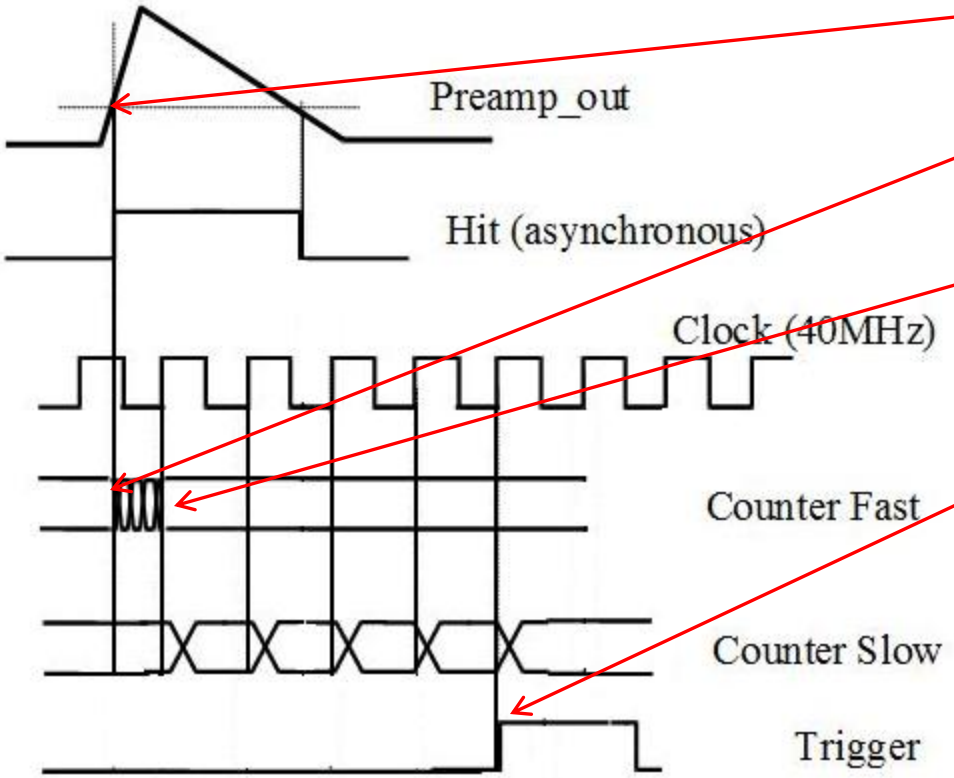


Physical implementation & testing

GOSSIPO-4



Design & testing



The signal goes above threshold

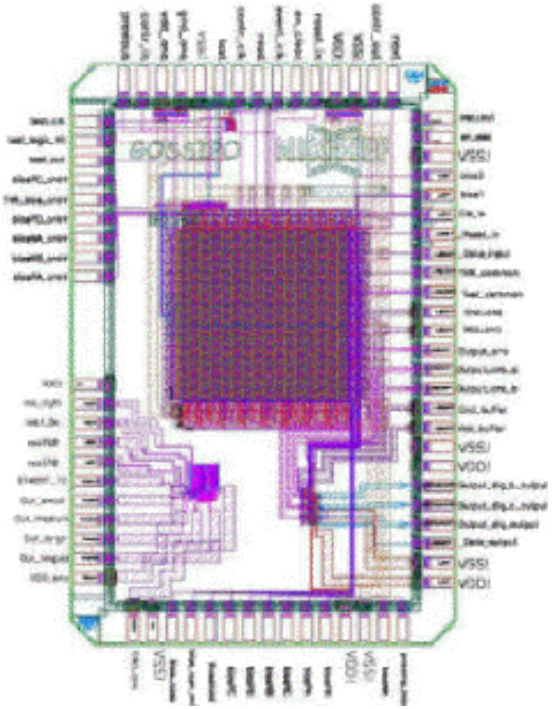
Fast oscillator starts

Fast oscillator stops at the first rising edge of the slow clock + slow counter starts

Trigger arrives: stop slow counter

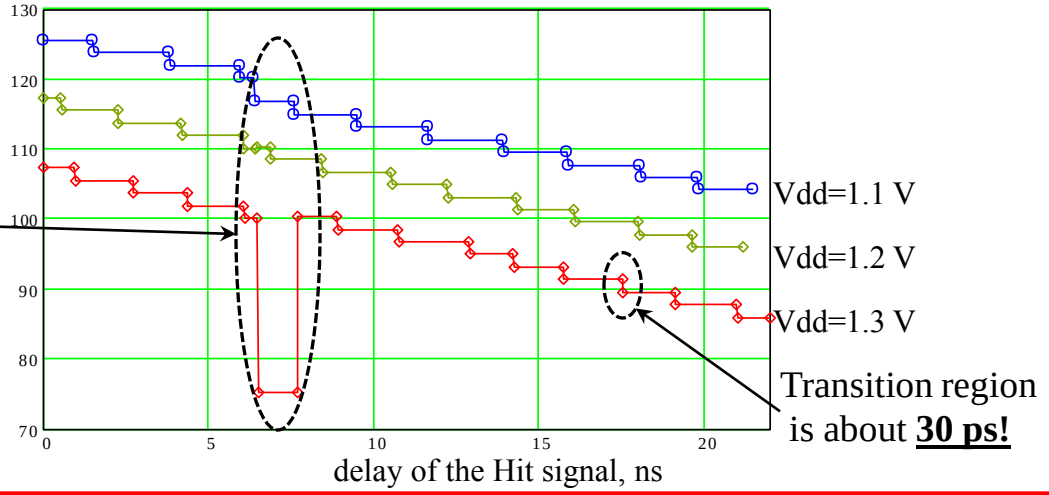
→ The combination of the fast and the slow count gives the Drift Time

Additional: a counter can record the number of clock cycles the signal is above threshold. The Time over Threshold information is related to the energy of the signal itself.



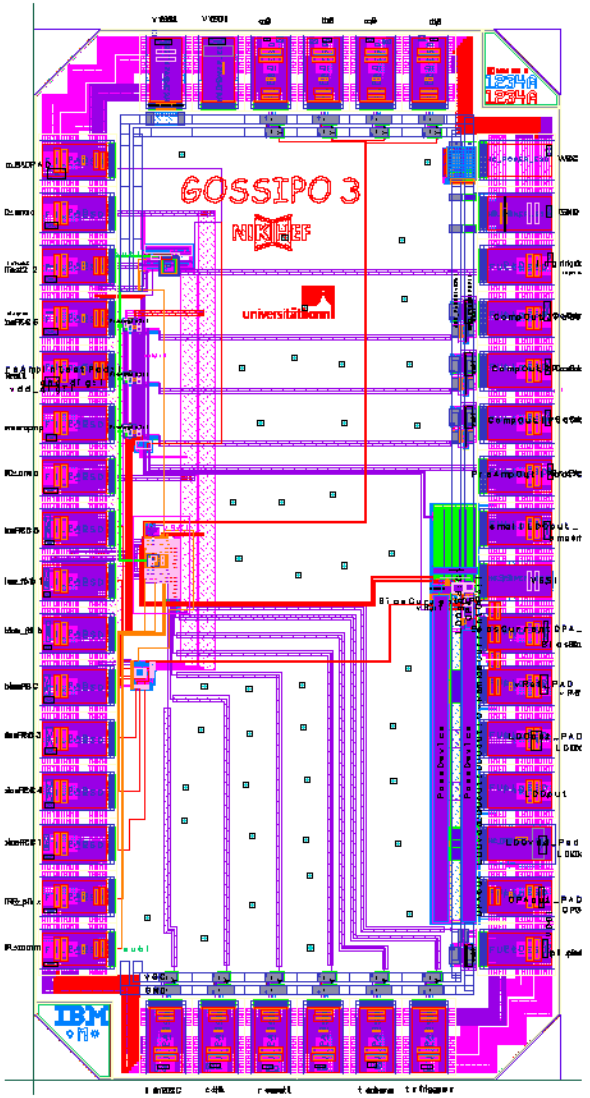
- GOSSIPO-2 is a fully functional chip developed at Nikhef in 2007
- 16 x 16 pixels (active area: 0.88 mm^2)
- Pixel size: 55 x 55 µm
- The chip itself has been already electrically tested and the problems that have been seen there lead to the design of GOSSIPO-3
- There is now a plan to build a basic GridPix detector with it: my job will focus on testing the detector with a source

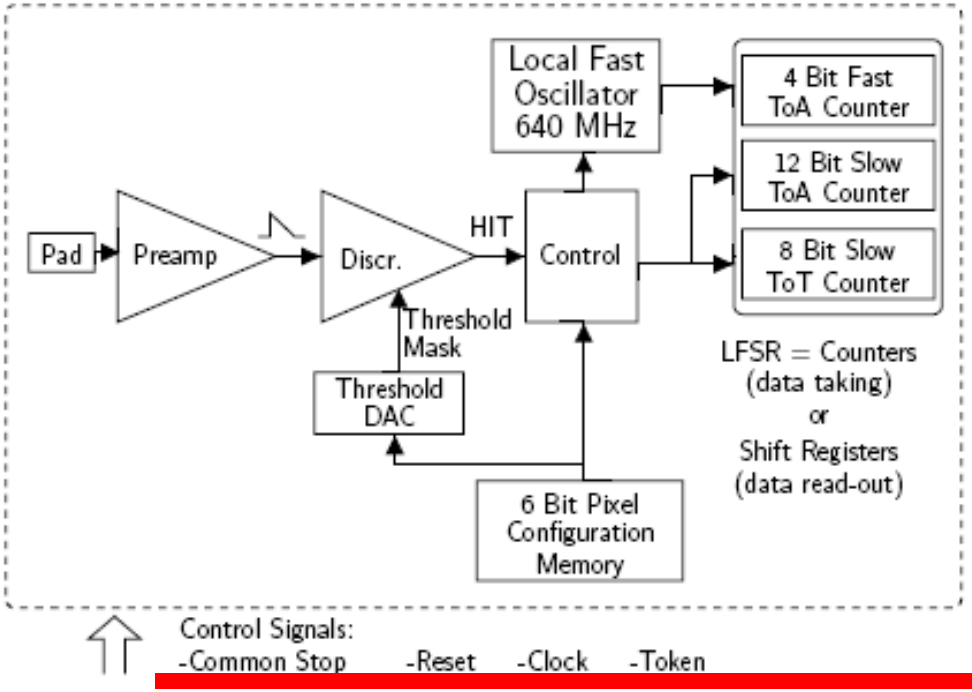
Discontinuity occurs when the Hit signal goes over the leading edge of the slow clock ("slow") signal.



GOSSIPO-3 main features:

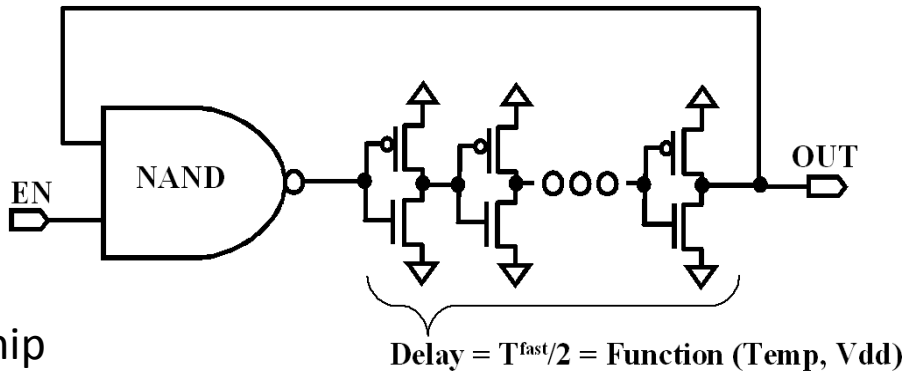
- Designed in collaboration between Nikhef & Bonn University (Submitted October 2009, tested in 2010)
- 130 nm technology
- Pixel size: 60 x 60 µm
- 2 pixels: one complete (called Analog) and one with only the digital blocks (Digital)
- Additional circuits in the chip: Low Drop Out regulators, Phase Locked Loop (PLL)
- ToA: 1.6 ns resolution with 102.5 µs dynamic range
- ToT: 25ns resolution with 6.4 µs dynamic range

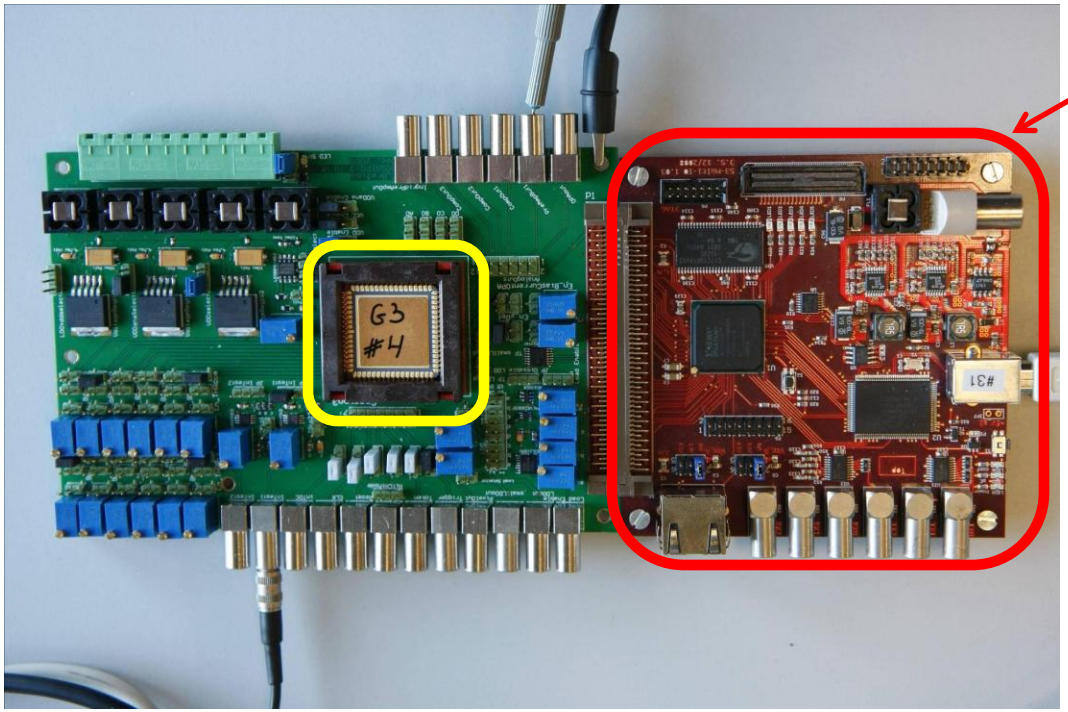




- Two operations mode: time count and hit count
- Oscillator in every pixel
- Linear Feedback Shift Register as counters→fast counter is 4 bits: 15 states available
- Serial readout

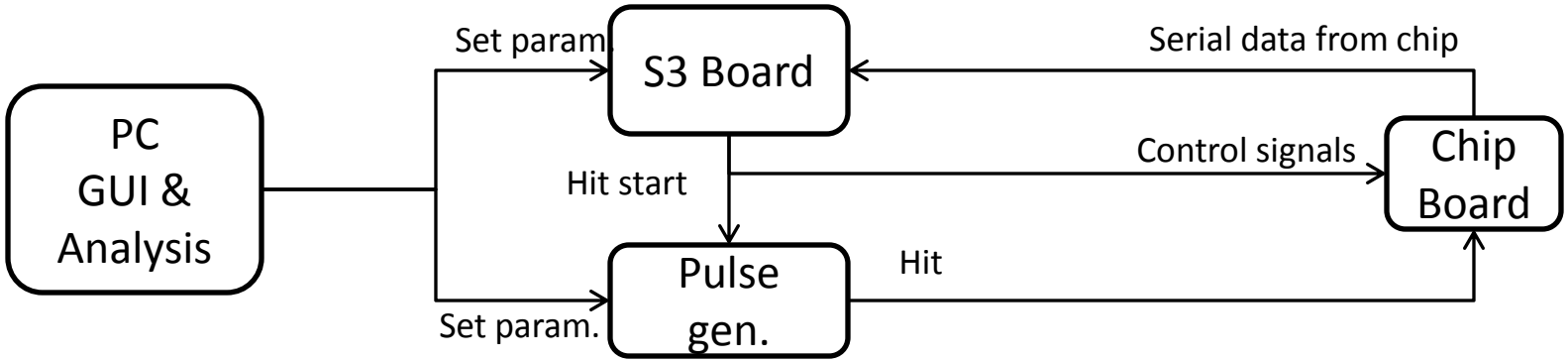
- Daisy-chained inverters to make the delay
- Feedback to create the oscillator
- Oscillation period depends on supply voltage and temperature
- Adjustments for channels mismatch is done on chip using Low Drop Out regulators

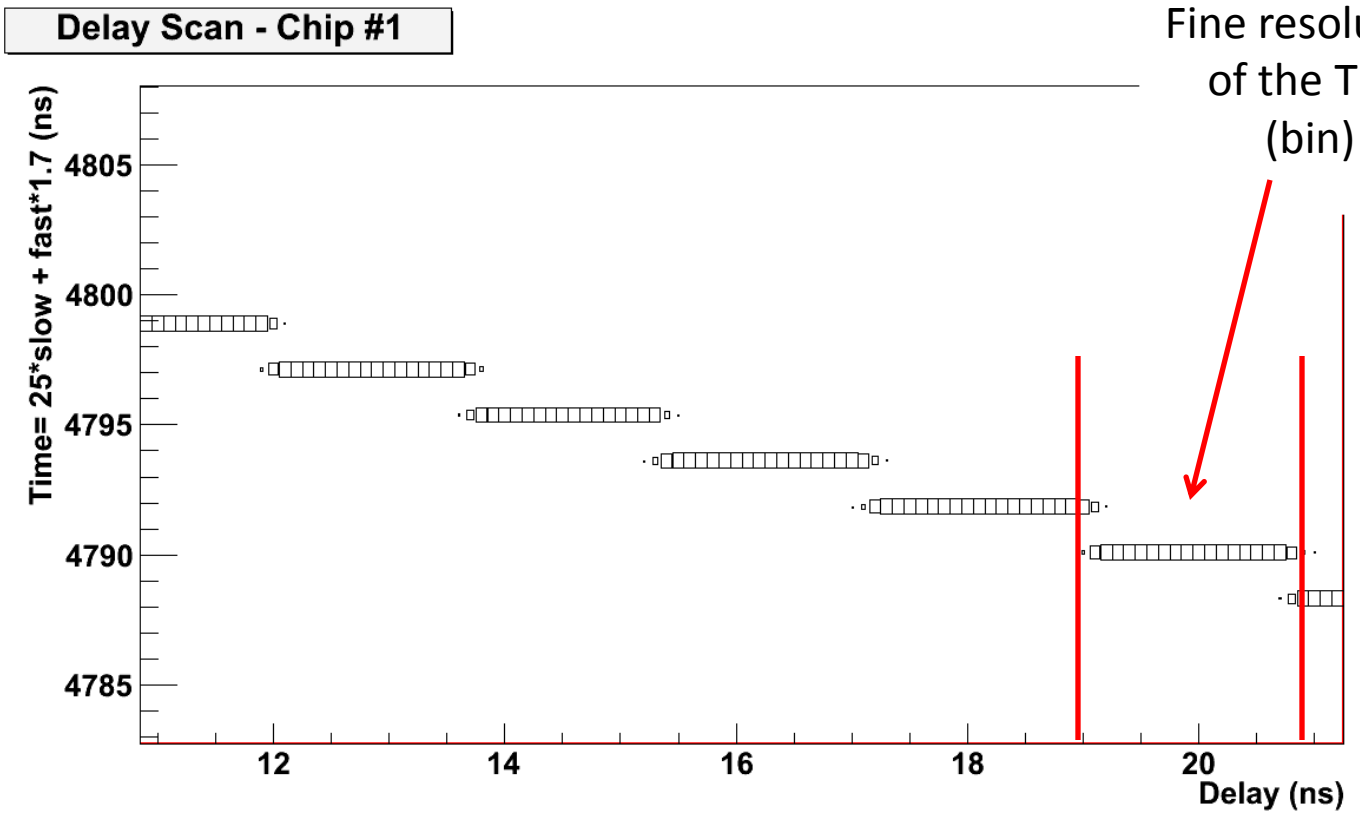




S3 test board (provided by Bonn)
- Xilinx FPGA
- USB control
- Dedicated API available

Development of:
- FPGA firmware
- C++/Qt GUI to control the test equipment
- Analysis programs

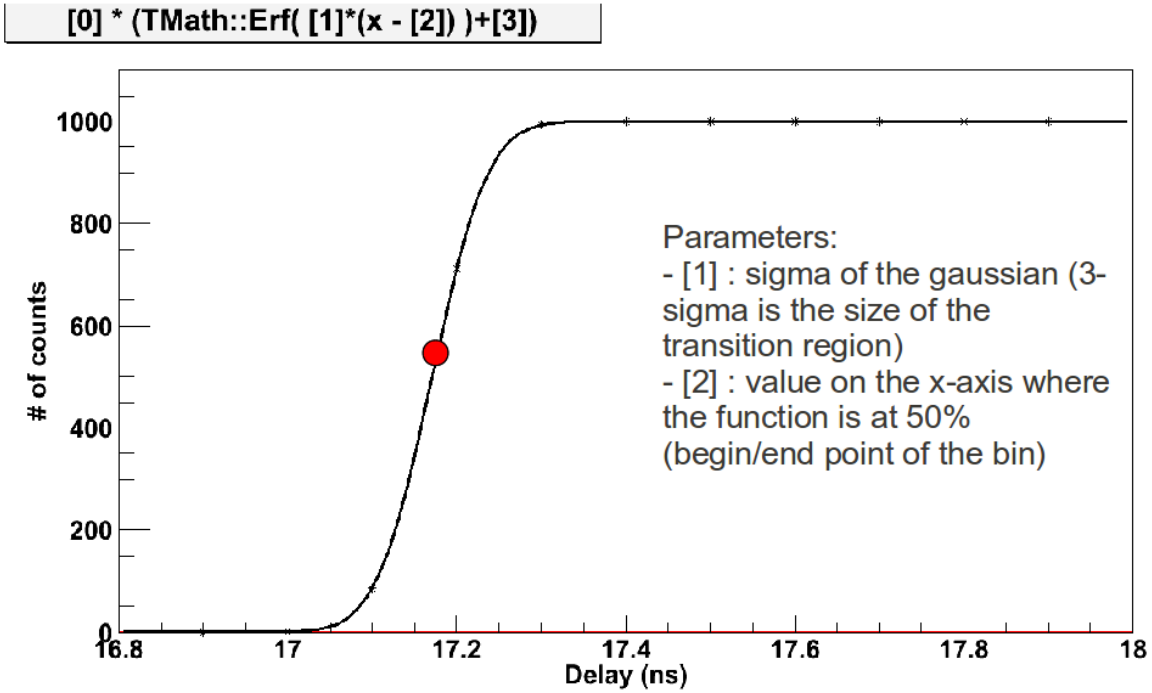




- Delay the input test pulse w.r.t. the Trigger
- Combine the values of the Fast and the Slow counter to obtain the ToA

→Characterize the TDC

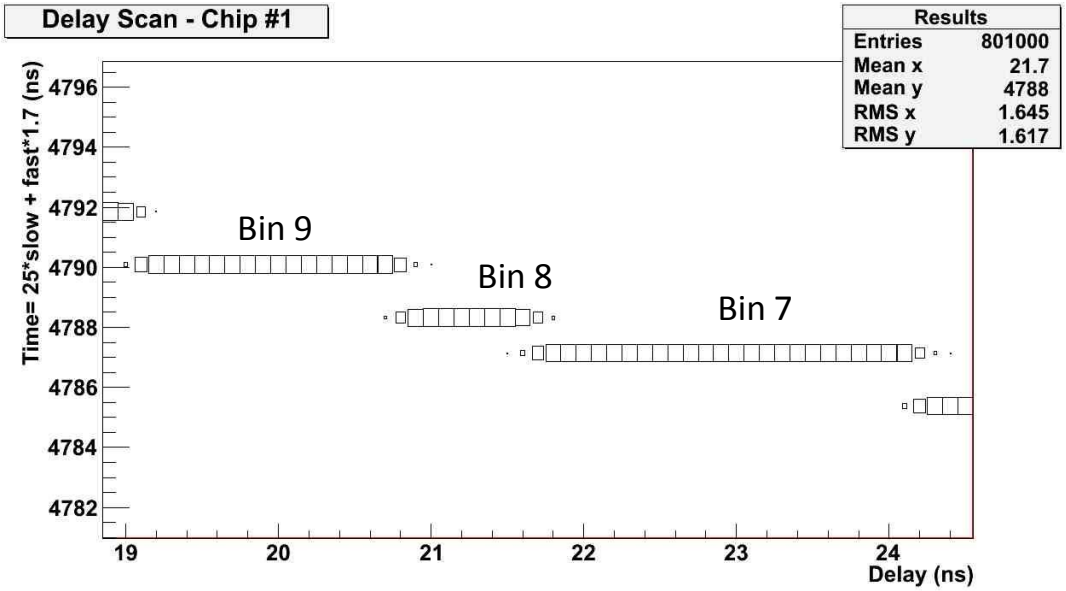
- 1000 pulses sent per delay value

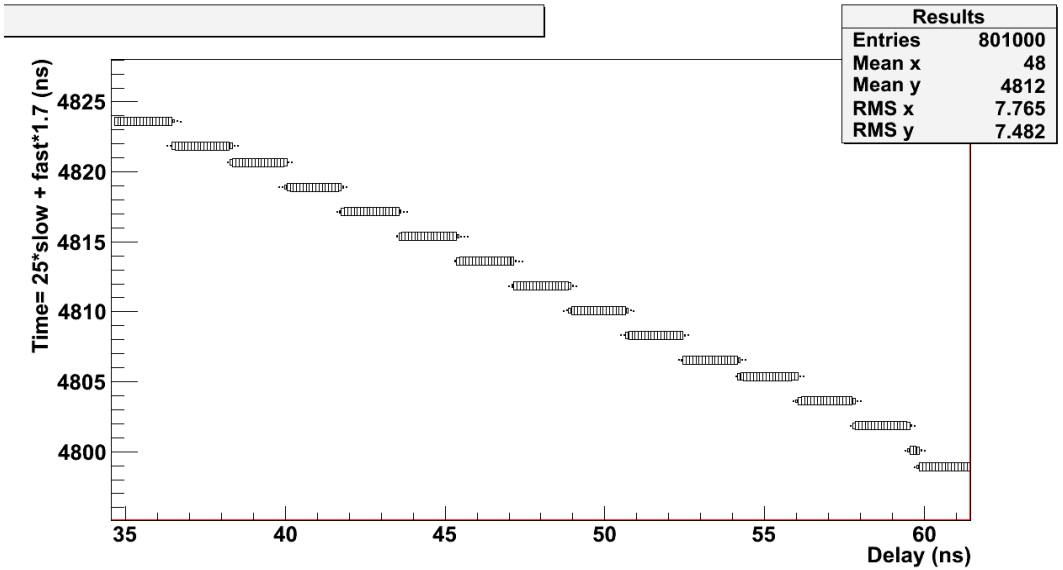


- Fit the transition region between bins of the TDC with the so-called error function
- The fit gives 3 parameters
- Determine the Differential Non Linearity to characterize the TDC

Differential Non Linearity:
parameter to quantify the precision of a converter (ADC, DAC or TDC).
The term differential refers to the difference in two consecutives values of the converter.

Chip 1	Bin Size (ns)	Error	Jitter (ns)	Error	DNL
Digital	1.7525	0.3217	0.052	0.006	19.9%
Analog	1.7701	0.2163	0.09	0.01	31.83%





- In the analog Pixel the DNL is large because of the big difference between bin 8 (small) and 7 (large)

- The cause of this difference is due to crosstalk effects with the falling edge of the system clock (40 MHz)

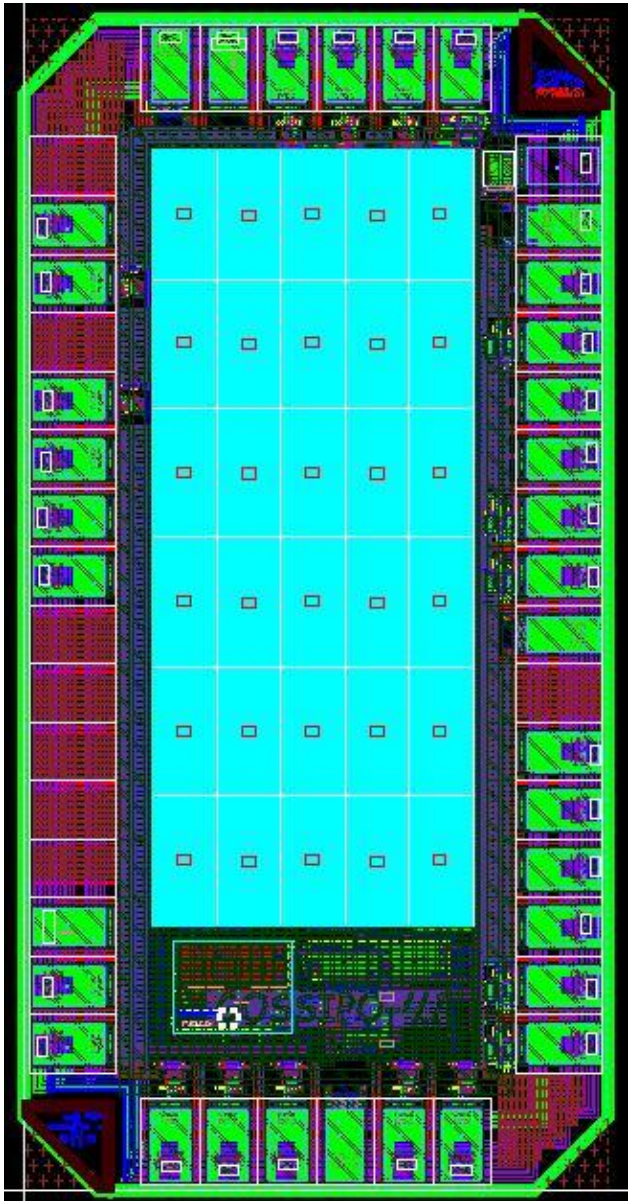
- Testing the TDC with a 20 MHz clock move the problem

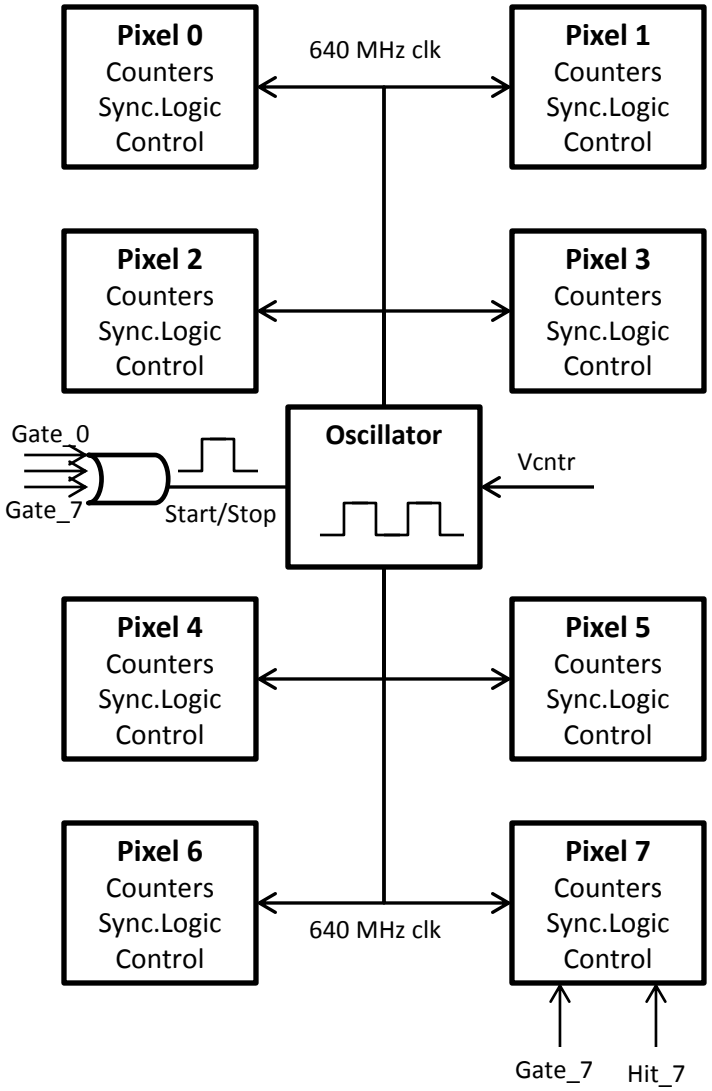
- Most likely, the quite high DNL is caused by noise in the supply voltage that influence the oscillation period

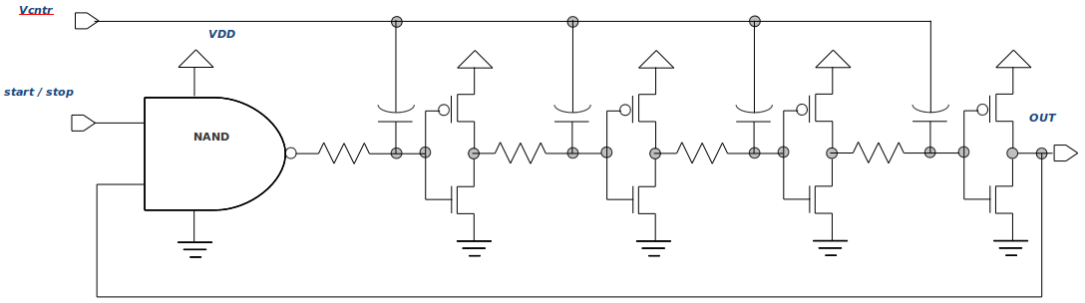
- This behavior is not fully reproduced by simulations

To overcome the problems of GOSSIPO-3, a new prototype has been planned in the framework of TimePix3 chip → GOSSIPO-4

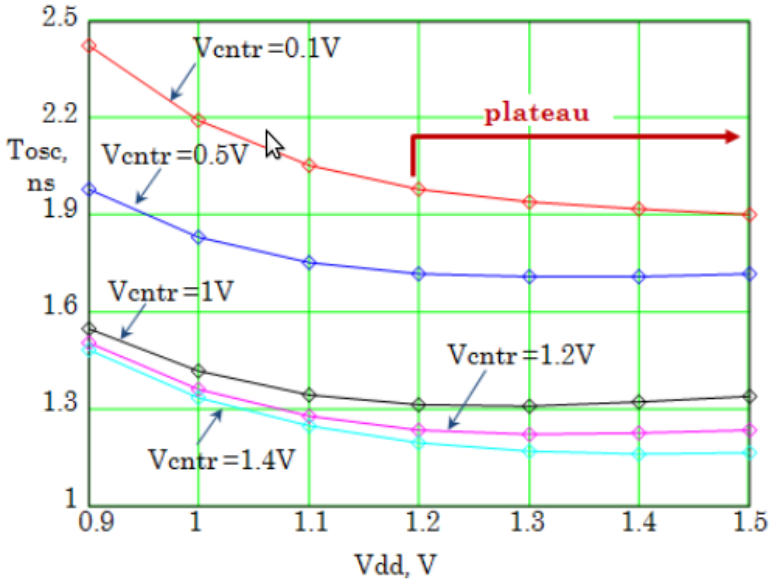
- New oscillator: to be less sensitive to variation in the supply voltage
- Shared oscillator and Super Pixel: to save area and power
- Testing of a new High Density library designed at CERN: can it operate at high frequency?
- New design for the Phase Locked Loop (PLL)
- Testing of Rail-to-Rail buffers to distribute the control voltage supplied by the PLL



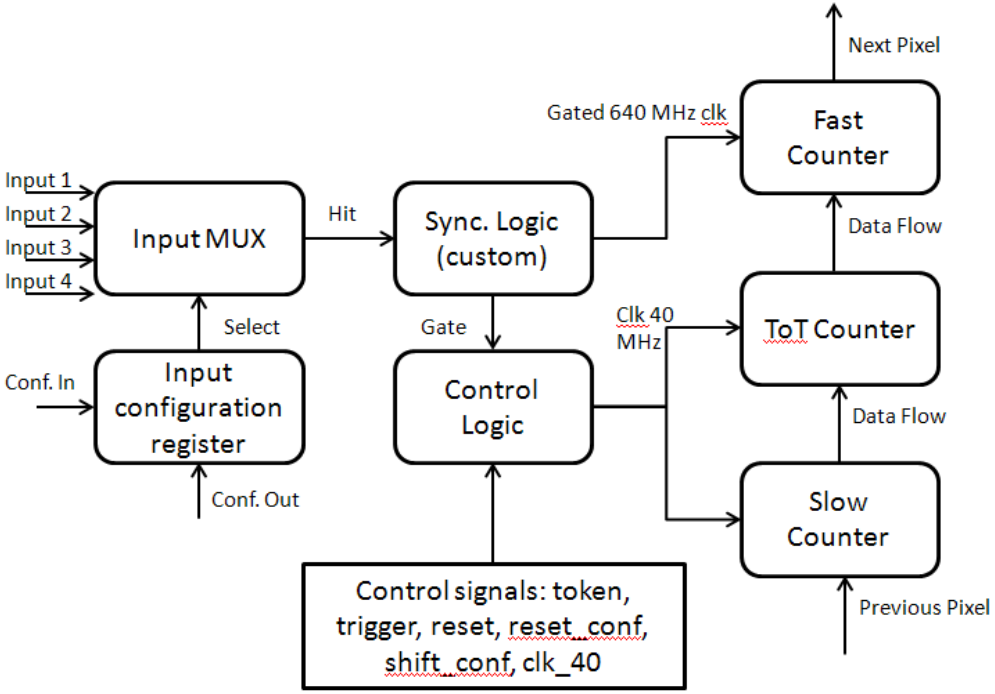




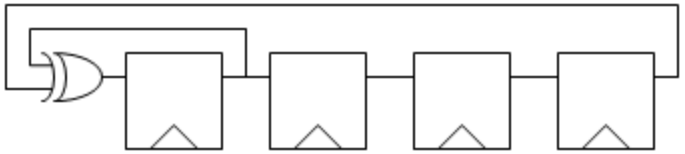
Vcntr and VDD (supply) are separated. Vcntr is provided by the PLL in the periphery. Delay introduced by the RC structure, inverters used for buffering



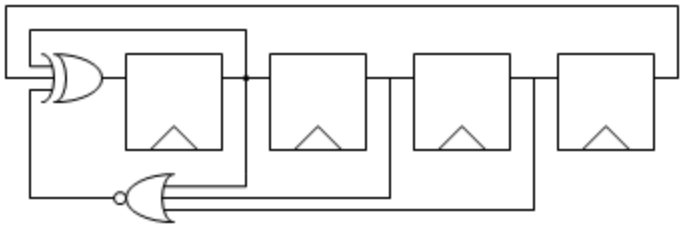
Notice that for supply voltage (VDD) > 1.2V the oscillation period is independent from VDD



- One operation mode: time count
- No analog frontend
- Linear Feedback Shift Register as counters
- Serial readout

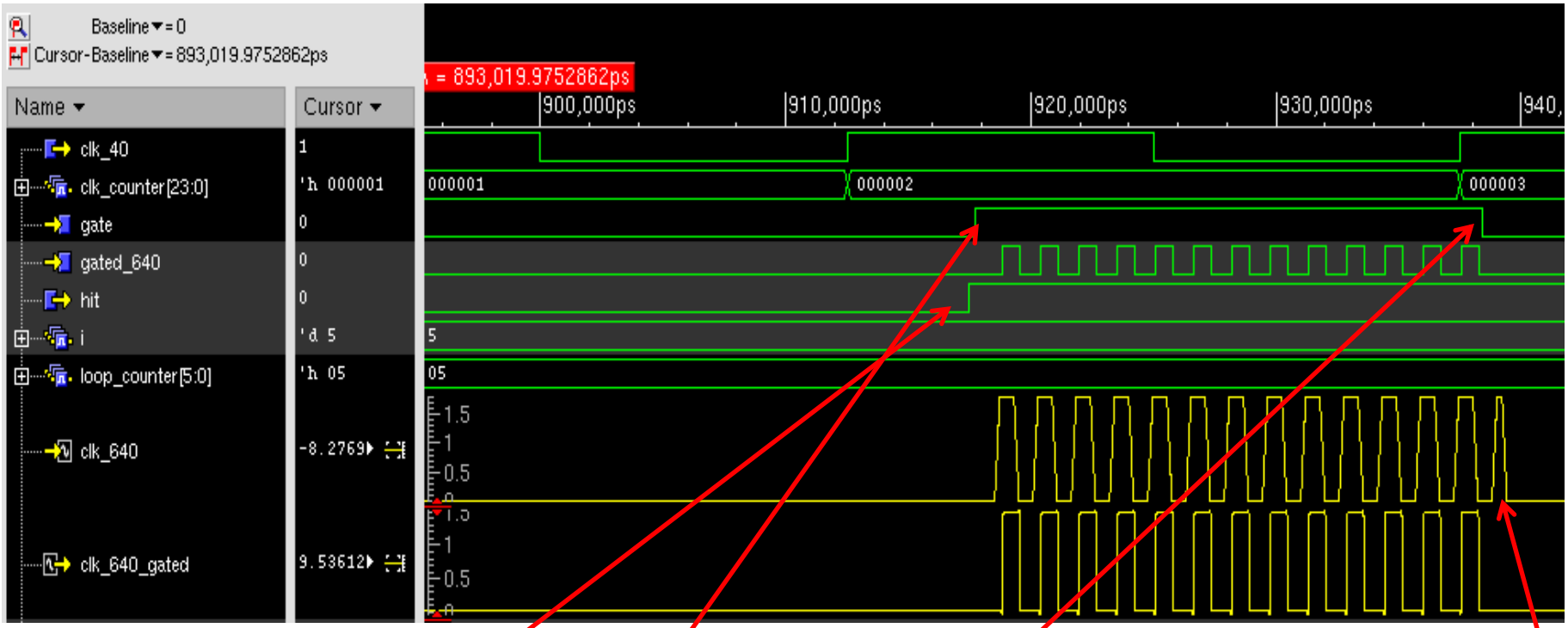


Regular LFSR: 4 bit, 15 states



De Bruijn LFSR: 4 bit, 16 states

Maximum length LFSR	De Bruijn Sequence
1111	1111
0111	0111
1011	1011
0101	0101
1010	1010
1101	1101
0110	0110
0011	0011
1001	1001
0100	0100
0010	0010
0001	0001
1000	0000
1100	1000
1110	1100
	1110



Hit arrives

Gate = 1

At rising edge of clk_40: Gate = 0

Gated clk_640: no glitch propagation

GOSSIPO-4 (version 2) has been submitted at the beginning of August 2012; expected to be back at Nikhef in October/November

First prototype submitted in August 2011: FAIL!

Due to:

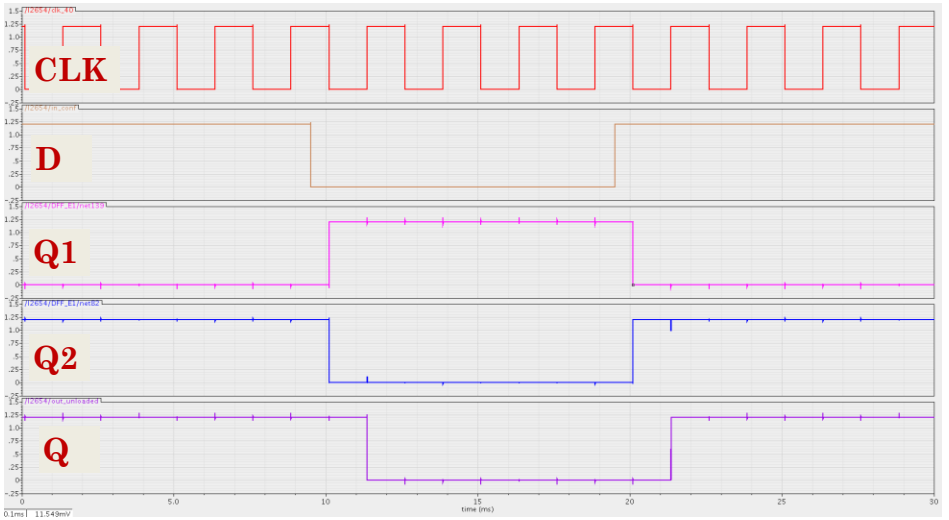
• lack of time: design done “by hand” (including interconnections, chip ring and some blocks) with almost no simulations

• wrong behavior of a Flip-Flop: if the load exceeds 30 fF the internal nodes of the FF do not follow the input behavior

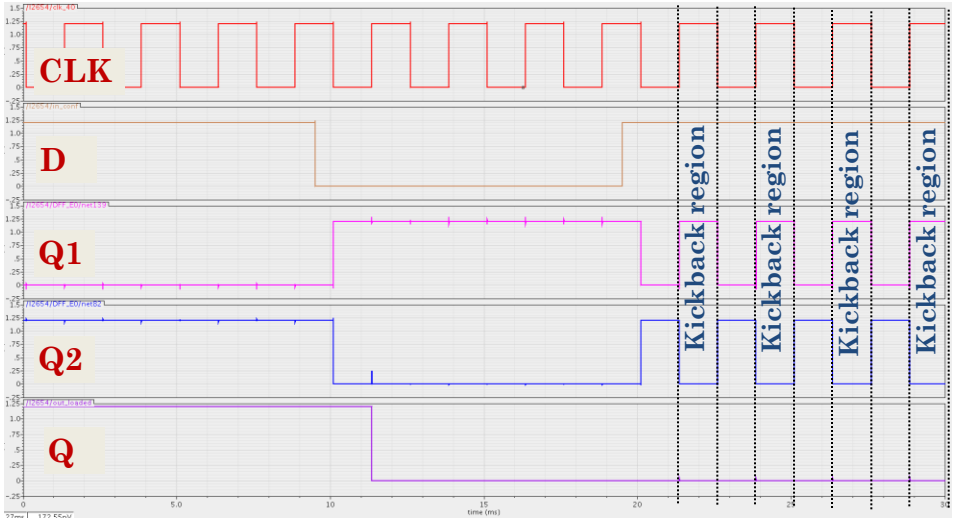
→The combination of these reasons resulted in a non-working chip, no possibility to extract useful information from the Pixels

Second prototype submitted in August 2012

No load : proper operation (400 Hz, vdd=1.2V)



Loaded with capacitance : wrong operation (400 Hz, vdd=1.2V)



Being a PhD in MC-PAD

Goal of the PhD: to become a chip designer

Previous knowledge: basics of analog and digital electronics, basic Verilog knowledge

The topic of my work is not directly related to physics, it has more connection with electronic engineering = I had to learn everything useful for my work from scratch

In my daily work the courses I had at the university were not sufficient!

→ Understanding and applying the design flow (from the requirements to the final chip)
→Using the Cadence environment both for analog and digital design&simulations
→ Testing of the chip: how to perform it, understanding the results
→ Data analysis: “usual” C++/ROOT usage

Good:

- Goal of the PhD clear since the beginning
- A lot of expertise at Nikhef on the subject
- Training and additional activities well organized (both MCPAD and Nikhef specific)

Bad:

- Planning not always done in advance
- When planning was there, still a lot of changes in the activity (some intrinsic in the research activity, other could have been foreseen in advance)
- Time lost due to poor communication with external institutes

MCPAD general evaluation

Training events:
• Relevant to my work
• Well organized
• Slightly too short
• More “lab” practice would have been a plus

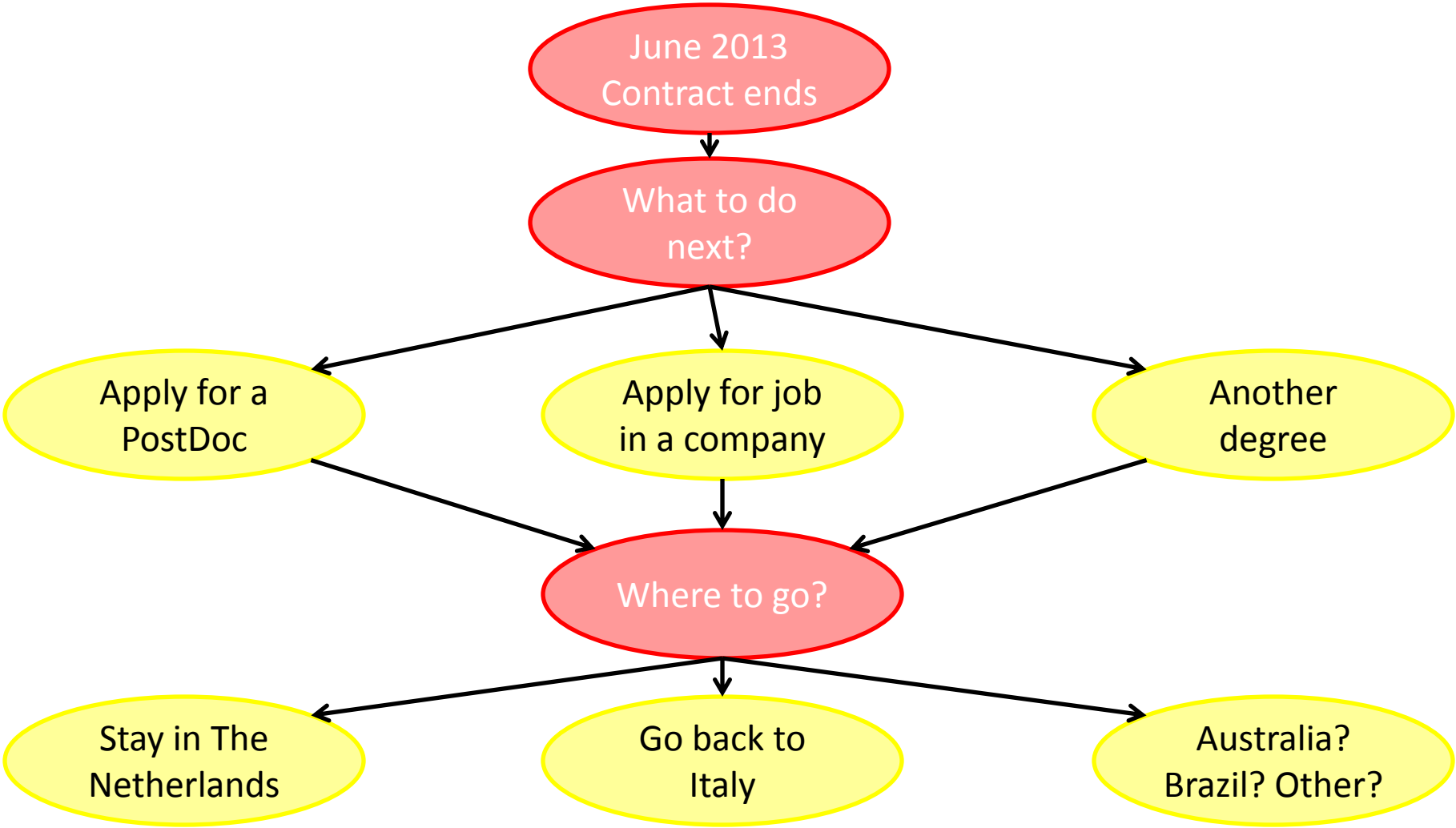
Work with Industry:
• completely absent

Work with another partner institute:
• completely absent (in my case, because the “partner” position never started)

Contact with other students in the network: absent, except for the training events

Very nice environment to be part of

Good financial aspect, with money for courses, books, travel



Very interesting alternative: open a hostel in New Zealand!

A short (and probably incomplete) list of people to thank for these 3 years (and counting) of PhD

• Els Koffeman for offering me the position in the network

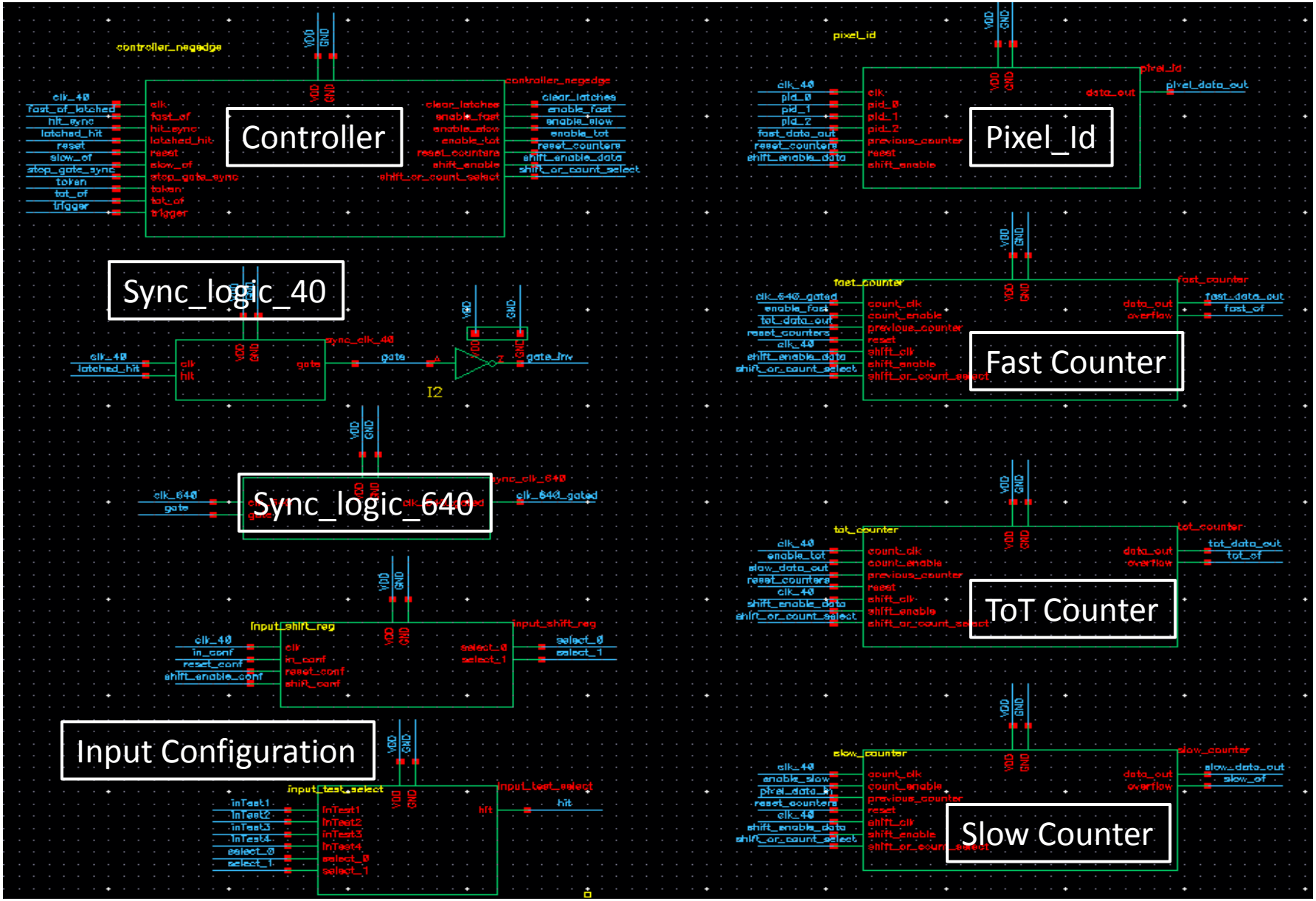
• Martin Van Beuzekom for being a great supervisor

• The Nikhef R&D group for help and the fun during the PhD

• The Nikhef Electronic Group (Ruud kluit, Vladimir Gromov, Vladimir Zivkovic, Deepak Gajanana) for their constant help and support

• The MC-PAD people: supervisors, students, external guests, to make all the events memorable. A special mention to Veronique: without her help we would have been lost!

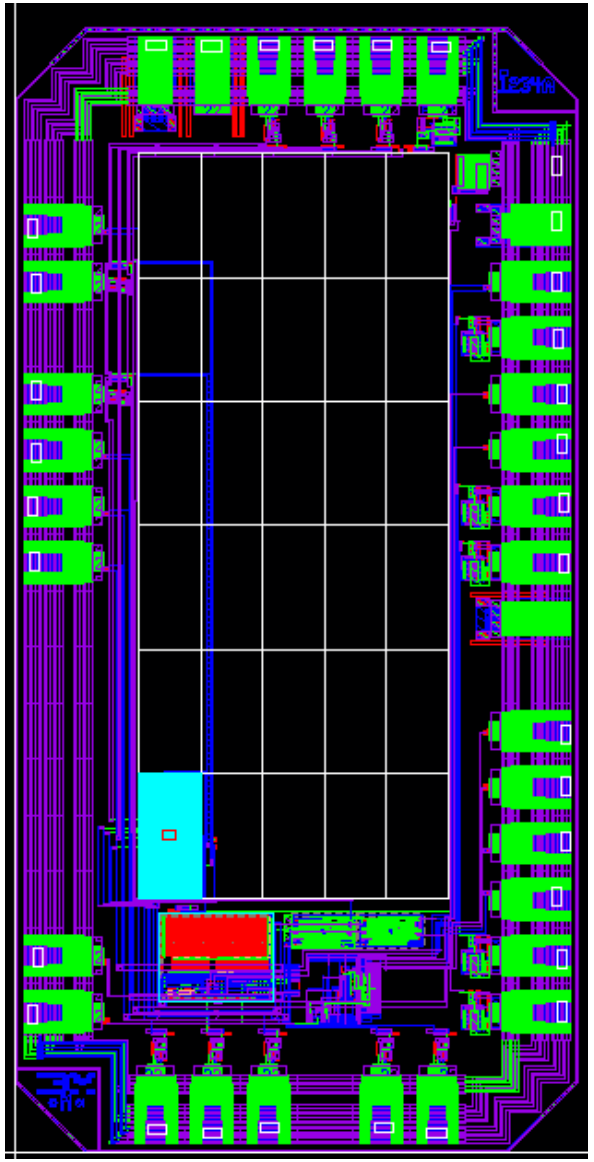
Backup slides


Controller
Pixel_Id
Sync_logic_40
Fast Counter
Sync_logic_640
ToT Counter
Input Configuration
Slow Counter

Due to lack of time we decided to take a 2 stages approach:
- Stage 1: prepare a chip with only 1 Super Pixel: this is a safe net, in case we don't manage to finish the matrix (30 super pixels structure)
- Stage 2: prepare the matrix

Design flow:
- Synthesis: RTL Compiler
- Post-Synthesis simulations (done): we found some wrong behavior in the design at this level and this helped us in fixing it
- P&R: completely automatic with Encounter
- Post-layout simulations (done)
- AMS simulations with the extracted parameters of the oscillator
- Top level integration done in Virtuoso + simulations

Submission:
-Deadline: 6th of August
- Subimission of a fully simulated stage 1 design the 8th of August (accepted for fabrication)
- We have worked to submit the final "matrix" (30 Super Pixel). It is now finished but there was no possibility to submit it (request sent the 17th of August: the designs have already been sent for fabrication)



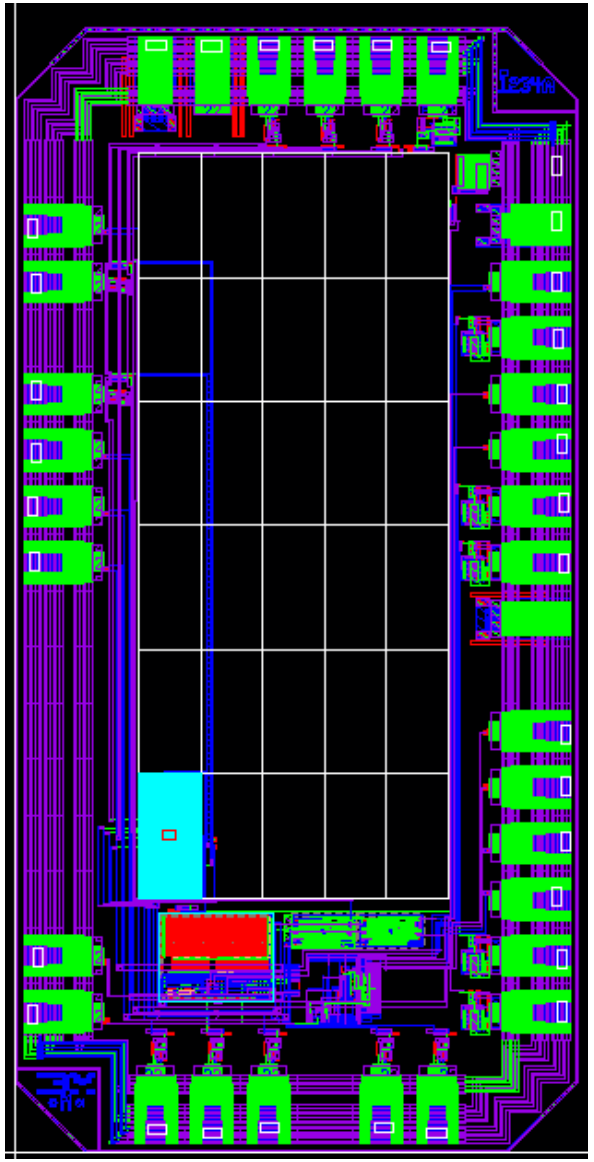
Blocks:

- Fast Counter is the same used in TMPX3

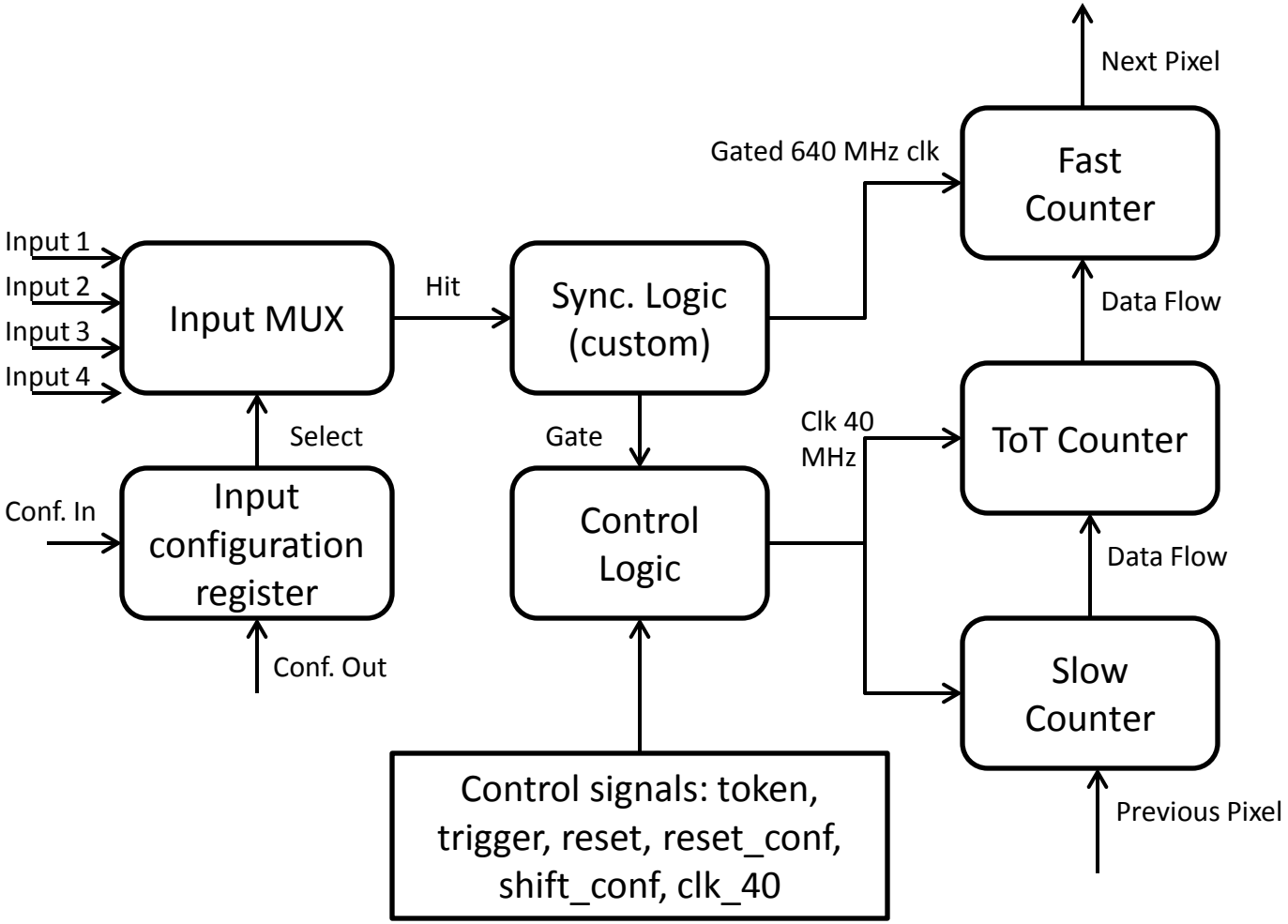
- Sync Logic is the one designed at Nikhef: there was no time to compare the Nikhef and the Cern one and I felt more confident in using what I designed

- PLL has been modified as discussed in previous meetings

- The oscillator has been modified to match the HD library (no more substrate connection problems in LVS)



GOSSIPO-4: single pixel block diagram



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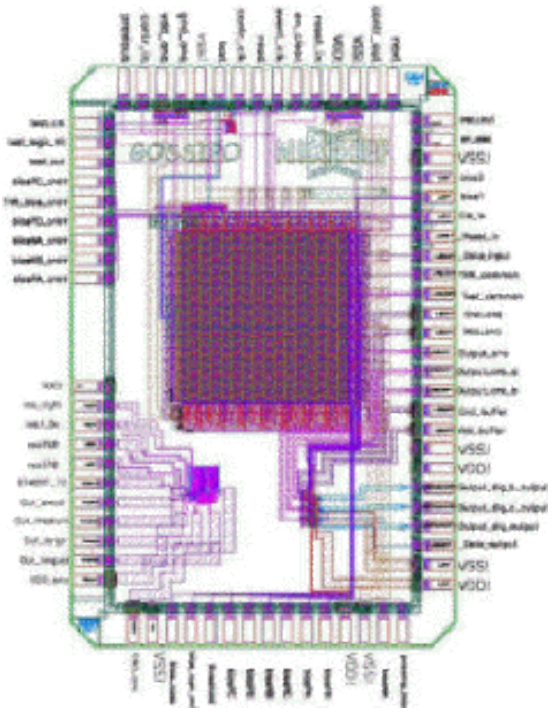

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