Front End Electronics (P11)

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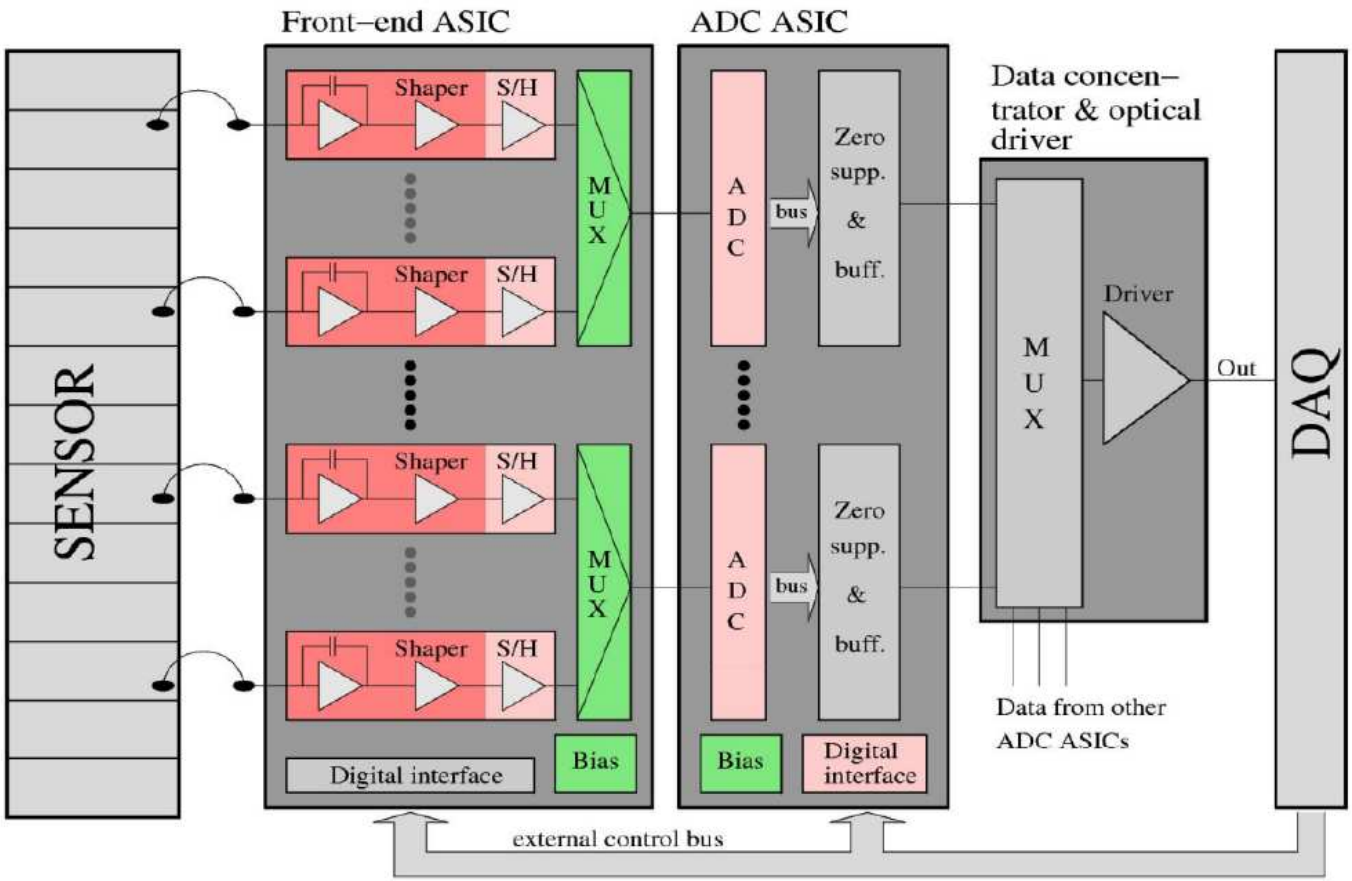
Outline

- Readout System
- Review -ADC Test & Measurement
- Review - SPI like interface for multi channel ADC
- Multi-channel ADC -Slow control with I^2C
- Conclusion

Readout system



ADC Test & Measurement

- 10-bit pipelined ADC.
- Six different versions.
- Power scaling type.

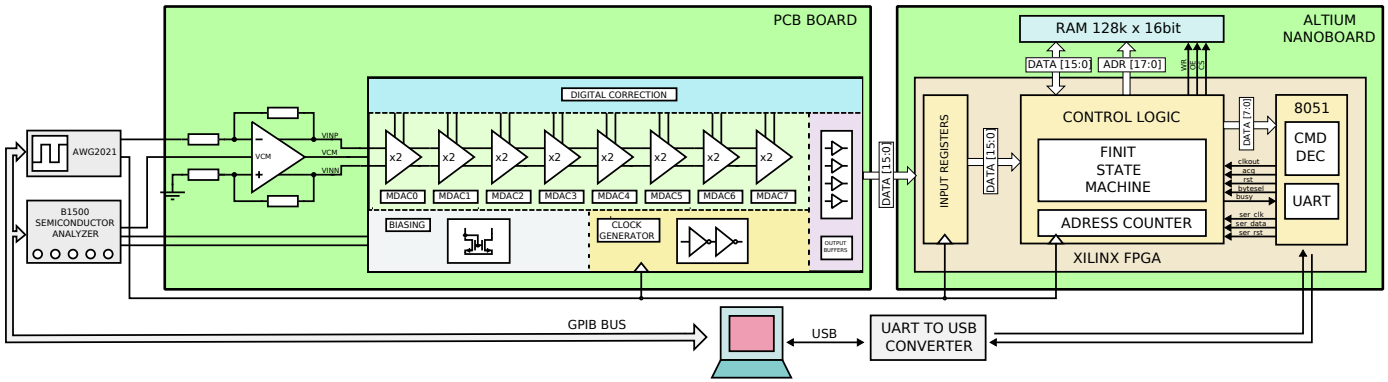


Figure: The Test Setup

Measurements

- ADC is functional
- Differential nonlinearity is $-0.5 < DNL < 0.5$
- Integral nonlinearity is $-1.0 < INL < 1.0$
- Signal to noise ratio at 58.3 dB upto 25MHz
- $ENOB > 9.3 bits$

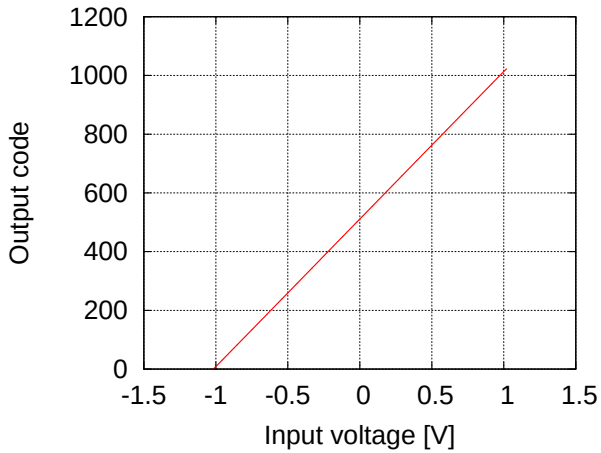


Figure: Transfer function

Command decoder, SPI, Protocol

- Serial Peripheral Interface
- LumiMulti ADC chip as a Slave

Header(6b)	Control command(2b)	Data set(8b/9b)

Table: Serial command

Command type	**Code**	**Data interpretation**
config	00	Mode(2b), Test ADC(3b), Low power(2b)
active adc	01	Select ADC(8b)
dac0	10	DAC0 value(9b)
dac1	11	DAC1 value(9b)

Table: Control commands

Slow control for Multichannel ADC using I^2C bus Interface

I^2C compatible serial interface

- I^2C Bus = Inter-Integrated Circuit Bus
- Bus developed by the Philips in the early 80s
- Two types of devices on the bus: Master & Slave
- On I^2C bus, there can be more than one master and many slaves(each with a specific address).
- Simple bi-directional 2-wire bus: Serial Data(SDA) & Serial Clock(SCL)
- A worldwide industry standard, used by major IC manufacturers.

I^2C Bus configuration

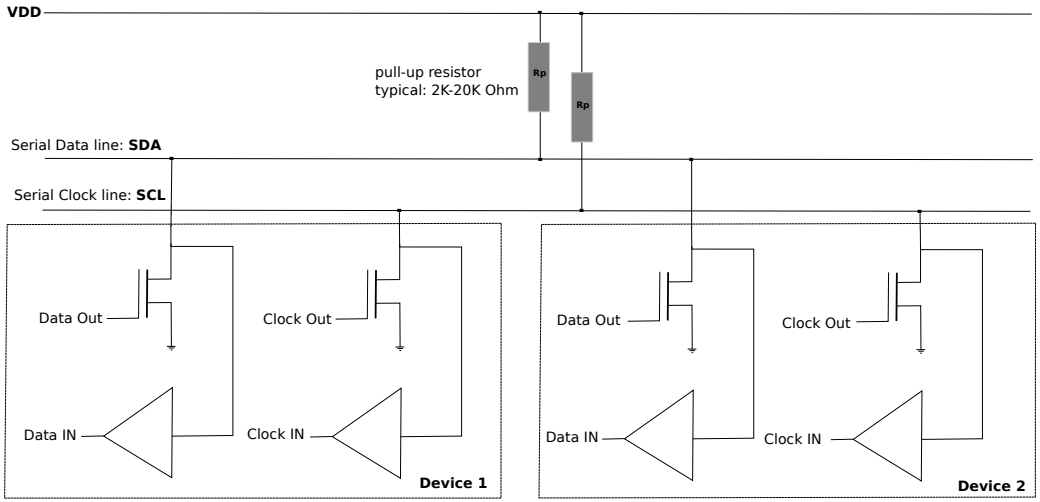


Figure: Wired-AND Configuration

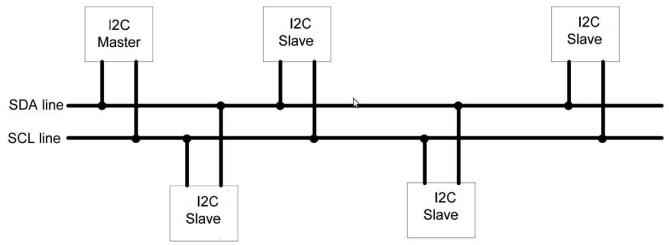


Figure: I^2C Bus Configuration

I^2C Protocol

- Transfers are byte oriented, MSB first.
- Start: A special sequence.
- Master sends address of slave (7-bits) on next 7 clocks.
- Next is data direction bit.
- Every byte is followed by an ACK.
- Stop: Also a special sequence.

I^2C Protocol

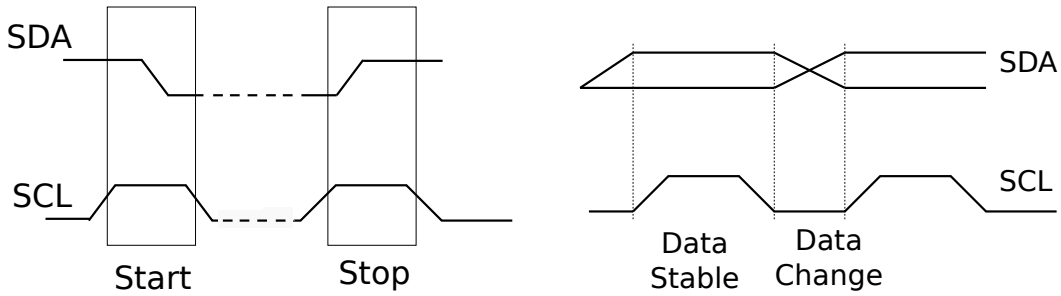


Figure: I^2C Protocol

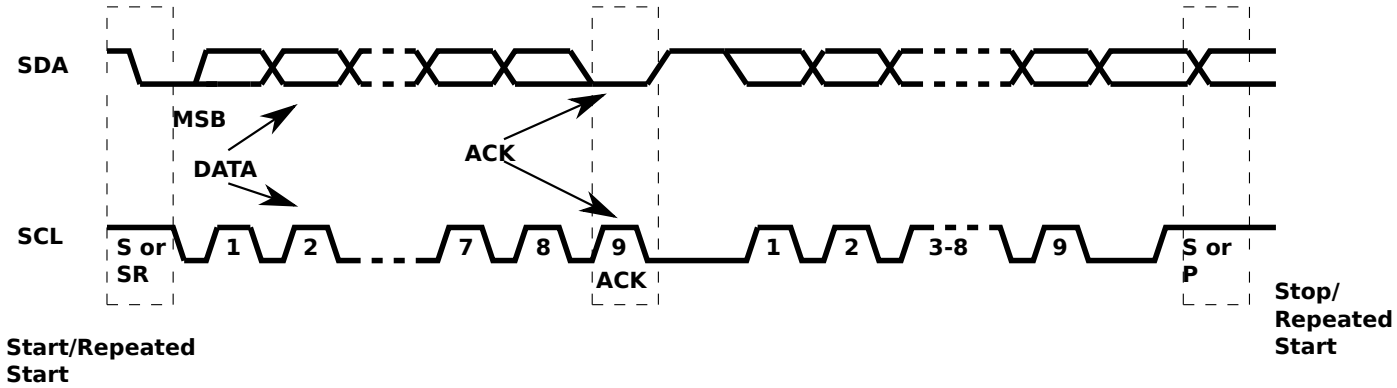


Figure: I^2C Data transfer

I^2C Master Device

- I^2C 7-bit addressing.
- Bus supports 100kbits/sec & 400kbits/sec.
- Design was coded and verified in Verilog HDL
- Automated verification using opencores I^2C Slave core.
- FPGA prototype with MCP23008(an 8-bit I/O Expander)

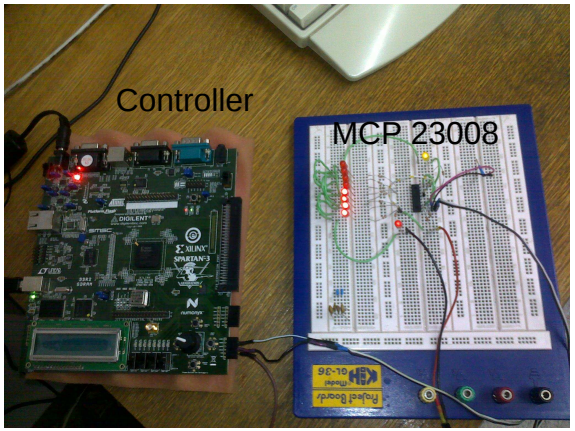


Figure: Master-Test Setup

I^2C Slave Device

- Compatible with I^2C bus specification.
- Support I^2C 7-bit addressing mode.
- Supports random read/write.
- Start/Stop/Repeated Start detection.
- Use ACK/NACK to communicate with I^2C master.
- Some additional features(Not specified in I^2C standard): Supports sequential read/write & Address auto-increment.

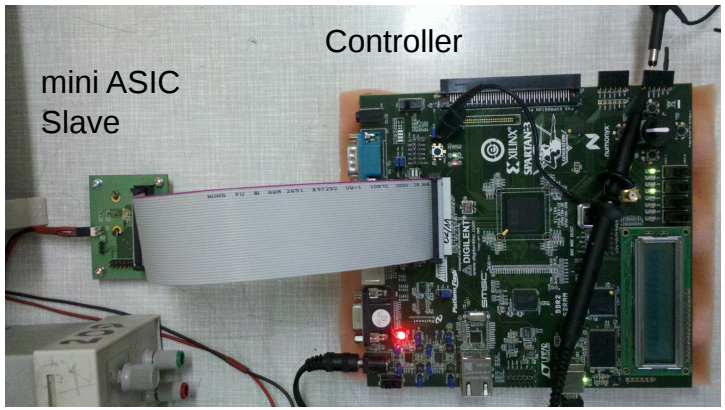
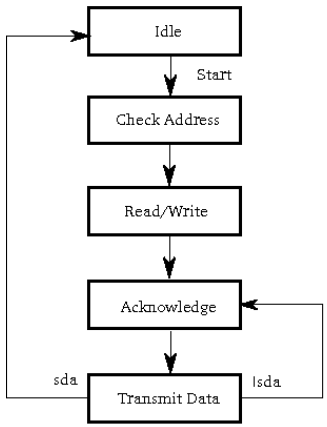


Figure: Slave-Test Setup

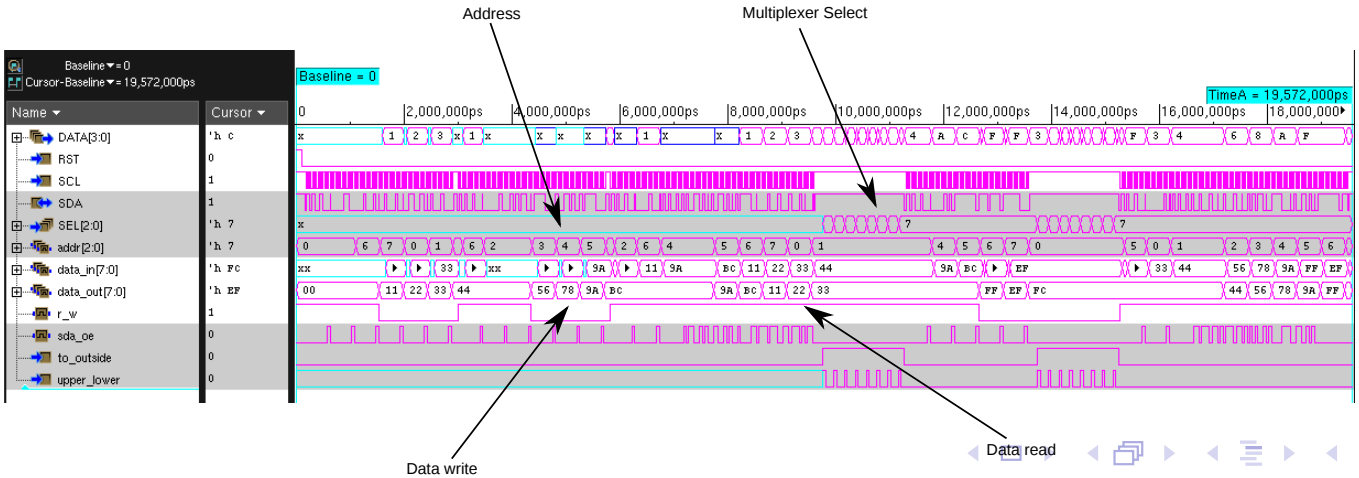
Design Flow 'Front-end'

- Behavioral design
- Simulation & Verification
- Synthesis

State flow chart



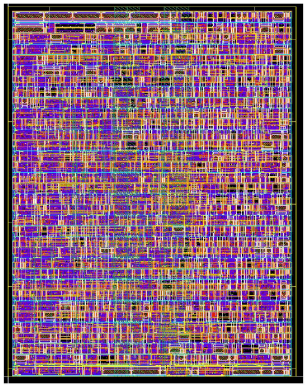
Functional Simulation



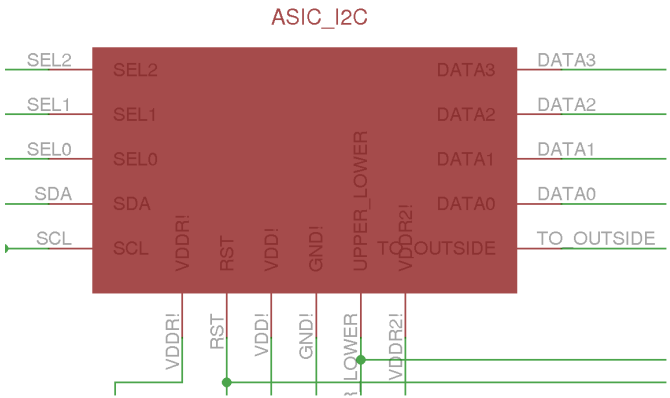
Design Flow 'Back-end'

- Placement
- Routing
- Netlist & Post-layout Simulation

Layout



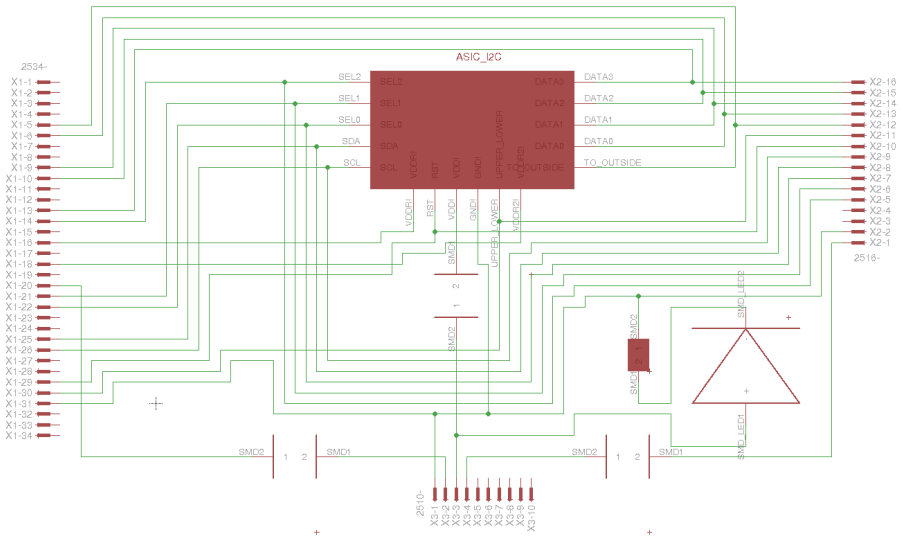
Bonding schematic



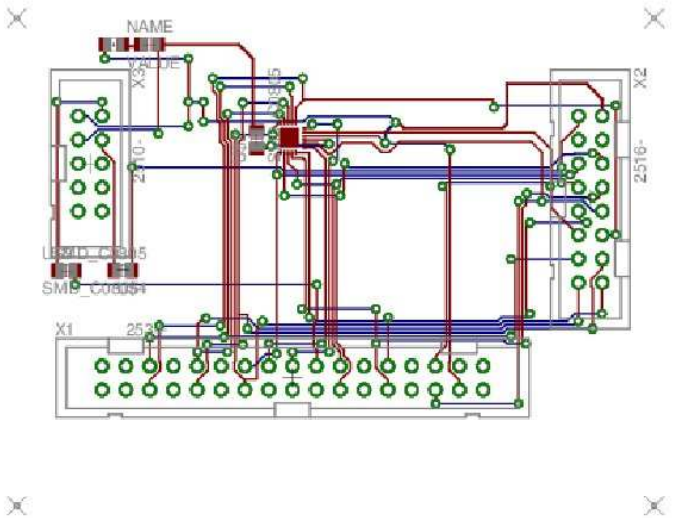
Post silicon Validation

Board design

Board Schematic



Board layout



Post silicon Validation

The Assembly:

- PicoBlaze Processor
- Wishbone bus interface
- Assembly project

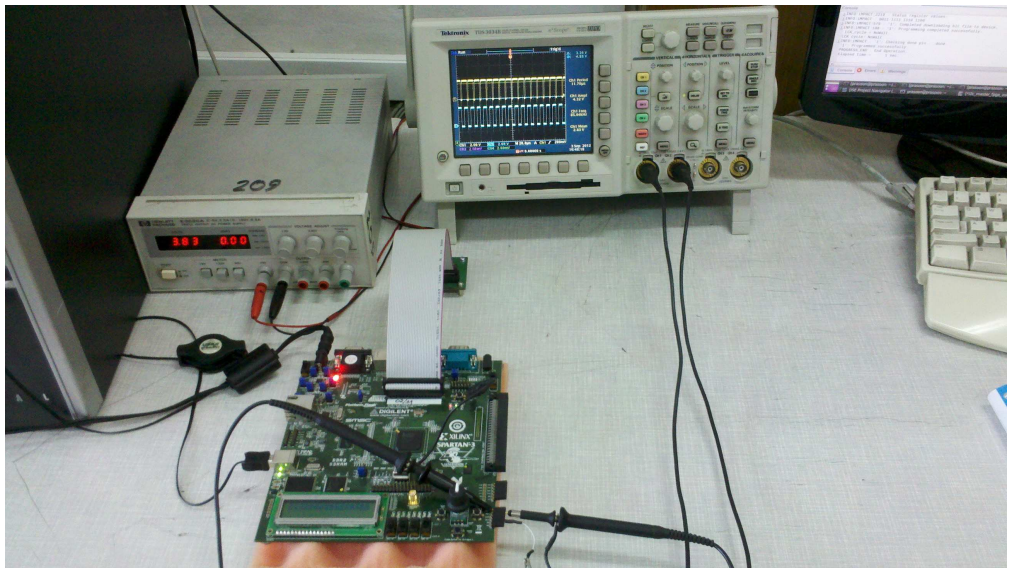


Figure: Assembly

Soft-core Processor

- Picoblaze processor as an on chip test & debug processor.
- 8-bit soft-core processor(HDL).
- ISE can be configured to provide EDA for the processor.
- Very low resources on FPGA
- 8-b ALU, 64-byte SRAM, 256 IO ports, 31 stack location.
- The processor has an architecture which makes it very useful as a controller.
- The IO operations of the processor are compulsive to be used as FSM, very suitable for low speed peripherals.
- Standard instruction set.

The processor

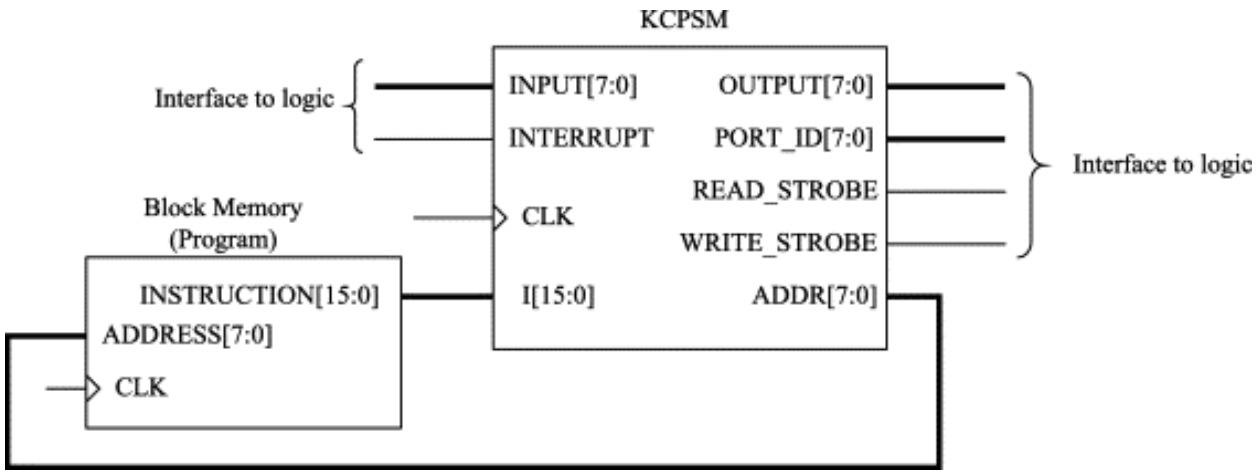


Figure: PicoBlaze Architecture

Wishbone SoC Interconnections

A design methodology for interconnecting IP cores.

- define the standard data exchange between core modules.
- building common interfaces in IP cores.
- portability and reliability
- faster turn around time.

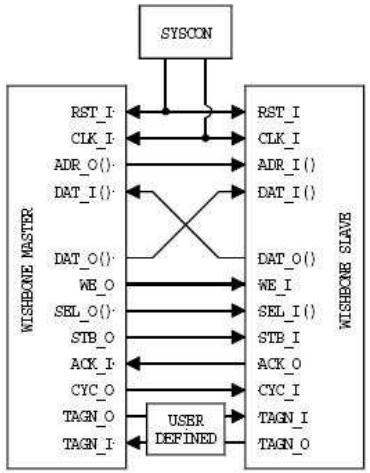
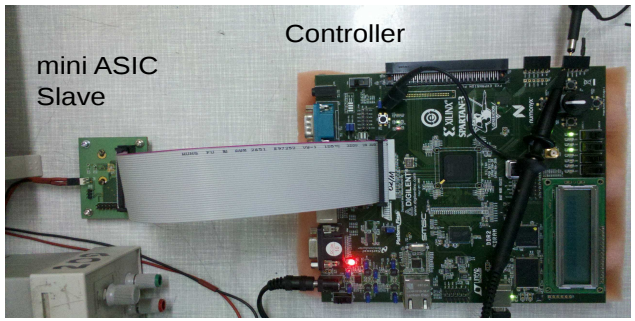


Figure: Wishbone Interconnect Architecture

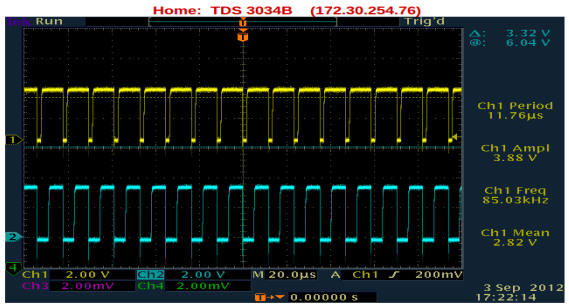
Testing

A sample run of serial data and serial clock, between controller and slave.

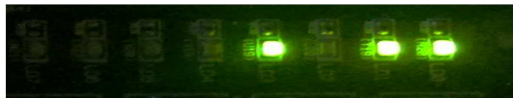
Controller & Slave

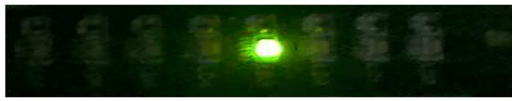


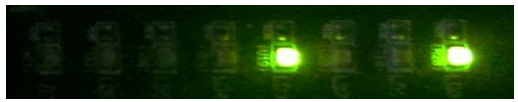
SDA & SCL



Test runs, results







P11- Front End Electronics

- ADC testing & characterization was completed.
- Multichannel ADCs with SPI based command decoder fabricated.
- Newer version of multichannel ADC will use I^2C based slow controls.

MCPAD Fellowship and future..

- Network training events.
- FCAL collaboration workshops.
- IDESA training events.
- Secondment (Industry participation)
- PhD Studies in Failure safe Processor Design
- Next, sabbatical - Component Design Engineer