July 13th, 2012
SuperB-SVT meeting

update on Strasbourg activities on CMOS pixel developments

Isabelle Ripp-Baudot
IPHC Strasbourg
CNRS/IN2P3 and Université de Strasbourg

MIMOSA-32: 0.18 µm technology exploration

- Submitted in Oct. 2011, delivered in January 2012.

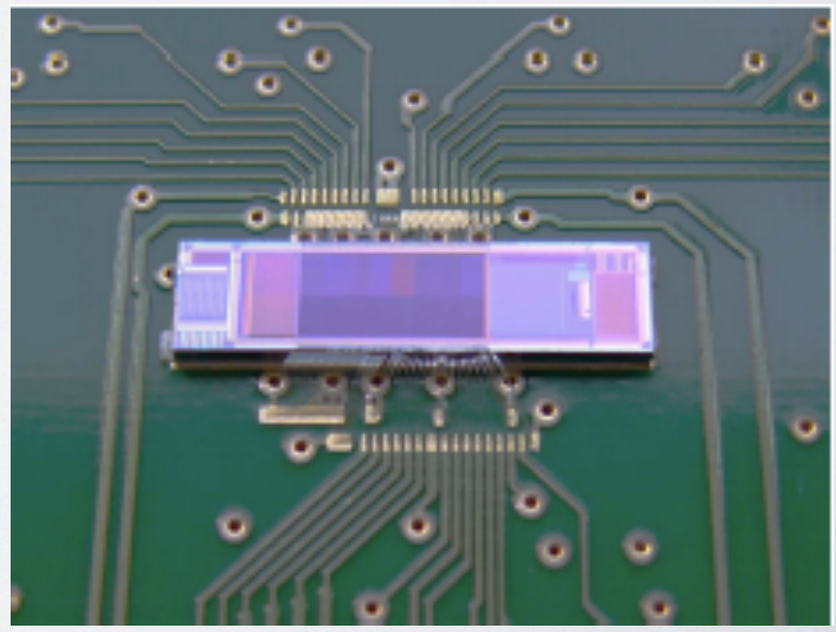
- Technology:
  - epitaxial layer: 18 µm thick, High-Resistivity 1-5 kΩ.cm.
  - quadruple well: deep P-type skin embedding N-well hosting P-MOS transistors.
  - 4 Metal Layers (6 ML at next submission in 2012).

- Prototype sub-divided in several blocks:
  - Explore pixel sizes: 20x20, 20x40 and 20x80 µm^2.
  - Explore charge amplification / collection systems: diode sizes ~9-15 µm^2, N-MOS and P-MOS transistor based amplifiers.
  - Explore discrimination: 1 sub-array of 128 columns with 1 discriminator at each column end, and one sub-array with in-pixel discrimination (16x80 µm^2 pixels).

➛ total surface ~ 43 mm^2.

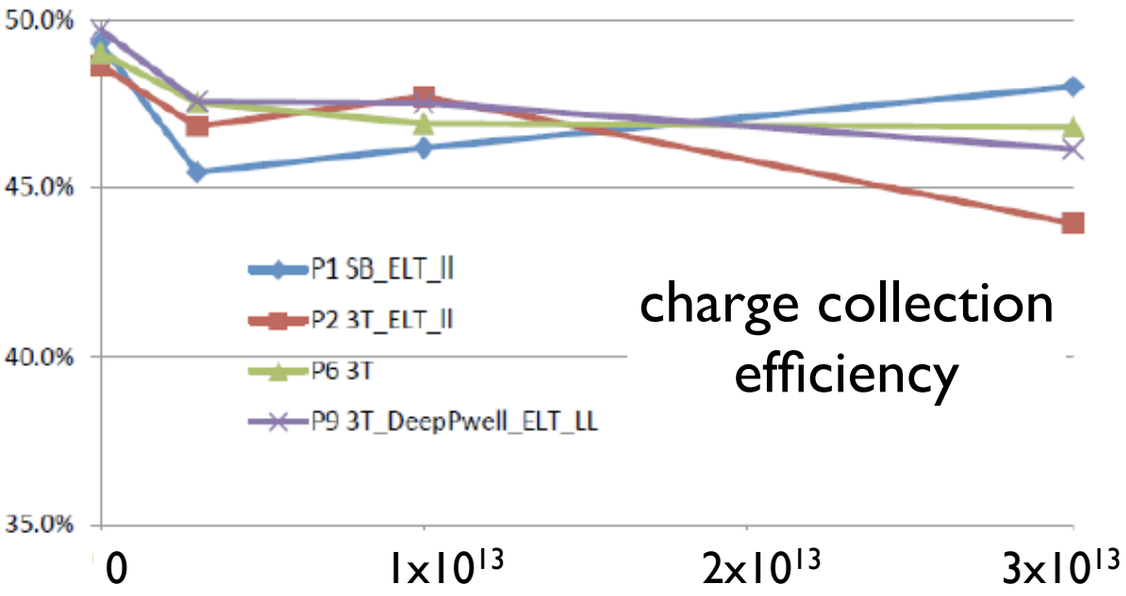
- Several lab. test results already presented during previous SVT meetings:
  - charge collection efficiency,
  - noise,
  - ionising radiation tolerance (3 MRad, 30 °C).

➛ encouraging results.

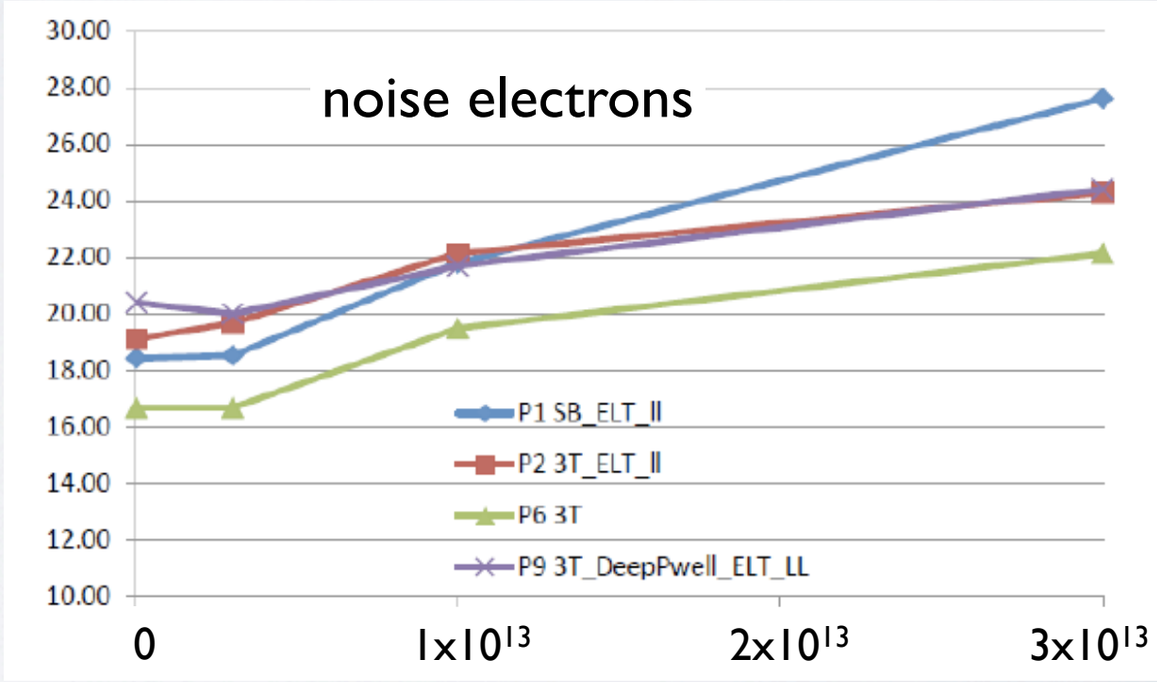


MIMOSA-32: non-ionising irradiation (1)

- Several MIMOSA-32 chips exposed to 1 MeV neutrons (20x20 μm^2):
  integrated doses of 0.3 - 1.0 - 3.0 $x10^{13}$ n_{eq} / cm^2.
- Lab. tests with ^{55}Fe source ,
  chips are cooled at +15 °C.



➢ signal seems not to be degraded by traps induced by bulk damages after non ionising radiations.

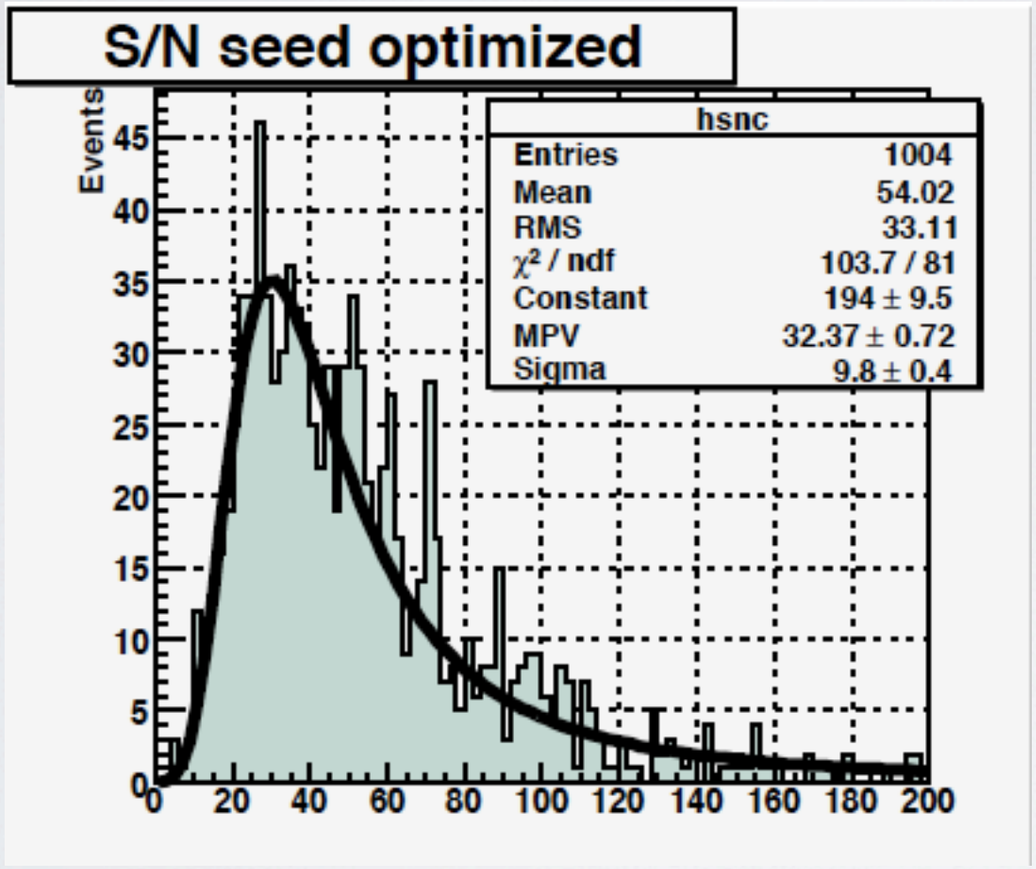


➢ evolution with fluence seems due to a typical effect of leakage current.
Noise increase modest up to fluences of $1x10^{13}$ n_{eq} / cm^2.

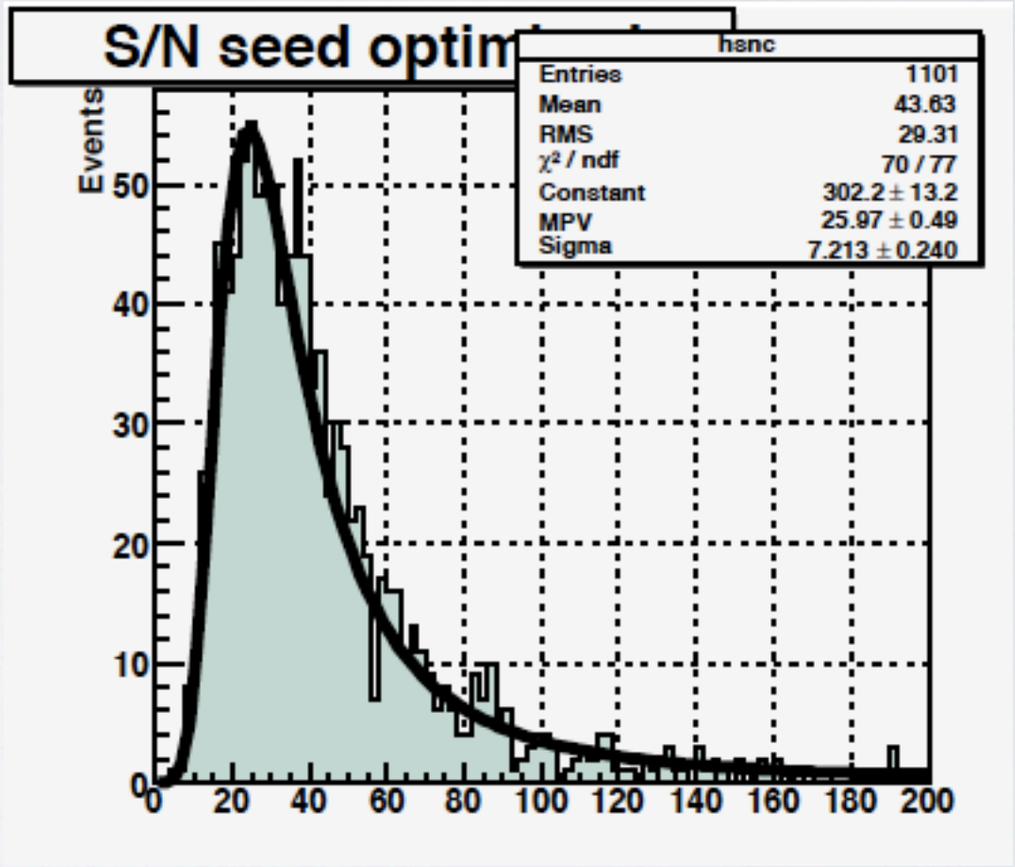
MIMOSA-32: non-ionising irradiation (2)

- Test in June 2012 with 60 GeV π^- beam (SPS-T4/H6):

  S/N ~ 32 before irradiation ➛ S/N ~ 26 after 1.0×10^{13} n_{eq} / cm^2 (at 30 °C).
  for 20x20 μm^2 pixels.



before irradiation



after 1.0×10^{13} n_{eq} /cm^2

- Other pixel sizes will be tested at CERN with beam (19-25 July 2012).