INFN/AExxx, LAL-xxx, SLAC-R-xxx

Super$B$ Detector Technical Design Report

Abstract

This report describes the technical design detector for Super$B$.

Contents

6 Silicon Vertex Tracker

6.1 Overview

The Silicon Vertex Tracker, as in *BABAR*, together with the drift chamber (DCH) and the solenoidal magnet provide track and vertex reconstruction capability for the Super$B$ detector. Precise vertex information, primarily extracted from precise position measurements near the IP by the SVT, is crucial to the measurement of time-dependent CP asymmetries in B^0 decays, which remains a key element of the Super$B$ physics program. In addition, charged particles with transverse momenta lower than 100 MeV/c will not reach the central tracking chamber, so for these particles the SVT must provide the complete tracking information.

6.1.1 SVT and Layer0

The above goals have been reached in the *BABAR* detector with a five-layer silicon strip detector with a low mass design, shown schematically in Fig. 6.1. The *BABAR* SVT provided excellent performance for the whole life of the experiment, thanks to a robust design that took into account the physics requirements as well as enough safety margin, to cope with the machine background, and redundancy considerations.

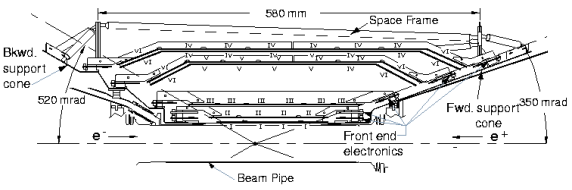

Figure 6.1: Longitudinal section of the *BABAR* SVT

The Super$B$ SVT design is based on the *BABAR* vertex detector layout with those modifications needed to operate at a luminosity of 10^{36} or more, and with a reduced center-of-mass boost. In particular the SVT will be equipped with an innermost layer closer to the IP (Layer0) to improve vertex resolution and compensate the reduced boost at the Super$B$ accelerator, thus retaining an adequte Δt resolution for B decays for time-dependent CP asymmetries.

Physics studies and background conditions, as explained in detail in the next sections, set stringent requirements on the Layer0 design: radius of about 1.5 cm; resolution of 10-15 μm in both coordinates; low material budget (about 1% X_0); and adequate radiation resistance.

Several options are under study for the Layer0 technology, with different levels of maturity, expected performance and safety margin against background conditions. These include striplets modules based on high resistivity double-sided silicon detector with short strips (tilted with respect to detector's edge), hybrid pixels and other thin pixel sensors based on CMOS Monolithic Active Pixel Sensor (MAPS).

The current baseline configuration of the SVT Layer0 is based on the striplets technology, which has been shown to provide the better physics performance, as detailed in the next sections. However, options based on pixel sensors, which are more robust in high background conditions, are still being developed with specific R&D programs in order to meet the Layer0 requirements, which include low pitch and material budget, high readout speed and radiation hardness. If successful, this will allow the replacement of the Layer0 striplets modules in a "second phase" of the experiment. For this purpose the Super$B$ interaction region and the SVT mechanics will be designed to ensure a relative

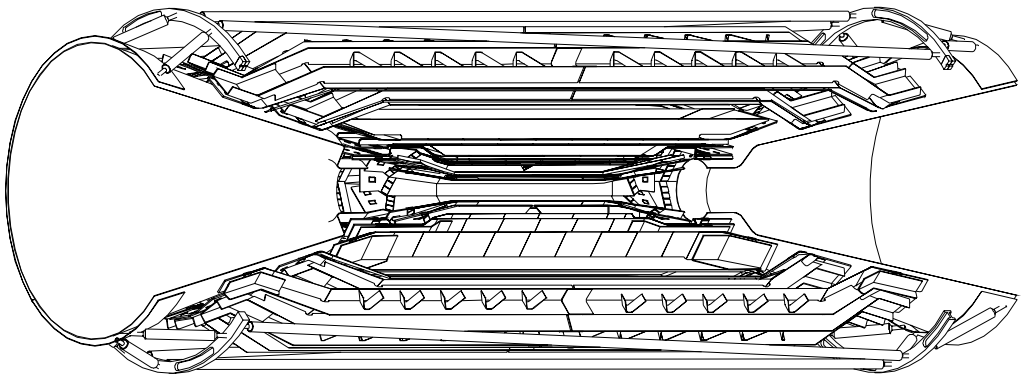

Figure 6.2: Three dimensional cutaway of the SVT.

rapid access to the detector for a replacement of Layer0.

The external SVT layers (1-5), with a radius between 3 and 15 cm, will be built with the same technology used for the *BABAR* SVT (double sided silicon strip sensor), which is adequate for the machine background conditions expected in the Super$B$ accelerator scheme (*i.e.*with low beam currents). Although SVT module design for layer1 to 5 will be very similar to the *BABAR* one, with a larger coverage, a complete new readout electronics chain need to be developed to cope with the higher background rates expected in Super$B$.

A review of the main SVT requirements will be given in the next section followed by an overview of the general detector layout. A detailed discussion of all the specific design aspects will be covered in the rest of the chapter.

6.2 SVT Requirements

6.2.1 Resolution

Without the measurement of the B decay vertex, no useful CP asymmetries can be extracted at the $\Upsilon(4S)$. Therefore one of the main goal of the SVT is the determination of the B decay positions, especially along the beam direction (z). Measurements performed in *BABAR* where the mean separation between B vertices is $\Delta z \simeq \beta\gamma c\tau_B = 250\,\mu$m, demonstrated that good sensitivity to time dependent measurement can be achieved with typical vertex resolution of 50-80 μm in the z coordinate for exclusively reconstructed modes, and 100-150 μm for inclusively modes (tag side in CPV measurements). The reduced Super$B$ boost ($\beta\gamma = 0.24$) with respect to PEP-II ($\beta\gamma = 0.55$) requires an improved vertex resolution, by about a factor 2, in order to mantain a suitable Δt resolution for time dependent analyses.

The *BABAR* resolution was achieved thanks to an intrinsic detector resolution of about 10-15 μm in the first measured point of the SVT, taken at a radius of about 3 cm, and keeping to the minimum the amount of material between the IP and the first measurement. The multiple scattering has in fact an important effect on impact parameter resolution for low momentum tracks and set a lower limit on the useful intrisic resolution on the various SVT layers, corresponding to a point resolution of about 10-15 μm for measurements made close to the IP and 30-40 μm for the outer layers [1].

The required improved track impact parameter and vertex resolution can be reached in Super$B$ with the same intrisic resolution used in *BABAR*, reducing the radius of the first measured

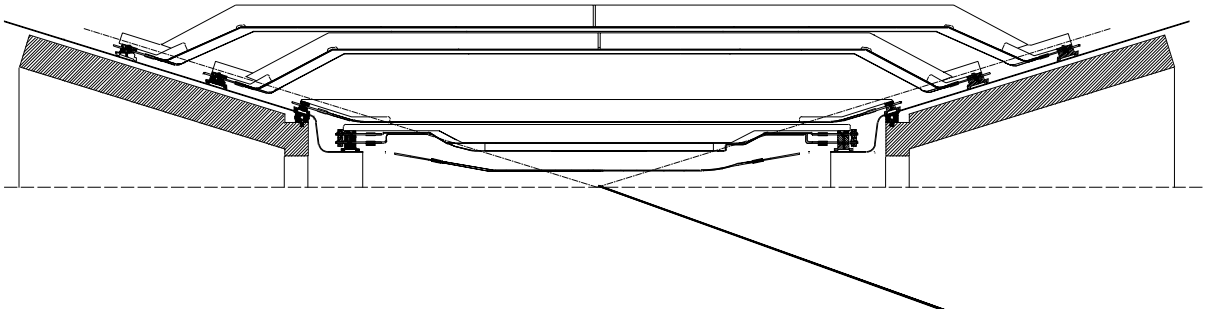

Figure 6.3: Cross section of the SVT in the plane containing the beam axis.

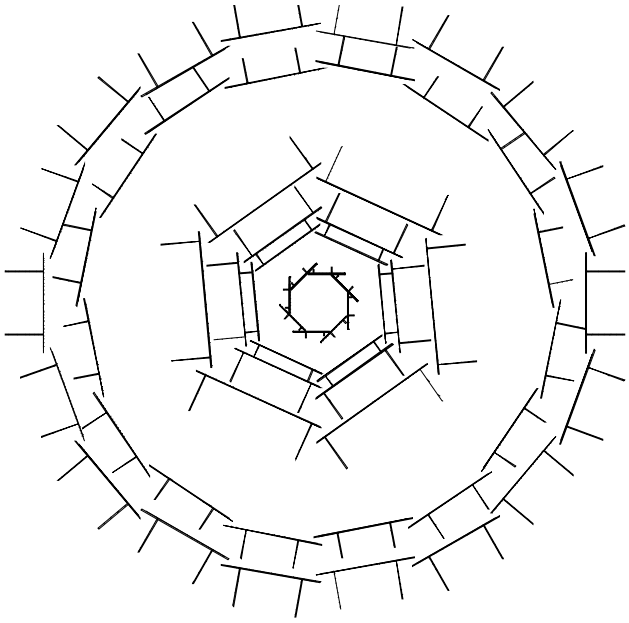

Figure 6.4: Cross section of the SVT in the plane perpendicular to the beam axis. The lines perpendicular to the detectors represent structural support beams.

SVT point by a factor of 2 (Layer0 radius at about 1.5 cm) and keeping a very low mass design for the beam pipe and the detector itself.

6.2.2 Acceptance

The coverage of the SVT must be as complete as technically feasible, given the constraints of the machine components close to the IP. The SVT angular acceptance, constrained by the Super$B$ interaction region design, will be 300 mrad in both the forward and backward directions, corresponding to a solid angle coverage of 95% in the $\Upsilon(4S)$ center-of-mass frame, thus increasing the acceptance with respect to *BABAR* SVT.

There should be as little material as possible within the active tracking volume. The minimization of the material between the IP and the first measurement is crucial to reduce the multiple scattering and preserve the impact parameter resolution. The small beam pipe (1 cm radius) in the dector acceptance requires an active cooling with liquid coolant to evacuate the large power dissipated from image beam currents. The total amount of radial material for the actual design of this new beryllium pipe is estimated to be less than 0.5% X_0. Material located beyond the inner layers does not significantly degrade the measurement of track impact parameters, but does affect the performance of the overall tracking system and leads to increased photon conversions in the active region.

6.2.3 Efficiency

Our goal is to achieve close-to-perfect track reconstruction efficiency within the active volume of the tracking detectors when information from both the drift chamber and the SVT is used. The pattern recognition capabilities of the combined tracking system must be robust enough to tolerate background levels up to 5 times nominal. *as defined in background section* Low momentum particles that do not traverse many drift chamber planes, such as many of the charged pions from D^* decays, must be reconstructed in the SVT alone. For this category of tracks, with p_T less than 100 MeV/c, we want to achieve reconstruction efficiencies of at least 80–90%. *check these number with fastsim results in high background* The SVT must also be efficient for particles such as K^0_Ss that decay within the active volume.

Together, these requirements determine the number of measurements along a track and the necessary single-hit efficiency. *do we need to quote some numbers here?*. The *BABAR* SVT design with 5 layers was optimized to ensure enough redundancy to keep an high tracking efficiency even in case of failure of some modules and inefficient detectors. The robustness of this choice was demonstrated with the good detector performance over the entire life of the experiment. The Super$B$ SVT design with 6 layers (inserting the Layer0) is inspired to the same philosophy. Specific simulation studies [2] indicated that a reduction in the number of layers, from 6 to 5 or 4, give very modest gain in tracking performance while show a sizeble reduction in the efficiency for low momentum tracks in D* reconstruction, in case of non perfect/real detector, or related to inefficiency in high background conditions.

6.2.4 Radiation Tolerance

The expected backgrounds set the requirements for the radiation resistance of all components located close to the interaction region. Whenever possible detectors and front-end electronics are specified to be able to withstand at least 5 times the total expected background integrated over the entire life of the experiment (75 ab^{-1} of accumulated data).

As described in Section:6.6, the effect of background depends steeply on radius. In Layer0 the expected integrated dose is about 3 Mrad/yr and the equivalent neutron fluence is about 5×10^{12} n_{eq}/cm^2/yr in the sensor area. In the other SVT layers radiation levels are at least one order of magnitude lower: in Layer1 TID $\simeq$ 0.4 Mrad/yr and an equivalent neutron fluence of about 7×10^{11} n_{eq}/cm^2/yr are expected.

With this scenario in the Layer1-5 the sensors are proven to be enough radiation hard to withstand the expected integrated dose and the equivalent neutron fluency over the entire life of the experiment (75 ab^{-1} of accumulated

data) even including a safety factor of five over the expected nominal background. *review this sentence after proper evaluation of S/N.* As an example this translate for Layer1 to a TID $\simeq$ 15 Mrad and an equivalent neutron fluence of about 3×10^{13} n_{eq}/cm^2 (75 ab$-$1 accumulated,

For Layer0, where the radiation is an order of magnitude higher, a quick replacement of the entire layer is foreseen, as frequent as necessary, depending on the actual background and the radiation hardness of the technology chosen.

6.2.5 Reliability

Although the SuperB interaction region and the SVT mechanics will be designed to ensure a relative rapid access to the detector for replacement of Layer0, the acces of the SVT is not possible without a major shutdown. The reliability requirements for the SVT are therefore more stringent than usual for such a device, with implications for engineering design at all levels. The detector layout must provide redundant measurements wherever possible; the electronic readout must be very robust; and the functionality of all components must not be compromised by exposure to the expected radiation levels. The detector monitoring and interlock system must serve as a safeguard against catastrophic failure in the event of a component malfunction or a simple human error.

6.3 Baseline Detector Concept

6.3.1 Technology

The SVT design is based on double-sided silicon microstrip detectors. The characteristics of this technology that make it attractive for the Super$B$ detector are: high precision for measuring the location of charged particles, tolerance to high background levels, and reduction in mass made possible through double-sided readout. Double-sided silicon detectors have been employed with success already in *BABAR* and in several other large-scale applications and are able to meet the performance standards outlined above.

6.3.2 Layout

The SVT will provide six measurements, in two orthogonal directions, of the positions of all charged particles with polar angles in the region 17° $< \theta <$167 °. A three-dimensional cutaway view of the SVT is shown in Figure 6.2. The Layer0 has eight detector modules while the rest of the detector keep the same modules numbers as in *BABAR* : layers 1-2-3 have six detector modules, arrayed azimuthally around the beam pipe, while the outer two layers consist of 16 and 18 detector modules, respectively. A side view of the detector is shown in Figure 6.3, and an end view is shown in Figure 6.4.

describe in some detail the Layer0 modules

The inner detector modules are traditional barrel-style structures, while the outer detector modules employ an arch structure, in which the detectors are electrically connected across an angle. The bends in the arch modules proven to be well functional in *BABAR* minimize the area of silicon required to cover the solid angle and also avoid very large track incident angles.

In order to satisfy the requirement of minimizing material in the detector acceptance region, one of the main features of the SVT design is the mounting of the readout electronics entirely outside the active detector volume. There is a 1 cm space between the 300 mrad stay-clear in the forward and backward directions and the first element of the IR region (i.e. the tungsten shield cones) and all of the electronics are mounted here. In both directions, space is very tight, and the electronic and mechanical designs are closely coupled in the narrow region available.

The layout specifications for this six-layer design are given in Table **??**. For layers 1 to 5 the strips on the two sides of the rectangular detectors in the barrel regions are oriented parallel (ϕ strips) or perpendicular (z strips) to the beam line. In the forward and backward regions of the two outer layers, the angle between the strips on the two sides of the trapezoidal detectors is approximately 90°, and the ϕ strips are tapered. Floating strips are used to improve the position resolution for near-perpendicular angles of

incidence; the capacitive coupling between the floating strip and the neighboring strips results in increased charge sharing and better interpolation. For larger incident angles with wider readout pitch minimizes the degradation in resolution that occurs because of the limited track path length associated with each strip. These issues are discussed in more detail in Section **??**.

The design has a total of xxx silicon detectors of seven different types. The total silicon area in the SVT is 0.94 m ^{2}, and the number of readout channels is ∼150,000.

6.3.3 Electronics

6.3.4 Mechanical Support

6.4 Layer0 Pixel Upgrade

6.4.1 Technology Options

6.4.2 Pixel Module Design

6.4.3 Mechanical Support and Cooling

6.5 R&D Main Activities

6.6 Backgrounds R.Cenci - 4 pages

Background considerations influence several aspects of the SVT design: readout segmentation; electronics shaping time; data transmission rate; and radiation hardness (particularly severe for Layer0).

The different sources of background have been simulated with a detailed Geant4-based detector model and beamline description to estimate their impact on the experiment.

Add a description of the detector model in Bruno ed insert reference to the main Background sections

Describe main feature of each source

6.6.1 Pair production

6.6.2 Radiative Bhabha

6.6.3 Touschek

6.6.4 Beam Gas

6.6.5 Other sources

Include summary tables with rates, doses, equivalent fluences for various layers

6.7 Detector Performance Studies N.Neri - 6 pages

6.7.1 Introduction

The Super$B$ vertex detector can be considered as the evolution of the *BABAR* one. It is capable of maintaining adequate performances for time-dependent measurements in presence of a lower boost of the center-of-mass frame (CM) ($\beta\gamma = 0.24$ compared to $\beta\gamma = 0.55$ of *BABAR*) and much higher background, mainly related to the increased istantaneous luminosity of about a factor 100 higher with respect to *BABAR*.

The beampipe has a small radius of about 1.0 cm which allows the positioning of the innermost layer of the SVT (Layer0) at an average radius of about 1.6 cm. The addional Layer0 measurement along with the low radial material budget of the beampipe (0.42% X_0) and Layer0 (0.45% X_0), is crucial for improving the decay vertex reconstruction of the B mesons and obtaining adequate proper time resolution for time-dependent CP violation measurements. The small size of the luminous region, about $(1 \times 1)\,\mu\text{m}^2$ in the transverse plane, also contributes to the improvement of the decay vertex reconstruction when imposing the constraint that the particles are originated from the interaction point.

6.7.2 The SVT layout

The Super$B$ SVT is composed by 6 layers of double-sided silicon strip detectors and has a symmetric coverage in the laboratory frame down to 300 mrad (17.2°) with respect to the forward and backward direction, corresponding to 95% angular coverage in the CM. The Layer0 strips are short ('striplets') and oriented

Table 6.1: *need to update the table* Parameters of the SVT layout.
See text for more detail on the meanings of the different quantities. The intrinsic resolution is calculated at 90° track incidence assuming $S/N = 20 : 1$. The z-ganging numbers represent the percentage of detector strips connected to one other strip (×2) or two other strips (×3).

Quantity	Layer 1	Layer 2	Layer 3	Layer 4a	Layer 4b	Layer 5a	Layer 5b
Radius (mm)	32	40	54	120	127	140	144
Wafers/Module	4	4	6	7	7	8	8
Modules/Layer	6	6	6	8	8	9	9
Silicon Area (cm^2)	457	683	1072	1506	1582	2039	2082
Overlap in ϕ (%)	2.4	1.8	1.8	4.0	4.0	2.0	2.0
Readout pitch (μm):							
ϕ	50	50	50	65–100		65–100	
z	100	100	100	200		200	
Floating Strips:							
ϕ	—	—	—	1		1	
z	1	1	1	1		1	
Intrinsic Resolution(μm):							
ϕ	10	10	10	10–12		10–12	
z	12	12	12	25		25	
R.O. Section/Module	4	4	4	4		4	
ICs/R.O. Section	6	8	10	4		4	
Readout Channels	18432	24576	30720	32768		36864	
Strip Length (mm):							
ϕ	95	115	136	177/223	186/232	232/241	241
z	39	48	64	35–52	35–52	35–52	35–52
z Ganging:							
Forward ×2	34%	18%	7%	82%	88%	71%	60%
Forward ×3						29%	40%
Backward ×2	34%	18%	7%	82%	71%	60%	60%
Backward ×3				18%	29%	40%	40%

Table 6.2: Reconstrucion efficiencies for $B^0 \to D^{*-}K^+$ for different SVT layout (4, 5 ,6 layers) and running conditions (A, B, C). A represents the case of ideal running conditions, B represents SVT with a damaged module in Layer3 with 70% z hit efficiency. Case C introduces additional inefficiency with respect to case B in Layer0: 60% hit efficiency for z and ϕ views.

	A	B	C
6 layers	66%	65%	64%
5 layers	64%	62%	60%
4 layers	60%	56%	53%

at $\pm 45°$ from the beam direction. The Layer1 to Layer5 silicon strip detectors are very similar to the BaBar ones in terms of radial position and strip pitches. The optimization of the strip z and ϕ pitches for the strip detectors is discussed in Section 6.8.2. A dedicated study for optimizing the SVT layout in terms of number of silicon sensors, radial positions was performed [2]. Several figure of merit were studied: the track parameters resolution, the reconstruction efficiency and kinematic variables resolution of B decays with low momentum tracks as $B^0 \to D^{*-}K^+$. Since low momentum tracks will not penetrate in the DCH, they are reconstructed using only SVT information. The *BABAR* experience has shown that at least 4 hits in the ϕ view and 3 hits in the z view are necessary for robust track reconstruction. The main result is that the 6 layer design is superior and more robust compared to the alternatives investigated, *i.e.* 4 layer and 5 layer layout. For example, when accounting for possible inefficiencies in hit reconstruction, due to damaged modules or high background, the 6 layer design allows higher reconstruction efficiencies for low momentum tracks compared to the other solutions.

In Table 6.2 are reported the reconstruction efficiencies for the decay $B^0 \to D^{*-}K^+$ for the 4, 5 and 6 layer configuration with in different running conditions: ideal conditions (A), with a damaged module in Layer3 (B) and with additional hit inefficiency in Layer0 with respect to case B (C). The outer radius of the SVT was ultimately constrained by the DCH inner radius to about 20 cm. It was demonstrated that there is no real advantage in increasing the outer layer of the SVT with respect to the BaBar design (14.4 cm) [3, 4, 5]. In addition, construction cost and technical difficulties would increase. The radial position of the Layer1 to Layer4 layers has very little impact on the track resolutions when comparing a layout with detectors equally separated and the BaBar-like layout.

6.7.3 Impact of Layer0 on detector performances

The additional Layer0 measurement is crucial for maintaining adequate resolution on the B^0 meson proper time difference $\Delta t \simeq \Delta z/(\beta\gamma c)$ in presence of a relatively low CM boost value $\beta\gamma = 0.24$. The average separation Δz of the the decay vertex positions of the two B along the z axis is about 110 μm, hence we need to determine the decay position of the B mesons with a significantly better precision in order to be able to separate them. In the case of Super$B$, the B vertex separation of about 25 μm in the transverse plane, with respect to the beam direction, is not completely negligible with the average Δz separation of about 110 μm and also contributes to the determination of Δt. The reference value for the Δt resolution, $\sigma(\Delta t)$, was determined by the resolution obtained in the *BABAR* experiment. According to simulation studies the sensitivity to the physics parameters is reduced of about 25% (*need to double check this number*) with respect to the case of perfect resolution. In Fig. 6.5 it is shown the dependence of the per-event error on the physics parameter S as a function of $\sigma(\Delta t)$ and compared with the sensitivity obtained in *BABAR*. In this simplified model $\sigma(\Delta t)$ corresponds to the width of the core Guassian of the Δt resolution function. The S per-event error is defined as the error on the parameter S normalized to the

number of signal events. S is measured in time-dependent analyses and corresponds to $\sin(2\beta)$ for $B^0 \to J/\Psi K^0_S$ decays. The resolution on the

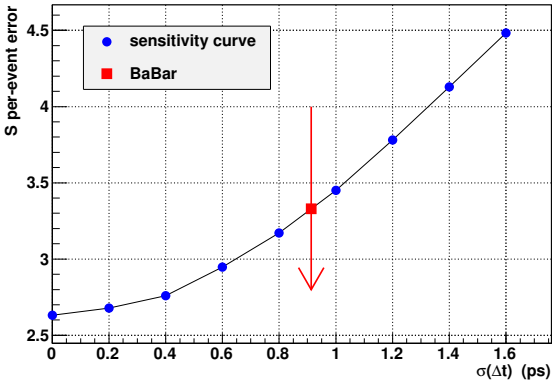

Figure 6.5: The curve represents the dependence of the error on the physics parameter S (*e.g.* $\sin(2\beta)$) versus $\sigma(\Delta t)$. The arrow indicates the $\sigma(\Delta t)$ value obtained in *BABAR* according to the Fast Simulation and the square point is the relative value on the sensitivity curve.

z coordinate of the B decay vertex depends on the geometry of the vertex detector and the hit resolution. In a simplified model with two hit measurements at radii r_1 and r_2 ($r_2 > r_1$) with z hit resolution σ_1 and σ_2 respectively, it can be approximated as:

$$\sigma_z = \frac{(\sigma_1 r_2)^2 + (\sigma_2 r_1)^2}{r_2^2 - r_1^2} = \frac{\sigma_1^2 + (\sigma_2 r_1/r_2)^2}{1 - (r_1/r_2)^2}. \tag{6.1}$$

In addition the tracks are deflected due to multiple scattering interactions with the material in the tracking volume. The scattering angle is approximately [9]:

$$\theta_{\text{m.s.}} = \frac{13.6\,\text{MeV}/c}{p_t}\sqrt{\frac{x}{X_0}}\left[1 + 0.0038\ln\left(\frac{x}{X_0}\right)\right] \tag{6.2}$$

where p_t is the momentum in the transverse plane of the colliding beams, x is the thickness of the material and X_0 is the interaction length. In order to minimize the uncertainty on σ_z it is important to measure the first hit at r_1 as small as possible with a good hit resolution σ_1. Minimize the material close to the interaction, *e.g.* the beampipe and Layer0 material budget is also important.

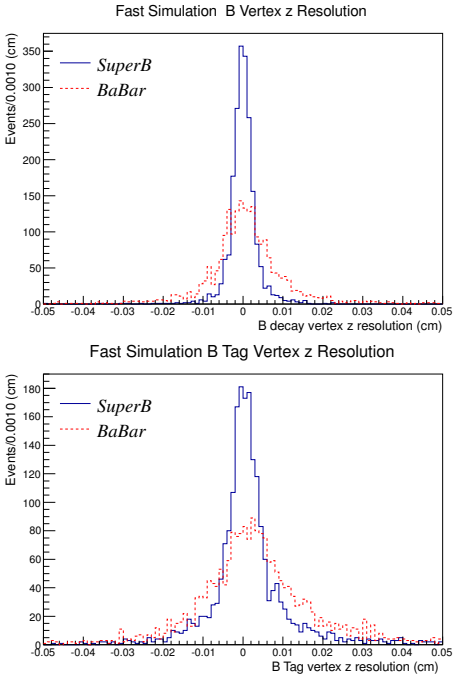

Figure 6.6: B decay vertex z position (top) and B tag z position (bottom) residual distributions for the case of Super$B$ with Layer0 striplets (open histogram) compared with *BABAR* (dashed histogram) according to Fast Simulation results.

In Fig. 6.6 are shown the residual distributions for B decay vertex z position for exclusively (top) and inclusively reconstructed (bottom) B decays. In Fig. 6.7 are shown the Δz (top) and Δt (bottom) residual distributions. One B is exclusively reconstructed in the $B^0 \to \phi K^0_S$ mode (B_{reco}), while the other B is inclusively reconstructed using the remaining tracks of the event and is used also for flavor tagging (B_{tag}). The Fast Simulation results for Super$B$ with Layer0 striplets are compared with the *BABAR* ones and are summarized in Table 6.3. For the case of Super$B$ we as-

Table 6.3: RMS of the residual distributions for decay vertex z position for exclusively reconstructed $B^0 \to \phi K^0_S$ decays ($B_{\rm reco}$), inclusively reconstructed B decays ($B_{\rm tag}$), Δz and Δt at Super$B$ and compared with *BABAR* results, according to Fast Simulation studies.

	Super$B$	*BABAR*
$B_{\rm reco}$ (μm)	40	105
$B_{\rm tag}$ (μm)	100	145
Δz (μm)	105	165
Δt (ps)	1.4	1.4

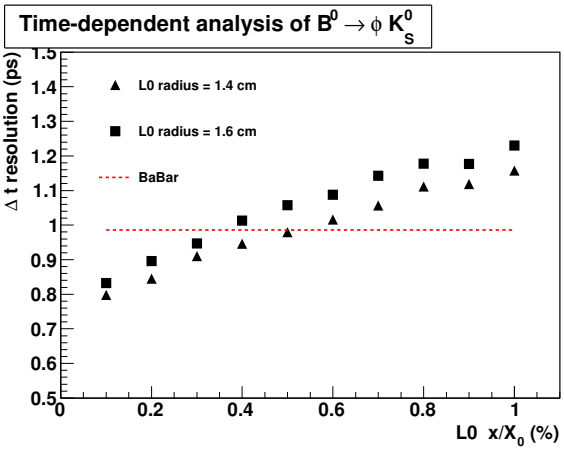

Figure 6.8: Resolution on Δt for different Layer0 configurations in terms of radius $r_1 = 1.4, 1.6\,$cm and material budget $x/X_0 = (0.1 - 1.0)\%$ compared with the reference value of *BABAR* (dashed line).

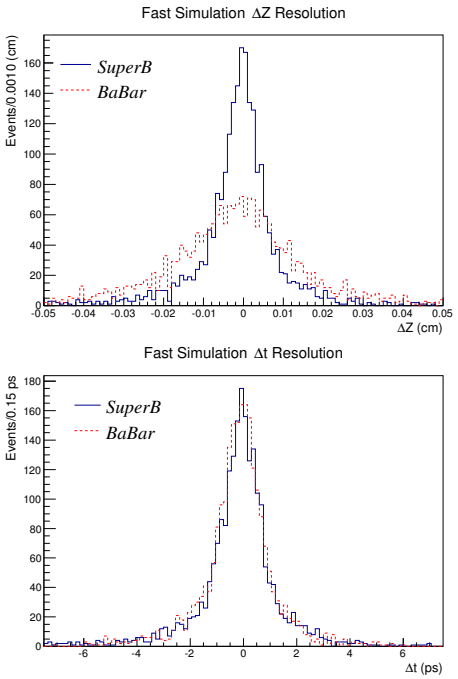

Figure 6.7: Δz (top) and Δt (bottom) residual distributions for the case of Super$B$ with Layer0 striplets (open histogram) compared with *BABAR* (dashed histogram) according to Fast Simulation results.

sume $\sigma_1 = 8\,\mu$m for both the u and the v hits, $r_1 = 1.60\,$cm and $x/X_0 \simeq 0.9\%$ including the beampipe and Layer0 striplets material budget. For striplets detectors the u and v coordinates are oriented at $\pm 45°$ with respect to the z axis and are perpendicular to each other. In the case of *BABAR* we have $\sigma_1 = 14\,\mu$m for the z hits and $10\,\mu$m resolution for the ϕ hits, $r_1 = 3.32\,$cm and $x/X_0 \simeq 1.6\%$. In the Super$B$ case the improvement in the Δz resolution is compensated by the reduced boost value, yielding a very similar Δt resolution to *BABAR*. In Fig. 6.8 it is shown the Δt resolution obtainable with different Layer0 radii, $r_1 = 1.4, 1.6\,$cm and material budget, $x/X_0 = (0.1 - 1.0)\%$. The dashed line represents the reference value of *BABAR*.

The impact of the hit resolution on the decay vertex reconstruction has also been studied. With $8\,\mu$m hit resolution in both views in Layer0, the error on the vertex position due multiple scattering interactions with the material dominates the overall vertex uncertainty also for high momentum tracks from $B^0 \to \pi^+\pi^-$ decays. Hence, there is no real advantage in further improving the hit resolution with respect to this value. The hit resolution from Layer1 to Layer5 has been chosen according to

low momentum track reconstruction. The hit resolution and relative hit efficiency used in the Fast Simulation are reported in Table 6.4 for the different SVT layers.

Table 6.4: Hit resolutions and hit efficiencies for the z and ϕ sides (Layer0 u and v sides) for the different layers.

	res. u (μm)	res. v (μm)	eff. u (%)	eff. v (%)
Layer0	8	8	99	99
	res. z (μm)	res. ϕ (μm)	eff. z (%)	eff. ϕ (%)
Layer1	14	10	98	98
Layer2	14	10	98	98
Layer3	14	15	98	96
Layer4	25	15	99	98
Layer5	25	15	99	98

6.7.4 Sensitivity studies for time-dependent analyses

The sensitivity to the physics parameter S has been considered as figure of merit for time-dependent analyses of neutral B decays. Several decay modes have been studied: $B^0 \to \phi K^0_S$, $B^0 \to \pi^+\pi^-$, $B^0 \to J/\Psi K^0_S$, $B^0 \to D^+D^-$ and also decay modes such as $B^0 \to K^0_S K^0_S$, $B^0 \to K^0_S\pi^0$ where the impact of the additional Layer0 measurement is less effective due to the presence of neutral and long-lived particles in the final state. The per-event error on the S parameter is consistent with the result obtained for the *BABAR* detector for all the decay modes but for $B^0 \to K^0_S K^0_S$, $B^0 \to K^0_S\pi^0$ decays where a reduction in sensitivity of about 15% is expected according to Fast Simulation studies [3, 5]. In the Fast Simulation studies only the effect of the Δt resolution on the measurements has been included. Possible improvements in the reconstruction efficiency, 95% angular coverage in the CM per track with respect to 91% in *BABAR*, and in flavor tagging performances due to improvements in particle identifications, have not been considered in these studies.

In the case of time-dependent analyses for mixing and *CP* violation in the neutral D meson system, the determination of the proper time (t) relies on the measurement of the flight length ($\vec{L}$) and the momentum of the D^0 ($\vec{p}$) according to $t = \frac{\vec{L}\cdot\hat{p}\ M}{|\vec{p}|}$ where M is the D^0 nominal mass. The D^0 mesons are selected from $e^+e^- \to c\bar{c}$ events and they gain a natural boost in the reaction. In this case the reduction of the CM boost does not affect the resolution on the proper time and the resolution obtained in Super$B$ is improved by about a factor 2 with respect to *BABAR* [6]. In Fig. 6.9 is reported the distribution of the proper time error in Super$B$ and compared with the case of *BABAR*. The average proper time error is about 0.16 ps in Super$B$ and 0.30 ps in *BABAR* for $D^0 \to K^0_S\pi^+\pi^-$ decays, to be compared with the D^0 lifetime of 0.410 ps.

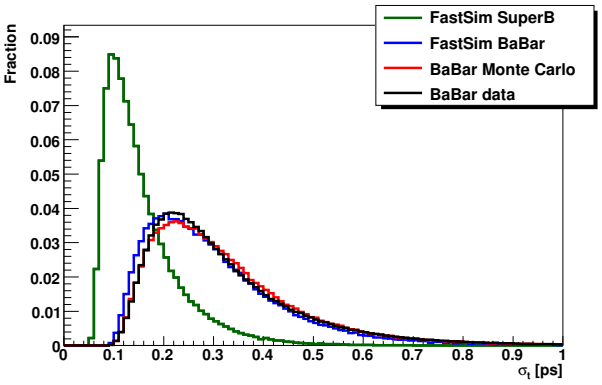

Figure 6.9: Distribution of the D^0 proper time error for Super$B$ (green line) and compared with the case of *BABAR* (blue line) according to Fast Simulation results. *BABAR* Monte Carlo (red line) and data (black line) are also reported in the plot. The average proper time error for $D^0 \to K^0_S\pi^+\pi^-$ decays is 0.16 ps at Super$B$ compared with 0.30 ps at *BABAR*.

The impact of machine background events on the performance of the vertex detector have been studied by adding background hits to signal events according to the rates estimated us-

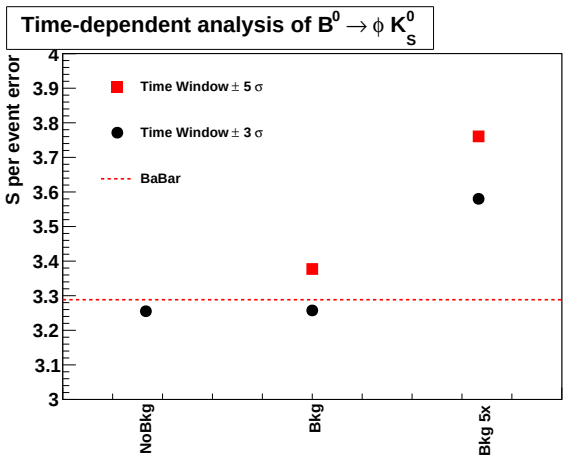

Figure 6.10: Variation of the S per event error in $B^0 \to \phi K^0_S$ time-dependent analysis in presence of background events and with 5 times the nominal background. A cut on the time of arrival of the hits has been applied at $\pm 3\sigma$ and $\pm 5\sigma$ with respect to the time of the event.

ing Full Simulation. Details on the estimates of the machine background events can be found in Section 6.6. Possible effects of background hits are the reduction of the hit reconstruction efficiency, the increase of the effective hit resolution, the reduction of efficiency of the pattern recognition for charged tracks along with the increase of fake tracks. Most of the above effects have been included in our Fast Simulation assuming that the charged track pattern recognition algorithm will work with similar performances to the *BABAR* one but fake tracks are not simulated. The hit efficiency of the readout chips that we have used in the Fast Simulation studies can be found in Table 6.10 for the case of nominal background and with 5 times the nominal background. In Fig. 6.10 it is reported the impact of the machine background events on the physics parameter S for the case of nominal background and with 5 times the nominal background rates. Background hits are rejected if they are not within a time window of $\pm 3\sigma$ ($\pm 5\sigma$) with respect to the time of the event. The resolution on the time of arrival of the hit, σ, varies for the different SVT layers depending mainly on the shaper peaking time of the front-end electronics and has been estimated using 'ad hoc' simulations. The reduction to the sensitivity to S is very small with nominal background ($< 3\%$) and is about 9% (14%) with 5 times the nominal background conditions when applying a $\pm 3\sigma$ ($\pm 5\sigma$) time window cut.

6.7.5 Vertexing and Tracking performances *(about 1 page)*

The tracking and vertexing performances at Super$B$ have been studied considering alternative solutions for the SVT and DCH layout [2, 3, 4]. In particular we have studied alternative SVT configurations: with different values of the SVT outer radius (from about 14 cm to about 22 cm), without Layer2 detector, different radial position of the layers (*e.g.* uniform distance between layers), different hit resolutions accounting for variations of about 50% with respect the nominal one reported in Table 6.4. The main result was that the *BABAR*-like layout for Layer1-Layer5 was very close to be the optimal choice in terms of resolutions for track parameters. Small improvements in track parameter resolutions would have been possible by removing Layer2. On the other hand, the six layer layout has been proved to be more robust against possible problems that might cause loss of efficiency in some layers of the detector [2] and was preferred for this reason. Optimization of the strip pitches for the z and ϕ sides of the different layers are discussed in Section 6.8.2. In Fig. 6.11 is shown the resolution of the impact parameter (d_0) as a function of the transverse momentum of the track for the case of *BABAR* and Super$B$ detectors. Results for alternative configurations of the SVT layout: with extended outer radius, with DCH lower radius with and without Layer2 are also shown. A significant improvements in the d_0 resolution of about a factor 2 is achieved with the Super$B$ detector with respect to the *BABAR*one. The alternative SVT layout options investigated give consistent results with the nominal Super$B$ solution.

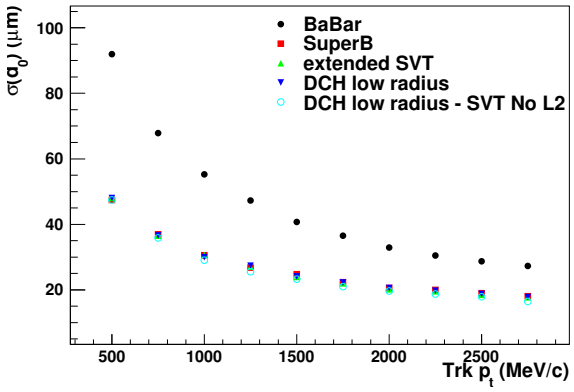

Figure 6.11: Resolution on the impact parameter of the track d_0 for the *BABAR* and the Super*B* detector. Alternative vertex detector configurations considered in this study (with extended SVT outer radius, with DCH lower radius with and without Layer2) give almost identical results to the one of the nominal Super*B* SVT configuration.

- considerations for pattern recognition, efficiency vs numbers of layers, reconstruction capabilities for low momentum tracks, K^0_S reconstruction.
- pattern recognition and tracking performances with background;

6.7.6 Particle Identification *(about 1/2 pages)*

- dE/dx resolution and relevance for QED pairs suppression.
- discussion of relevance of ToT information and number of bits of the FEE.

6.7.7 Performance with Layer0 pixel detectors

A Layer0 solution based on a high granularity silicon pixel sensor, *e.g.* 50×50 μm^2 cell, is considered for a possible upgrade of the baseline striplets solution. The different Layer0 technology options are described in Sec. **??** and are based on hybrid pixels, deep N-well CMOS monolithic sensors and monolothic pixels with CMOS quadruple well. All the different solutions adopt a digital sparsified readout with the area of the pixel cell of about $2500-3000\,\mu$m^2. The shape of the pixel can be optimized in such a way to reduce the sensor pitch in the z direction and improving the relative hit resolution while keeping the pixel area constant.

As we have discussed in Sec. 6.7.3, the determination of the decay vertex position is driven by the performance of the Layer0. The advantage of the Layer0 pixel solution is that it guarantees good detector performances also in presence of relatively high background. The detector occupancy, defined as the probability of having a noise hit in the sensitive time window, is about two order of magnitudes lower with respect to the striplets case, taking into account for the different detector granularity and resolution on the time of arrival of the hits. Occupancies at the level of 10^{-4} in a Layer0 pixel detector would correspond to occupancies of 10^{-2} with the striplets solution, which are about the highest achievable values in the Layer0 striplets at Super*B*. Therefore, the effect of the the background hits on the determination of the decay vertex and track impact parameters can be safely assumed to be negligible at Super*B* with a Layer0 pixel solution.

In Fig. 6.12 is reported the sensitivity to the S parameter in time-dependent CP violation analysis of the $B\to\phi K^0_S$ decays as a function of the material budget of the Layer0 radius $r_1 = 1.4, 1.6$ cm and material budget $x/X_0 = (0.1-1.0)\%$ also in presence of 5 times the nominal background.

The dashed line represents the reference value obtained in *BABAR*. Material budget in the range $x/X_0 = 0.35-0.50\%$ ($x/X_0 = 0.55-0.85\%$) is achievable for a Layer0 pixel solution based on CMOS monolithic active pixel sensors (hybrid pixels) depending on the results of the ongoing R&D activities. The S sensitivityy is very similar to the one obtained in *BABAR*. The maximal difference is about 6% (10%) in the worst case considered (including 5 times the nominal background).

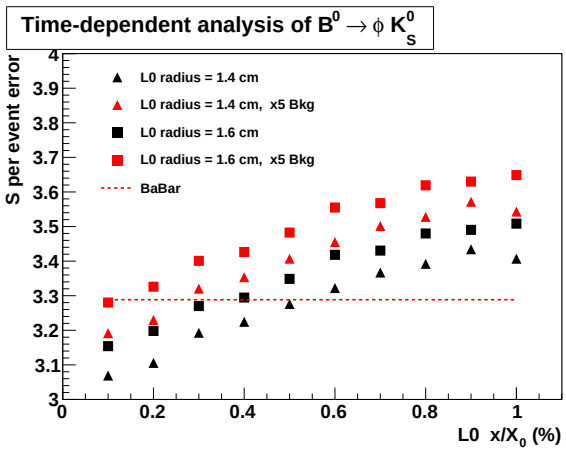

Figure 6.12: S per event error in $B^0 \to \phi K^0_S$ time-dependent analysis for different Layer0 radii $r_1 = 1.4, 1.6$ cm and material budget $x/X_0 = (0.1-1.0)\%$ compared with the reference value of *BABAR* (dashed line). Results in presence of 5 times the nominal background are also reported in the plot.

6.8 Silicon Sensors L. Bosisio - 8 pages

(Striplets will be discussed together with the other sensors)

Layers 1 to 5 of the SVT will be based on 300 μm thick double-sided silicon strip detectors, with integrated AC-coupling capacitors and polysilicon bias resistors. These devices are a technically mature and conservative solution to the requirements the SVT must meet to provide precise, highly segmented tracking near the interaction point. For the new layer 0, the baseline option also foresees double-sided silicon strip detectors, with short strips ('striplets'), 20 mm long, oriented at ± 45 degrees from the beam direction, fabricated on a 200 μm thick substrate. The detailed requirements which the detectors must meet are discussed below.

6.8.1 Requirements

To achieve good vertex resolution, it is especially important to minimize the material up to and including the first measurement. This requirement, and the need to provide precise vertexing in both z and ϕ, leads to the choice of double-sided detectors. Given the increased module length with respect to the BaBar SVT, in order to minimize the number of sensors required, the complexity of the assembly and the insensitive area between adjacent sensors and to ease the alignment task, we foresee to have the sensors fabricated on 150 mm diameter wafers, which is by now a widely available option from sensor suppliers. For layers 1 to 5 we plan to use 300 μm thick silicon wafers, which are a standard choice and present acceptable handling properties. For layer 0, given the very stringent limitations on the amount of material, we will be forced to go to 200 μm thick substrates. Processing double sided sensors on thin, 150 mm wafers is a significant challenge, which very few manufacturers are willing to tackle. Unfortunately, while the other layers could also be assembled from smaller sensors, fabricated on 100 mm wafers, layer 0 sensors do not fit in 100 mm wafers. This is due to the requirement to have only one sensor per layer 0 module, which in turn is dictated by the need to avoid insensitive regions and mechanical support structures, and also by limitations on the available number of readout channels. These difficulties are mitigated by the very small number of Mod. 0 sensors required and the fact that five of them can comfortably fit into a single 150 mm wafer. Because of this, a low fabrication and assembly yield can be tolerated for Layer 0 sensors.

Efficiency The silicon detectors must maintain high single-point efficiency in order to achieve the requirements given in Section xxx for high overall track reconstruction efficiency and good tracking resolution. Loss of efficiency can occur from intrinsic strip inefficiencies, from bad interconnections, or from faulty electronics channels. Intrinsic strip inefficiencies can occur due to fabrication defects or handling damage which can result in strips with high leakage currents,

poor insulation or broken AC-coupling capacitor. Good fabrication processes can achieve a total rate of defects below 1% with a reasonable yield ($> 70\%$).

Our goal is to achieve an overall single detector strip failure rate of less than 1%. Data from a large production of double-sided DC-coupled detectors (ALEPH) show that 60–70% can be achieved with a maximum inefficiency of 1%. On this basis, we expect that a 50% yield can be achieved for double-sided AC-coupled detectors while maintaining similar standards.

Resolution As described in Section xxx, we have determined from Monte Carlo simulations [xxx] that the intrinsic point resolution should be 15μm or better in both z and ϕ for the inner layers. These are the point resolutions for tracks at near-normal incidence. As the angle between the track and the plane normal to the strip increases, the resolution degrades. We require the resolution to degrade by no more than a factor of approximately 3 for angles up to 75° ($\lambda \sim 1.3$) from normal.

Radiation hardness A further requirement is that the quoted resolution values hold up to an integrated dose of ∼2 Mrad of ionizing radiation (electromagnetic in origin). This requirement leads to the use of AC-coupled detectors in order to avoid the problems associated with direct coupling of the large leakage currents which can occur at such large doses. It also has implications in the choice of the biasing scheme.

6.8.2 Sensor design and technology

From the above requirements and from the discussion in Sections xxx, we have arrived at the detector specifications and design parameters which are described in this section.

Substrate and implant type. The wafers will be n-type, with a resistivity in the range 4–8 kΩ cm, corresponding to a depletion voltage of 40 to 80 V. These values seem to be a reasonable compromise between the need to have a low depletion voltage and the need to avoid type inversion in the presence of radiation damage.

We will employ p^+ strips on the junction side and n^+ strips on the ohmic side, with p^+-blocking implants in between; see Figure xxx for a cross-sectional view. This choice has proven to be a mature, reliable technology xxx], requiring no R&D.

Coupling to preamplifier. The strips are connected to the preamplifiers through a decoupling capacitor, integrated on the detector by interposing a dielectric layer between the p or n-doped strip and the metal strip. AC coupling prevents the amplifier from integrating the leakage current with the signal; handling high leakage currents due to radiation damage imposes an additional burden on the preamplifier design and has other undesirable operational implications. On each sensor, the value of the decoupling capacitance must be much larger than the total strip capacitance on the same sensor, a requirement which is rather easily met by the fabrication technologies in use.

Bias resistors. We plan to use polysilicon bias resistors, because the alternative biasing method by exploiting the punch-through effect does not offer adequate radiation tolerance. The bias resistors values will range between 4 and 15 MΩ, depending on the layer. The choice of the R_B value is constrained by two requirements. A lower limit is determined by the need to limit the noise contribution, which has a $\sqrt{\tau/R_B}$ dependence, and if several strips are ganged together the effective resistance is correspondingly decreased. The requirement that, for floating strips, the product $R_B \cdot C_{TOT}$ must be much larger than the amplifier peaking time in order to allow for capacitive charge partition is fulfilled with ample margin for any reasonable values of R_B. An upper limit to R_B is dictated by the allowable potential drop due to the strip leakage current, which depends mainly on the irradiation level and decreases going from inner to outer layers. The maximum resistance value is also limited in practice by the need to limit the area occupied on the wafer. Values of 40 kΩ/square for the sheet resistance of polysilicon can be achieved. Thus, it is possible to fabricate a 10 MΩ resistor with a 6 μm-wide, 1500 μm-long polysilicon resistor. With a suitable shaping of the polysilicon line, the space re-

Table 6.5: Physical dimensions, number of strips and pitches for the nine different sensor models. Model VI has a trapezoidal shape.

Sensor Type	0	I	II	III	IVa	IVb	Va	Vb	VI
Dimensions (mm)									
z Length (L)	105.2	111.7	66.4	96.4	114.6	119.8	102.2	106.0	68.0
ϕ Width (W)	15.1	41.3	49.4	71.5	52.8	52.8	52.8	52.8	52.8-43.3
Thickness	0.20	0.30	0.30	0.30	0.30	0.30	0.30	0.30	0.30
PN junction side reads	u	z	z	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ
Strip Pitch (μm)									
z (u for Layer 0)	54	50	50	55	105	105	105	105	105
ϕ (v for Layer 0)	54	50	55	50	50	50	50	50	50 $\rightarrow$ 41
Readout Pitch (μm)									
z (u for Layer 0)	54	100	100	110	210	210	210	210	
ϕ (v for Layer 0)	54	50	55	100	100	100	100	100	100 $\rightarrow$ 82
Number of Readout Strips									
z (u for Layer 0)	1536	1104	651	865	540	565	481	499	318
ϕ (v for Layer 0)	1536	799	874	701	512	512	512	512	512

quired by the resistor will be less than 200 μm at 100 μm pitch (corresponding to strips at 50 μm pitch with resistors placed at alternate ends). A final requirement is that the bias resistor be quite stable for the expected radiation doses.

Considering the space needed to accommodate the biasing resistors and to gracefully degrade the electric field close to the edge with a guard ring structure, we specify the active region of the detectors to be 1.4 mm smaller than the physical dimensions, that is, the dead region along each edge has to be no more than 700 μm wide. This is the same specification chosen for the BaBar strip detectors and, although stricter than adopted by most silicon sensor designs, has proven to be feasible without difficulty, thanks to the choice of placing the polysilicon resistors in the edge region outside the guard ring. For Layer 0 sensors, which have a reduced thickness of 200 μm and smaller value, shorter bias resistors, we specify a 600 μm wide inactive edge region.

Optimization of z and ϕ readout strips. A major issue is which side of the detector (junction or ohmic) should read which coordinate (z or ϕ). The capacitance, and consequently, the noise is somewhat smaller on the junction side than on the ohmic side, and the strip pitch on the junction side can be 25 μm, while on the ohmic side, it is limited to about 50 μm because of the presence of the p-stop implant. For these reasons and because the z vertex measurement is more important from the point of view of physics, we use the junction side for the z strips on the inner layers. The better performance of the junction side also helps compensate for the additional resistance and capacitance imposed by the longer z fanout circuit.

In order to maintain acceptable signal-to-noise ratios for tracks at large dip angles, we employ a 100 μm readout pitch for these z strips with one floating strip in between every two readout strips. We have considered using a wider readout pitch, for example, 200Zμm for the very forward and backward regions in order to increase the signal at large dip angles. However, this would involve yet another detector design, and based on our present estimates of achievable electronic noise, it does not appear to be necessary.

Acceptable resolution can be obtained for the ϕ strips on the inner layers using the ohmic side.

Table 6.6: Number of the different sensor types per module, area of the installed sensors, number of installed sensors and number of sensors including spares. Spare sensors include one spare module per module type (two for layer 0), plus additional sensors accounting for possible losses during the whole SVT assembly process.

Sensor Type	0	I	II	III	IVa	IVb	Va	Vb	VI	All
Layer0	1	-	-	-	-	-	-	-	-	1
Layer1	-	2	-	-	-	-	-	-	-	2
Layer2	-	-	4	-	-	-	-	-	-	4
Layer3	-	-	-	4	-	-	-	-		4
Layer4a	-	-	-	-	4	-	-	-	2	6
Layer4b	-	-	-	-	-	4	-	-	2	6
Layer5a	-	-	-	-	-	-	6	-	2	8
Layer5b	-	-	-	-	-	-	-	6	2	8
Silicon Area (m^2)	0.013	0.055	0.079	0.167	0.194	0.203	0.291	0.302	0.222	1.52
Nr. of Sensors	8	12	24	24	32	32	54	54	68	308
Nr. Including Spares	20	20	40	35	44	44	72	72	92	439

Two solutions are possible; either a 50 μm readout pitch without floating strips, since there is no room for them on the ohmic side, or a 100 μm readout pitch with one floating strip. Either solution is feasible, and they should give roughly equivalent position resolution for single tracks. Double-track resolution is better for the first solution, and the noise contribution due to detector leakage currents is doubled in the latter solution. Therefore, preference goes to a 50 μm readout pitch without floating strips. Although this choice has twice as many readout channels, the cost implications are not very important because the electronics cost is dominated by the development effort and consequently the per channel incremental cost is not significant.

The physical dimensions, strip numbers and pitches for the various sensor models are listed in Table 6.5.

6.8.3 Wafer layout and quantities

Table 6.6 reports the sensor composition of the different detector modules, the number of installed sensors of each type, with the corresponding silicon areas, and the total numbers of sensors including spares. Spare sensors account for one spare module of each type (two for Layer 0), plus an additional 20% to compensate for possible losses during the assembly process. We see that the current design employs nine different types of sensors, for a total of 308 installed sensors covering 1.52 m^2. Using 150 mm diameter wafers and a dedicated sensor model for each module type allows to cover the ~ 1.5 times larger area with a smaller number of sensors with respect to *BABAR*, at the expense of having nine different models of sensors. However, through optimized usage of the wafer area it is possible to accommodate all nine sensor types in seven different wafer layouts, i.e. seven mask sets, and to fabricate all 439 sensors (spares included) on 287 wafers. This is illustrated in Table 6.7.

6.8.4 Prototyping and tests

... for the electrical parameters one can see Table 6.8

6.8.5 z-side strip connection options

On z-side, the readout pitch is set at 100 μm in Layers 1 and 2, 110 μm in Layer 3 and 210 μm in Layers 4 and 5, with a 'floating' strip in between, to improve spatial resolution for particle tracks with large incidence angles. Since the number of readout strips exceeds the number of

Table 6.7: List of different mask sets for 150 mm wafers, specifying the content of each wafer layout, the minimum value of the distance between the sensors and the wafer edge, the number of wafers required for each design and the total number of wafers. The numbers quoted include the spare sensors, but not the fabrication yield.

Mask Design	Wafer content	Min. Clearance to Wafer Edge (mm)	Number of Wafers
A	5×Mod 0	10.2	5
B	Mod I + Mod VI	8.2	20
C	Mod III	15.0	35
D	Mod IVa	11.9	44
E	Mod IVb	9.5	44
F	Mod Va + Mod VI	9.8	72
G	Mod Vb + Mod II	6.9	72
Total			287

available electronic channels, it is necessary to 'gang' together up to three (depending on the SVT layer) strips. This 'ganging' scheme connects two or three far apart strips to the same readout channel (Fig.6.13), thus preserving the strip pitch at the expense of a higher capacitance and series resistance, plus ambiguities in the hit position. For tracks at small θ angles with respect to the beam direction (that is, large incidence angles on the sensor), the signal-to-noise ratio is further degraded by the fact that a track traverses several z-strips (up to nine in the inner layers) and the signal becomes approximately proportional to the strip readout pitch (only 1/3 the wafer thickness in layers 1 to 3). This suggest adopting an alternative connection scheme, in which two (or more, at large incidence angles) *adjacent* strips are bonded to a single fanout trace, effectively increasing the strip pitch and the signal into a readout channel, with a less than proportional increase in capacitance, and no increase in series resistance. We call this connection scheme 'pairing'.

At small θ angles, this gives better S/N and efficiency when compared to individually connected strips. The improvement is even more important in comparison to the 'ganging' scheme, where the strip capacitance is proportional to the number of strips ganged together, but the signal remains that of a single strip. Moreover, for paired strips also the fanout capacitance and resistance can be made lower, because of the larger trace pitch.

Due to the lower noise, at small θ angles pairing is also expected to give better spatial resolution with respect to ganging. In order to avoid a significant increase of the input capacitance, pairing will be made between the 'readout' strips (at 100 μm pitch) so that a 'floating' strip is always present *between* two adjacent groups of paired strips. However, we are also evaluating the option of connecting also the intermediate (otherwise floating) strips *within* a group of paired strips, as shown by the 'upper' bonds in Fig.xxx.

Strip capacitance measurements performed on test sensors (Ref. xxx) confirm that pairing yields significantly lower capacitance with respect to ganging the same number of strips; the advantage in capacitance of pairing with respect to ganging increases for higher pairing/ganging multiplicity. The additional increase in total capacitance when connecting also the intermediate strips is $4-5\%$ on p-side, $\sim 6\%$ on n-side. In front of this, a better signal collection efficiency is expected.

Table 6.8: Electrical parameters for the different detector models *(Numbers to be updated).*

Detector Model	z (u for model 0) readout Side			ϕ (v for model 0) readout Side		
	C_{strip} (pF/cm)	C_{AC} (pF/cm)	R_{series} (Ω/cm)	C_{strip} (pF/cm)	C_{AC} (pF/cm)	R_{series} (Ω/cm)
0	2.5	40	4	2.5	30	8.5
I	1.7	40	5	2.5	30	9
II	1.7	40	4	2.5	30	7
III	1.7	30	7	1.7	40	4
IVa	1.7	60	3	1.7	40	4
IVb	1.7	60	3	1.7	40	4
Va	1.7	60	3	1.7	40	4
Vb	1.7	60	3	1.7	40	4
VI	1.7	60	3	1.7	30	4.5

6.9 Fanout Circuits L.Vitale - M.Prest4+4 pages

(Layer0 will be treated separately from the other ones)

6.9.1 Fanouts for layer0

6.9.1.1 Requirements

6.9.1.2 Technology

6.9.1.3 Design

6.9.1.4 Prototyping and tests

6.9.2 Fanouts for outer layers

6.9.2.1 Requirements

The requirements will be fixed by the detector designs. From the production point of view, the minimum line width is 15 μm with a space between the lines of 15 μm. With the present technology, it is not possible to go below these numbers. No constraints are present on the fanout length given the same machines used for the micropattern gas detector production will be used.

6.9.2.2 Material and production technique

The BaBar fanouts were produced on 50 μm Upilex (by UBE) with a deposit of 150 nm of Cr, 4.5 μm of copper followed by a layer of 150 nm of Cr and 1.5 μm of amorphous gold. The SuperB SVT fanouts will be produced on a similar material by UBE (50 μm of polyamide with 5 μm of copper directly deposited on the base material) which should ensure less defects and thus a better yield. This material will be tested in the prototype phase. The old Upilex is anyway still available if the new material would prove not adequate.

A new technique for the production will be implemented in order to reduce the production times. In the BaBar production line, the photoresist was impressed through a mask after its being deposited on the Upilex requiring to work in a clean room. For SuperB, the idea is to impress the photoresist directly with a laser; this means the photoresist is solid and allows to complete the procedure in a much faster way. This technique has already been tested on the same pitches foreseen for the SVT fanouts.

The increase in the production speed allows to repeat the production of pieces with defects without delaying the SVT assembly. All the pieces will be gold plated with 1.5 μm of amorphous gold for the bonding.

6.9.2.3 Design

The design will follow the same rules of the BaBar fanouts adapting it to the different length of the modules. Differently from the BaBar pieces, no test-tree is foreseen (see next

section). To allow the gold plating, all the lines will be shorted. A suitable cutting device will be developed to cut the shorting line after the visual inspection.

Table 6.9 summarizes the geometrical parameters as well as the number of readout strips and channels, the typical pitch and the total number of required circuits per layer and type.

Fig. 6.13 presents a sketch of the ganging principle proposed for the design of layers z 3-4-5.

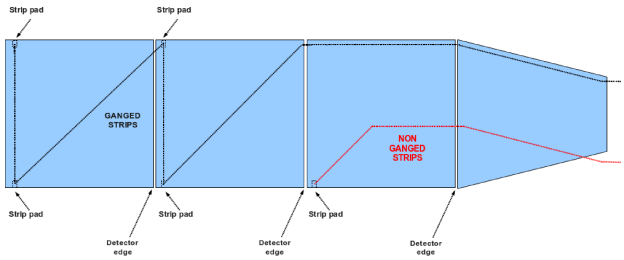

Figure 6.13: Schematic view of two z strips ganged through the fanout circuit.

6.9.2.4 Tests and prototyping

All the fanouts will be automatically optically checked by a dedicated machine which will use the gerber files of the fanouts to find shorts or open lines. The machine can work with 25 μm lines. The region with smaller lines (15 μm with a 15 μm space) corresponding to the bonding area (1.5 mm long and around 6 mm wide) will have to be controlled manually.

Given the much shorter time needed for the production, no correction is foreseen for shorts or open lines; the damaged pieces will be produced again. On the other hand, if a short is present in the larger pitch region, the same correction procedure used for BaBar (the use of a microprobe) can be implemented.

As far as the tests are concerned, a batch of fanouts will be produced starting from the BaBar design to check the whole production and test chain. These fanouts in principle can be used with working detectors to test also the assembly procedures.

Figure 6.14 shows the design of a z fanout prototype of layer 3. These prototypes were also used to measure the typical capacitance and resistance.

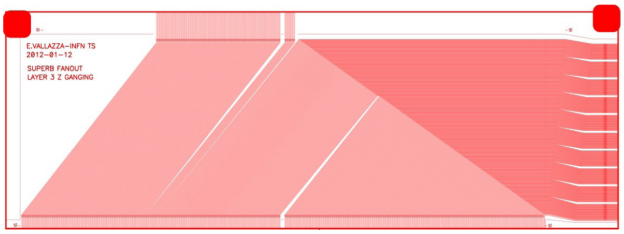

Figure 6.14: Design of a z fanout prototype of layer 3.

6.10 Electronics Readout 28 pages

6.10.1 Readout chips V.Re - 10

6.10.1.1 Electronic Readout for Strip and Striplet Detectors

The front-end processing of the signals from the silicon strip detectors will be performed by custom-designed ICs mounted on hybrid circuits that distribute power and signals, and thermally interface the ICs to the cooling system. As discussed below, the very different features of inner (Layer 0-3) and outer layers (4 and 5) of the SVT set divergent requirements to the readout chips, which most probably makes it necessary to develop two distinct integrated circuits. This obviously holds also in the case a different technology (pixels) is adopted for Layer 0 instead of short strips (striplets). Generally speaking, both types of ICs will consist of 128 channels, each connected to a detector strip. The signals from the strips, after amplification and shaping will be compared to a preset threshold. If a signal exceeding the threshold is detected, a 3-4 bit analog information about the signal amplitude will be provided by an ADC: this will mostly serve for calibration and monitoring purposes in the innermost layers, whereas in outer

Table 6.9: Summary of fanout circuit characteristics.

Layer	Fanout Type	Length (mm)		Number of Readout		Typical Pitch at (μm)		Number of Circuits
		Left	Right	Strips	Channels	Input	Output	
1	z	200.5	196.5	1104	896	100	45	12
	ϕ	93.82	89.82	799	896	50	45	12
2	z	196.501	200.501	1302	896	100	45	12
	ϕ	68.611	72.611	874	896	55	45	12
3	z	242.485	242.485	1730	1280	110	45	12
	ϕ	54.635	54.635	701	1280	100	45	12
4a	z	326.538	322.538	1398	640	210	45	16
	ϕ	34.563	30.563	512	640	82	45	16
4b	z	326.536	322.536	1448	640	210	45	16
	ϕ	23.826	19.826	512	640	82	45	16
5a	z	401.267	405.266	1761	640	210	45	18
	ϕ	31.747	35.746	512	640	82	45	18
5b	z	401.266	405.266	1815	640	210	45	18
	ϕ	20.346	24.346	512	640	82	45	18

layers it will be essential for dE/dx measurements. The dimensions of the readout IC are expected to be about 6×4 mm^2. As discussed in the SVT HDI subsection of this TDR, the dimensions of the HDI set a 6 mm upper limit on the side of the chip with the bonding pads for the interconnection with the strip sensors. The power dissipation will be below 4 mW/channel including both analog and digital sections. For each channel with a signal above threshold, the strip number, the amplitude information, the chip identification number and the related time stamp will be stored inside the chip waiting for a trigger signal for a time corresponding to the trigger latency (about 7 μs, corresponding to a 150 kHz trigger rate). When a trigger is received, data will be read out and transmitted off chip, otherwise they will be discarded. The data output from the microstrip detector will be sparsified, i.e. will consist only of those channels generating a hit. The readout integrated circuits must remain functional up to 5 times nominal background.

The option of operating in a data push fashion could be preserved for the external layers, where this will be allowed by the low strip hit rate. This will give the possibility to feed data from these layers to the trigger system.

6.10.2 Readout chips requirements

The microstrip electronics must ensure that the detector system operates with adequate efficiency, but also must be robust and easy to test, and must facilitate testing and monitoring of the microstrip sensors. AC coupling is assumed between the strips and the readout electronics.

- **Mechanical Requirements:**
  Number of channels per chip: 128

Chip size: width ≤6 mm, length ≤4 mm
Pitch of input bonding pads: <45 μm

- **Operational Requirements:** Operating temperature: <40 °C
  Radiation tolerance: >4 Mrad/year, >$6{\cdot}10^{12}$ n_{eq}/cm^2/year (these are the expected values in Layer 0; in outer layers, radiation levels are at least on order of magnitude lower)
  Power dissipation: <4 mW/channel
  Detector and fanout capacitance: 10 pF ≤C_D≤ 70 pF (the chip must be stable when sensor strips are disconnected from the input pads of the analog channels)

- **Dynamic range:** The front-end chips must accept signals from either P and N-side of the strip detectors. A linear response of the analog processing section is required from a minimum input charge corresponding to 0.2 MIP up to a full dynamic range of 10-15 MIP charge for dE/dx measurements.

- **Analog Resolution:** The front-end chips have to provide an analog information about the charge collected in the detector, which will be also used for calibrating and monitoring the system. A resolution of 0.2 MIP charge is required for dE/dx measurements. In case of a compression-type ADC, based on the time-over-threshold technique (ToT), this may translate in 3-4 bits of information.

- **Efficiency:** At design luminosity, the microstrip readout must have a hit efficiency of at least 95% during its entire operational lifetime. This includes any loss of data by readout electronics or readout dead time.

- **Readout bandwidth:** Data coming out of the chip will be substantially reduced by operating in a triggered mode. The chips can use up to 4 output LVDS lines, as it is needed to handle the higher data throughput in inner SVT layers.

- **Radiation Tolerance:** All the components of the microstrip readout system must remain operational up to 10 years of SuperB running at the nominal luminosity.

- **Peaking Time:** The constraints for the peaking time of the signal at the shaper output are dictated by different needs in inner and outer layers. In Layer 0, the high occupancy due to background and the need to avoid pulse overlap and consequent hit inefficiencies set the maximum peaking time at t_p=25 ns, which also allow for a high timing resolution (see below). In the external layers 4 and 5, where background hit frequency is much smaller and where strips are longer and have a larger capacitance, the peaking time will be mostly determined by the need of reducing series noise contributions and has to be in the range of 0.5-1.0 μs.

- **Signal-to-Noise Ratio:** Concerning the signal, this requirement has to take into account the different thickness of silicon detectors in inner (200 μm) and outer (300 μm) layers, as well the signal spread among various strips that depends on the track angle inside detectors and that, again, may vary in different SVT layers. Noise-related parameters (strip capacitance and distributed resistance) also sizably vary across the SVT. A signal-to noise ratio of 20 has to be ensured across the whole SVT and should not decrease significantly after irradiation. Here are the two extreme cases (where the equivalent noise charge ENC includes the thermal noise contribution from the distributed resistance of the strips):

  - Layer 0 striplets: ENC ≈700 e- at C_D=10 pF and at t_p=25 ns
  - Layer 5 strips: ENC ≈1000 e- at C_D=70 pF and at t_p=1 μs

- **Threshold and Dispersion:** Each microstrip channel will be read out by comparing its signal to a settable threshold around 0.2 MIP. Threshold dispersion must be low enough that the noise hit rate and the efficiency are degraded to a negligible extent. Typically, this should be 300 rms electrons at most and should be stable during its entire operational lifetime.

- **Comparator Time Resolution:** The comparator must be fast enough to guarantee that the output can be latched in the right time stamp period.

- **Time Stamp:** 30 ns time stamp resolution is required for inner layers to get a good hit time resolution in order to reduce the occupancy in the offline time window (50-100 ns). In the outer layers the time stamp resolution is less critical since the hit time resolution will be dominated by the long pulse shaping time. A single 30 ns time stamp clock in all layers will be used.

- **Chip clock frequency:** Two main clocks will be used inside the readout chip, the time stamp clock (about 30 MHz) and the readout clock (132 MHz or 198 MHz). These clocks will be synchronized with the 66 MHz SuperB system clock. In case the analog-to-digital conversion is based on the Time-Over-Threshold method, a ToT clock has to be generated inside the chip. The ToT clock period should at least match the pulse shaping time to get a good analog resolution. A faster ToT clock could slightly improve the analog resolution but an upper limit (≈3.5) on the ratio between ToT clock frequency and the shaping time frequency is imposed by the required dynamic range needed for low momentum particle dE/dx measurements (≈10-15 MIP) and the number of bits available for ToT. With the experience of the BaBar Atom chip a ToT clock frequency 3 times higher than the pulse shaping frequency could be used: 132 MHz for L0, 66 MHz for L1-2, 16.5 MHz for Layer3 and 6.6-3.3 MHz for L4-5.

- **Mask, Kill and Inject:** Each micro-strip channel must be testable by charge injection to the front-end amplifier. By digital control, it shall be possible to turn off any micro-strip element from the readout chain.

- **Maximum data rate:** Simulations show that machine-related backgrounds dominate the overall rates. At nominal background levels (including a safety factor of 5), the maximum hit rate per strip goes from about 1 MHz/strip in Layer 0 to about 50 kHz/strip in Layer 5, z-side.

- **Deadtime limits:** The maximum total deadtime of the system must not exceed 10 % at a 150 kHz trigger rate and background 5 times the nominal expected rate.

- **Trigger specifications:** The trigger has a nominal latency of about 7 μs, a maximum jitter of 0.1 μs, and the minimum time between triggers is 70 ns. The maximum Level 1 Trigger rate is 150 kHz.

- **Cross-talk:** Must be less than 2 %.

- **Control of Analog Circuitry on Power-Up:** Upon power-up, the readout chip shall be operational at default settings.

- **Memory of Downloaded Control of Analog Circuitry:** Changes to default settings shall be downloadable via the readout chip control circuitry, and stored by the readout chip until a new power-up cycle or additional change to default settings.

- **Read-back of Downloadable Information:** All the data that can be downloaded also shall be readable. This includes data that has been modified from the default values and the default values as applied on each chip when not modified.

- **Data Sparsification:** The data output from the microstrip detector shall be only of those channels that are above the settable threshold.

- **Microstrip output data content:** The microstrip hit data must include the time stamp and the microstrip hits (strip number and relevant signal amplitude) for that time stamp. The output data word for each strip hit should contain 16 bits (7 strip address, 4 ToT, 1 type (Hit or Time Stamp) 4 bits to be defined). A 10-bit time stamp information (with 6 additional bits: 1 type, 5 bits to be defined) will be attached to each group of hits associated to a given time stamp (hit readout will be time-ordered).

6.10.3 Readout Chip Implementation

The SuperB SVT readout chips are mixed-signal integrated circuits in a 130 nm CMOS technology and are being designed to comply with the requirements discussed above. Each chip comprises 128 analog channels, each consisting of a charge-sensitive preamplifier, a unipolar semi-Gaussian shaper and a hit discriminator. A polarity selection stage will allow the chip to operate with signals delivered both from n- and p-sides of the SVT double-sided strip detectors. A symmetric baseline restorer may be included to achieve baseline shift suppression. When a hit is detected, a 3-4 bit analog-to-digital conversion will be performed by means of a Time-Over-Threshold (ToT) detection. The hit information will be buffered until a trigger is received; together with the hit time stamp, it will be then transferred to an output interface, where data will be serialized and transmitted off chip on output LVDS lines. An n-bit data output word will be generated for each hit on a strip. A programming interface accepts commands and data from a serial input bus and programmable registers are used to hold input values for DACs that provide currents and voltages required by the analog section. These registers have other functions, such as controlling data output speed and selecting the pattern for charge injection tests.

Given the very different requirements of inner and outer layers, in terms both of detector parameters and hit frequency, two different chips will be designed; they will be based on a same data protocol, but will be optimized for operation at different clock frequencies. The block diagram of the analog channel is shown in Fig. 6.15.

The digital readout of the matrix will exploit the architecture that was originally devised for a high-rate, high-efficiency readout of a large CMOS pixel sensor matrix. Each strip has a dedicated array of pre-trigger buffers, which can be filled by hits with different time stamps. The size of this buffer array is determined by the maximum strip hit rate (inner layers) and by the trigger latency. After arrival of a trigger, only hits with the same time stamp as the one provided by the triggering system send their information to the back-end. The array of 128 strips is divided in four sections, each with a dedicated sparsifier encoding the hits in a single clock cycle. The storage element next to each sparsifier (barrel level-2) acts like a FIFO memory conveying data to a barrel-L1 by a concentrator which merges the flux of data and preserves the time order of the hits. This barrel-L1 will drive the output data bus which will use up to four

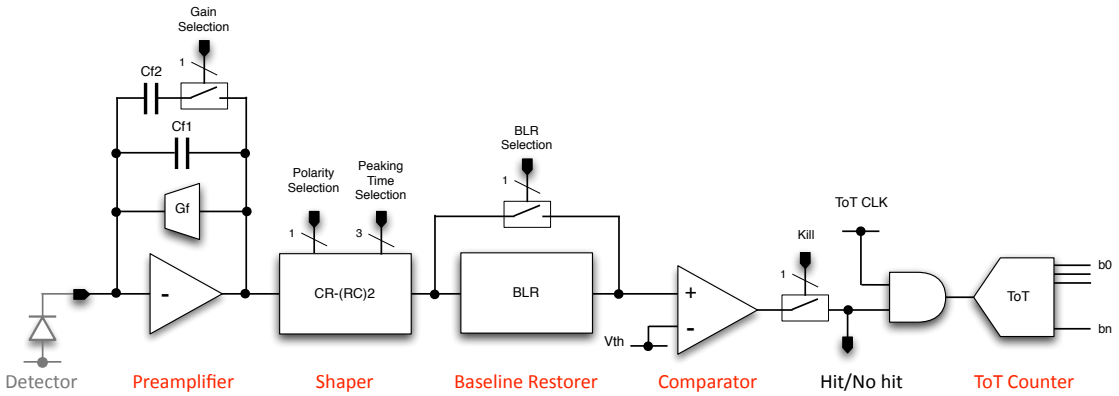

Figure 6.15: Analog channel block diagram.

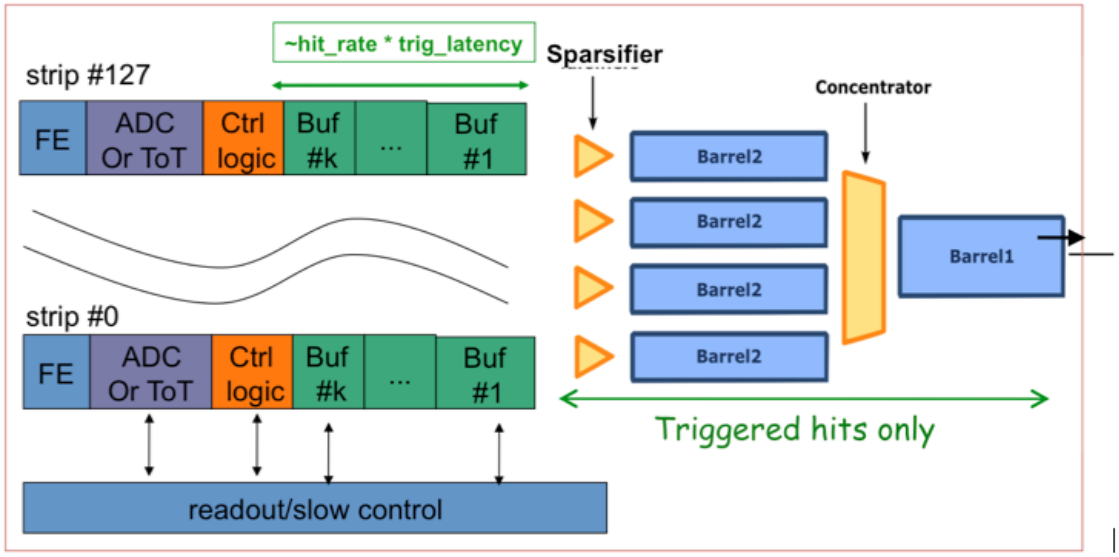

Figure 6.16: Readout architecture of the SVT strip readout chips.

output lines depending on the data throughput and will be synchronous to a 120 MHz clock.

6.10.4 R&D for strip readout chips

The R&D to support the development of the SuperB strip readout chips has begun in 2011. The chosen technology for integration is a 130 nm CMOS process: this has an intrinsically high degree of radiation resistance, which can be enhanced with some proper layout prescriptions such as enclosed NMOS transistors and guard rings. There is a large degree of experience with mixed-signal design in this CMOS node that was gained in the last few years inside the HEP community.

The readout architecture is being tested with realistic data created by Monte Carlo analysis of the interaction region. Verilog simulations demonstrate that the chip will be able to operate with a 99 % readout efficiency in the worst case condition, which includes the safety factor of 5 in the background levels.

The analog section of the chip is being optimized from the standpoint of noise, comparator threshold dispersion and sensitivity to variations of process parameters. It will be possible to select the peaking time of the signal at the shaper output (25-100 ns for inner layers, 1 μs for outer layers) by changing the value of capacitors in the shaper. In this way the noise performances of the chip can be optimized according to the signal occupancy, preserving the required efficiency. Table 6.10 shows the main parameters of the analog section, according to simulation estimates for realistic values of detector parameters and strip hit rates. The loss in efficiency is determined by the limits in the double pulse resolution of the analog section, which depends on the signal peaking time. An acceptable compromise will be found here with the noise performance.

In 2012, the submission of two chip prototypes including 64 analog channels and a reduced-scale version of the readout architecture is foreseen.

The submission of the full-scale, 128-channels chip prototypes is then scheduled in late 2013. This version will have the full functionality of the final production chip.

6.10.5 Hybrid Design M.Citterio - 10

6.10.6 Data Transmission M.Citterio - 10

6.10.7 Power Supply - 2

6.11 Mechanical Support & Assembly S.Bettarini/F.Bosi - 14 pages

- Introduction

6.11.1 I.R. Constraint

- Description of the IR components: Be-pipe, L0, SVT, W shielding, QD0
- Active region definition and clearances
- Mechanical architecture (how each components is constrained to what)
- Staging area assembly
- Quick demounting motivations and removable support cage concept

6.11.2 Module Assembly

- L0 module baseline components and assembly procedure
- L 1-5 module components and assembly procedure

6.11.3 Detector Assembly and Installation

6.11.3.1 Half Detector Assembly

- L0 module assembly on the cold flanges
- Cold flanges descriptions, required features and jig
- L 1-5 module assembly on the Support cones
- Support cones, buttons, cooling ring description, required features and jig
- Space frame features

Table 6.10: Main parameters of the analog section of the SVT strip readout chips.

Layer	C_D [pF] including fanout (with ganging)	t_p [ns] Available	t_p [ns] Selected	Total ENC [e rms]	Total ENC [e rms] after 7.5 years	Total ENC [e rms] after 7.5 years with ×5 safety factor	Hit rate/strip [kHz] nominal	Efficiency 1-N nominal	Efficiency 1-N with ×5 safety factor
0-side 1	11.2		25				187	0.99	095
0-side 2	4.0		25				187	0.99	0.97
1 phi	33.4		75	850	930	1180	170	0.98	0.92
1 z	27.6	25-200	75	925	1025	1345	134	0.98	0.91
2 phi	37.2	with 25 ns	100	815	895	1165	134	0.98	0.90
2 z	30.3	steps	100	910	1010	1335	134	0.98	0.88
3 phi	35.7		150	890	1040	1505	116	0.96	0.82
3 z	40.8		150	1030	1140	1505	79	0.98	0.90
4 phi	52.5		500	1075	1265	1805	25	0.98	0.92
4 z	47.2	375, 500	500	895	1115	1715	13.4	0.99	0.95
5 phi	65.5	750, 1000	750	1085	1205	1530	16.2	0.98	0.93
5 z	52.2		750	855	965	1280	8.8	0.99	0.95

6.11.3.2 Mount L0 on the Be-pipe and L 1-5 on the W Shielding

- HDMF assembly description for L0 on the be-pipe
- HDMF assembly for the L 1-5 on the W shielding
- Displacement w.r.t. the IR
- Gimbal ring and support cage description
- Optical modules survey
- Electrical testing and connection to the transition Card

6.11.3.3 Installation of Complete Assembly into the SuperB Detector

- Constrains and scenario of mounting, stiffness and clearance required

6.11.3.4 Quick Demounting

- Infrastructure required and SVT demounting/mounting procedure

6.11.4 Detector Placement and Survey

6.11.4.1 Placement accuracy

6.11.4.2 Survey with tracks

6.11.5 Detector Monitoring

6.11.5.1 Position Monitoring System

6.11.5.2 Radiation Monitoring

6.11.6 R&D Program

6.11.6.1 Cables

6.11.6.2 hybrid

6.11.6.3 Inner layer sextant

6.11.6.4 Arch modules

6.11.6.5 Cones and space frame

6.11.6.6 Full-scale model of IR

6.12 Layer0 Upgrade Options

G.Rizzo/L.Ratti - 10 pages

With the machine operated at full luminosity, the layer 0 of the silicon vertex tracker may

benefit from upgrading to a pixellated detector. This solution can actually provide some significant advantages with respect to the baseline striplet option. In particular

- the occupancy per detector element from machine background is expected to fall to a few kHz, with a major impact on the speed specifications for the front-end electronics, mainly set by the background hit rate in the case of the striplet readout chip;
- better accuracy in vertex reconstruction can be achieved with a detector pitch of 50 μm or smaller; the shape of the pixel can be optimized in such a way to reduce the sensor pitch in the z direction while keeping the area in the range of 2500-3000 μm^2, which guarantees enough room for sparse readout functionalities.

A few technology alternatives for pixel detector fabrication are being investigated and R&D activities are in progress to understand advantages and potential issues of the different options.

6.12.1 Technology options

Following is a description of the technology options that are being considered for the upgrade of the SuperB SVT innermost layer.

6.12.1.1 Hybrid pixels

Hybrid pixel technology has reached quite a mature stage of development. Hybrid pixel detectors are currently used in the LHC experiments [16, 17, 18, 19], with pitch in the range from 100 μm to a few hundred μm, and miniaturization is being further pushed forward in view of the upgrade of the same experiments at the High Luminosity LHC (HL-LHC) [38, 21, 22]. Hybrid pixel systems are based on the interconnection between a sensor matrix fabricated in a high resistivity substrate and a readout chip. Bump-bonding with indium or indium-tin or tin-lead alloys is the mainstream technology for readout chip-to-sensor interconnection. The design of a hybrid pixel detector for the SVT innermost layer has to meet some challenging specifications in terms of material budget and spatial resolution. Since the readout chip and the sensor are laid one upon the other, hybrid pixels are intrinsically thicker detectors than microstrips. Interconnect material may further degrade the performance, significantly increasing the radiation length equivalent thickness of the detector. As far as the readout and sensor chips are concerned, substrate thinning to 100-150 μm and subsequent interconnection are within present technology reach. Further thinning may pose some issues in terms of mechanical stability and, as the detector thickness is reduced, of signal-to-noise ratio and/or front-end chip power dissipation. Concerning interconnection, the vertical integration processes currently under investigation in the high energy physics community might help reduce the amount of material. Among the commercially available technologies, the ones provided by the Japanese T-Micro (formerly known as ZyCube), based on so called micro-bumps, and by the US based company Ziptronix, denoted as direct bonding technique, seem the most promising [23]. The Fraunhofer EMFT has developed a bonding technique called SLID and based on a very thin eutectic Cu-Sn alloy to interconnect the chips [24]. The spatial resolution constraints set a limit to the area of the elementary readout cell and, as a consequence, to the amount of functionalities that can be included in the front-end electronics. A planar, 130 nm CMOS technology may guarantee the required density for data sparsification and in-pixel time stamping in a 50 μm$\times$50 μm pixel area (as already observed, a different aspect ratio might be preferred to improve the resolution performance in one particular direction). The above mentioned interconnection techniques can fully comply with the detector pitch requirements (in the case of the T-Micro technology, pitches as small as 8 μm can be achieved). A fine pitch (30 μm minimum), more standard bump-bonding technology is also provided by IZM. This technology has actually been successfully used to bond the SuperPIX0 front-end chip (to be described later on in this section) to a 200 μm thick pixel detector.

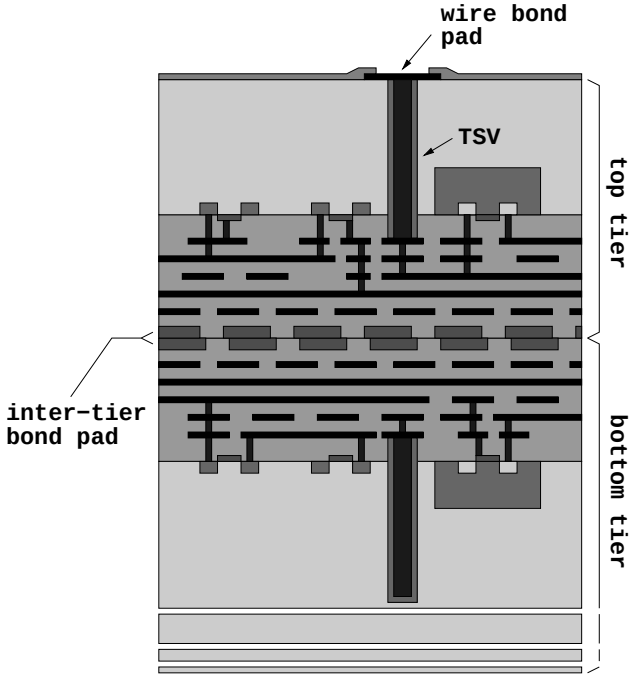

Figure 6.17: cross-sectional view of a double-layer 3D process.

Denser CMOS technologies (belonging to the 90 or 65 nm technology) can be used to increase the functional density in the readout electronics and include such functions as gain calibration, local threshold adjustment and amplitude measurement and storage. In this case, costs for R&D (and, eventually, production) would increase significantly. Vertical integration (or 3D) CMOS technologies may represent a lower cost alternative to sub-100 nm CMOS processes. The technology cross section shown in Fig. 6.17, in particular, points to the main features of the extremely cost-effective process provided by Tezzaron Semiconductor [25] which was used for the design of the SDR1 chip. The Tezzaron process can be used to vertically integrate two (or more) layers, specifically fabricated and processed for this purpose by Chartered Semiconductor (now Globalfoundry) in a 130 nm CMOS technology. In the Tezzaron/Chartered process, wafers are face-to-face bonded by means of thermo-compression techniques. Bond pads on each wafer are laid out on the copper top metal layer and provide the electrical contacts between devices integrated in the two layers. The top tier is thinned down to about 12 μm to expose the through silicon vias (TSV), therefore making connection to the buried circuits possible. Among the options available in the Chartered technology, the low power (1.5 V supply voltage) transistor option is considered the most suitable for detector front-end applications. The technology also provides 6 metal layers (including two top, thick metals), dual gate option (3.3 V I/O transistors) and N- and P-channel devices with multiple threshold voltages. The main advantages deriving from a vertical integration approach to the design of a hybrid pixel front-end chip can be summarized as follows:

- since the effective area is twice the area of a planar technology from the same CMOS node, a better trade-off can be found between the amount of integrated functionalities and the detector pitch;
- separating the digital from the analog section of the front-end electronics can effectively prevent digital blocks from interfering with the analog section and from capacitively coupling to the sensor through the bump bond pad.

The design of a 3D front-end chip for pixel detectors is in progress in the framework of the VIPIX experiment funded by INFN.

6.12.1.2 Deep N-well CMOS monolithic sensors

Deep N-well (DNW) CMOS monolithic active pixel sensors (MAPS) are based on an original design approach proposed a few years ago and developed in the framework of the SLIM5 INFN experiment [11]. The DNW MAPS approach takes advantage of the properties of triple well structures to lay out a sensor with relatively large area (as compared to standard three transistor MAPS [26]) read out by a classical processing chain for capacitive detectors. As shown by the technology cross section in Fig. 6.18, the sensor, featuring a buried N-type layer with N-wells (NW) on its contour according to a typical

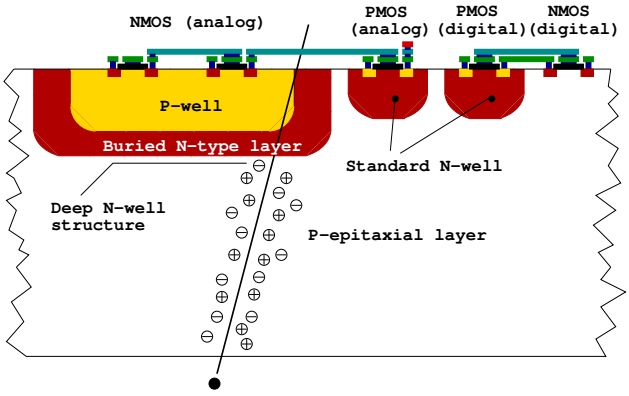

Figure 6.18: simplified cross-sectional view of a DNW MAPS. NMOS devices belonging to the analog section may be built inside the sensor, while the other transistors cover the remaining area of the elementary cell, with PMOSFETs integrated inside standard N-wells.

deep N-well scheme, collects the charge released by the impinging particle and diffusing through the substrate, whose active volume is limited to the uppermost 20-30 μm thick layer below the collecting electrode. Therefore, within this extent, substrate thinning is not expected to significantly affect charge collection efficiency, while improving momentum resolution performance in charged particle tracking applications. As mentioned above, DNW MAPS have been proposed chiefly to comply with the intense data rates foreseen for tracking applications at the future high energy physics (HEP) facilities. The area taken by the deep N-well collecting electrode can actually be exploited to integrate the NMOS parts of the analog front-end inside the internal P-well. A small amount of standard N-well area can be used for PMOS devices, instrumental to the design of high performance analog and digital blocks taking full advantage of CMOS technology properties. In this way, both analog functions, such as signal shaping, and digital functions, such as time stamping and data storing, buffering and sparsification, can be included in the pixel operation. Note that the presence of N-wells other than the sensor is instead strongly discouraged in standard MAPS design, where the operation of the tiny collecting electrode would be jeopardized by the presence of any N-type diffusion in the surrounding. Based on the concept of the DNW monolithic sensor, the MAPS detectors of the Apsel series (see Section 6.12.2.2), which are among the first monolithic sensors with pixel-level data sparsification [27, 28], have been developed in a planar, 130 nm CMOS technology. In 2008, the Apsel4D, a DNW MAPS with 128×32 elements has been successfully tested at the Proton Synchrotron facility at CERN [31]. More recently, vertical integration technologies, like the ones discussed in the previous section for hybrid pixels, have been considered for the design of 3D DNW monolithic sensors. Some specific advantages can derive from the vertical integration approach to DNW MAPS. In particular, all the PMOS devices used in digital blocks can be integrated in a different substrate from the sensor, therefore significantly reducing the amount of N-well area (with its parasitic charge collection effects) in the surroundings of the collecting electrode and improving the detector charge collection efficiency (CCE). The first prototypes of 3D DNW MAPS [33, 34] have been submitted in the framework of the 3D-IC collaboration [35]. Characterization has started in the last quarter of 2011.

6.12.1.3 Monolithic pixels in CMOS quadruple well technology

In DNW MAPS, charge collection efficiency can be negatively affected, although to a limited extent, by the presence of competitive N-wells including the PMOS transistors of the pixel readout chain, which may subtract charge from the collecting electrode. Inefficiency is related to the relative weight of N-well area with respect to the DNW collecting electrode area. A novel approach for isolating PMOS N-wells has been made available with a planar 180 nm CMOS process called INMAPS, featuring a quadruple well structure [28]. Fig. 6.19 shows a simplified cross section of a pixel fabricated with the INMAPS process. By means of an additional

processing step, a high energy deep P-well implant is deposited beneath the PMOS N-well (and not under the N-well diode acting as collecting electrode). This implant creates a barrier to charge diffusing in the epitaxial layer, preventing it from being collected by the positively biased N-wells of in-pixel circuits and enabling a theoretical charge collection efficiency of 100%. The NMOS transistors are designed in heavily doped P-wells located in a P-doped epitaxial layer which has been grown upon the low resistivity substrate. Epitaxial layers with different thickness (5, 12 or 18 μm) and resistivity (standard, about 50 Ω·cm, and high resistivity, 1 kΩ·cm) are available. The epitaxial layer is obviously expected to play an important role in improving charge collection performance. Actually, carriers released in the epitaxial layer are kept there by the potential barriers at the P-well/epi-layer and epi-layer/substrate junctions. A test chip, including several different test structures to characterize both the readout electronics and the collecting electrode performance has been submitted in the third quarter of 2011. Results from the preliminary characterization of the prototypes are discussed in Section 6.12.2.3.

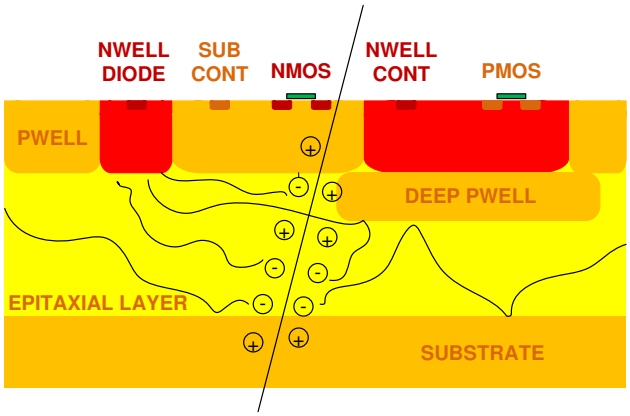

Figure 6.19: cross-sectional view of the INMAPS CMOS technology; emphasis is put on the deep P-well layer.

6.12.2 Overview of the R&D activity

6.12.2.1 Front-end electronics for hybrid pixels in planar and 3D CMOS technology

A prototype hybrid pixel detector named SuperPIX0 has been designed as a first iteration step aimed at the development of a device to be used for the layer0 upgrade. The main novelties of this approach are the sensor pitch size (50×50μm) and thickness (200μm) as well as the custom front-end chip architecture providing a sparsified and data-driven readout. The SuperPIX0 pixel sensor is made of n-type, Float Zone, high-resistivity silicon wafers, with a nominal resistivity larger than 10 kΩ. The SuperPIX0 chip, fabricated in the STMicroelectronics 130nm CMOS technology, is composed of 4096 channels (50x50 μm^2) arranged into 128 columns by 32 rows. Each cell contains an analog charge processor (shown in Fig. 6.20) where the sensor charge signal is amplified and compared to a chip-wide preset threshold by a discriminator. The in-pixel digital logic, which follows the comparator, stores the hit in an edge-triggered set reset flip-flop and notifies the periphery of the hit. The charge sensitive amplifier uses a single-ended folded cascode topology, which is a common choice for low-voltage, high gain amplifiers. The 20 fF MOS feedback capacitor is discharged by a constant current which can be externally adjusted, giving an output pulse shape that is dependent upon the input charge. The peaking time increases with the collected charge and is in the order of 100 ns for 16000 electrons injected. The charge collected in the detector pixel reaches the preamplifier input via the bump bond connection. Alternatively, a calibration charge can be injected at the preamplifier input through a 10 fF internal injection capacitance so that threshold, noise and crosstalk measurements can be performed. The calibration voltage step is provided externally by a dedicated line. Channel selection is performed by means of a control section implemented in each pixel. This control block, which is a cell of a shift register, enables the injection of the charge though the calibration capacitance. Each pixel features a digital mask used to isolate single noisy chan-

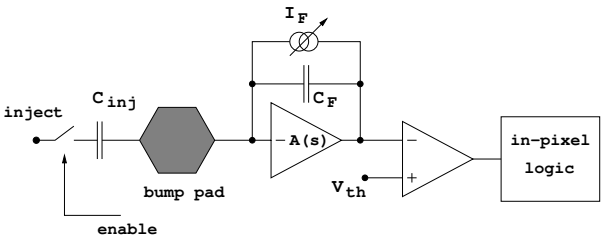

Figure 6.20: block diagram of the analog front-end electronics for the elementary cell of the SuperPIX0 readout chip.

nel. This mask is implemented in the readout logic. The input device (whose dimensions were chosen based on [29]) featuring an aspect ratio W/L=18/0.3 and a drain current of about 0.5 μA, is biased in the weak inversion region. A non-minimum length has been chosen to avoid short channel effects. The PMOS current source in the input branch has been sized to have a smaller transconductance than the input transistor. The analog front-end cell uses two power supplies. The analog supply (AVDD) is referenced to AGND, while the digital supply is referenced to DGND. Both supplies have a nominal operating value of 1.2 V. Since single-ended amplifiers are sensitive to voltage fluctuations on the supply lines, the charge preamplifier is connected to the AVDD. The threshold discriminator and voltage references are connected to the AVDD and AGND as well. The in-pixel digital logic is connected to the digital supply. The substrate of the transistors is connected to a separate net and merged to the analog ground at the border of the matrix. The SuperPIX0 chip has been fabricated in a six metal level technology. Special attention has been paid to layout the channel with a proper shielding scheme. Two levels of metal have been used to route the analog signals, two for the digital ones and two for distributing the analog and digital supplies. The supply lines, at the same time, shield the analog signals from the digital activity. For nominal bias conditions the power consumption is about 1.5 μW per channel. More details on the design of the analog front-end can be found in the literature [30]. The measured threshold dispersion in the chip is around 490 e- with an average pixel noise of about 60 e- (without the sensor connected). Since the threshold dispersion is a crucial characteristic to be considered in order to meet the required specifications in terms of noise occupancy and efficiency, circuits for threshold fine-adjusting have to be implemented in the next version of the chip. These results have been extracted using the gain measured with an internal calibration circuit, implemented in the pixel, injecting a charge from 0 to 12 fC in each channel preamplifier. An average gain of about 40 mV/fC with a dispersion at the level of 5% has been obtained. The front-end chip has been connected by bump-bonding to a high resistivity pixel sensor matrix of 200 μm thickness. The bump-bonding process has been performed by the Fraunhofer IZM with electroplating of SnAg solder bumps. Measurements on the bump-bonded chip show a working sensor and a good quality of the interconnection at 50 μm pitch. The measured gain and threshold dispersion are compatible with the ones extracted from the front-end chip only. We observe an increase of the noise of around 20%, up to about 76 e-, due to the added capacitive load of the sensor connected.

6.12.2.2 The Apsel DNW MAPS series

DNW MAPS in planar CMOS technology

Deep N-well MAPS were proposed a few years ago as possible candidates for charged particle tracking applications. The Apsel4D chip is a 4096 element prototype MAPS detector with data-driven readout architecture, implementing twofold sparsification at the pixel level and at the chip periphery. In each elementary cell of the MAPS matrix integrated in the Apsel4D chip, a mixed signal circuit is used to read out and process the charge coming from a deep N-well (DNW) detector. This design approach, relying upon the properties of the triple well structures included in modern CMOS processes, has been described in Section 6.12.1.2. In the so called DNW MAPS is integrated with a relatively large (as compared to standard three transistor MAPS) collecting electrode, featuring a buried N-type layer, with a classical read-

out chain for time invariant charge amplification and shaping. In the Apsel4D prototype, the elementary MAPS cells feature a 50 μm pitch and a power dissipation of about 30 μW/channel. The block diagram of the pixel analog front-end electronics is shown in Fig. 6.21. The first block of the processing chain, a charge preamplifier, uses a complementary cascode scheme as its forward gain stage, and is responsible for most of the power consumption in the analog section. The feedback capacitor C_F is continuously reset by an NMOS transistor, biased in the deep subthreshold region through the gate voltage V_f. The preamplifier input device, featuring an aspect ratio $W/L = 14\ \mu m/0.25\mu m$ and a drain current of 20 μA, was optimized for a DNW detector about 900 μm^2 in area and with a capacitance C_D of about 300 fF. The charge preamplifier is followed by a CR-RC, bandpass filtering stage, with open loop gain $T(s)$, featuring a programmable peaking time which can be set to 200 or 400 ns. C_1 is a differentiating capacitor at the CR-RC shaper input, while G_m and C_2 are the transconductance and the capacitance in its feedback network. A discriminator is used to compare the processed signal to a global voltage reference V_t, thereby providing hit/no-hit information to the cell digital section. More details on the design of the analog front-end can be found in the literature [32]. A dedicated readout architecture to perform on-chip data sparsification has been implemented in the Apsel4D prototype. The readout logic provides the timestamp information for the hits. The timestamp, which is necessary to identify the event to which the hit belongs, is generated by the bunch-crossing signal. The key requirements in this development are 1) to minimize logical blocks with PMOS inside the active area, thus preserving the collection efficiency, 2) to reduce to a minimum the number of digital lines crossing the sensor area, in particular its dependence on detector size to allow the readout scalability to larger matrices and to reduce the residual crosstalk effects, and 3) to minimize the pixel dead time by reading hit pixels out of the matrix as soon as possible. With these criteria a readout logic in the periphery of the matrix has been developed, as schematically shown in Fig 6.22. To minimize the number of digital lines crossing the active area the matrix is organized in MacroPixels (MP) with 4x4 pixels. Each MP has only two private lines for point-to-point connection to the peripheral logic: one line is used to comunicate that the MP has got hits, while the second private line is used to freeze the MP until it has been read out. When the matrix has some hits, the columns containing fired MPs are enabled, one at a time, by vertical lines. Common horizontal lines are shared among pixels in the same row to bring data from the pixels to the periphery, where the association with the proper timestamp is performed before sending the formatted data word to the output bus. The chip has been designed with a mixed mode de-

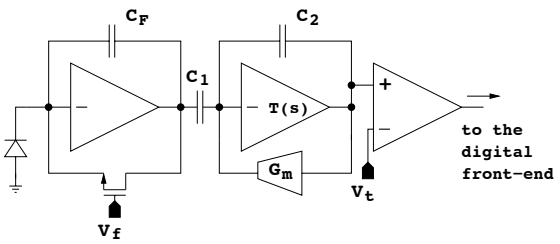

Figure 6.21: block diagram of the analog front-end electronics for the elementary cell of the Apsel4D prototype.

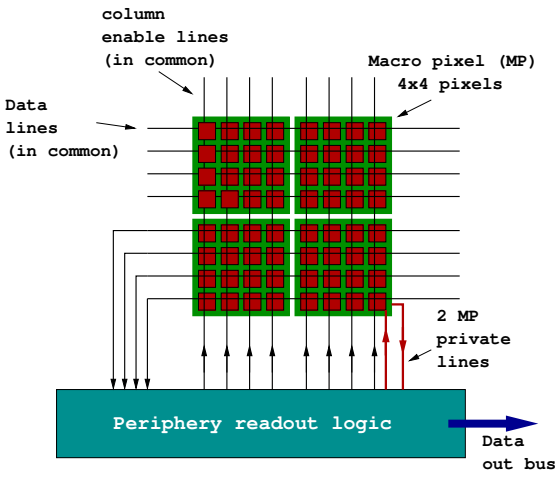

Figure 6.22: schematic concept of the architecture for MAPS matrix readout.

sign approach. While the pixel matrix has a full custom design and layout, the periphery readout architecture has been synthetized in standard cell starting from a VHDL model; automatic place-and-route tools have been used for the layout of the readout logic [27]. The chip has been designed to run with a readout clock up to 100 MHz (20 MHz in test beam), a maximum matrix readout rate of 32 hit pixels/clock cycle and a local buffer of maximum 160 hits to minimize the matrix sweep time. Apsel4D has been successfully tested with 12 GeV/c protons at the PS-T9 beam line at CERN [31]. The efficiency of the DNW MAPS as a function of threshold for two devices with different silicon thickness (Chip 22 is 300 μm thick, while Chip 23 is 100 μm thick) has been measured. Figure 6.23 shows the measured hit efficiency, determined as described in a published work [31]. At the lowest thresholds a maximum efficiency

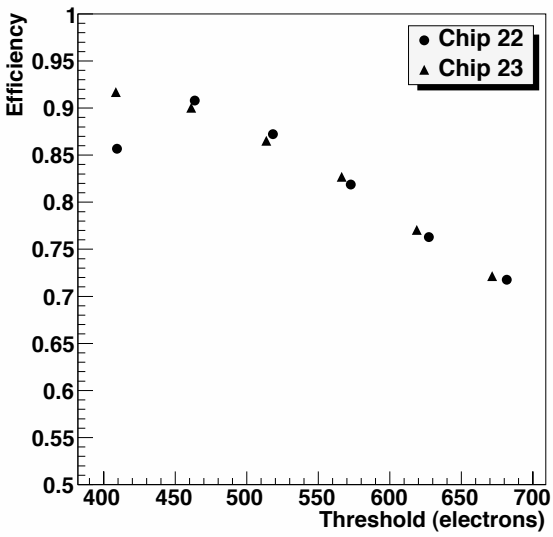

Figure 6.23: efficiency results for two MAPS detectors (the statistical uncertainty on each point is smaller than the size of the plotting symbol).

of approximately 92% and the expected general behavior of decreasing efficiency with increasing threshold can be observed. The noise occupancy for this range of thresholds was found to vary from 2.5×10^{-3} to 1×10^{-6}. The low efficiency observed for Chip 22 at the lowest threshold appears to have been caused by a readout malfunction. Investigations have shown that a small localized area on the detector had very low efficiency, while the rest of the detector behaved normally with good efficiency. Additionally, the efficiency for detecting hits as a function of the track extrapolation point *within a pixel* has been studied. Since the pixel has internal structure, with some areas less sensitive than others, we expect the efficiency to vary as a function of position within the cell. The uncertainty on the track position, including multiple scattering effects is roughly 10 microns, to be compared to the 50 μm pixel dimension. The pixel has been divided into nine square subcells of equal area and the hit efficiency within each sub-cell has been measured. The efficiencies thus obtained are "polluted" in some sense due to the migration of tracks among cells. We obtain the true sub-cell efficiencies by unfolding the raw results, taking into account this migration, which we characterize using a simple simulation. The result can be seen in Figure 6.24, where the efficiency measured in each sub-cell is shown. A significant variation in sensitivity within the pixel area can be observed, as expected. In particular, the central region is seen to be virtually 100% efficient, while the upper part of the pixel, especially the upper right-hand sub-cell, shows lower efficiency due to the presence of competitive n-wells. The position of this pixel map relative to the physical pixel is not fixed. This is a consequence of the alignment, which determines the absolute detector position by minimizing track-hit residuals, as described above. If the pixel area is not uniformly efficient, the pixel center as determined by the alignment will correspond to the barycenter of the pixel efficiency map. Thus, it is not possible to overlay Figure 6.24 on a drawing of the pixel layout, without adding additional information, for example a simulation of internal pixel efficiency. The efficiency as a function of position on the MAPS matrix has also been investigated, since disuniformity could indicate inefficiencies caused by the readout. Generally, a

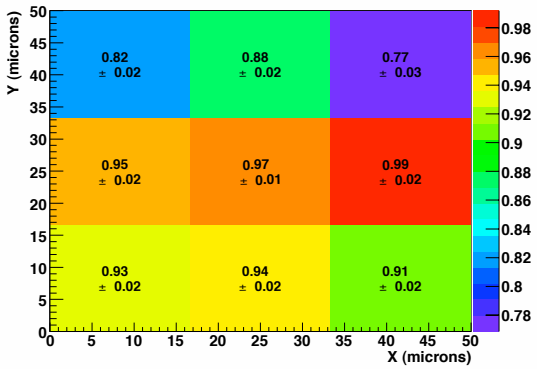

Figure 6.24: hit effiencies measured as a function of position within the pixel (the picture, which is not to scale, represents a single pixel divided into nine sub-cells).

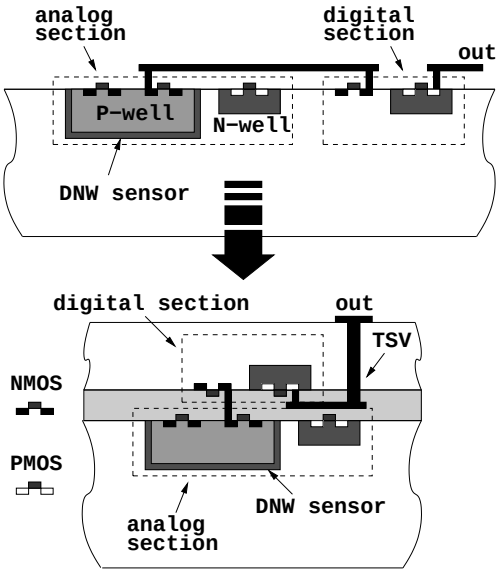

Figure 6.25: cross-sectional view of a DNW CMOS MAPS: from a planar CMOS technology to a 3D process

uniform efficiency across the area of the MAPS matrix was observed. The intrinsic resolution σ_{hit} for the MAPS devices was measured as already described in a published paper [31]. The expected resolution for cases where the hit consists of a single pixel is given by $50/\sqrt{12} = 14.4$ μm, where 50 microns is the pixel dimension.

DNW MAPS in 3D CMOS technology As already mentioned in Section 6.12.1.2, the DNW monolithic sensors have been designed and fabricated also in the Tezzaron/Globalfoundry technology, based on the vertical integration of two 130 nm CMOS layers. The conceptual step from the DNW MAPS in a planar CMOS technology to its vertically integrated version is illustrated in Fig 6.25, showing a cross-sectional view of a 2D MAPS and of its 3D translation. The prototype include two small 3×3 matrices for analog readout and charge collection characterization and a larger one, 8×32 in size, equipped with a digital readout circuit with data sparsification and time stamping features. The pixel pitch is 40 μm. A number of different problems were encountered during fabrication of the first device batch. Among them, the misalignment between the two tiers prevented the analog and digital sections in each pixel cell to communicate to each other [36]. At the time of the TDR writing, other 3D wafers are being processed and devices from the first run are under characterization.

Fig. 6.26 shows the analog front-end channel of the 3D DNW MAPS (quite similar to the analog processor of the SuperPIX0 chip, see Fig. 6.20), simply consisting of a charge preamplifier, whose bandwidth was purposely limited to improve the signal-to-noise ratio (so called shaperless configuration). Equivalent noise charge of between 30 and 40 electrons (in good agreement with circuit simulations)

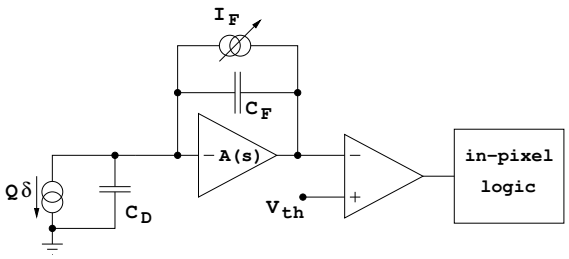

Figure 6.26: block diagram of the analog front-end electronics for the elementary cell of the 3D DNW MAPS of the apsel family.

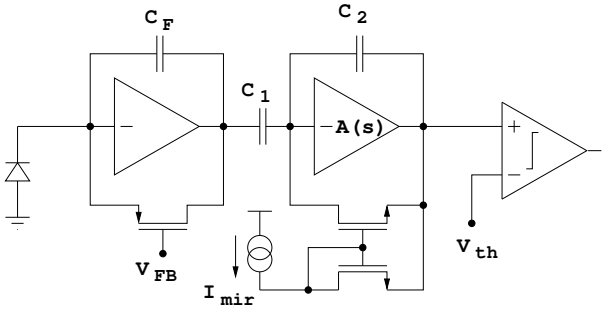

Figure 6.28: block diagram of the analog front-end electronics for the elementary cell of Apsel4well monolithic sensor.

and a charge sensitivity of about 300 mV/fC (a factor of 2 smaller than in simulations) were obtained from prototype characterization. Fig. 6.27 shows the ^{90}Sr spectrum detected by the cluster of 3×3 pixels in a small matrix.

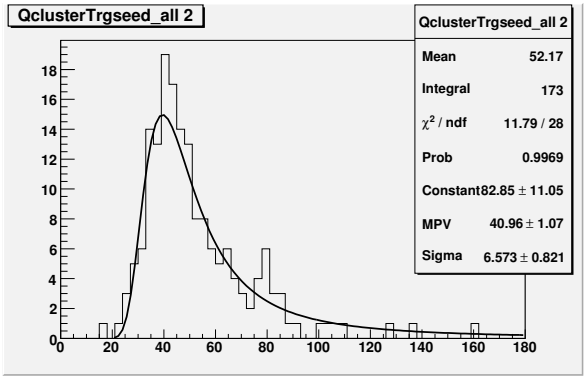

Figure 6.27: spectrum of a ^{90}Sr source detected by a 3×3 matrix of 3D DNW MAPS.

The most probable value of the collected charge is about 100 electrons. Pseudo-3D DNW MAPS (here, the term pseudo-3D refers to devices consisting of just one tier but suitable for 3D integration) have been tested on the PS beam at CERN. Very promising results were obtained in terms of detection efficiency, as displayed in Fig. **??**.

6.12.2.3 The Apsel4well quadruple well monolithic sensor

As already mentioned in section 6.12.1.3, a test chip in the INMAPS, 180 nm CMOS technology, called Apsel4well, has been submitted in August 2011. The chip includes four 3×3 matrices with different number (2 or 4) of the collecting electrodes (each consisting of a 1.5 μm×1.5 μm N-well diffusion), with or without the shielding deep P-well implant, with or without enclosed layout transistors as the input device of the charge preamplifier. The prototype also contains a 32×32 matrix with sparsified digital readout. The test of the first version of the chip, featuring a 5.5 μm thick epitaxial layer with standard resistivity, about 50 Ω·cm) was in progress during the writing of this TDR. Monolithic sensors with a thicker (12 μm) and more resistive (about 1 kΩ·cm) are expected to be out of the foundry by June 2012. Fig. 6.28 shows the analog readout channel of the Apsel4well MAPS. It includes a charge preamplifier, a shaping stage with a current mirror in the feedback network and a two-stage threshold discriminator. Several digital blocks are also integrated in each individual pixel element for data sparsification and time stamping purposes. Time from a peripheral Gray counter is distributed to each pixel in the matrix and is latched to a time stamp register upon arrival of a hit. When a timestamp request is sent to the matrix, a pixel FastOR signal activates if the latched timestamp is the same as the requestd one. The

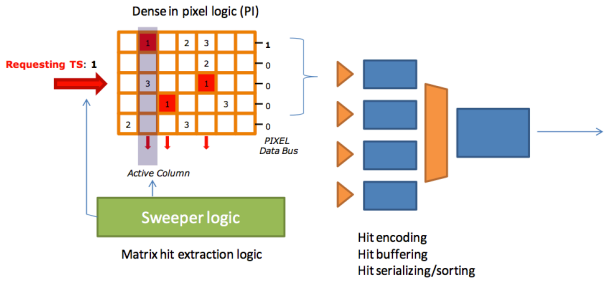

Figure 6.29: conceptual view of the digital readout architecture of the Apsel4well chip operated in the triggered mode.

columns with an active FastOR signal are enabled and read out in a sequence; 1 clock cycle per column is needed. A conceptual view of the digital readout architecture is shown in Fig. 6.29. Readout circuits can be operated either in triggered or in data-push mode. They take care of encoding, buffering and serializing/sorting the hits retrieved from the sensor matrix. In order to achieve the remarkably high readout frequency set by the SuperB experiment, the architecture can be subdivided in a number of modules, each serving a submatrix. This choice improves the scalability features of the readout section and makes it suitable for experiment scale detectors. Efficiency well in excess of 99% have been obtained in Monte Carlo simulations with hit rates of 100 MHz/cm^2. Fig. 6.30 shows the signal at the shaper output as a response to an input charge signal with varying amplitude. Figures provided by the preliminary experimental characterization of the analog section are very close to simulation data, with a gain of about 960 mV/fC and an equivalent noise charge of about 30 electrons. The plot in Fig. 6.31 represents the collected charge in a Apsel4well pixel (5 μm epitaxial layer thickness, standard resistivity) illuminated with an infrared laser source. The position of the collecting electrodes is easily detectable.

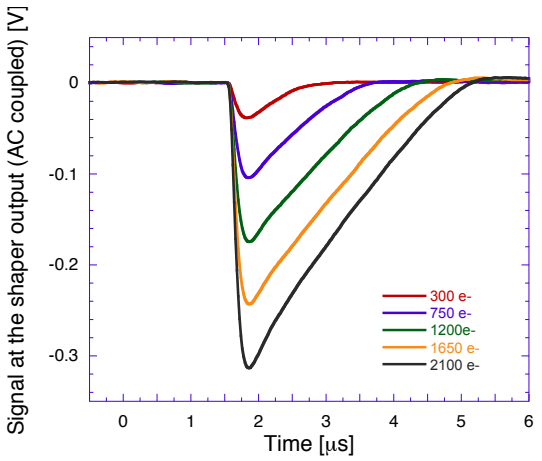

Figure 6.30: signal at the shaper output as a response to an input charge signal with varying amplitude in an Apsel4well sensor.

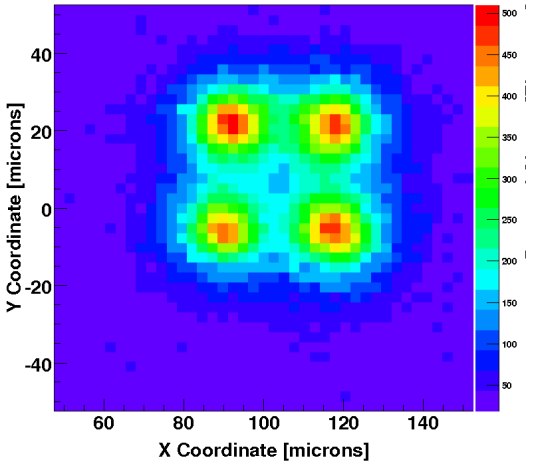

Figure 6.31: collected charge in a Apsel4well pixel illuminated with an infrared laser source.

6.12.3 Radiation tolerance

Hybrid pixels. The high degree of radiation tolerance of modern CMOS technologies, coming as a byproduct of the aggressive scaling down of device minimum feature size, is having a beneficial impact in high energy physics (HEP) applications. Beginning with the 130 nm CMOS processes, which entered the sub-3 nm gate oxide thickness regime, direct tunneling contribution to the gate current has assumed a significant role as compared to trap assisted mechanisms [37]. This may account for the very high degree of radiation hardness featured by devices belonging to the most recent technology nodes, which might benefit from relatively fast annealing of holes trapped in the ultrathin gate oxides. Tolerance to a few hundred of Mrad(SiO_2) has been recently proven in front-end circuits for hybrid pixel detectors [38]. Charge trapping in the thicker shallow trench isolation (STI) oxides is considered as the main residual damage mechanism in 130 nm N-channel MOSFETs exposed to ionizing radiation [39, 40], especially in narrow channel

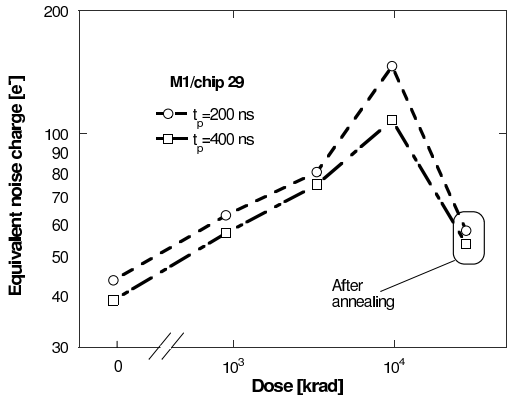

Figure 6.33: equivalent noise charge as a function of the absorbed dose and after the annealing cycle for DNW monolithic sensor. ENC is plotted for the two available peaking times.

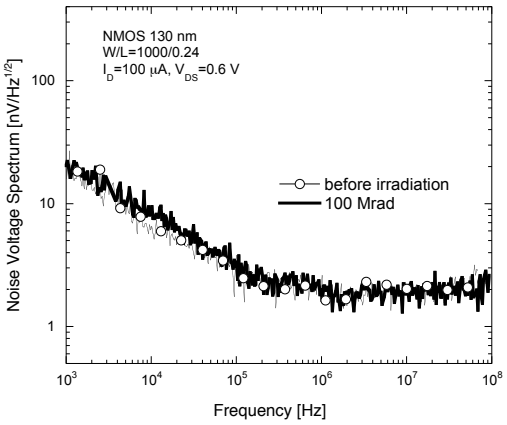

Figure 6.32: noise voltage spectrum for a 130 nm NMOS device with enclosed layout.

transistors [41]. Ionizing radiation was found to affect also the 90 nm and 65 nm CMOS nodes, although to an ever slighter extent, likely due to a decrease in the substrate doping concentration and/or in the STI thickness. As far a as analog front-end design is concerned, ionizing radiation damage mainly results in an increase in low frequency noise, which is more significant in multifinger devices operated at a small current density. This might be a concern in the case of the front-end electronics for hybrid pixel detectors, where the input device of the charge preamplifier is operated at drain currents in the few μA range owing to low power constraints. However, at short peaking times, typically below 100 ns, the effects of the increase in low frequency noise on the readout channel performance is negligible. Also, use of enclosed layout techniques for the design of the preamplifier input transistor (and of devices in other critical parts of the front-end) minimizes the device sensitivity to radiation [42]. For this purpose, Fig. 6.32 shows the noise voltage spectrum for a 130 nm NMOS transistor with enclosed layout, featuring no significant changes after irradiation with a 100 Mrad(SiO_2) total ionizing dose. On the other hand, CMOS technologies are virtually insensitive to bulk damage, since MOSFET transistor operation is based on the drift of majority carriers in a surface channel.

DNW CMOS MAPS DNW MAPS have been thoroughly characterized from the standpoint of radiation hardness to evaluate their limitations in harsh radiation environments. In particular, the effects of ionizing radiation, with total doses of about 10 Mrad(SiO_2), have been investigated by exposing DNW MAPS sensors to a ^{60}Co source [43]. In that case, some performance degradation was detected in the noise and gain of the front-end electronics and in the sensor leakage current, while no significant change was observed as far as the charge collection properties are concerned. Fig. 6.33 shows the equivalent noise charge as a function of the absorbed dose and after the annealing cycle for a DNW monolithic sensor. The significant change can be ascribed to the increase in the flicker noise of the preamplifier input device as a consequence of parasitic lateral transistors being turned on by positive charge buildup in the shallow trench isolation oxides and contributing to the overall noise. Use of an enclosed layout approach is expected to significantly reduce the effect of ionizing radiation. Fig. 6.34 shows event count rate for a DNW monolithic sensor exposed to a ^{55}Fe source before irradiation, after exposure to γ-rays and after the annealing cycle. As the absorbed dose increases, the 5.9

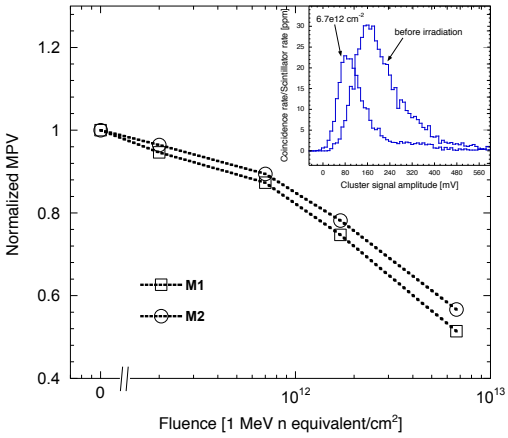

Figure 6.35: most probable value (MPV) of the ^{90}Sr spectra (shown in the inset for one of the tested chips before irradiation and after exposure to a 6.7×10^{12} cm^{-2} neutron fluence) normalized to the pre-irradiation value as a function of the fluence for DNW MAPS with different sensor layout.

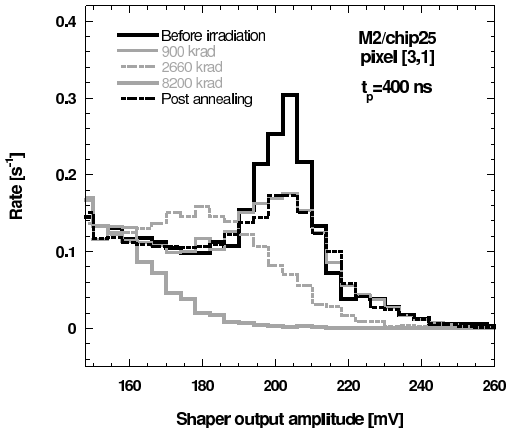

Figure 6.34: event count rate for a DNW monolithic sensor exposed to a ^{55}Fe source before irradiation, after exposure to γ-rays and after the annealing cycle.

keV peak gets broader as a consequence of the noise increase (in fair agreement with data in Fig. 6.33. At the same time, the peak is shifted towards lower amplitude values, as a result of a decrease in the front-end charge sensitivity also due to charge build up in the STI of some critical devices. DNW MAPS of the same kind have also been irradiated with neutrons from a Triga MARK II nuclear reactor to test bulk damage effects [44]. The final fluence, 6.7×10^{12} 1 MeV neutron equivalent/cm^2, was reached after a few, intermediate steps. The devices under test (DUT) were characterized by means of several different techniques, including charge injection at the front-end input through an external pulser, sensor stimulation with an infrared laser and spectral measurements with ^{55}Fe and ^{90}Sr radioactive sources. Neutron irradiation was found to have no sizable effects on the front-end electronics performance. This can be reasonably expected from CMOS devices, whose operation is based on the drift of majority carriers in a surface channel, resulting in a high degree of tolerance to bulk damage. Exposure to neutrons was instead found to affect mainly the charge collection properties of the sensors with a reduction in the order of 50% at the maximum integrated fluence. Fig. 6.35 shows the most probable value (MPV) of the ^{90}Sr spectra normalized to the pre-irradiation value as a function of the fluence for DNW MAPS with different sensor layout. A substantial decrease can be observed, to be ascribed to a degradation in the minority carrier lifetime. A higher degree of tolerance was instead demonstrated in monolithic sensors with high resisitivity (1 kΩ cm) epitaxial layer [46]. Actually, doping concentration plays a role in determining the equilibrium Fermi level, which in turn influences the effectiveness of neutron-induced defects as recombination centers [45].

6.13 Services, Utilities and E.S. & H issues - 8 pages

6.13.1 Service and Utilities

- Data and control lines
- Power
- Cooling water

- Dry air or nitrogen

6.13.2 ES&H Issue

Bibliography

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