P - SuperB

Programma di attività e preventivo di spesa 2013

Sezione di Pavia

11 luglio 2012

Gruppo P-SUPERB Pavia

Responsabile: Valerio Re

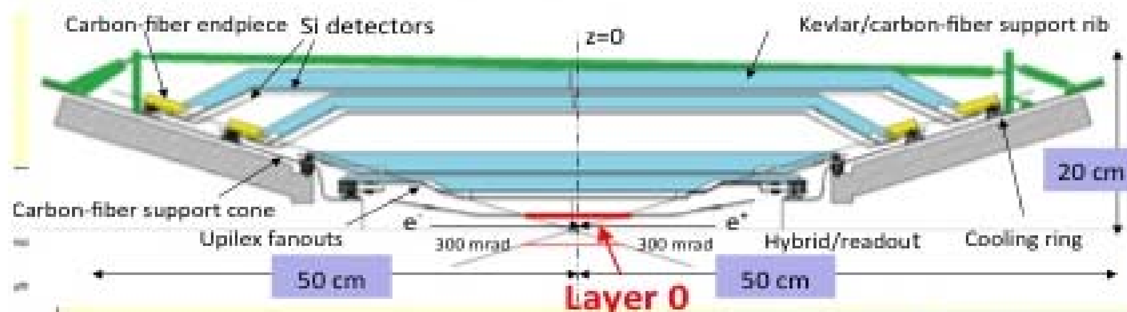
- Università di Pavia
- Università di Bergamo

Attività principali

- Sviluppo di MAPS (Monolithic Active Pixel Sensors) CMOS per il Layer 0 di SVT
- Chip di lettura rivelatori a strip di SVT, opzione a pixel ibridi per Layer 0

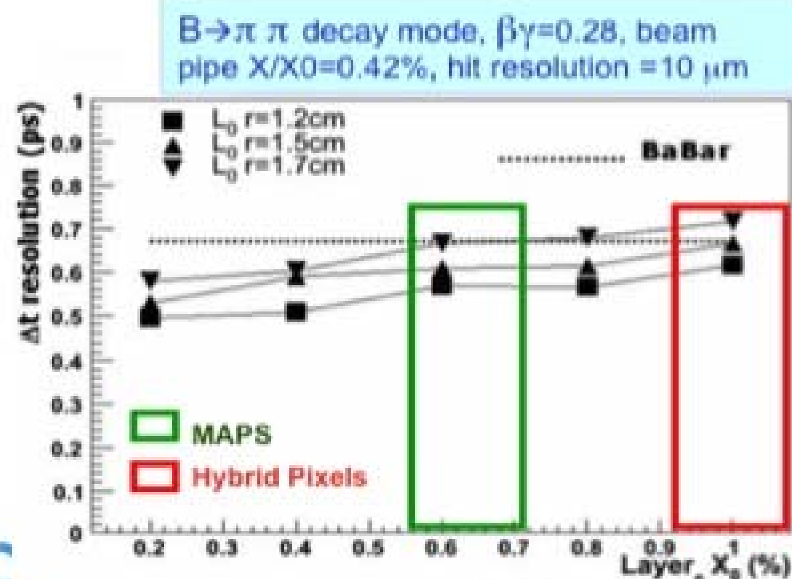
The SuperB Silicon Vertex Tracker

The SVT provides precise tracking and vertex reconstruction, crucial for time dependent measurements.



BaBar SVT

- 5 Layers of double-sided Si strip sensor
- Low-mass design. (P_t < 2.7 GeV)
- Stand-alone tracking for slow particles.
- 97% reconstruction efficiency
- Resolution ~15μm at normal incidence



SuperB SVT based on Babar SVT design for R>3cm. BUT:

1) reduced beam energy asymmetry (7x4 GeV vs. 9x3.1 GeV) requires an improved vertex resolution (~factor 2)

- Layer0 very close to IP (@1.5 cm) with low material budget (<1% X_0) and fine granularity (50 μm pitch)
- Layer0 area 100 cm²

2) bkg levels depend steeply on radius

- Layer0 needs to be fast and rad hard
  hit rate 20 MHz/cm², TID 3 MRad/yr, eq. neutron fluence 5 x 10^{12} n/cm²/yr
  x5 safety factor to be inlcuded!

Front-end for striplets/strips

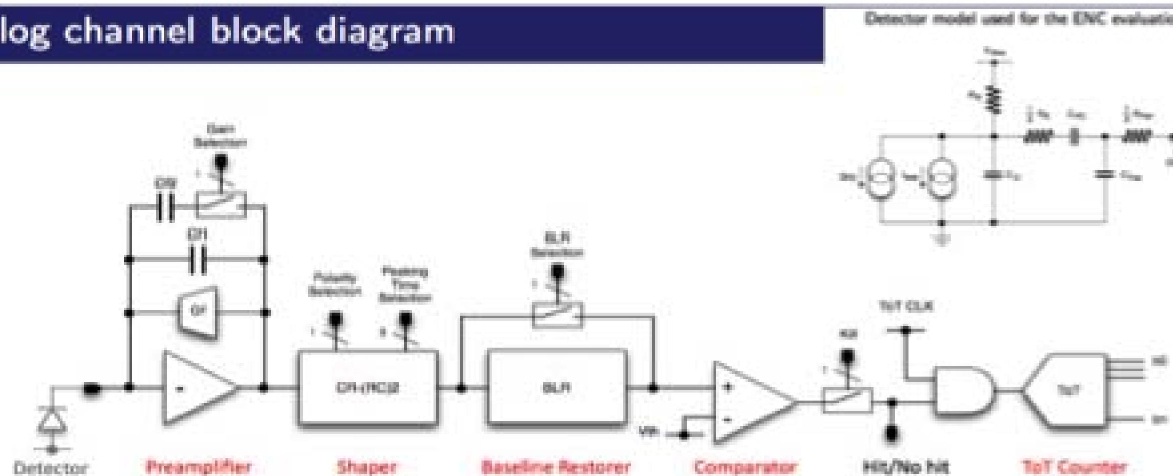
- Striplets (layer 0) and strips (layer 1 to 5) are the baseline option for the SuperB vertex detector
- Very hard (if possible at all) to cope with such a large span of detector capacitances (from 10 pF in the innermost to 70 pF in the outermost layer) and hit rate values (from 1 MHz/strip to 20 kHz/strip) with a single design
- Proposed solution
  - fast readout (25 ns to 200 ns peaking time) for low capacitance/high hit rate layers (0 to 3)
  - slow readout (from 400 ns to 750 ns peaking time) for high capacitance/low hit rate layers (4 and 5)

  Work is in progress to achieve an analog front-end design that is able to comply with all these requirements in a single chip)
- Amplitude information available through local A/D conversion with time over threshold techniques
- Digital readout architecture virtually the same for both readout channels (pipeline depth requirements are less severe for the slow front-end)

FE chip for Striplets/Strip (Analog) PV/MI

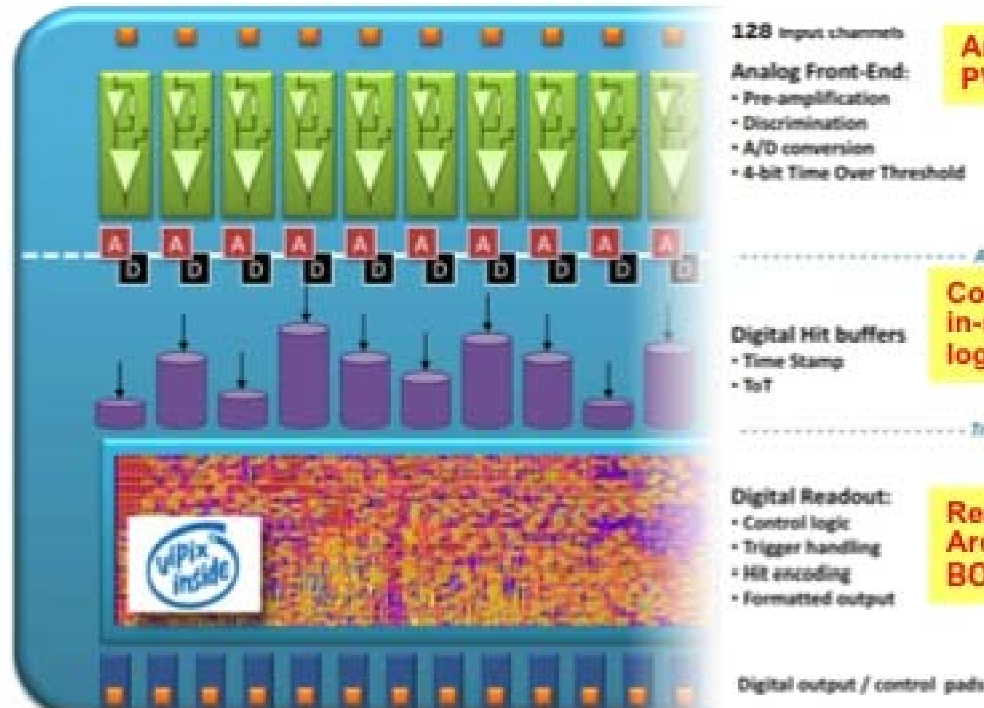
- Analog FE simulation well advanced:
- Analog front-end for fast and slow channels simulated
  - the shaping time flexibility [25;200, 400-1000]ns will allow a S/N optimization in the actual background conditions. An example in this table→
- Inefficiency due to pile up evaluated (analog dead time) with nominal & x5 background
- Hit time resolution simulated (important to reduce offline time window and related background occupancy)

Layer	View	Shaping time	S/N at the start of data taking	S/N in 75 ab-1	S/N in 75 ab-1 x5 bkg
0	1	25	18	18	17
0	2	25	18	18	17
1	phi	75	22	21	18
1	z	75	34	30	21
2	phi	100	22	21	18
2	z	100	36	31	21
3	phi	150	28	23	16
3	z	150	36	29	19
4	phi	500	22	19	13
4	z	500	29	23	14
5	phi	1000	22	20	15
5	z	1000	30	26	18



The Strip/Striplet front-end Chip Diagram

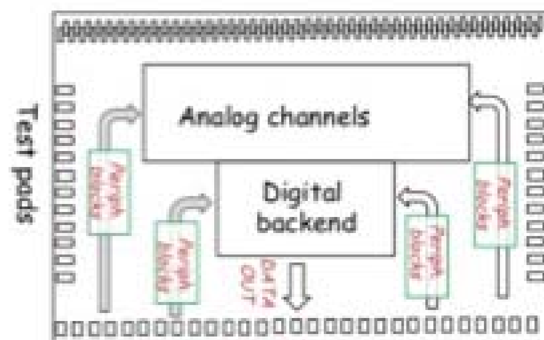
Responsability



Analog PV/MI

Control in-strip logic - PI

Readout Architecture - BO



Auxiliary blocks (PV/MI/BO/PI+ Valencia) + some blocks developed from CERN IBM 130 nm

- First meeting with S. Marchioro in June.

Milestones for FE chip development

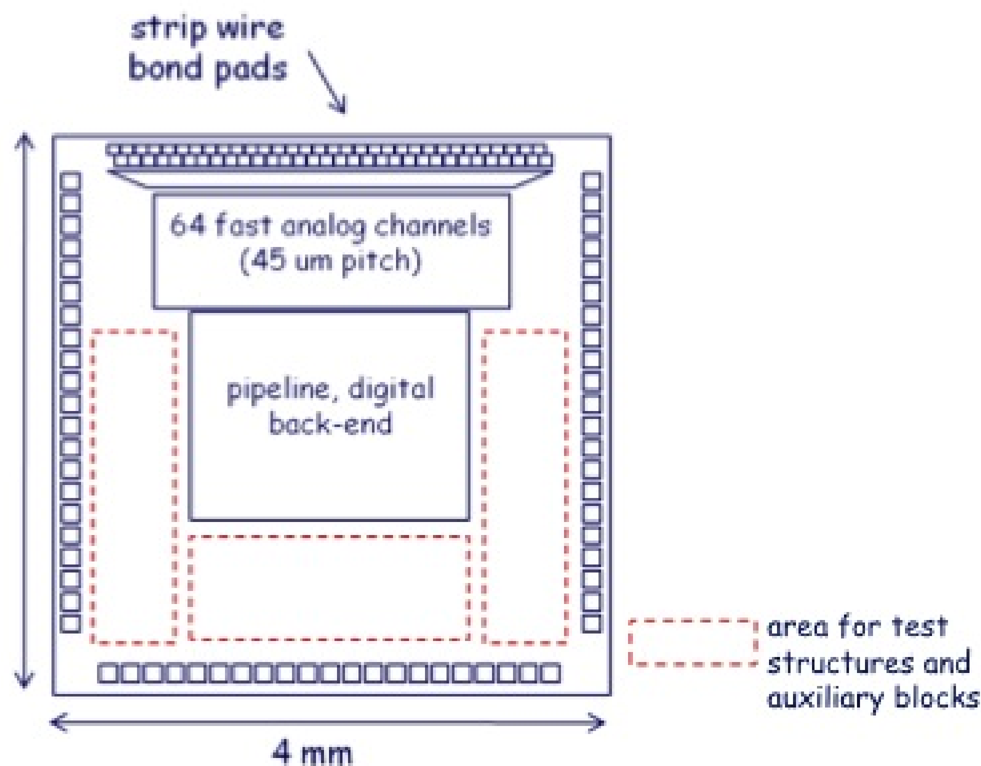
- 4Q 2012: first test structures, 64 channels (fast and slow front-end), auxiliary blocks
- 4Q 2013: first fully operational prototype chip - 128 channels (fast and slow readout) + test structures
- 4Q 2014: production run
- Account for some contingency after the first or the second step

- LAYOUT of the first FE chip prototype (64 ch fast and slow + auxiliary blocks) is starting (IBM 130 nm). Submission Nov. 2012 with funding 2012 (45 kE – sblocco sj PV)

G. Rizzo

Strip front-end development

- Fast and slow front-end prototype chip (IBM 130 nm)



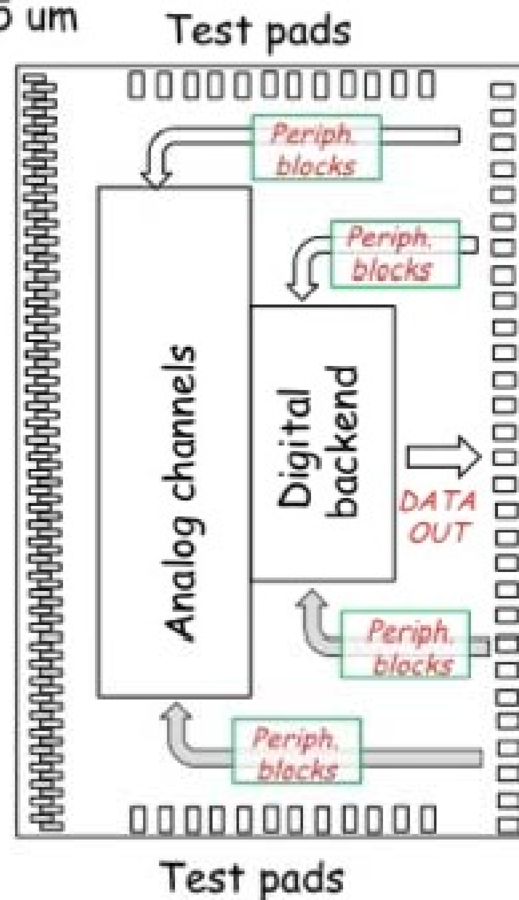
- Milestones for strip front-end development
  - 4Q 2012: first test structures, 64 channels (fast and slow front-end), auxiliary blocks
  - 4Q 2013: first fully operational prototype chip – 128 channels (fast and slow readout)
  - 4Q 2014: production run
  - Account for some contingency after the first or the second step

- About 2000 128-channel chips are needed to read out the SuperB SVT

Mechanical Requirements:
Number of channels per chip: 128
Chip size: width ≤ 6 mm, length ≤ 4 mm
Pitch of input bonding pads: < 45 um

Separate analog and digital supply pads
AVDD, DVDD: 1.5 V
Shunt LDO regulators to provide 1.2V to analog and digital circuits
(from other projects, e.g. FE-I4, as for other peripheral blocks)

Input bonding pads (to strips)



I/O bonding pads: AVDD, AGND, DVDD, DGND (how many pads for voltage supplies?)
Input clocks
Serial input and output for slow control
Output lines

Strip front-end prototype

- Past experience with the design of the microstrip front-end electronics for the BaBar and BTeV experiments
  - AToM chip (BaBar): first test structure included 64 channels with 50 μm pitch
  - FSSR chip (BTeV): first test structure included 114 channels (covering the area of 128 channels with 50 μm pitch, the area of the 14 missing channels being used for the probing pads of individual channels)
- 64 channels (50 μm pitch or less) in a single or two separate test chip are needed to fully understand power distribution problems
- Supplementary area for the test of auxiliary blocks (DC-DC converters, LDO regulators, LVDS or SLVS transceivers, voltage references)
- Design to be submitted in the IBM 130 nm CMOS technology - several groups are working with this process, some building blocks and auxiliary electronics may be already available from CERN design team

SVT Attivita' 2013

- Dopo il TDR entriamo in fase di costruzione.

Construction phases (from BaBar experience)

- Design & prototype: 2013 baseline,
  - 2013 R&D on pixels for L0 upgrade: technology choice in 2013-2014?
- Procure and Fabricate (+test) (2014-15)
  - 2015-2016 for pixel upgrade
- Module Assembly & Det. Assembly (2016-17)
  - 2017 for pixel upgrade
- Commissioning 2017-2018
  - 2019 possible installation of pixel

- Per la baseline e' necessario costruire alcuni prototipi nel 2013 per finalizzare il design dell'intero rivelatore ed entrare in produzione con i vari componenti nel 2014
- Per i pixel del Layer0 nel 2013 continua R&D sulle varie opzioni per arrivare alla decisione sulla tecnologia nel 2013-14
- Sottomissione INMAPS su grandi dimensioni si rimanda al 2014.

Attivita' 2013 per Layer 0 a pixel

- R&D sui pixel

- Continua attivita' sui vari fronti (INMAPS, pixel ibridi) ma senza richieste finanziarie importanti
- Nuova sottomissione INMAPS nel 2014 dopo risultati completi I chip+irraggiamento+testbeam2012.

Pixels: Evolution of DNW MAPS and Testbeam

APSEL4D – DNW MAPS

Charge collection efficiency main limitation of DNW MAPS for application in Layer0:

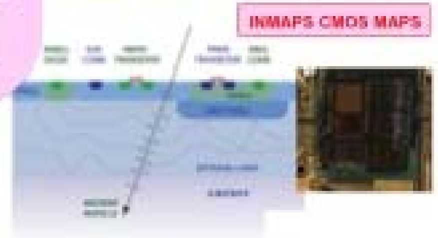
- Area of competive Nwell increses with more complex in-pixel logic (fast readout needed)
- Charge collection further reduced by radiation damage

Two approaches to improve MAPS performance

- **3D MAPS with wertical integration:**
  - 2 tiers for sensor&analog + digital)
  - fill factor and efficiency can improves significantly even introducing more in-pixel logic
- **2D MAPS with INMAPS 180 nm process**
  - 4th well (deep Pwell), below competitive Nwells, used to avoid parassitic charge collection
  - high resistivity epitaxial layer also available for improved charge collection and radiation hardness!

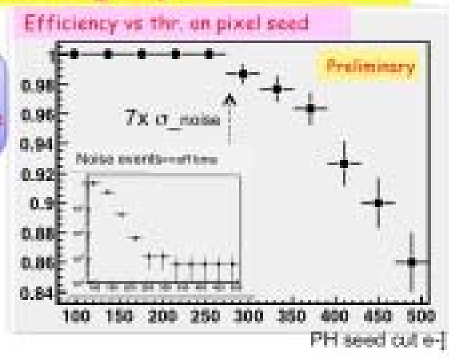
3D CMOS MAPS

INMAPS CMOS MAPS



Beam test @ CERN on 3D MAPS analog layer

Efficiency > 98% thanks to reduced PMOS N-wells in the pixel cell with 3D

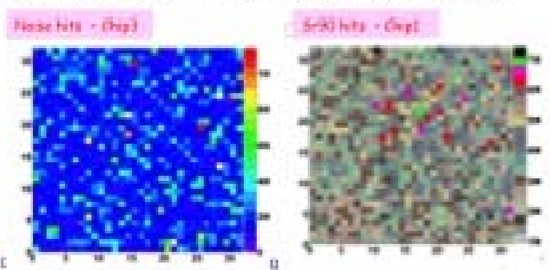


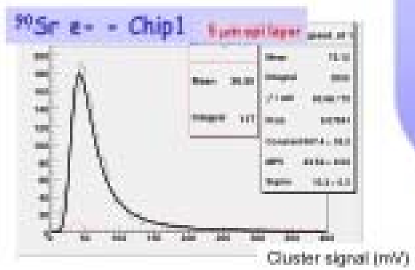
Noise events==off time window (w.r.t. scintillator)

R&D on pixel: first results on new MAPS with INMAPS process: very promising option for thin pixel upgrade for Layer0.

- Noise and gain measured in good agreement with simulation:
  - ENC = 30 e- (~20% dispersion)
  - Gain=920 mV/fC (~10% dispersion)
- Standard functionality of new readout architecture verified in the two operation modes available on chip: data push & triggered.

- Few dead pixels: ~ 0.3% (on 3 chips 32x32)





Attività prevista (II semestre 2012/I e II semestre 2013)

- Test di radiation hardness su MAPS a quadrupla well su alta resistività
- Progetto e sottomissione front-end per striplet/strip e blocchi ausiliari
- Test prototipi in tecnologia a integrazione 3D

II semestre 2012

- Test primo prototipo front-end per strip e blocchi ausiliari
- Avvio progetto secondo prototipo front-end per strip

I semestre 2013

- Sottomissione secondo prototipo front-end per striplet/strip
- R&D su sensori CMOS e pixel ibridi

II semestre 2013

Fondi sottomissione primo prototipo chip strip IBM 130nm

- Chiederemo a settembre lo sblocco dei 45 kEuro assegnati sub judice per il primo chip prototipo di circa 15 mm^2 (costo tecnologia IBM 130 nm tramite CERN: 3 kEuro/mm^2)

Fondi sottomissione secondo prototipo chip strip IBM 130nm

- Per fine 2013, abbiamo in programma la sottomissione di un prototipo "full-size" del chip di lettura delle strip

- Richiesta su costruzione apparati di 29 mm^2 in CMOS 130nm IBM:

  24 mm^2 per chip a 128 canali (full size and functionality)

  5 mm^2 per consentire un test approfondito delle soluzioni progettuali che consentono di unificare in unico chip le prestazioni richieste da tutti i Layer 0-5 di SuperB

- E' necessario rafforzare i contatti con il gruppo del CERN (missioni estere), grazie al quale avremmo accesso a blocchi elettronici di servizio già sviluppati per altri chip (DAC, regolatori di tensione, I/O pads, ecc.)

Preventivo di spesa 2013 Pavia

Missioni interne	Contatti sviluppi chip e test prototipi (Milano, Bologna, Pisa)	3 kEuro
	3 meeting SuperB in Italia * 5 persone	12 kEuro
Missioni all'estero	Trasferte a CERN per sviluppo chip di front-end strip (4 mesi uomo)	10 kEuro
	1 meeting SuperB all'estero * 5 persone	7.5 kEuro
Consumo	Sviluppo di fast front-end e slow front-end per striplets/strips, 1 chip 128 ch. + 1 chip strutture di test per unificare canali lenti e veloci (24+5 mm2 x 3kE/mm2)	87 kEuro
	Realizzazione di PCB per test prototipi chip, componenti elettronici, picoprobe tips	5 kEuro
	Metabolismo	7 kEuro
	TOTALE	131.5 kEuro

Personale impegnato nel progetto

NOME e COGNOME	Qualifica	Gruppo di afferenza	Percentuale
RICERCATORI			
Valerio Re (responsabile locale)	PO		50%
TECNOLOGI			
Luigi Gaioni	Assegnista		100%
Alessia Manazza	Dottorando		20%
Massimo Manghisoni	RU		80%
Lodovico Ratti	RU		50%
Gianluca Traversi	RU		30%
Stefano Zucca	Assegnista		100%
NUMERO TOTALE DI RICERCATORI		1 (0.5 FTE)	
NUMERO TOTALE DI TECNOLOGI		6 (3.8 FTE)	
PERSONALE FULL TIME EQUIVALENT		4.3	