

ATLAS

F. Tartarelli

CdS, 05/07/2012

ATLAS Milano

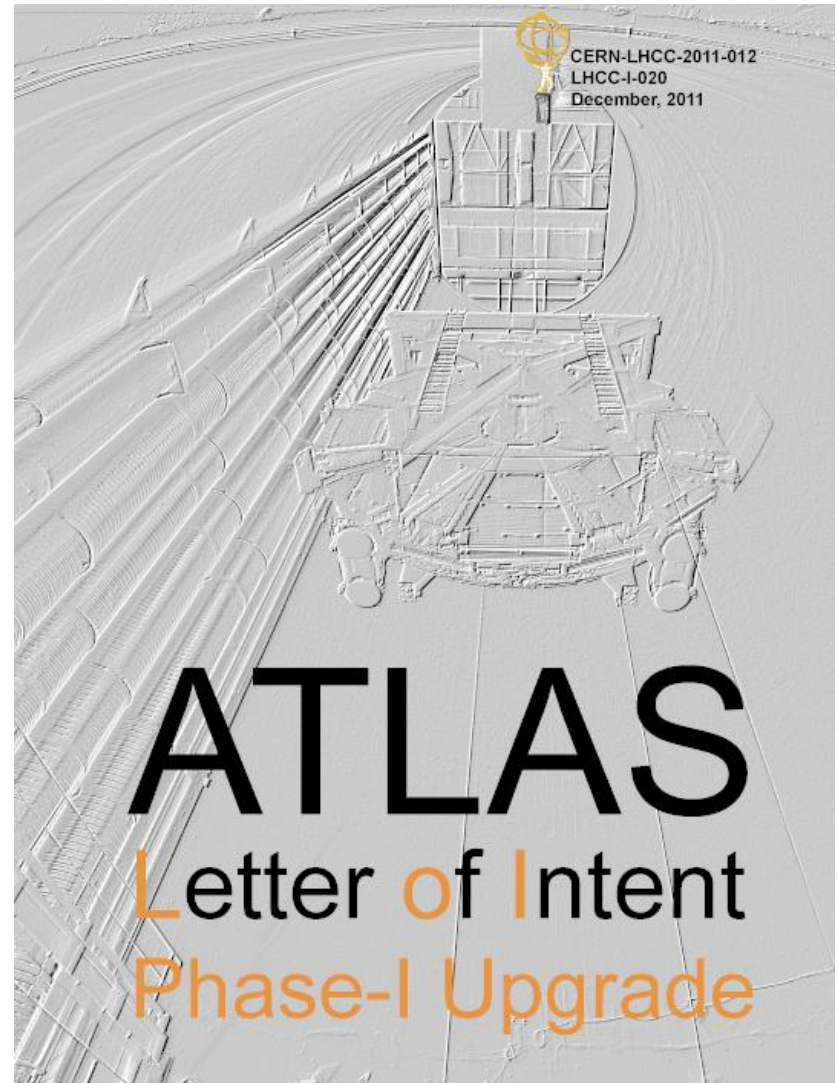
- Extraordinary ATLAS physics results thanks to great effort of the Collaboration in:
 - Detector performance, maintenance, running, operation, shifts, performance, simulation, physics analysis
- Large Milano involvement in many aspects:
 - Calo, ID, Computing CR shifts
 - Pixel on-call, Pixel DQ, Lar HW on-call, LAR HV sw/DCS, offline DQ
 - Tracking, pixel reco, vertexing performance
 - Egamma calibration and performance
 - MET performance, TES calibration (Z- \rightarrow $\tau\tau$)
 - Higgs and SUSY analyses

ATLAS Milano

- As of **today 29 people (25.9 FTE)**:
 - 5 PhD students
 - 3 post-doc
 - 6 tecnologiLaureandi: 6 triennali + 6 magistrali negli ultimi 12 mesi
- **Several responsibilities:**
 - A. Andrezza: tracking CP convenor (till October)
 - C. Troncon: ID SC chair, SCAB deputy chair
 - L. Carminati: co-convenor egamma calibration, D3PD production
 - S. Resconi: MET convenor, sw coordinator MET
 - D. Giugni: NSQP
 - F. Tartarelli: Lar HV software and DCS
 - M. Citterio: sLAR electronic upgrade co-convenor, FTK AMboard
 - V. Liberali: FTK Amchip
 - C. Meroni: coordinatore upgrade ATLAS-Italia (fino a Dicembre 2012)
 - ...

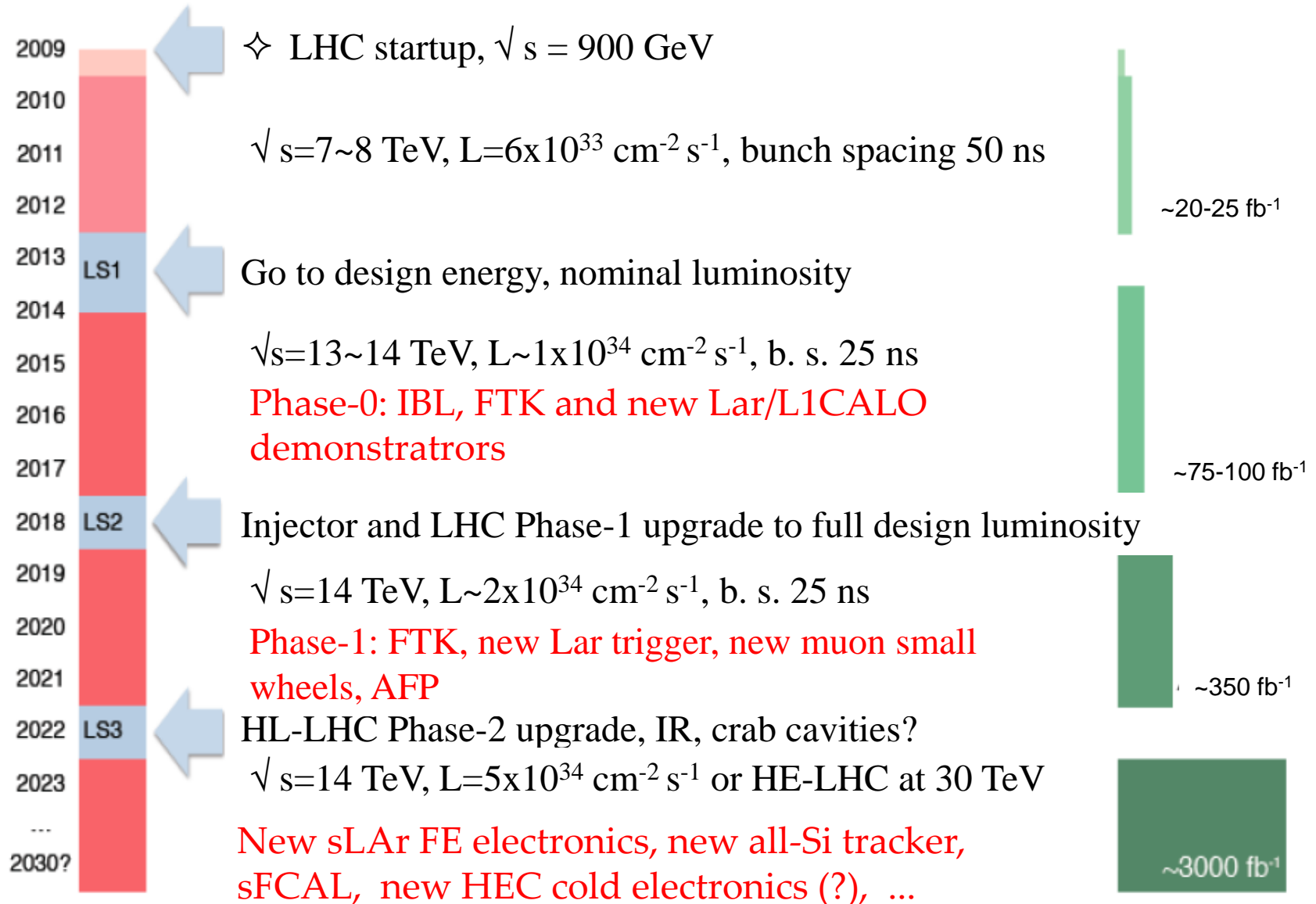
Upgrade

- The Collaboration has already started a large upgrade program:
 - Consolidate and improve the physics capabilities of the detector
 - Cope with the planned LHC luminosity increases
- Important recent events
 - Sign of the IBL MOU
 - Preparation of the ATLAS Letter of Intent for the Phase-I upgrade



LHC Schedule Assumptions

<https://indico.cern.ch/getFile.py/access?contribId=31&sessionId=5&resId=1&materialId=slides&confId=164089>



LHC schedule change

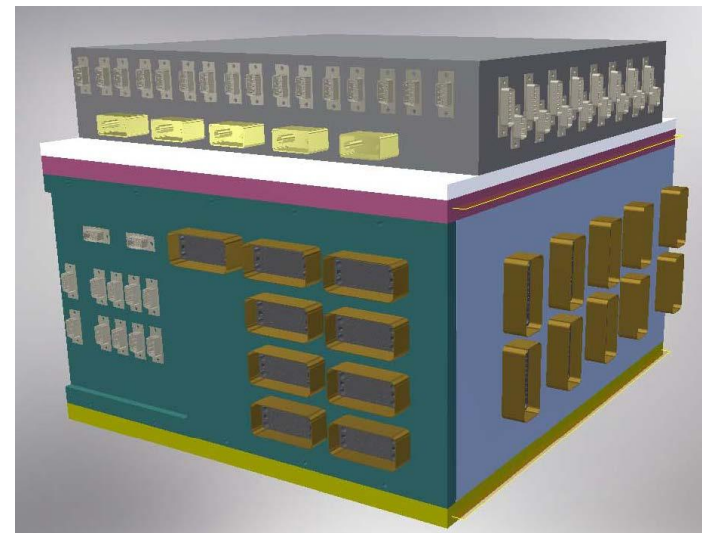
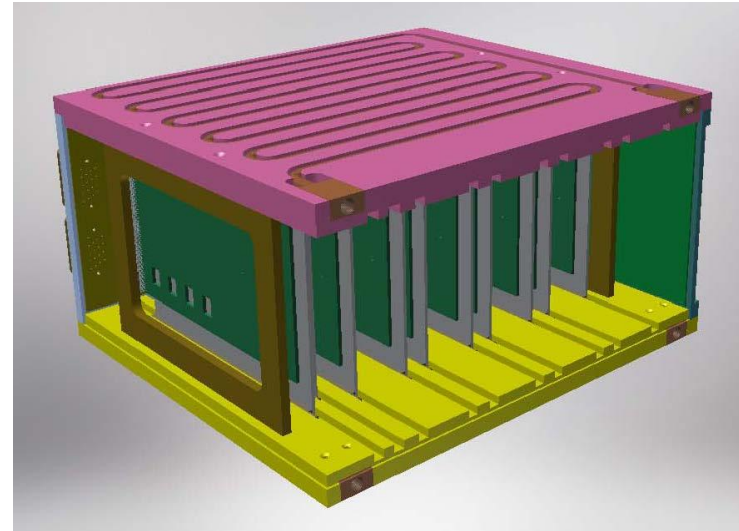
- Latest news: **run extension in 2013**
 - pp physics up to December 15, 2012
 - Xmas shutdown
 - p-Pb run in February (4 weeks)
 - MD in March
 - **LHC shutdown beginning of April**

Milano Upgrade activities

- On-going activities: approved by ATLAS and INFN
 - IBL: Insertable B-Layer
 - FTK: Fast Tracker
- New activities: under approval
 - Upgrade of LAr calo system trigger at LVL1
 - AFP (ATLAS Forward Proton)

IBL

- Insertable B-Layer (IBL): 4th layer of pixel to be installed during LS1 (~Sep 2013) for operation in Phase-0
- Two installation scenarios (still to be decided):
 - Installation in the pit
 - On surface (extracting pixel and replacing SQP -> nSQP)
- Milano is responsible for the production of the LV regulation stations (PP2):
 - Evolution of the design done for the pixels PP2

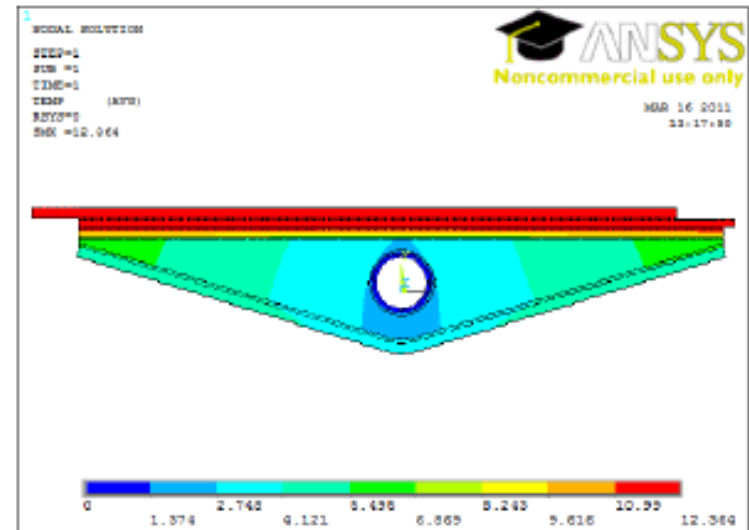


IBL

- We have to produce, test and deliver:
 - 8 crates (4 for IBL, 2 for surface tests, 2 spares)
 - Relative boards (controller, LV boards, VVDC boards)
- In case of nSQP installation we will also produce (paid by CERN):
 - 2 + 2 additional crates
 - 30 LV boards

Other IBL activities

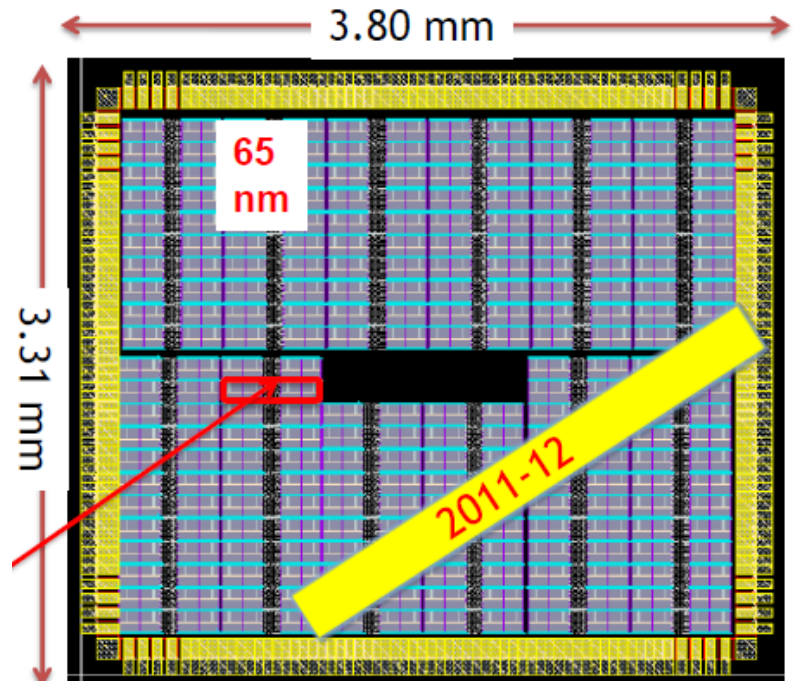
- FEM analysis of stave deformations and thermal performance + measurement of the stave deformations induced by cooling
- Reassembly of the Integration and Testing Tool (ITT) at CERN (scope depends on decision on installation scenario)



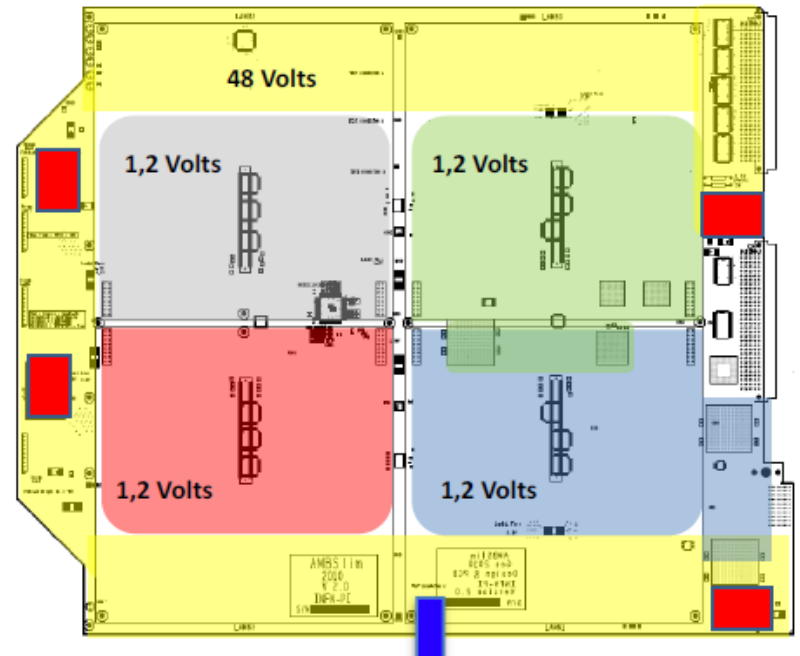
Picture 22 - IBL-Stave pipe I.D. 1.5 mm opt.1 (3 plies)



FTK



- Highly parallel hardware track trigger at LVL2 using information from Pix+Si hits:
 - Works up to $3 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$, sustaining a 100 kHz LVL1 rate with 100 μs max latency per event
- At the heart of the system is a dedicated custom AM (Associative memory) ASICs for pattern matching:
 - Additional logic provided via a series of FPGA
- System arranged in several AMBFTK boards (+AUX board); each board contains 4 mezzanine boards (LAMB) in turn containing 32 AM chip each



FTK

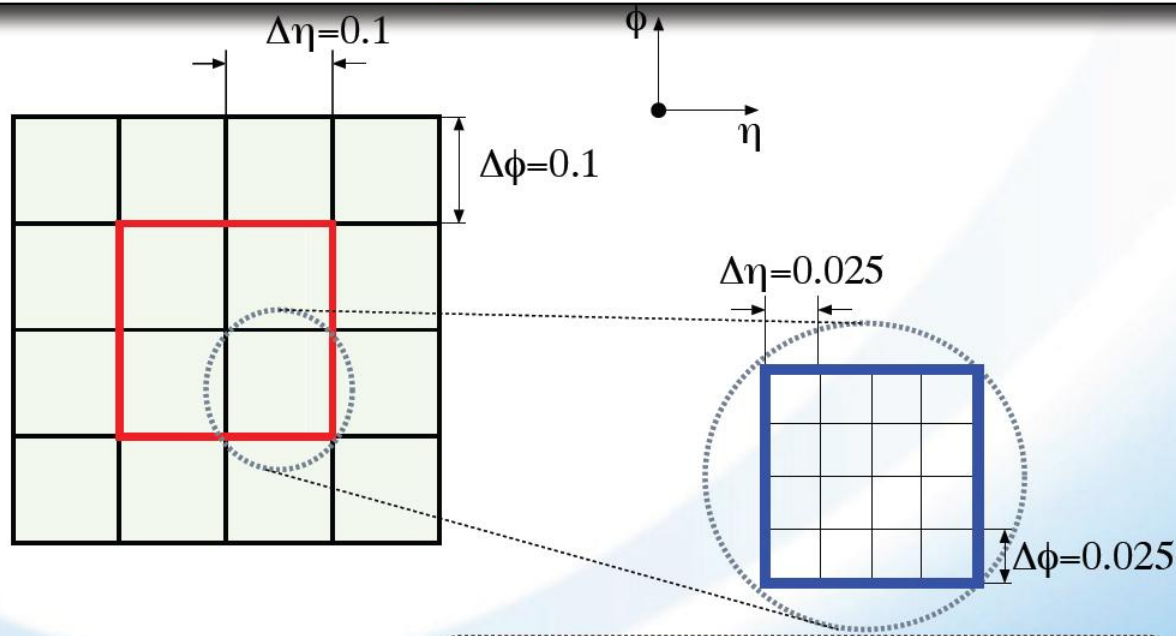
- FTK plans include:
 - VS (Vertical Slice) covering a small η - ϕ region to test integration with TDAQ, RT performance with data and test bed for prototype boards
 - Demonstrator: covering 2 45° wedges in barrel for installation during LS1 in 2014 for Phase-0
 - Full system for Phase-1
- Milano is involved in the AMBoard design, layout, FPGA FW and in the design and testing of the AM chip:
 - AMBFTK board produced: will be soon available for test
 - AMchip04 in 2012: 14 mm² chip in 68 nm technology with 8192 patterns. Under test now
 - AMchip05 in 2012: x2 patterns and serial in/out as a further step towards final chip (x10 patterns)

sLAr

- LAr in Phase 1
- Modify LVL1 L1CALO trigger in order to be able to cope to higher lumi without increasing the pT thresholds
- Increase tower granularity (within the current FE electronics framework) in order to be able to compute lateral and longitudinal shower shapes in each sampling of the calorimeter
 - => possibility to implement new shower shape algorithms to reject jet background

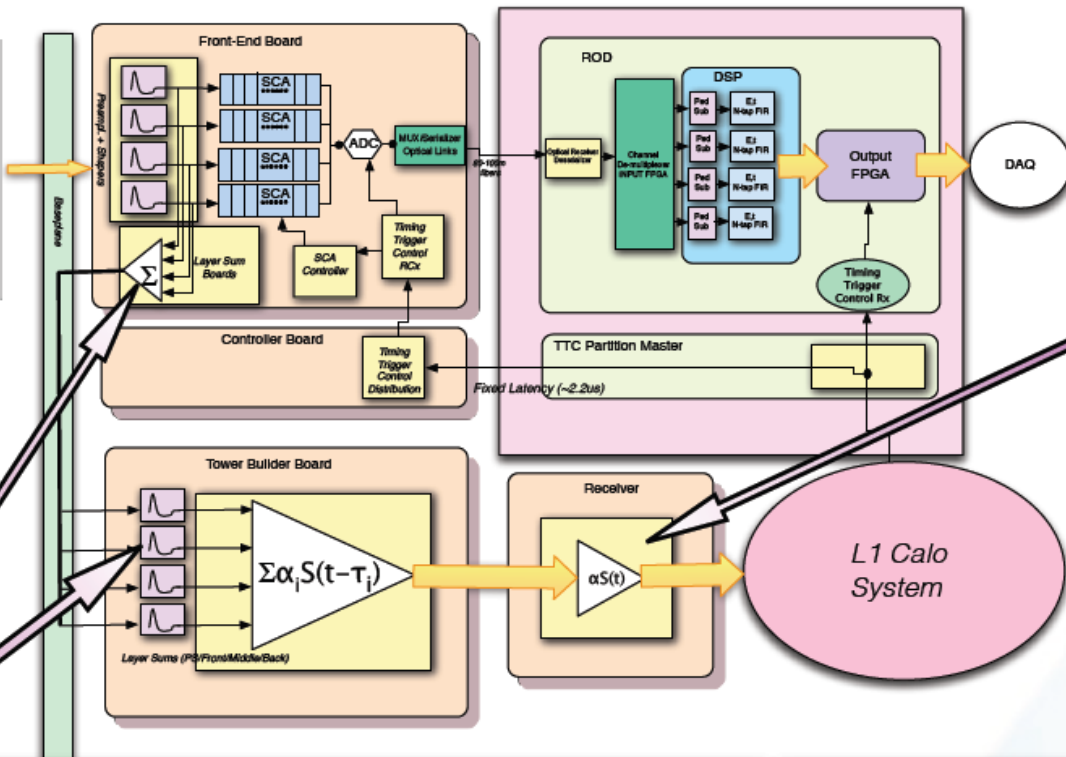
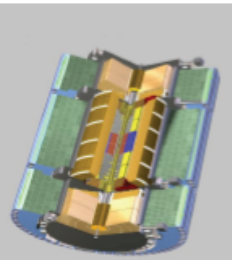
Current and Proposed Solution

- **Goal: Preserve un-prescaled Level-1 thresholds for single electron triggers at $p_T \sim 25$ GeV for LHC operation beyond the nominal design (Phase-I LHC and HL-LHC)**
 - ▶ Finer granularity readout (of the trigger path) allow for the implementation of algorithms based on the features of the EM shower lateral and longitudinal development
 - ◆ Super-Cells formed in the Front-End shaper sum ASIC and individually digitized
 - ▶ and ultimately improve rejection against jets faking electrons, allowing to lower thresholds for the same trigger rate



In the 2nd layer of the EM calorimeter a single trigger tower is made of 16 calorimeter cells.

Overview Current System



Receiver System (USA-15):

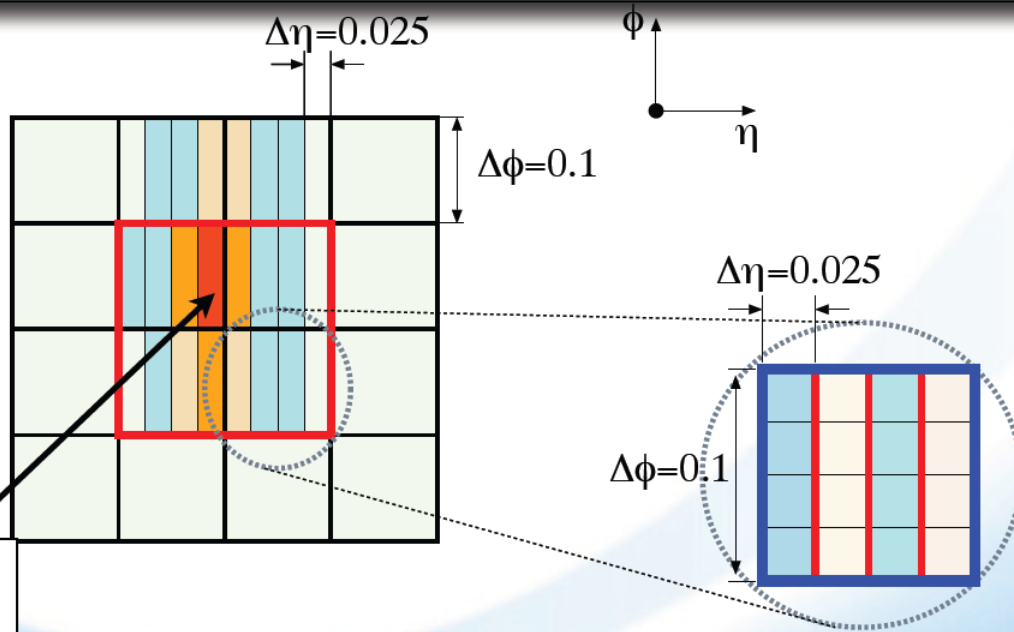
- ▶ 6 Crates
- ▶ 72 Receiver Modules (16/crate)

- On-Detector Trigger Electronics
 - ▶ EMB (32 Crates):
 - ◆ 1728 LSB: $32 * (26 \text{ FEBs} * 2 \text{ LSB/feb} + 2 \text{ FEBs} * 1 \text{ LSB})$
 - ◆ 64 TBBs: 2 TBBs/crate
 - ▶ EMEC: (24 Crates)
 - ◆ 1120 LSBs
 - ✓ $16 \text{ Std. Crates} * (26 \text{ FEBs} * 2 \text{ LSB/feb} + 2 \text{ FEB} * 1 \text{ LSB}) = 864$
 - ✓ $8 \text{ Spc. Crates} * (16 \text{ FEBs} * 2 \text{ LSB/feb} + 1 \text{ FEB} * 1 \text{ LSB}) = 256$
 - ◆ 56 TBBs
 - ✓ $16 \text{ Std. Crates} * 2 \text{ TBB/crate} = 32$
 - ✓ $8 \text{ Spc. Crates (incl. EMEC Inner Wheel)} * 3 \text{ TBB/crate} = 24$

- On-Detector Trigger Electronics
 - ▶ HEC (8 Crates):
 - ◆ 96 LSBs ($6 \text{ FEB/crate} * 2 \text{ LSB/feb} * 8 \text{ crates}$)
 - ◆ 16 TDBs (8 crates, 2 TDB/crate)
 - ▶ FCAL (2 Crates):
 - ◆ 56 LSBs ($2 \text{ crates} * 14 \text{ FEB/crate} * 2 \text{ LSB/crate}$)
 - ◆ 4 TDBs ($2 \text{ crates} * 2 \text{ TDB/crate}$)

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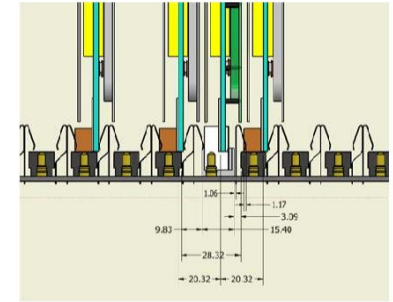
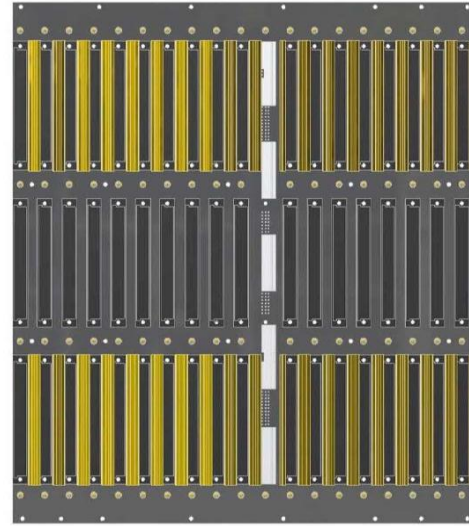
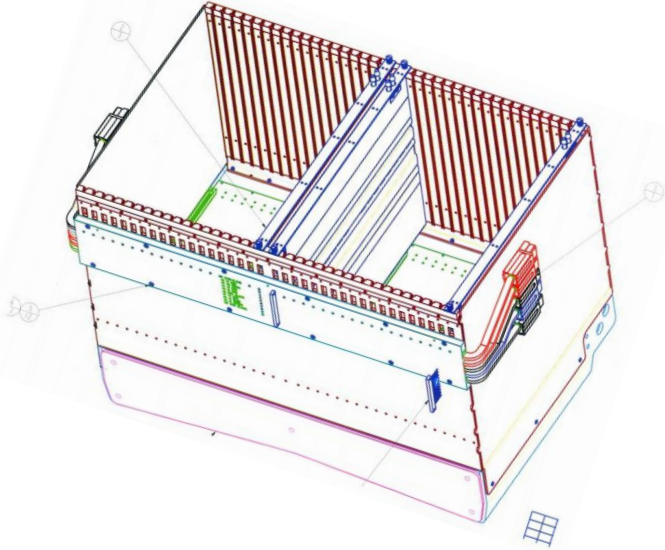
Exemplification of an EM shower and its lateral energy profile across the Super-Cells

"Super-Cells" are formed by grouping 4 cells in ϕ inside the Front-End Boards. The signals of the SuperCells are digitized in the new TBB

sLAr

- Milano interests/ possible contributions to the upgrade
- **Baseplanes:**
 - Redesign, testing
 - ~ 1/3 of the production in Italy [collaboration with US-BNL, IN2P3-LAL Orsay]
- **Layer Summing Boards:**
 - Redesign, testing
 - ~ 1/3 of the production in Italy [collaboration with US-BNL, JINR-Dubna, MPI-Munich]
- **On-detector new DTBB:**
 - power distribution on the DTBB, design and prototyping
 - POL instead of LVDS, extension of the Gruppo V - APOLLO Project [collaboration with US-BNL]
 - FEM/FEA thermal analysis of the power dissipation on new trigger board and test set-up

Baseplane redesign

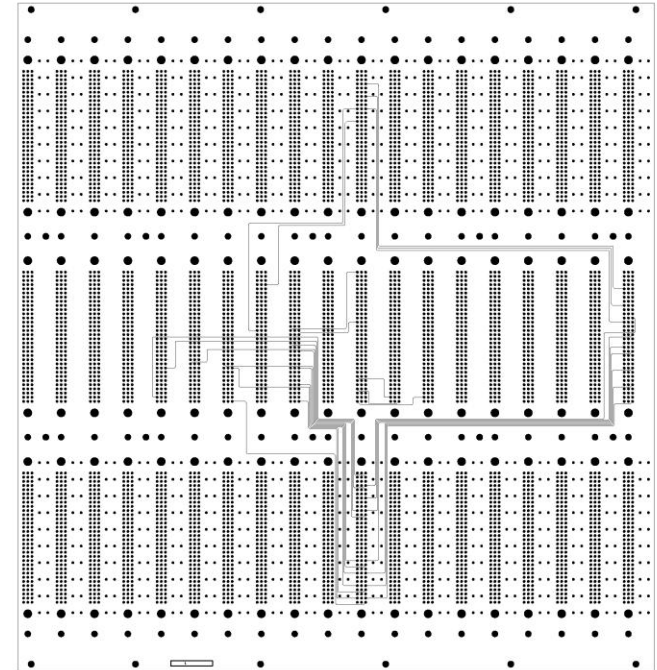


Baseplanes must be re-designed to provide the new granularity to the Digital Tower Builder Board (DTBB).

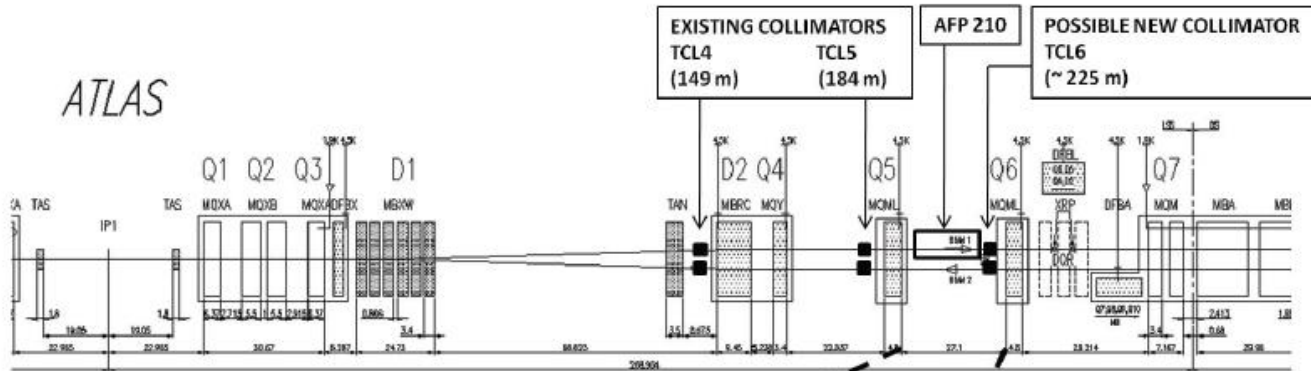
For the EM barrel the DTBB will have 284 channels.
Space for the DTBBs exist in the crates ... FEB position shifts implemented in the new baseplane layout
A “common” baseplane for all crates could be possible.

Signal integrity is a must in the baseplane, i.e. transport of low level analog signals.

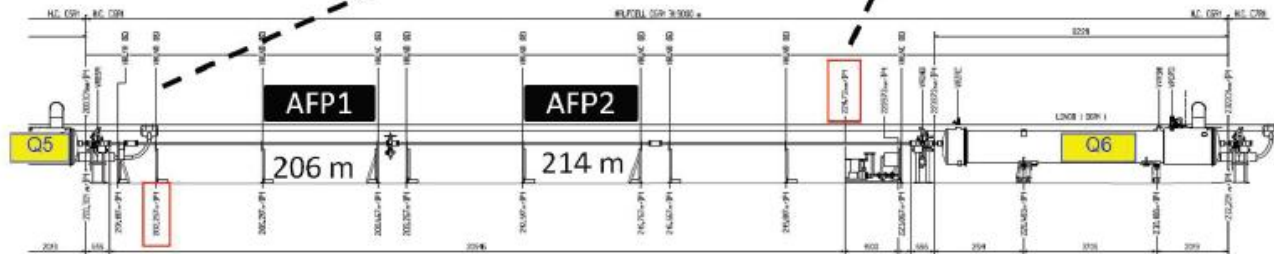
New baseplane samples, together with new LSB, needed to demonstrate upgrade feasibility (Phase 0)



AFP



IP



6-layer Si tracker

6-layer Si tracker +
timing detector (Cerenkov)

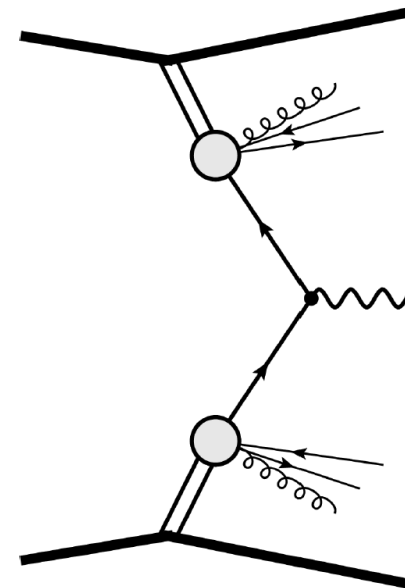
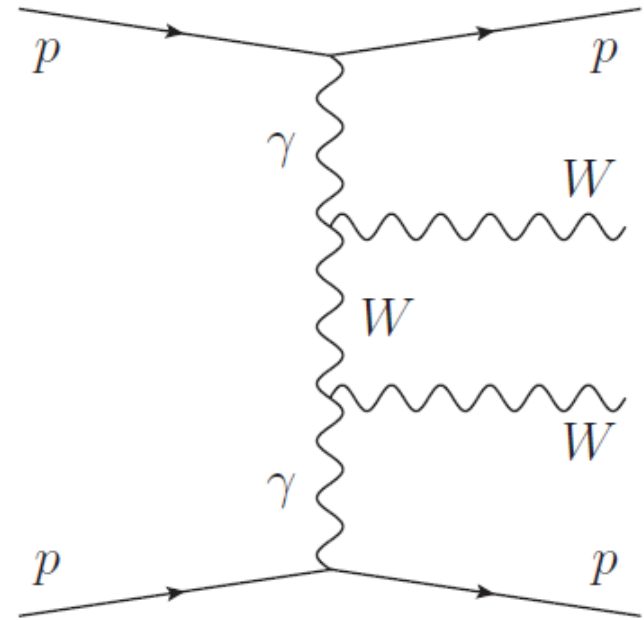
2 arms

Physics Motivations

- The aim of AFP will be to tag and measure the momentum, angle, and time-of-flight of protons emerging intact from the pp interactions
- Timing detectors allow to reconstruct with a few mm precision (~ 10 ps) the pp interaction vertex using the two tagged protons
 - reject pile-up background of a central system superimposed on two single and independent diffractive proton events in the same bunch crossing.

Physics Motivations

- Improve and extend ATLAS reach for both SM and BSM physics.
- BSM: probing for extra dimension models, eg through the sensitivity to anomalous couplings between γ and W/Z (in dim 6)
- Signature of 2 W 's central decays + 2 diffractive protons in AFP
- Measurement of rapidity gaps in central diffractive processes
 - Study of flavour composition of pomeron



Double Pomeron Exchange

AFP

- AFP based upon:
 - 4 identical Si detectors, with 6 sensor planes each (24 SC modules)
 - Planar or 3D (edgeless or IBL type) sensor
 - Detector installed in the LHC Tunnel (two distinct locations)
- Readout based on FE-I4B chips (IBL readout chip)
 - In general, adoption of IBL hardware

Milano contributions:

- Power distribution based on “voltage regulation” in detectors proximity
 - IBL PP2 crate: 2 crates in total, 6+6 boards
 - Crates installed few meters away from detectors (< 10 m)
 - Voltage regulators together with opto link electronics in the same crate
 - Estimated of radiation exposure of electronics in the LHC tunnel is critical
- Bump bonding of sensors (Selex)

Tier2

- Le richieste per il 2013 sono determinate da:
 - simulazione MC di tutti i dati 2010-2012 + inizio simulazione a 13 TeV
 - reprocessing dei dati 2011-2012 con software più performante
 - processamento della *delayed stream*, raccolta nel 2012 e archiviata su tape
 - 130 Hz di trigger speciali (200 TB di RAW data)
 - analisi di gruppo e utenti

Tier 2

- Attivita' 2013 e dello share della cloud italiana in atlas (10% per le CPU e 7% per il disco)
 - 0 CPU aggiuntive - 200 TB aggiuntivi
 - sostituzione delle risorse ormai obsolete (3 anni per le CPU e 5 anni per il disco): 6.16 kEH per le CPU - 500 TB per il disco per un totale di Euro - 86,2 kE per le CPU - 245 kE per il Disco
- Richieste:
 - Disco - 175 TB = 61,3 kE == 61 kE
 - CPU -1,54 kHS = 21,6 kE == 22 kE
 - Rete = 4,4 kE == 4 KE [6% fin. CPU + 5% fin. disco]
 - Server = 5,8 kE == 6 kE [7% (cpu + disco)]
 - 5kE di consumo

Richieste ai servizi

- Progettazione e officina
 - 7mu progettazione, 7mu officina
 - 30% S. Coelli
 - Attività' PP2 (IBL, AFP), IBL (installazione), Lar (FEA of power dissipation new boards), tracker upgrade Phase-II
- Servizio Elettronica
 - 12mu per progettazione FTK
 - 6mu LAr
 - 6mu per produzione e qualifica schede regolatori PP2
 - 50% M. Citterio

Richieste Finanziarie

CONSUMO	1. Tier2 - Consumi	5.00	
	2. FTK - produzione AMchip05	100.00	
	3. LAr - MOFB (RRB April 2012) 61 kCHF (1euro = 1.2CHF)	51.00	
	4. FTK - Test Stand AMboard	5.00	
	5. sLAr - produzione nuovi baseplane FEC e LSB per il demonstrator	14.00	
	6. SLAr - componentistica per LV POL e set-up per test termico (dummy board,...)	4.00	
	7. Metabolismo: 25.9FTE*1ke+2ke+0.4ke*25.9FTE	38.00	217.00
APPARATI	1. Tier2 - CPU: 1,54(obs) kHS	22.00	
	2. Tier2 - Apparato di rete	4.00	
	3. Tier2 - Server	6.00	
	4. Tier2 - Disco: 50(new)+125(obs)TB	61.00	
	5. IBL - produzione schede	30.00	
	6. IBL - HV/DCS patch box	5.00	
	7. AFP - 2 PP2 boxes with boards	12.00	140.00
INTERNO	1. FTK - attivita' AMchip I e II	4.00	
	2. Riunioni e gruppi di lavoro analisi: 0.7x25.9FTE	18.00	22.00

+ circa 300 keuro ME => totale 679 keuro